HARDWARE SCHEDULED
WITH FORWARDING
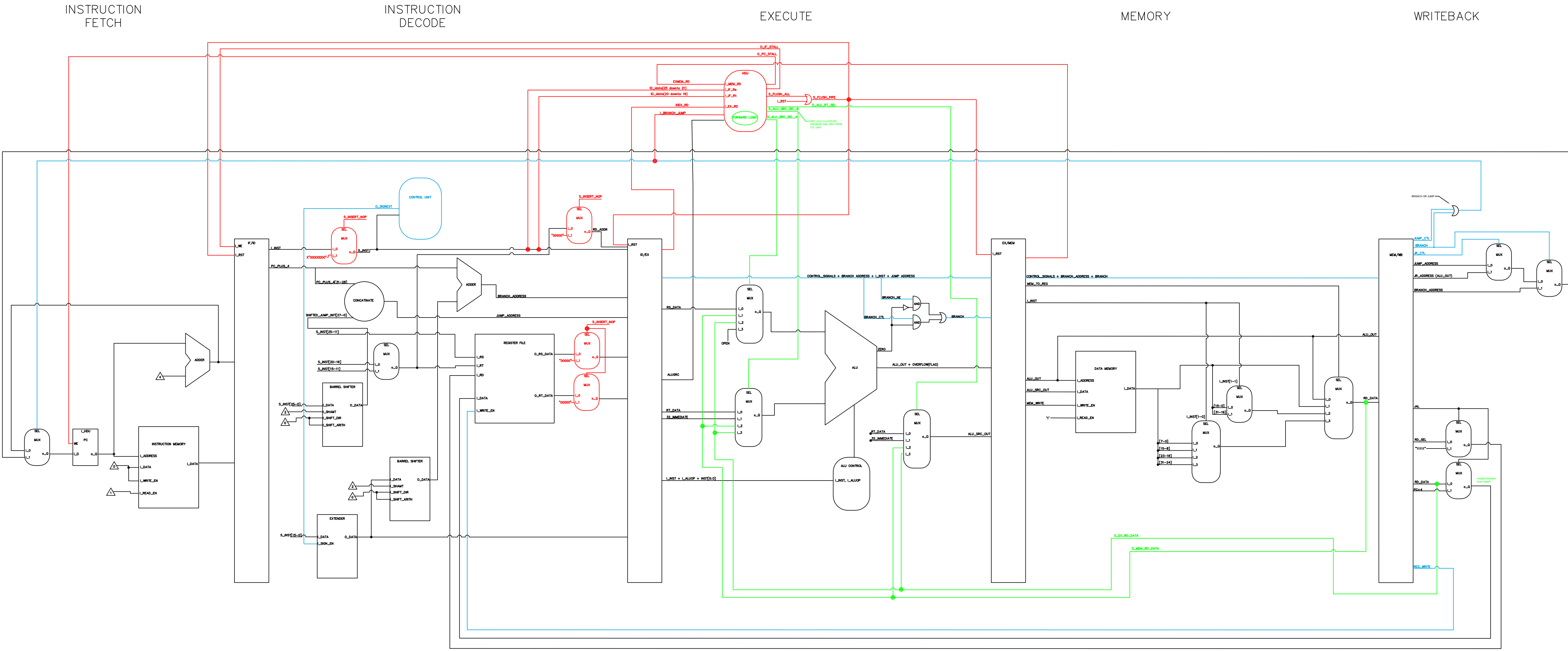
INSTRUCTION
FETCH

INSTRUCTION
DECODE

EXECUTE

MEMORY

WRITEBACK

KEY:
BLACK: BASIC DATAPATH
BLUE: CONTROL
RED: HAZARD DETECTION RELATED
GREEN: FORWARD LOGIC

No.	Revision/Issue	Date
1	REVISION 1	04/22
2	REVISION 2	04/25

CPRE 381
HARDWARE SCHEDULED PIPELINE

PIPELINED PROCESSOR
THIS IS REVISION 2 OF OUR HARDWARE
PIPELINE WITH FORWARDING AND HAZARD
DETECTION AND AVOIDANCE.

Project	Sheet
PIPELINED PROCESSOR	1/1
Date 04/22/2025	
Scale VERY SMALL	

CONTROL UNIT

INSTRUCTION MEMORY

REGISTER FILE

BARREL SHIFTER

EXTENDER

ADDER

CONCATENATE

ALU

ALU CONTROL

DATA MEMORY