RF Transmitter Design

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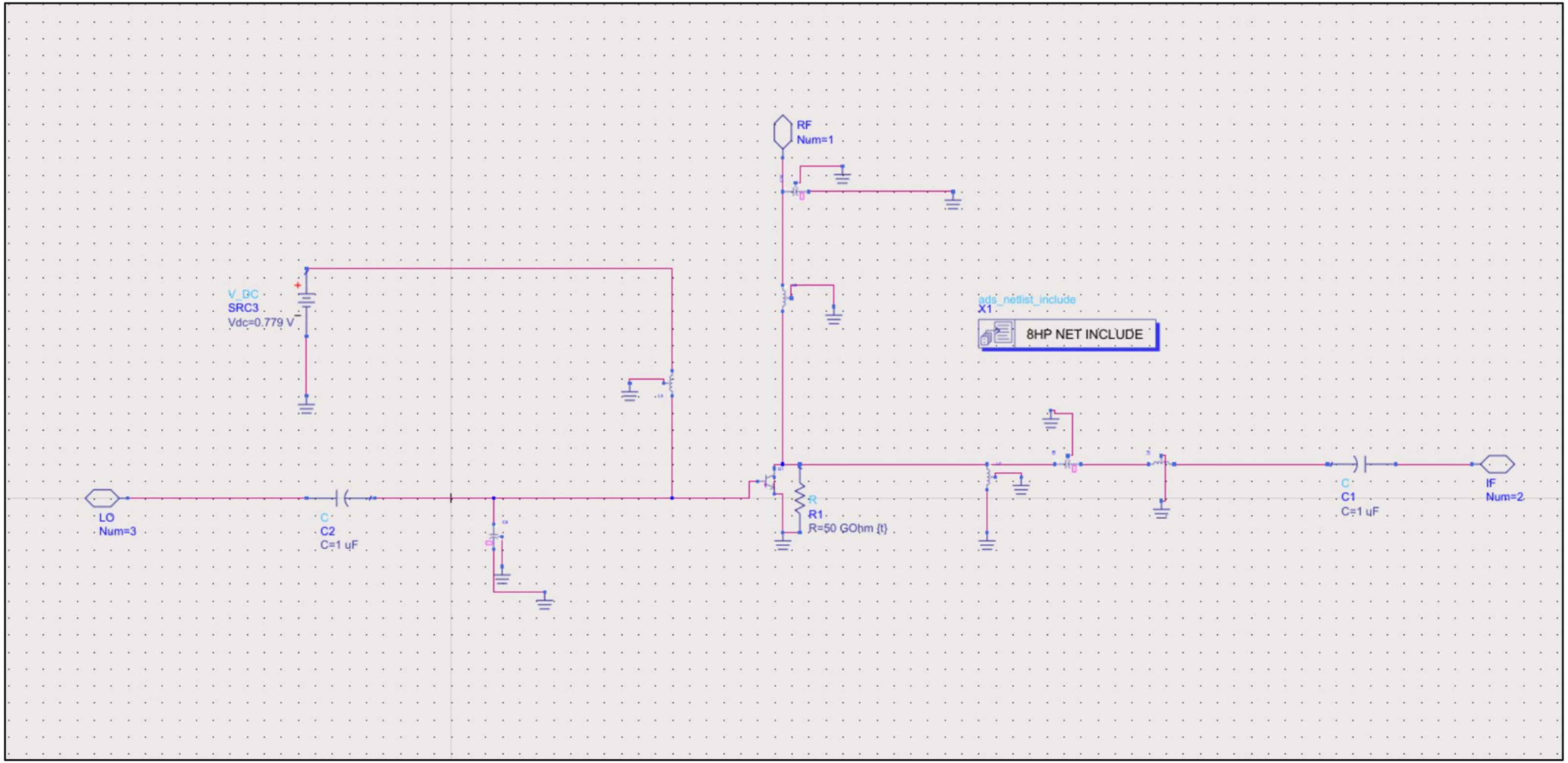
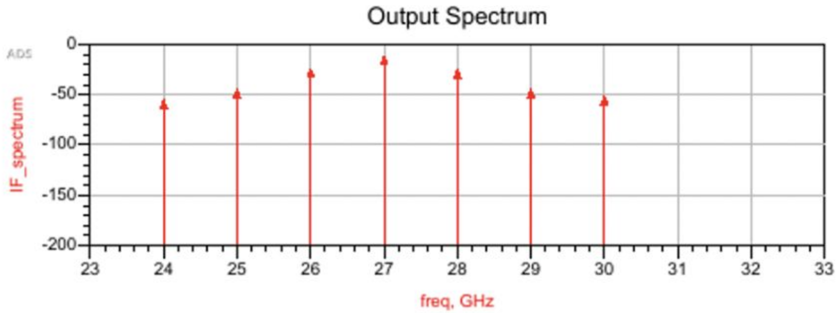
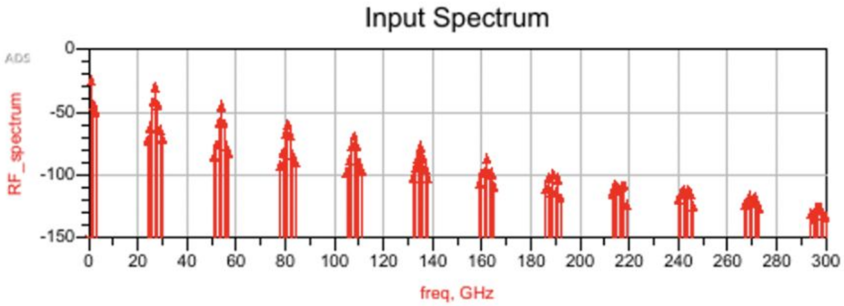
Mixer Design



Mixer Performance



Note: Very small amplitude predictions (less than -100 dBm) are not likely to be accurate.



Output Frequency	Down Conversion Gain (dB)	Output voltage
26.00 GHz	3.291	0.029 / 82.813

Output Frequency	Up Conversion Gain (dB)	Output voltage
28.00 GHz	2.890	0.028 / 73.1...

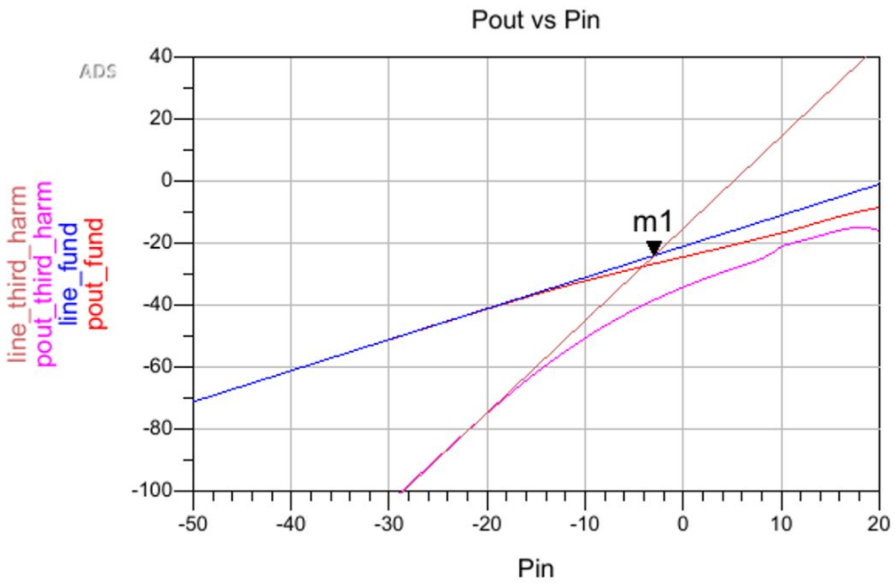
PORT-TO-PORT ISOLATION

LO to Output isolation (dB)	LO to Input isolation (dB)	Input to Output isolation (dB)
P_LO2IF	P_LO2RF	P_RF2IF
13.5	26.3	3.8

- Up conversion gain (2.89dB) evaluated using single-ended mixer characterization test bench, f_LO = 27 GHz, f_RF = 1 GHz

- In this simulation, the input power of the RF signal is set to -30dB and the input power of the LO signal is set to 0dB

Mixer Performance - Linearity



m1
Pin=-3.000
line_fund=-23.915

Eqn iip3 = indep(m1)

Eqn linearity_spec = iip3 - gain_comp_1dB

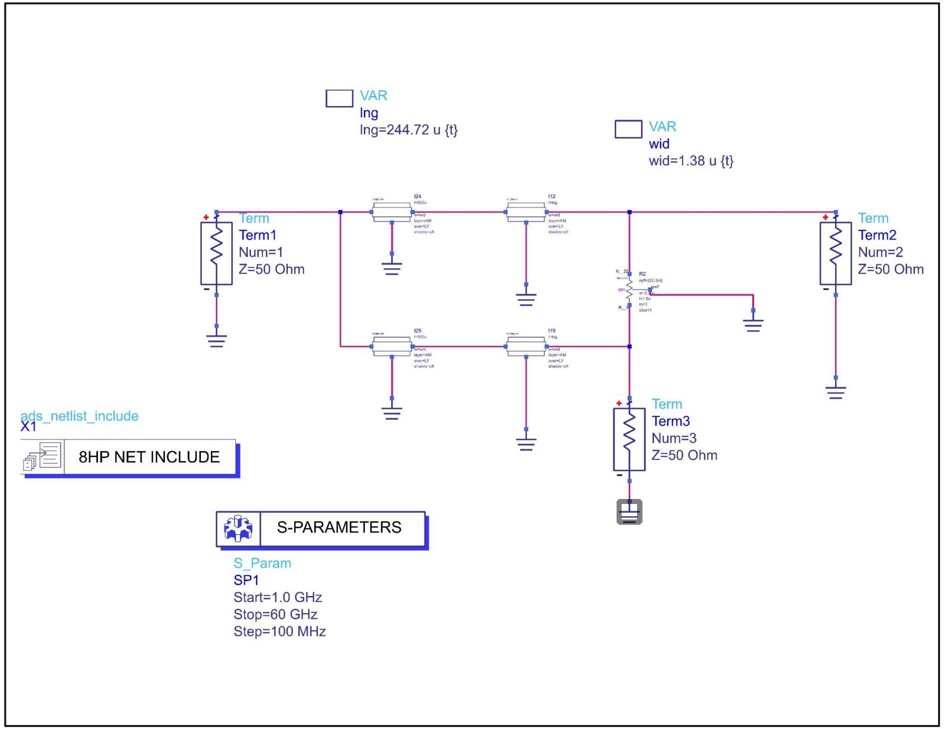
iip3	gain_comp_1dB
-3.000	-10.572

linearity_spec
7.572

gain_comp_1dB	gain_comp_1dB_out
-10.572	-32.487

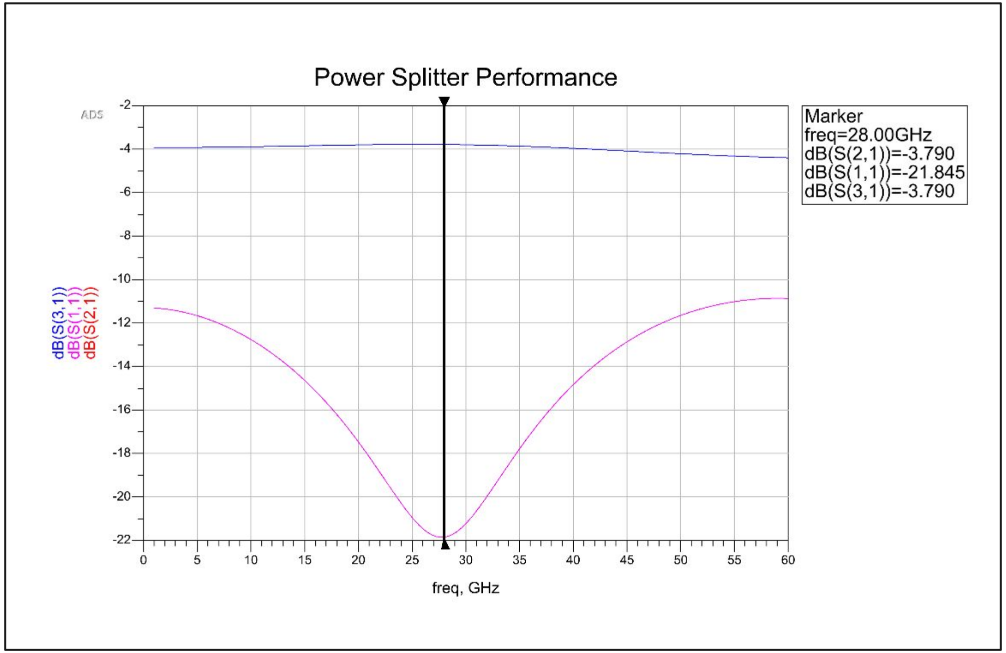
- We evaluate linearity by taking the difference of the third order intercept of the circuit and the 1dB compression point of the fundamental input. When this value is high, it means the fundamental and third order gains are similar (i.e. the system is linear).
- In general, a linearity_spec of about 10dB or more shows that the circuit has strong linearity. We have 7.56dB.

Power Splitter Design



- Wilkinson Power Combiner/Splitter Design
- SGLWIREs & NS_RES used to model
- Upper and lower branches:
  - Length: 1144 um
  - Width: 1.38 um

Power Splitter Performance



- Near optimal performance at across frequency band
- S(2,1) & S(3,1) @ -3.8 dB @ 28 GHz
- S(1,1) @ -21.845 dB @ 28 GHz

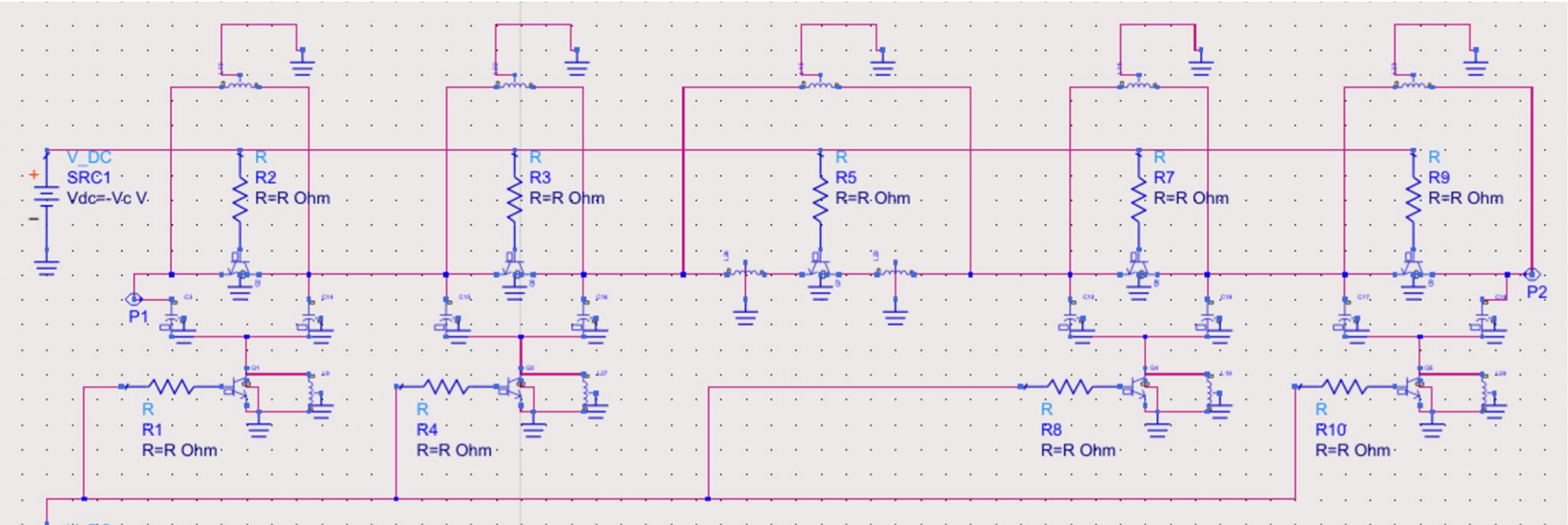
Phase Shifter Design

Comments

- Our passive design uses the switched t-line topology discussed in the phased array lecture. Ideally, it offers 22.5 degree resolution for beam forming.
- Passive phase shifters generally have high insertion loss at high frequencies, but should also exhibit strong linearity and low power loss.
- We utilize BJTs instead of FETs. Our BJTs have 0.12um emitter widths and multiplicities of 3. BJTs have higher switching losses than FETs, which dominates the insertion loss of our phase shifter. Knowing this, it makes sense that BJTs worked better than FETs for our design, as we used a passive topology and expect higher insertion loss at high frequencies.
- We were able to meet all the design specs for the phase shifter, as shown in slides 8 - 12.

Phase Shifter Design

Schematic - Switched T-Line



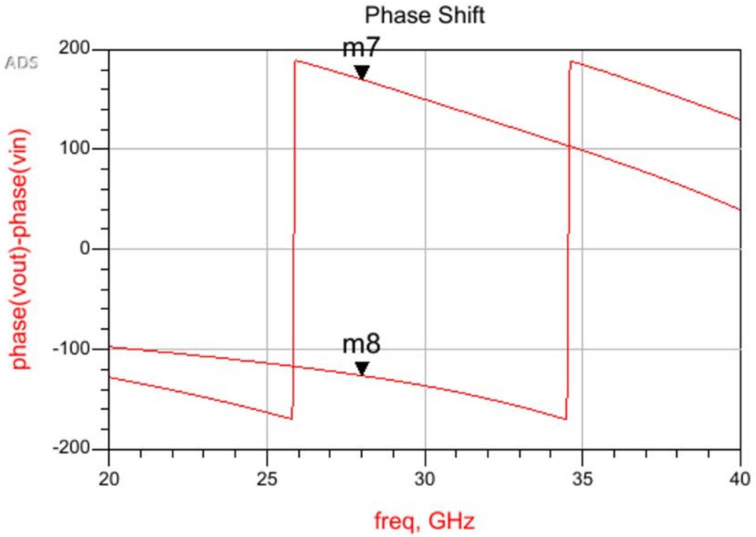
- In this setup, R=0 turns ON all phase shift elements for maximum shift
- R=1e11 turns OFF all phase shift elements for minimum shift

- Our testbench setups we made to evaluate tunable range, linearity, and S parameters can be found in the appendix

- We can adjust the phase shift by turning off the power to the 4 different sections of the circuit

Phase Shifter Design

Tuning Range



Eqn max_shift = m7

Eqn min_shift=m8

Eqn tunable_range = max_shift - min_shift

m7
freq=28.00GHz
phase(vout)-phase(vin)=169.686
R=0.000

max_shift	min_shift
169.686	-126.537

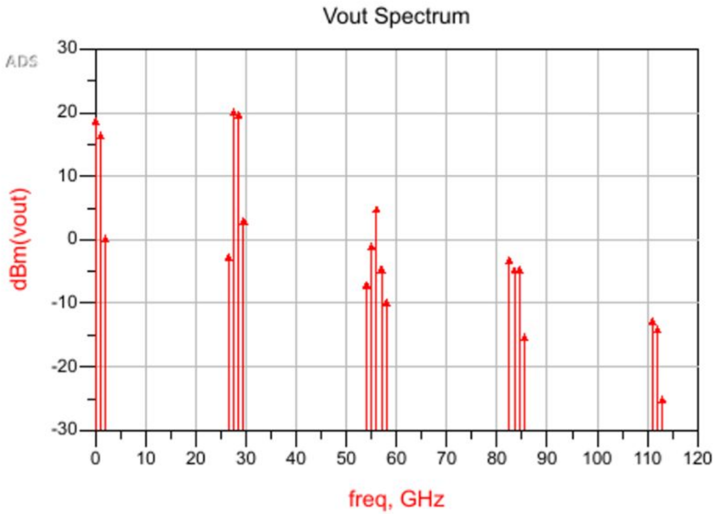
m8
freq=28.00GHz
phase(vout)-phase(vin)=-126.537
R=1.000E11

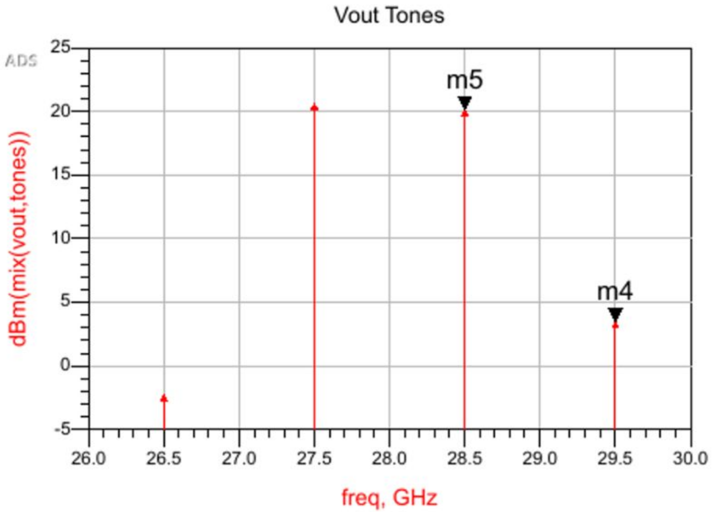
tunable_range
296.223

- R=0 turns ON phase shift elements for maximum shift
- R=1e11 turns OFF phase shift elements for minimum shift
- Units of phase are in degrees
- Tunable range meets design spec of >60 degrees

Phase Shifter Design

Linearity





iip3_upper	iip3_lower
28.467	32.087

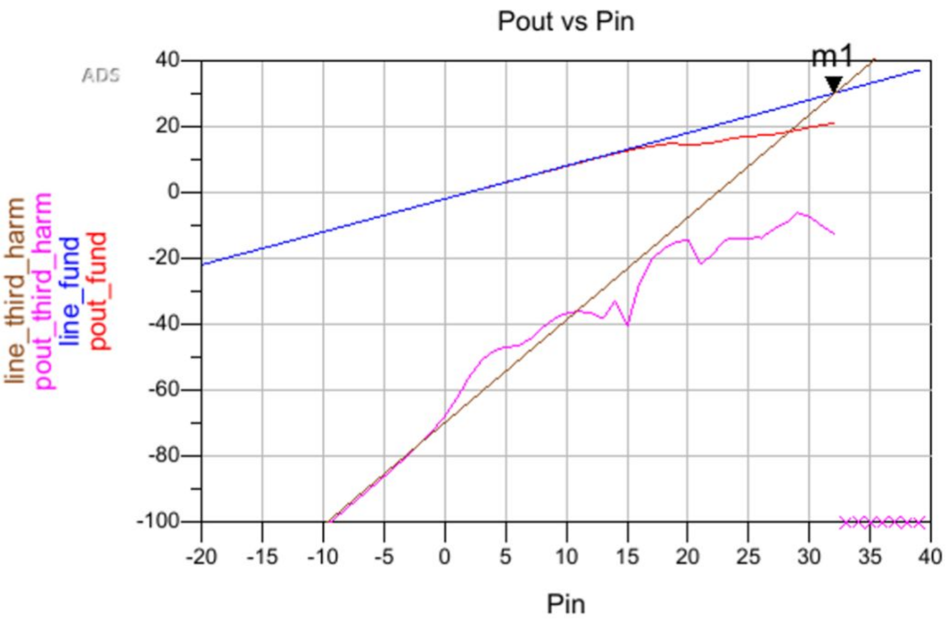
m4
freq=29.50GHz
dBm(mix(vout,tones))=3.496

m5
freq=28.50GHz
dBm(mix(vout,tones))=20.143

- We implement a multi-tone input to generate the vout spectrum seen on the left
- We highlight the fundamental and third order tones (right) and extrapolate the third order intercept (iip3) from the two sets of tones
- iip3_upper, e.g., is calculated from m5 and m4. We can then plot Pout/Pin curves of these tones to analyze circuit linearity and confirm the toi.

Phase Shifter Design

Linearity



m1
Pin=32.000
line_fund=30.086

Eqn iip3 = indep(m1)

Eqn linearity_spec = iip3 - gain_comp_1dB

iip3	gain_comp_1dB
32.000	16.796

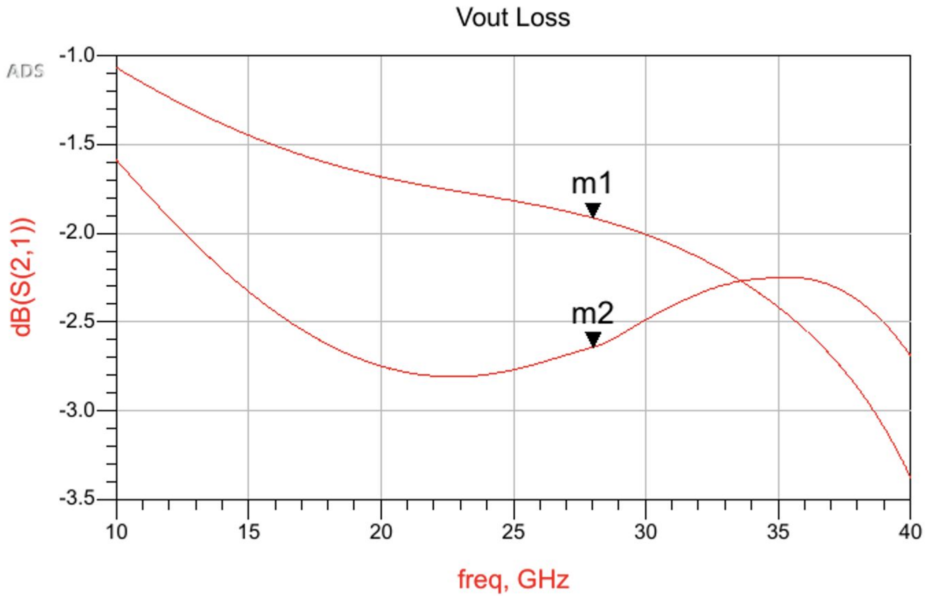
linearity_spec
15.204

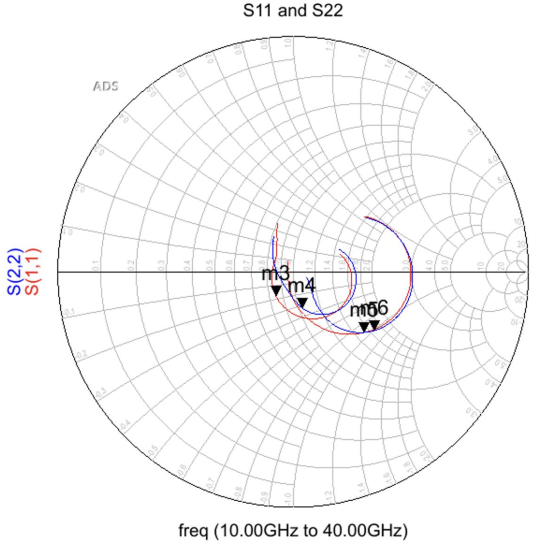
gain_comp_1dB	gain_comp_1dB_out
16.796	13.881

- We evaluate linearity by taking the difference of the third order intercept of the circuit and the 1dB compression point of the fundamental input. When this value is high, it means the fundamental and third order gains are similar (i.e. the system is linear).
- A linearity_spec of about 10dB or more shows that the circuit has strong linearity. We have 15.2dB
- iip3 is estimated to be 32dB, which matches our calculation from the previous slide.

Phase Shifter Design

S-Parameters





m4
freq=28.00GHz
S(2,2)=0.157 / -76.099
R=0.000
impedance = Z0 * (1.028 - j0.321)

m3
freq=28.00GHz
S(1,1)=0.125 / -126.088
R=0.000
impedance = Z0 * (0.846 - j0.174)

m5
freq=28.00GHz
S(1,1)=0.396 / -40.415
R=1.000E11
impedance = Z0 * (1.523 - j0.927)

m6
freq=28.00GHz
S(2,2)=0.425 / -35.717
R=1.000E11
impedance = Z0 * (1.670 - j1.012)

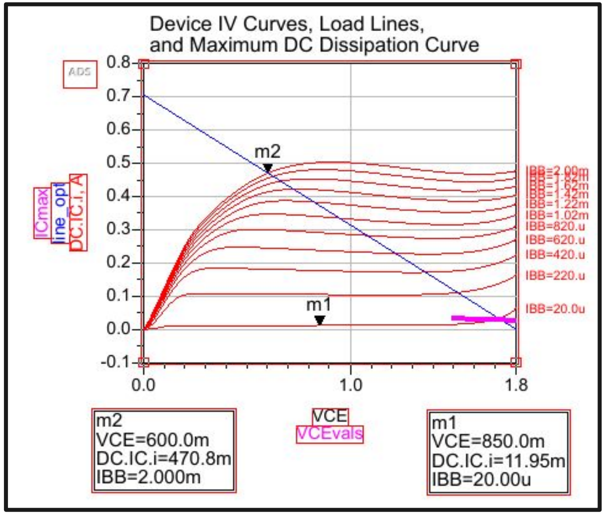
Eqn loss_at_max_shift = m1   Eqn loss_at_min_shift=m2

loss_at_max_shift	loss_at_min_shift
-1.914	-2.641

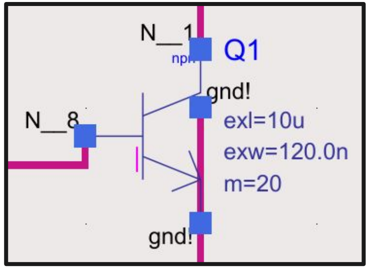
- R=0 turns ON phase shift elements for maximum shift
- R=1e11 turns OFF phase shift elements for minimum shift
- Low loss (less than 3dB) across the desired bandwidth of 27 - 29 GHz

PA Design (1: Bias Point)

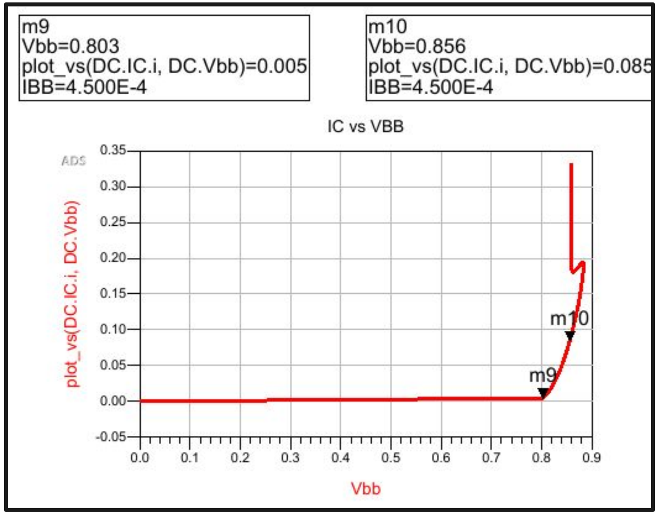
Class A - for simplicity and high gain.



20 Fingers



18.96dBm; 32% Efficiency

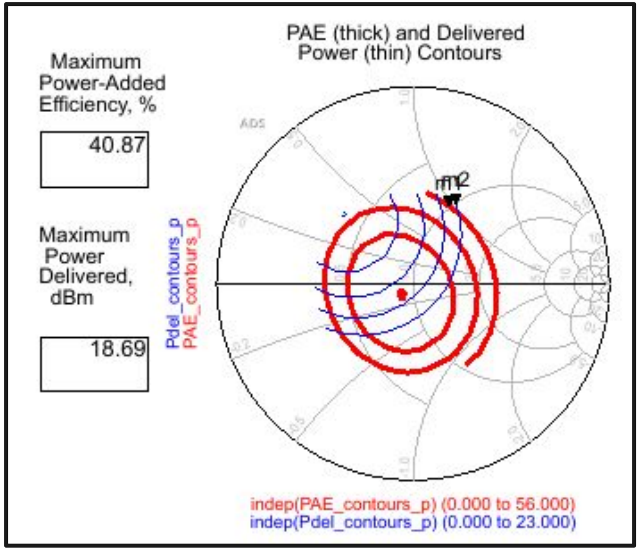


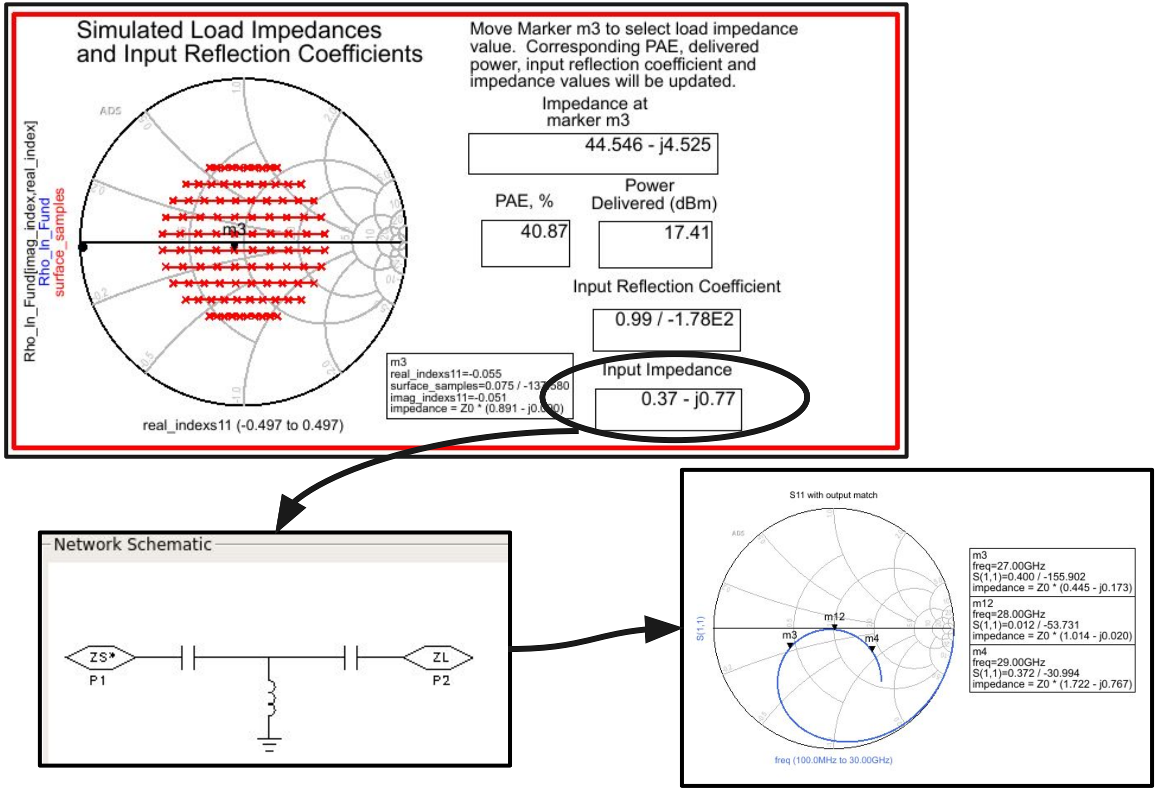
Class A -> Vbb ~ 0.856V
Class B -> Vbb = 0.803V

PA Design (2: Load Pull / Matching)

Needed to Match Load to Z = 5.005 + j1.27Ω

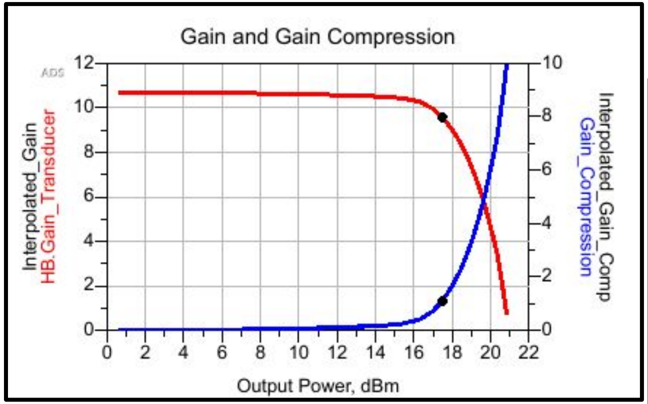
Vbb = 0.833V

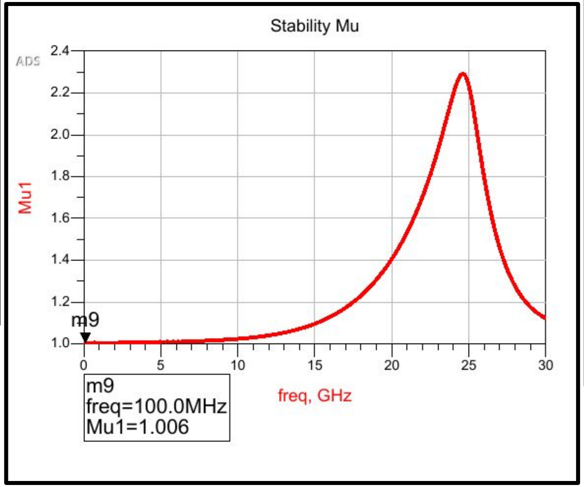


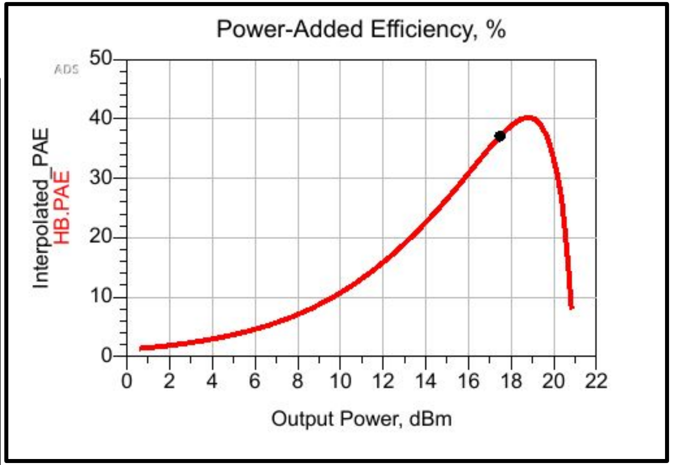


PA Design (3: Analysis PDK)

Fundamental Output Power dBm	Transducer Power Gain	Gain Comp. (dB)	Power- Added Efficiency, %	DC Power Consumpt. Watts	High Supply Current	Thermal Dissipation Watts
17.476	9.576	1.103	37.065	0.134	0.112	0.084







PA Design (4: with Layout)

Fundamental Output Power dBm	Transducer Power Gain	Gain Comp. (dB)	Power- Added Efficiency, %	DC Power Consumpt. Watts	High Supply Current	Thermal Dissipation Watts
17.999	10.099	1.071	13.399	0.425	0.354	0.367

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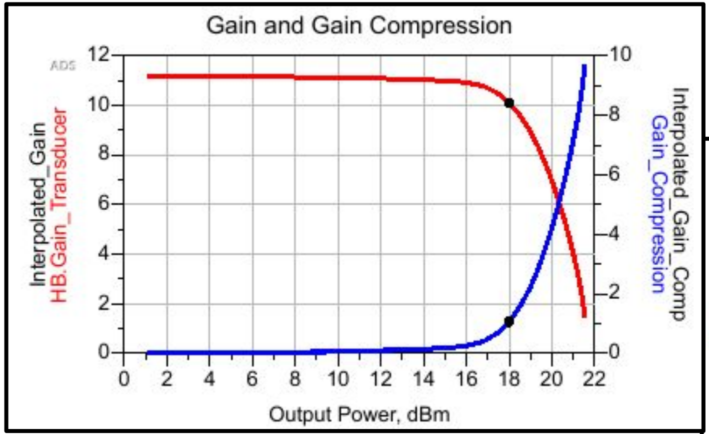
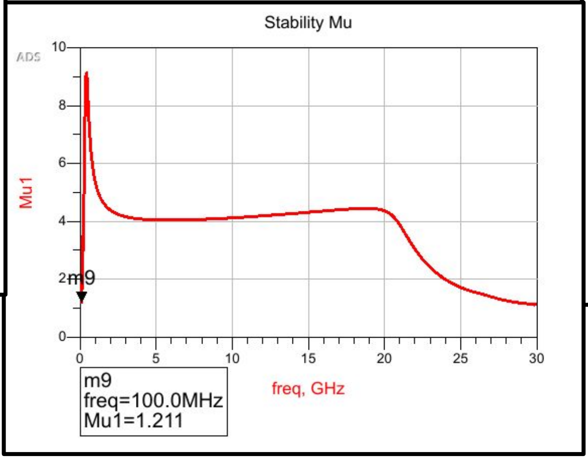
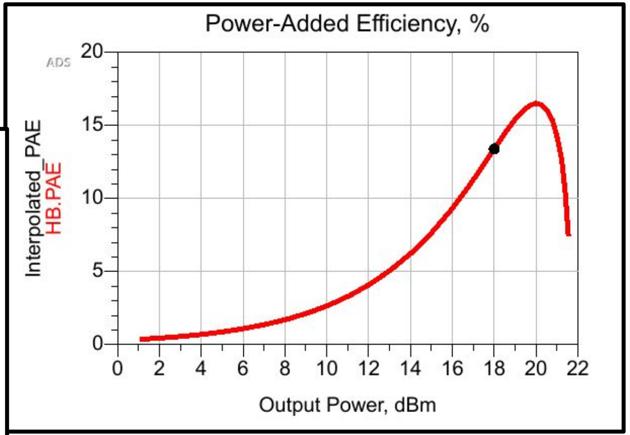
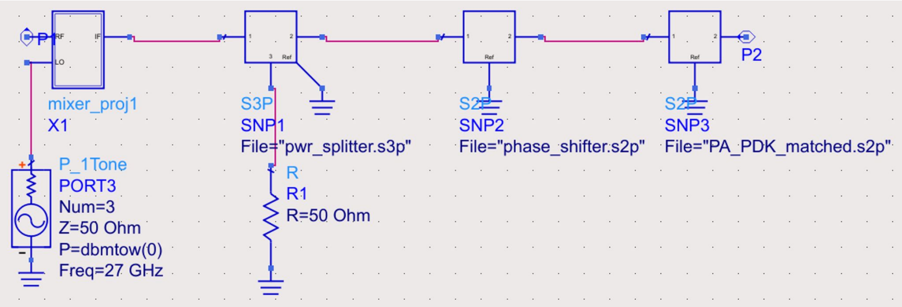
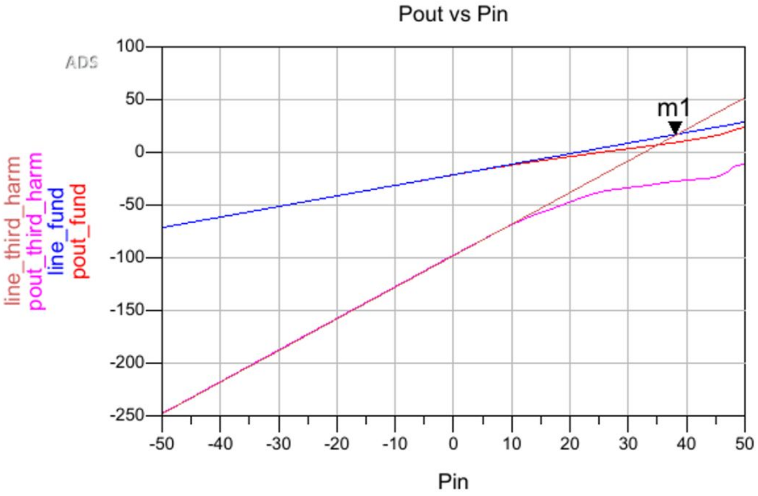






Transmitter Performance - Linearity





m1
Pin=38.000
line_fund=16.611

Eqn iip3 = indep(m1)

Eqn linearity_spec = iip3 - gain_comp_1dB

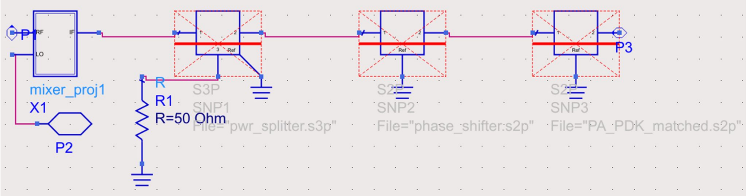
iip3	gain_comp_1dB
38.000	11.937

linearity_spec
26.063

gain_comp_1dB	gain_comp_1dB_out
11.937	-10.451

- Strong linearity is achieved when all elements are combined in series

Transmitter Performance - Conversion Gain

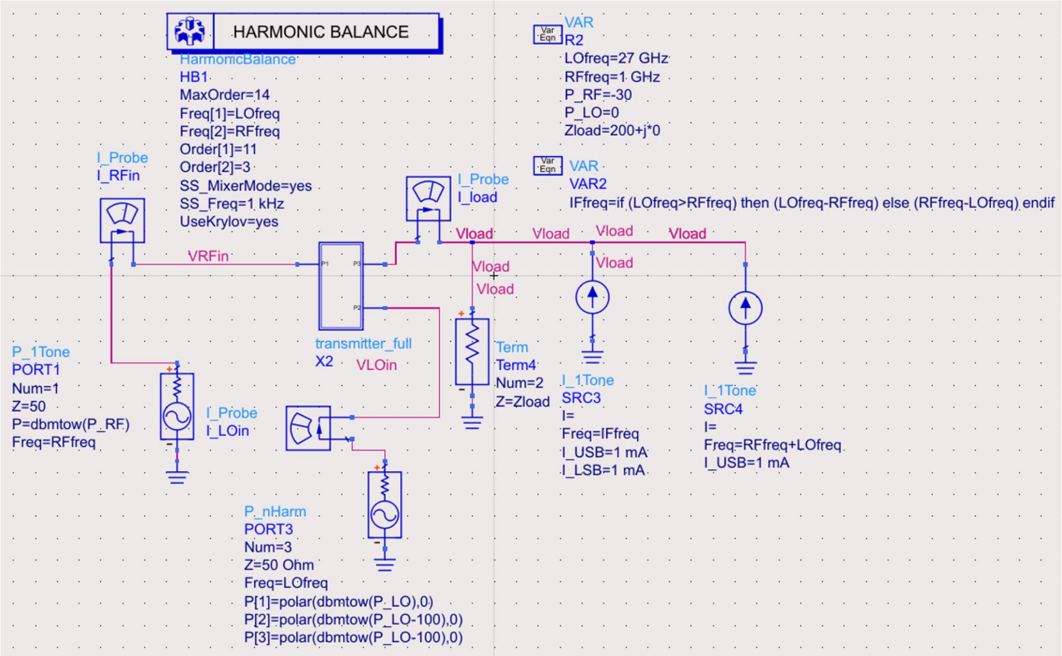


Output Frequency	Down Conversion Gain (dB)	Output voltage
26.00 GHz	3.291	0.029 / 82.813

Output Frequency	Up Conversion Gain (dB)	Output voltage
28.00 GHz	2.890	0.028 / 73.1...

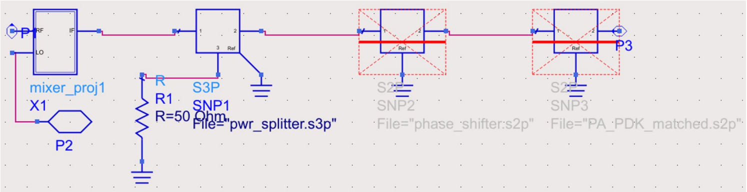
PORT-TO-PORT ISOLATION

LO to Output isolation (dB)	LO to Input isolation (dB)	Input to Output isolation (dB)
P_LO2IF	P_LO2RF	P_RF2IF
13.5	26.3	3.8



- Up conversion gain of the mixer is measured at 8.397dB

Transmitter Performance - Conversion Gain

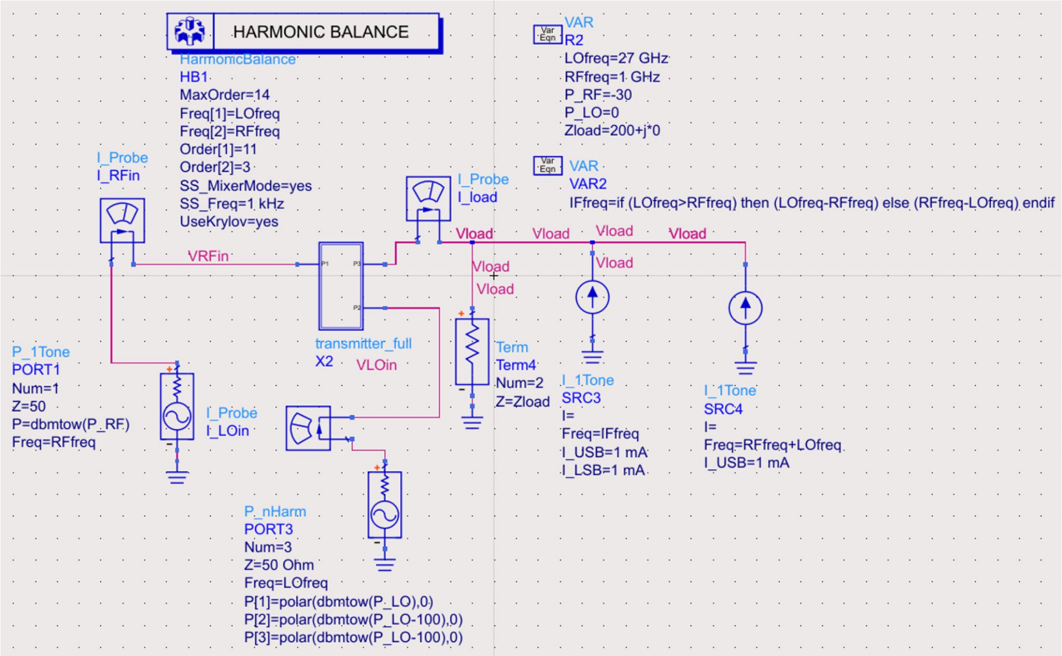


Output Frequency	Down Conversion Gain (dB)	Output voltage
26.00 GHz	1.022	0.022 / -21.8...

Output Frequency	Up Conversion Gain (dB)	Output voltage
28.00 GHz	-0.364	0.019 / -53.1...

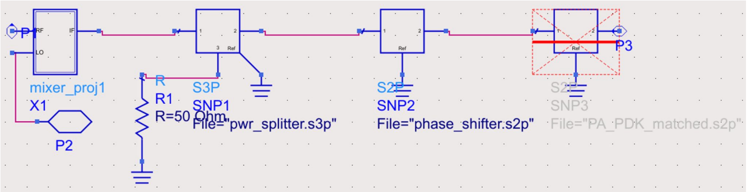
PORT-TO-PORT ISOLATION

LO to Output isolation (dB)	LO to Input isolation (dB)	Input to Output isolation (dB)
P_LO2IF	P_LO2RF	P_RF2IF
17.3	26.9	15.2



- Up conversion gain is measured at -0.364dB with the splitter added in series

Transmitter Performance - Conversion Gain

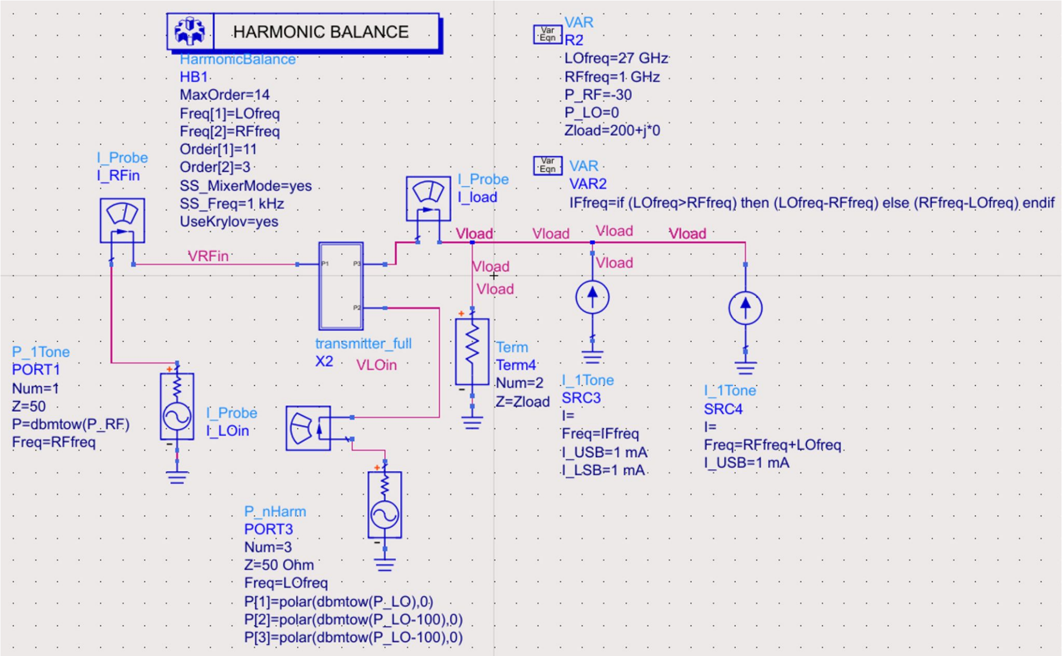


Output Frequency	Down Conversion Gain (dB)	Output voltage
26.00 GHz	-0.979	0.018 / 155.3...

Output Frequency	Up Conversion Gain (dB)	Output voltage
28.00 GHz	-2.747	0.015 / 107....

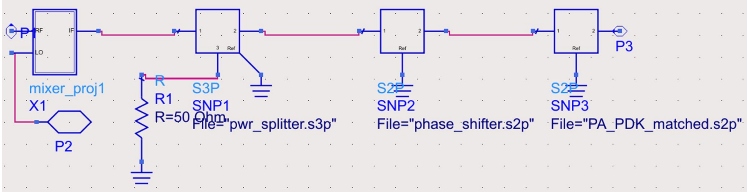
PORT-TO-PORT ISOLATION

LO to Output isolation (dB)	LO to Input isolation (dB)	Input to Output isolation (dB)
P_LO2IF	P_LO2RF	P_RF2IF
20.0	26.7	15.0



- Up conversion gain is measured at -2.747dB with the phase shifter added in series
- The phase shifter is set to maximum shift (least amount of loss)

Transmitter Performance - Conversion Gain

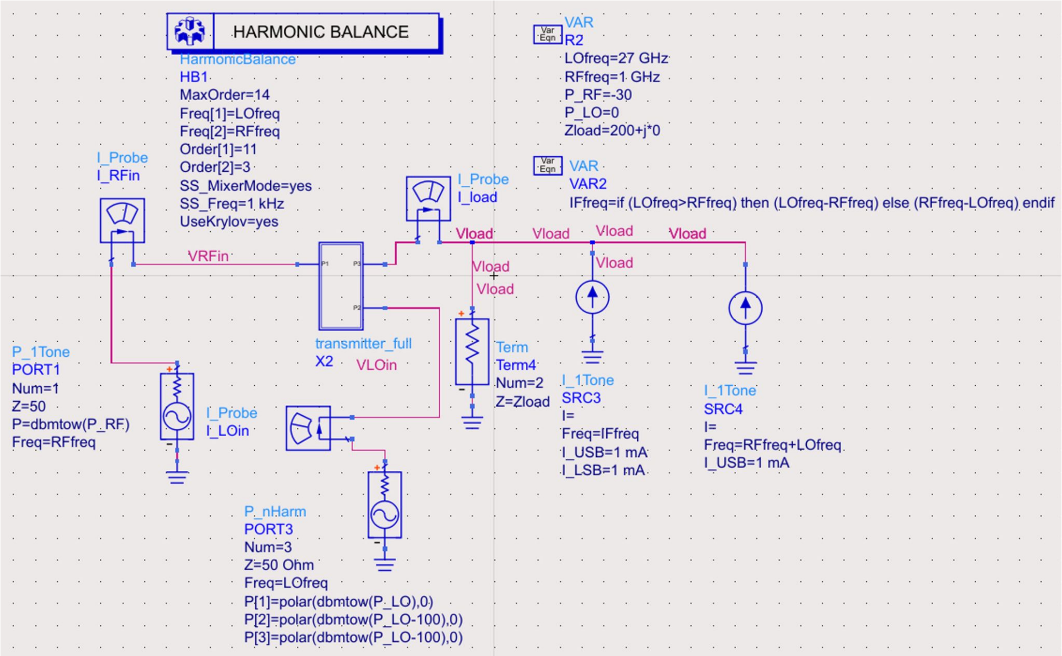


Output Frequency	Down Conversion Gain (dB)	Output voltage
26.00 GHz	4.429	0.033 / 114.8...

Output Frequency	Up Conversion Gain (dB)	Output voltage
28.00 GHz	8.397	0.053 / -0.290

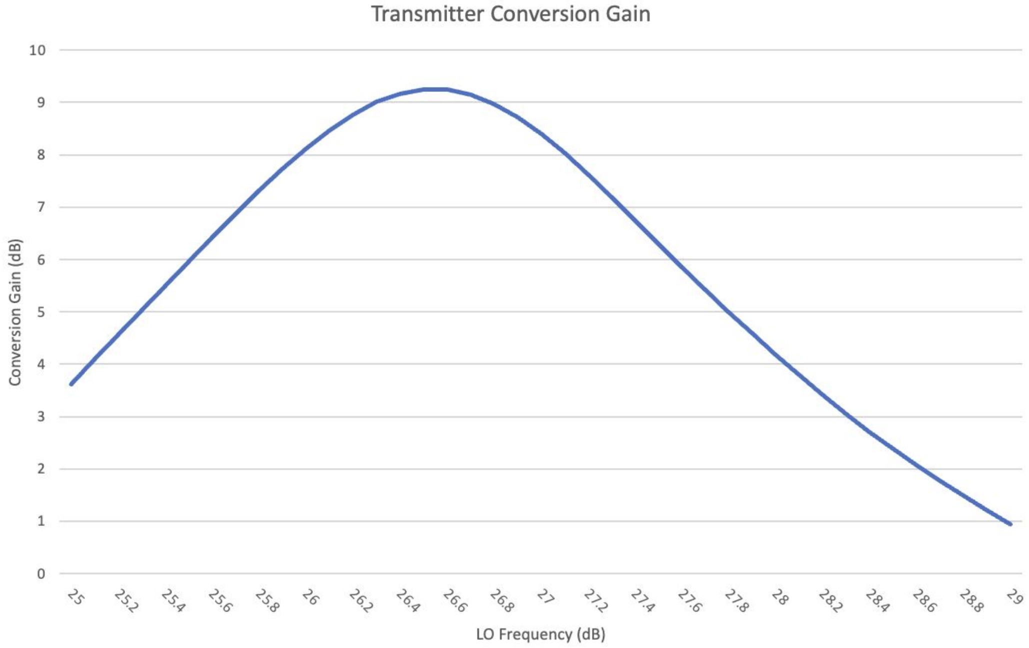
PORT-TO-PORT ISOLATION

LO to Output isolation (dB)	LO to Input isolation (dB)	Input to Output isolation (dB)
P_LO2IF	P_LO2RF	P_RF2IF
9.6	26.7	133.9



- Up conversion gain of the transmitter is measured at 8.397dB

Transmitter Performance - Conversion Gain



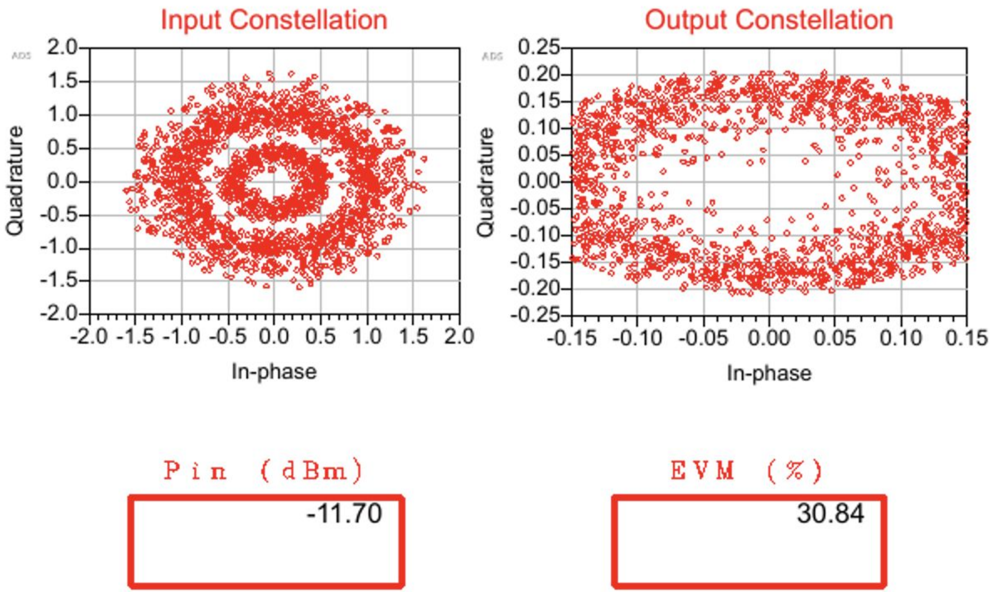
- This plot was created in Excel after recording the transmitter conversion gain at different LO frequencies.
- We see that the peak conversion gain occurs when the LO signal is at about 26.6GHz, which corresponds to an IF frequency of 27.6GHz.
- Conversion gain stays above 4dB across the desired IF bandwidth of 27-29GHz

Transmitter Performance

Link Budget	Expected Power [dB]	Measured Power [dB]
PA	9.576	11.144
Phase Shifter	-1.914	-2.383
Power Splitter	-3.8	-3.254
Mixer	2.89	2.89
Total	6.752	8.397

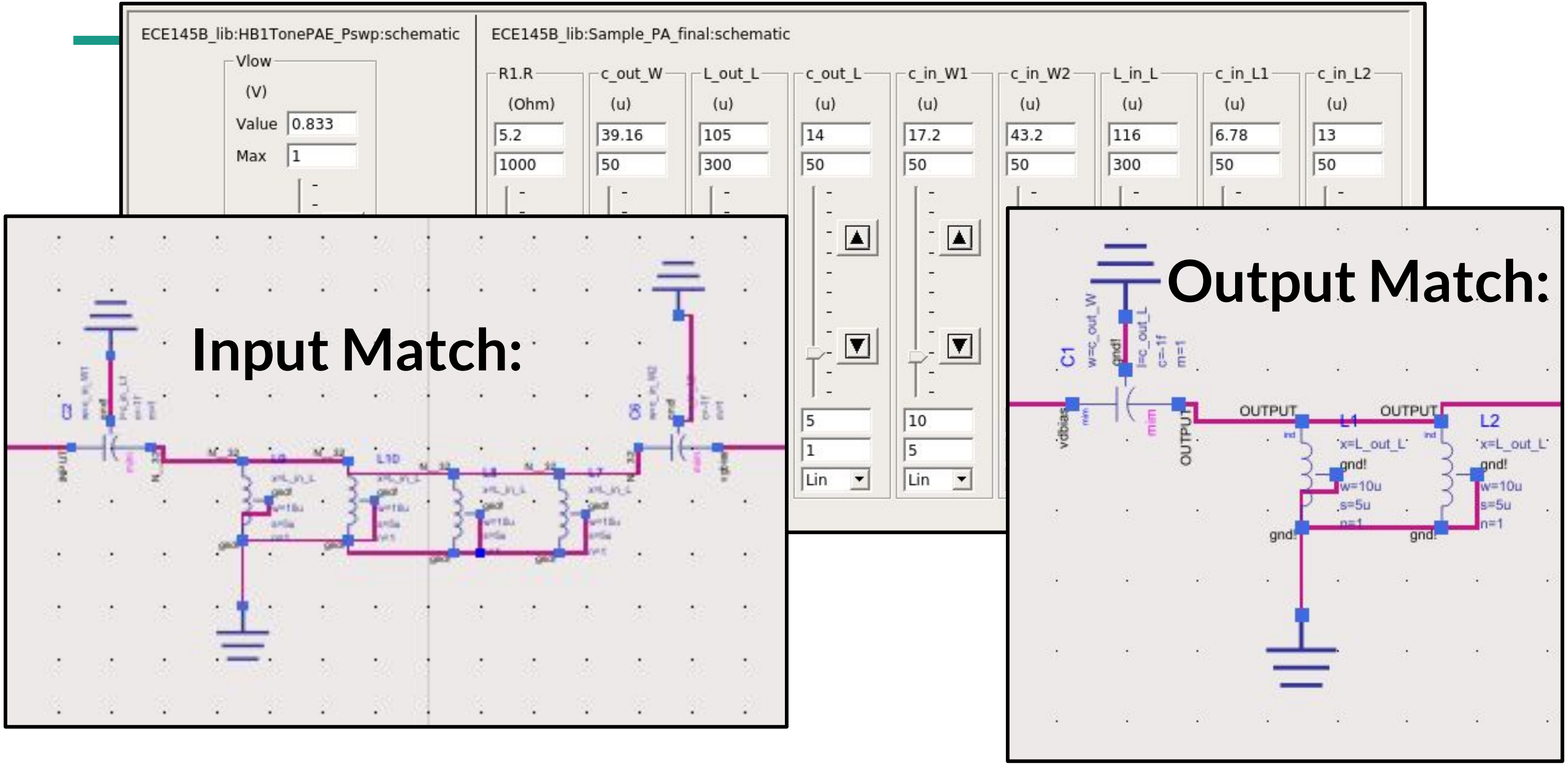
- This is a comparison of what we expected out of each circuit component of the transmitter and the measured impact each component had on the conversion gain
- The results are relatively close to as we expected. We believe that discrepancies can be mostly attributed to the impedance matching between each of the components

Transmitter Performance

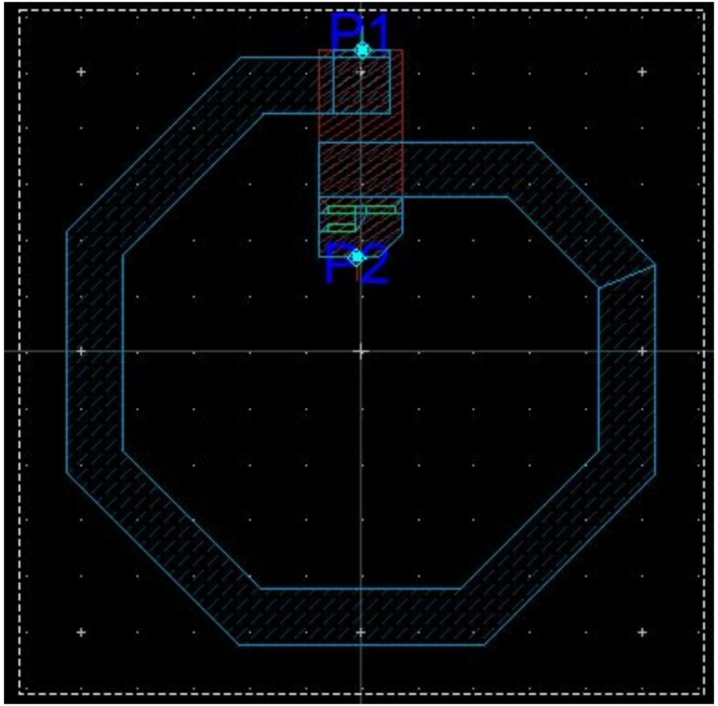


- We see massive gain compression
- We expect that we did not do this properly, but our testbench can be found in the Appendix

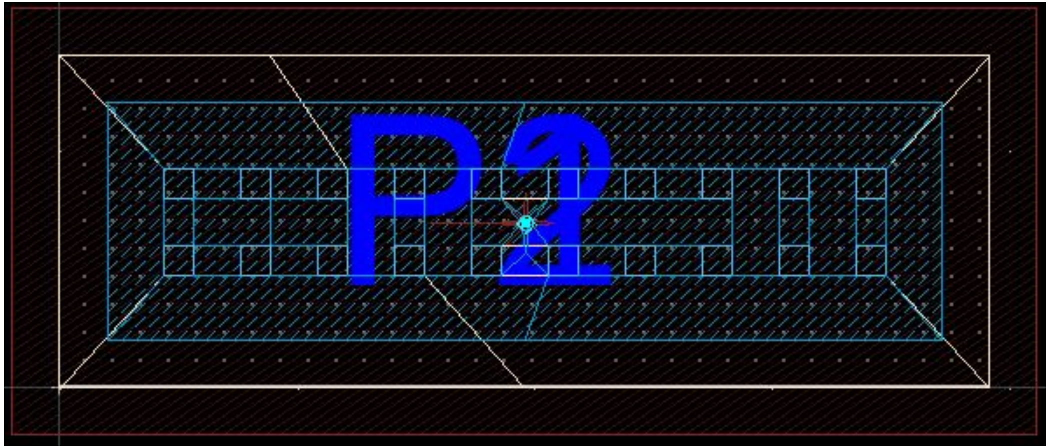
Appendix (PA PDK Values)



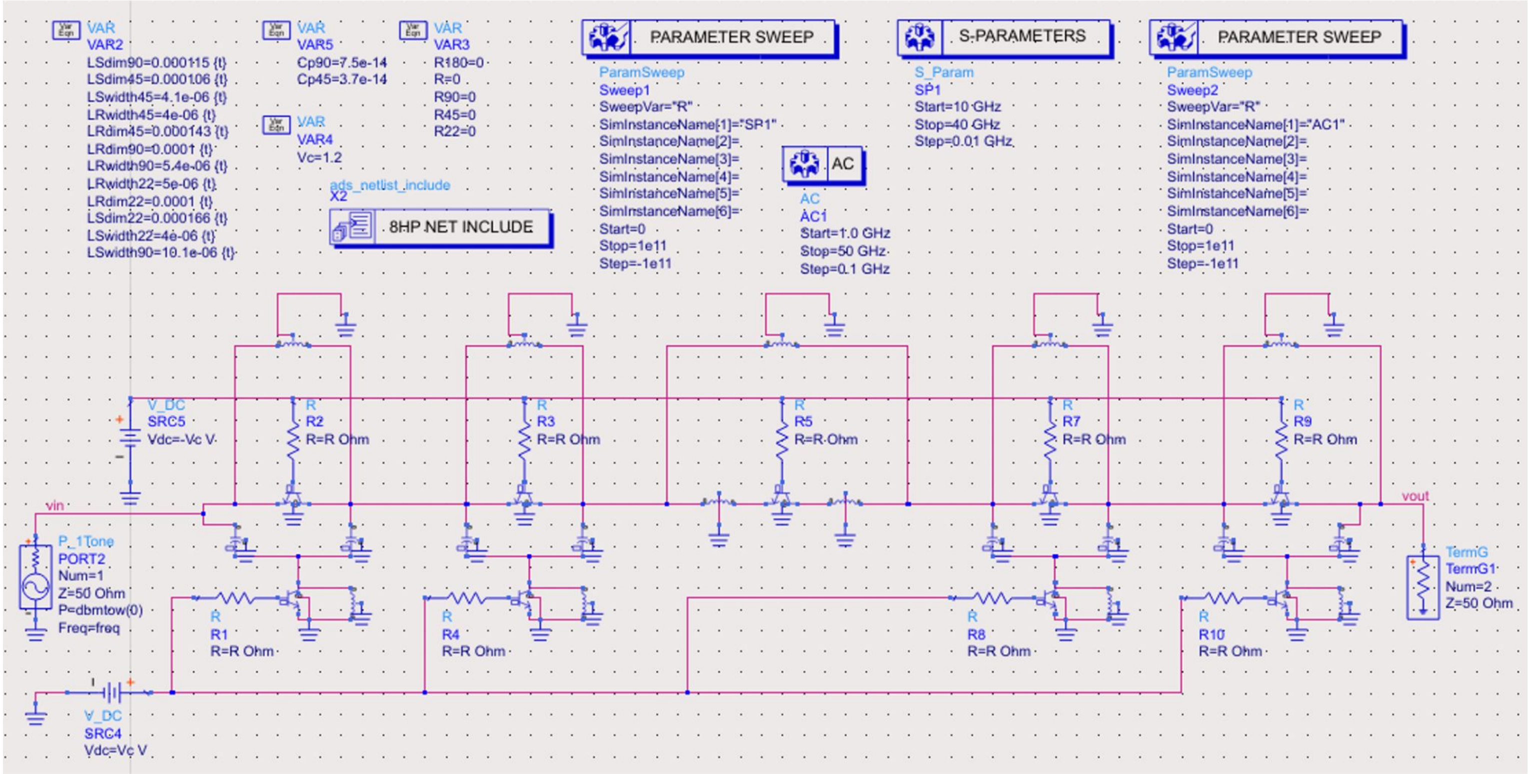
Appendix (Layout)



- Layout only attempted on PA output matching network.
- PDK elements used everywhere else

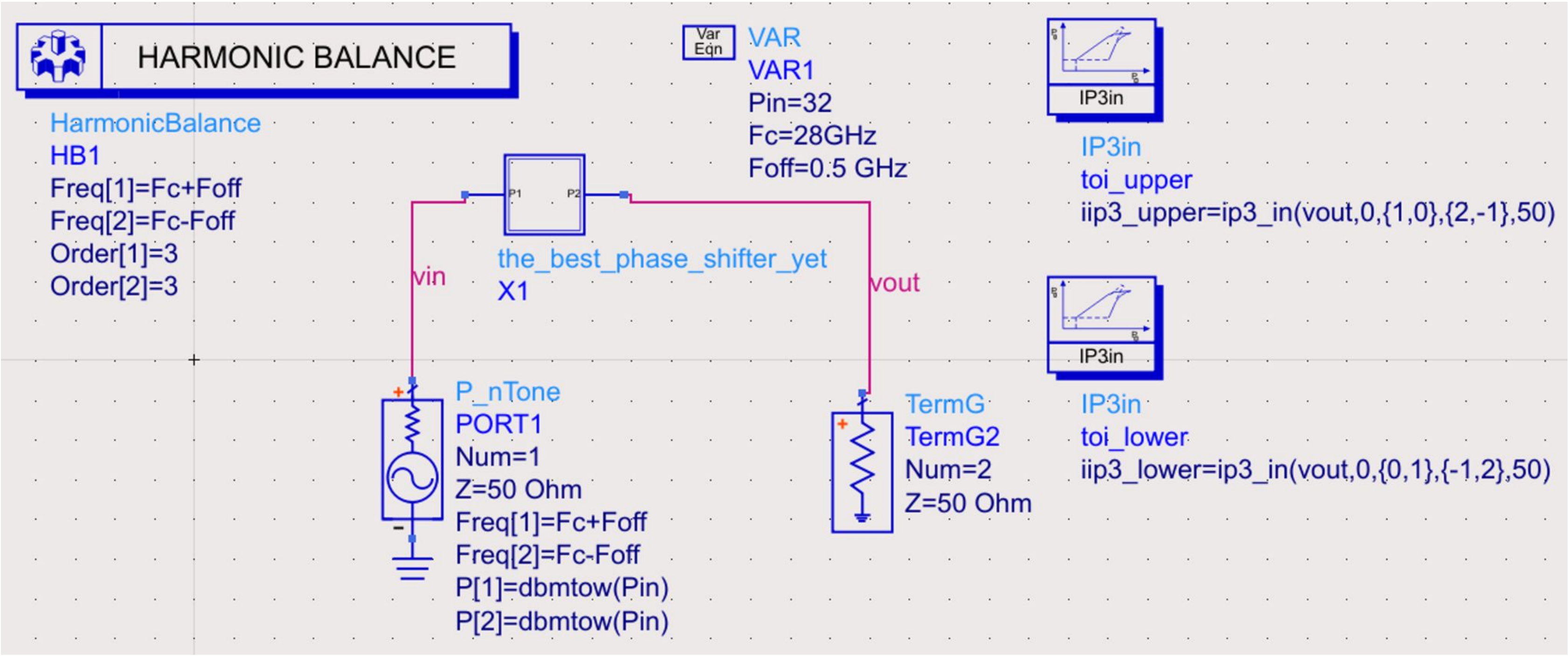


Appendix (Phase Shifter Testbenches)



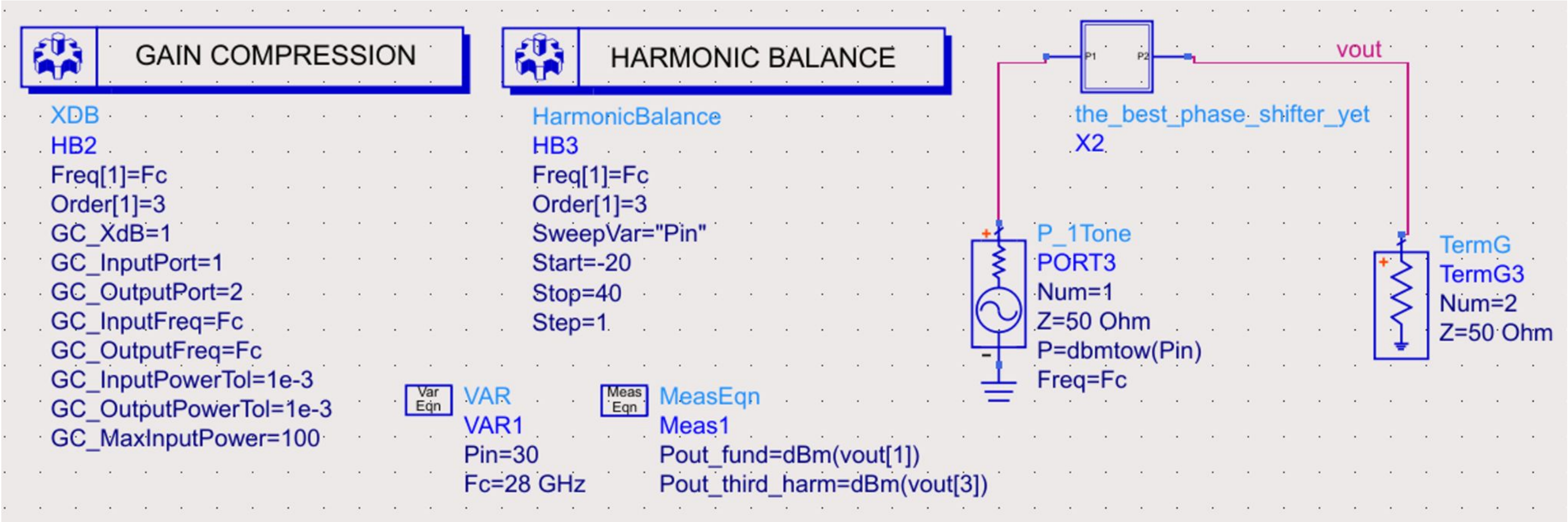
- Outputs data on slide 9 and slide 12
- Toggles “R” to plot maximum tunable phase shift range
- Evaluates S Parameters at the phase shift extremes

Appendix (Phase Shifter Testbenches)



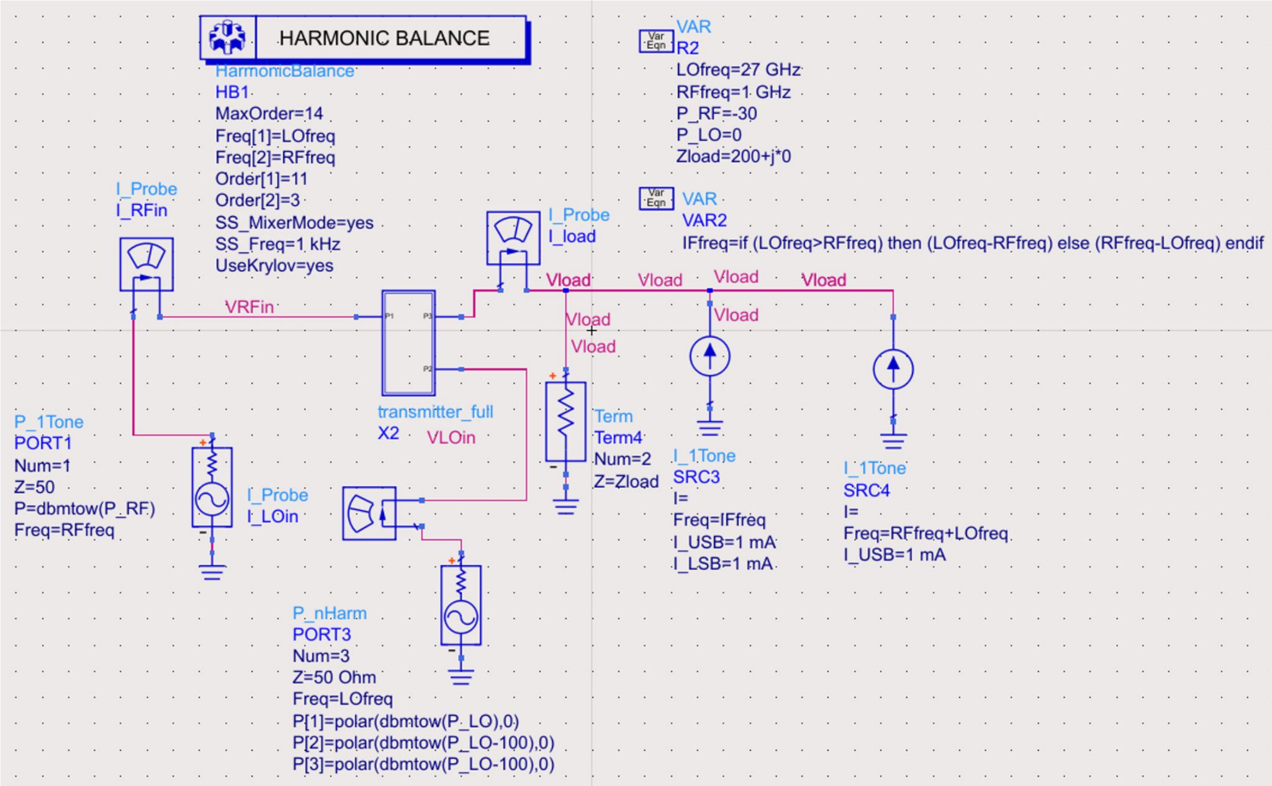
- Outputs data on slide 10
- Calculates third order intercepts from tones

Appendix (Phase Shifter Testbenches)



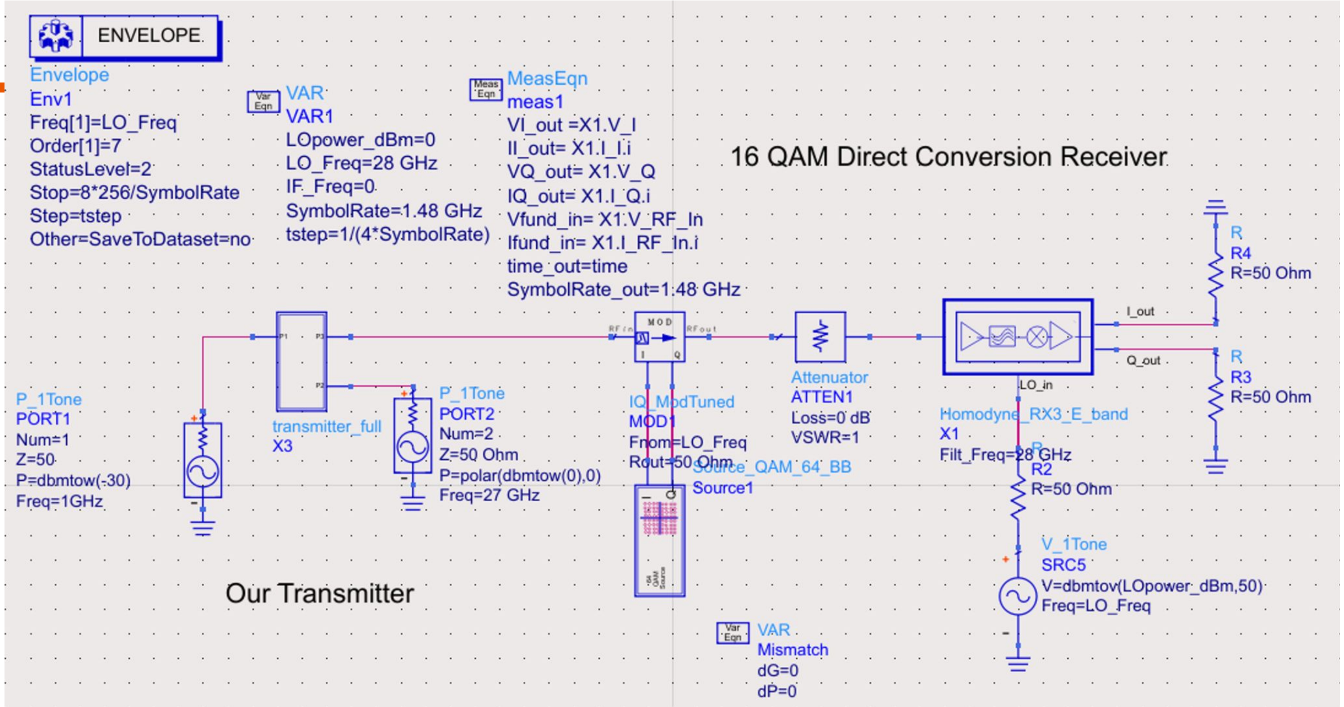
- Outputs data on slide 11
- Sweeps Pin to determine gain compression
- Used to plot Pout/Pin curves of the first and third harmonics

Appendix (Conversion Gain Testbench)



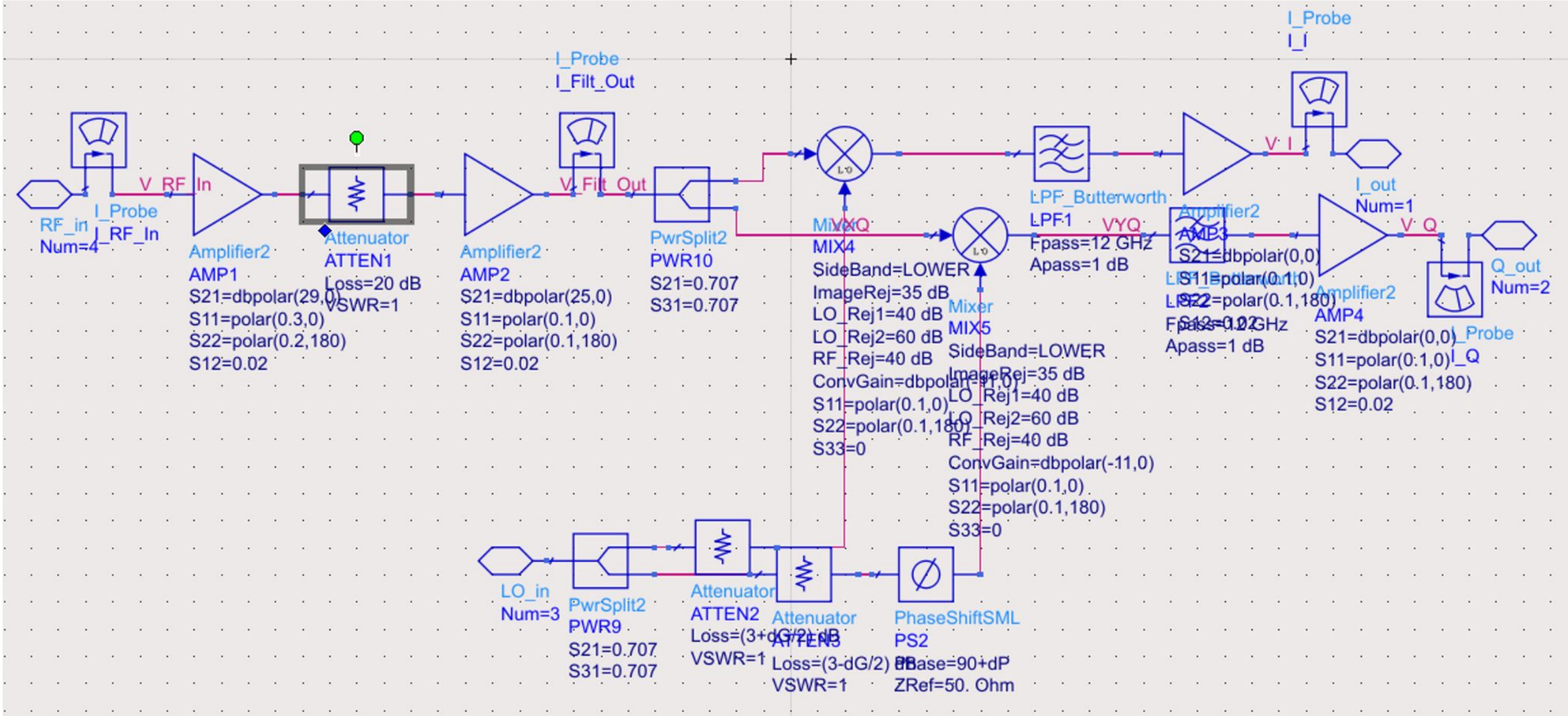
- Outputs data on slides 18-21
- Analyzes output spectrum

Appendix (EVM Testbench)

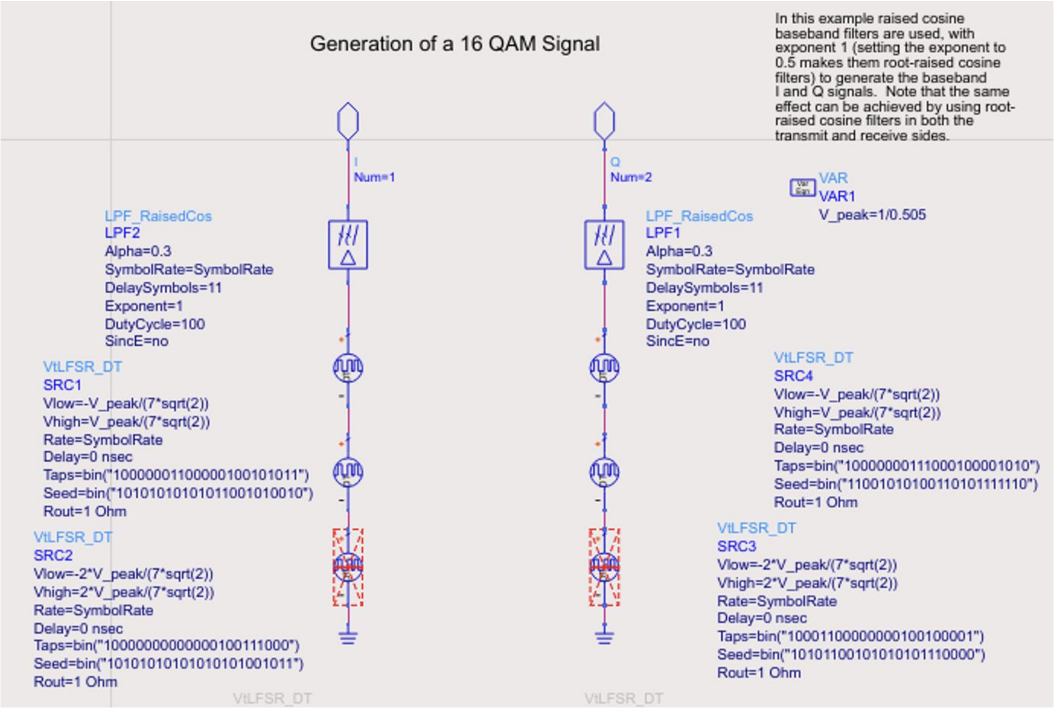


- Connects output to ideal receiver
- Calculates EVM

Appendix (EVM Testbench - Receiver)



Appendix (EVM Testbench - Modulation)



- Started with a 64QAM template and removed two bits

References

- “Harmonic Balance Simulations.” ADS Fundamentals, 2009. *Utdallas.edu.*
- “Switched Line Phase Shifters.” Microwaves101.COM. *microwaves101.com.*
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