

YM3812

DATA BITS:

D7	D6	D5	D4	D3	D2	D1	D0
Tremolo	Vibrato	EnvType	EnvScale	Frequency Multiplier			
Level Scaling		Total Level					
Attack Rate				Decay Rate			
Sustain Level				Release Rate			
x	x	x	x	x	x	Waveform	
Frequency Number (L)							
x	x	Key On	Frequency Block			FNum (H)	
x	x	x	x	Feedback			Algorithm
x	x	x	Test				
Timer 1							
Timer 2							
IRQ RST	Mask T1	Mask T2	x	x	x	ST2	ST1
CSM	SEL	x	x	x	x	x	x
Deep Trem	Deep Vib	Rhythm	BD	SD	Tom	TC	HH

REGISTER LOCATIONS:

	Channel 1		Channel 2		Channel 3		Channel 4		Channel 5		Channel 6		Channel 7		Channel 8		Channel 9	
Slot:	1	2	1	2	1	2	1	2	1	2	1	2	1	2	1	2	1	2
	M1	C1	M2	C2	M3	C3	M4	C4	M5	C5	M6	C6	M7	C7	M8	C8	M9	C9
Op:	1	4	2	5	3	6	7	10	8	11	9	12	13	16	14	17	15	18
	+0	+3	+1	+4	+2	+5	+8	+B	+9	+C	+A	+D	+10	+13	+11	+14	+12	+15

Drum Channels (if enabled): x x x

Base Address

Operator Register Locations (HEX):

20	20	23	21	24	22	25	28	2B	29	2C	2A	2D	30	33	31	34	32	35
40	40	43	41	44	42	45	48	4B	49	4C	4A	4D	50	53	51	54	52	55
60	60	63	61	64	62	65	68	6B	69	6C	6A	6D	70	73	71	74	72	75
80	80	83	81	84	82	85	88	8B	89	8C	8A	8D	90	93	91	94	92	95
E0	E0	E3	E1	E4	E2	E5	E8	EB	E9	EC	EA	ED	F0	F3	F1	F4	F2	F5

Channel Register Locations (HEX):

A0	A0	A1	A2	A3	A4	A5	A6	A7	A8
B0	B0	B1	B2	B3	B4	B5	B6	B7	B8
C0	C0	C1	C2	C3	C4	C5	C6	C7	C8

Global Register Locations (HEX):

01	01
02	02
03	03
04	04
08	08
BD	BD

+5V DC	VCC	1	24	CLK	Master Clock Input (3.568 MHz)
Interrupt Request (Open Drain)	IRQ	2	23	SY	Clock Output to D/A Converter
Initialize / Clear	IC	3	22	NC	
Register / Data Select	A0	4	21	SO	Serial Output to D/A Converter
Write	WR	5	20	SH	Sample & Hold to D/A Converter
Read	RD	6	19	NC	
Chip Select	CS	7	18	D7	Data Bus Input
	NC	8	17	D6	Data Bus Input
	NC	9	16	D5	Data Bus Input
Data Bus Input	D0	10	15	D4	Data Bus Input
Data Bus Input	D1	11	14	D3	Data Bus Input
Ground	GND	12	13	D2	Data Bus Input