ENG306 - Power Electronics - Lab 3

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Contents

1 Introduction

This lab report outlines the experimental investigation of three distinct types of DC-DC converters, namely the buck converter, the boost converter, and the buck-boost converter. Throughout the lab, we explored the efficiency and performance of each topology. The buck converter lowers the input voltage while providing a higher output current. The boost converter elevates input voltage and is essential for applications needing higher voltage levels from a lower voltage supply. Finally, the buck-boost converter combines the features of both buck and boost converters, allowing for both voltage step-up and step-down operations. By conducting a series of measurements, including voltage ripples, efficiency at various operating points, and comparing theory with experimental results, we obtained a deeper understanding of how DC-DC converters work.

2 Buck Converter

Table 1: Data collected from buck converter

Duty Cycle (%)	Input Voltage (V)	Input Current (mA)	Output Voltage (V)	Output Current (mA)	Calculated Efficiency (%)
0	20	0	0	0.0004	0
10	20	3	1.5	15	33
20	20	7	3.4	30	71
30	20	15	5.2	48	83
40	20	30	7.0	71	83
50	20	48	9.2	92	88
60	20	69	12.0	109	95
70	20	94	13.0	133	92
80	20	120	15.0	148	93
85	20	137	16.0	158	92

1 Ohm resistors were placed in series with the capacitor and inductor because it would allow the oscilloscope to measure the current. Using Ohms law it can be seen that $V = IR = I$ if the resistance is 1, hence the voltage over the resistor is equal to the current. This allows us to place the oscilloscope probes over the resistor to measure the current.

Oscilloscope probes ground clips are all connected together, there is a direct connection from probe 1 ground to probe 2 ground and so on. This means that if they are not connected to the sample place then a short will occur, which will effect how the circuit will function. For this circuit it was chosen that ground probe to be placed at the same node that connects the inductor, capacitor and load as it would allow us to measure the inductor voltage, inductor current, output voltage and capacitor current on oscilloscope plot.

The 1 Ohm resistor should be closest to the common measurement point (oscilloscope ground clip). This is because the only the voltage over the 1 ohm resistor should be measured to display the current capacitor waveform. If the resistor was placed after the capacitor (the ground side), the measurement would be the capacitor voltage and the 1 ohm resistor voltage which is not equivalent to the capacitor current.

Channels 3 and 4 will need to be inverted to display positive waveforms. V_o will be inverted as the positive and negative probes are inverted. i_c is also inverted as the positive probe is at the negative side of the current sensing resistor.

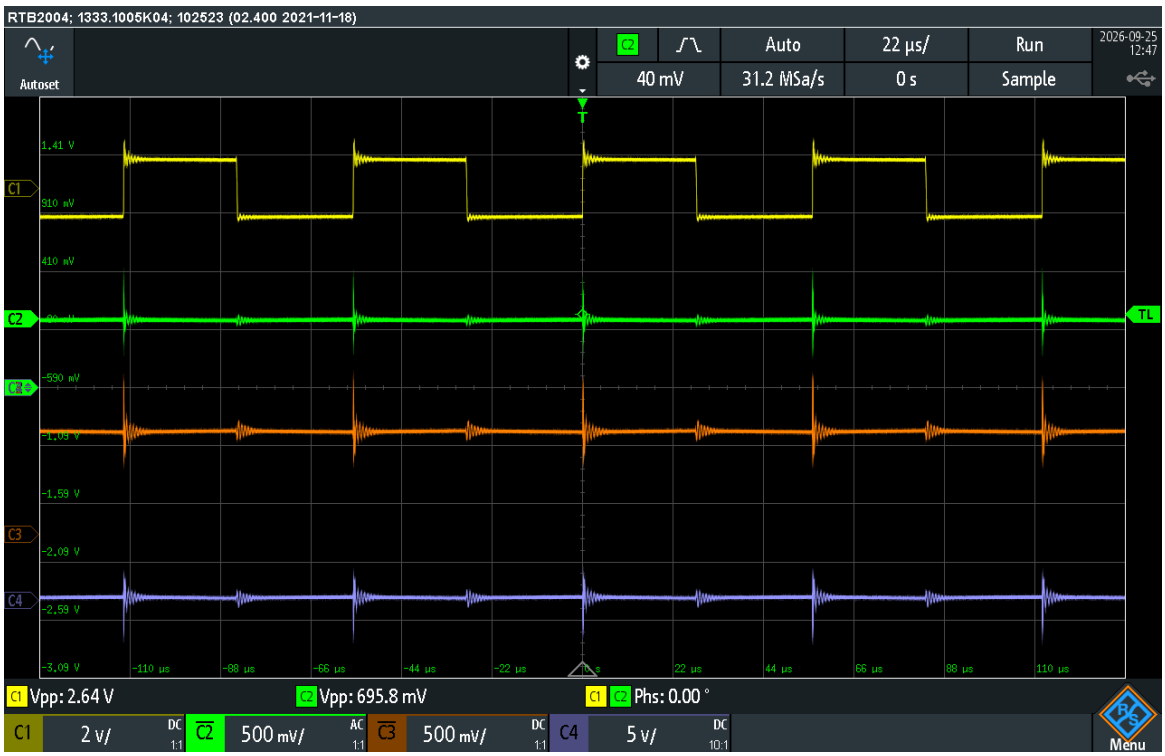

Figure 1: Buck converter oscilloscope plot with one inductor. Ch1: inductor voltage, Ch2: inductor current, Ch3: output voltage and Ch4: capacitor current

Looking at Figure 1 it can be seen that the voltage across the inductor varied with the duty cycle, as the duty cycle was increased the amount of time the inductor voltage was non-zero increased, this can be seen from the circuit diagram. When the MOSFET is on the voltage across the inductor is equal to the input voltage, and when the MOSFET is off the inductor voltage is zero. As the duty cycle was varied the output voltage varied with it, increasing the duty cycle increased the output voltage and vice versa for decreasing the duty cycle. This can easily be seen to be correct by looking at the equation $V_o = DV_d$, the output voltage is directly proportional to the duty cycle.

To determine when the buck converter is CCM we can use the following calculation.

$$
\begin{aligned}
L_{\min} &= \frac{(1-D)R}{2f_s} \\
\Rightarrow D &= 1 - \frac{2L_{\min}f_s}{R} \\
D &= 1 - \frac{2 \cdot 3 \times 10^{-3} 15 \times 10^3}{100} \\
D &= 10\%
\end{aligned}
$$

This indicates that operating the converter below 10% duty cycle then it will be running in DCM.

For a 20% duty cycle the minimum required frequency can be calculated, as seen in the following.

$$
\begin{aligned}
L_{\min} &= \frac{(1-D)R}{2f_s} \\
\Rightarrow f_s &= \frac{(1-D)R}{2L_{\min}} \\
f_s &= \frac{(1-0.2)100}{2 \cdot 3 \times 10^{-3}} \\
f_s &= 13.3\ kHz
\end{aligned}
$$

The acquired frequency is 13.3 kHz, which is close to the approximate frequency used of 15 kHz, so it would be expected that the efficiency is particularly bad for some duty cycle close to 20% as the buck converter would enter DCM. It can be seen in Table 1 that the efficiency is very low for a 10% duty cycle and moderately low for a 20% duty cycle, this means that the converter must have entered DCM at point between 10% and 20% duty cycle.

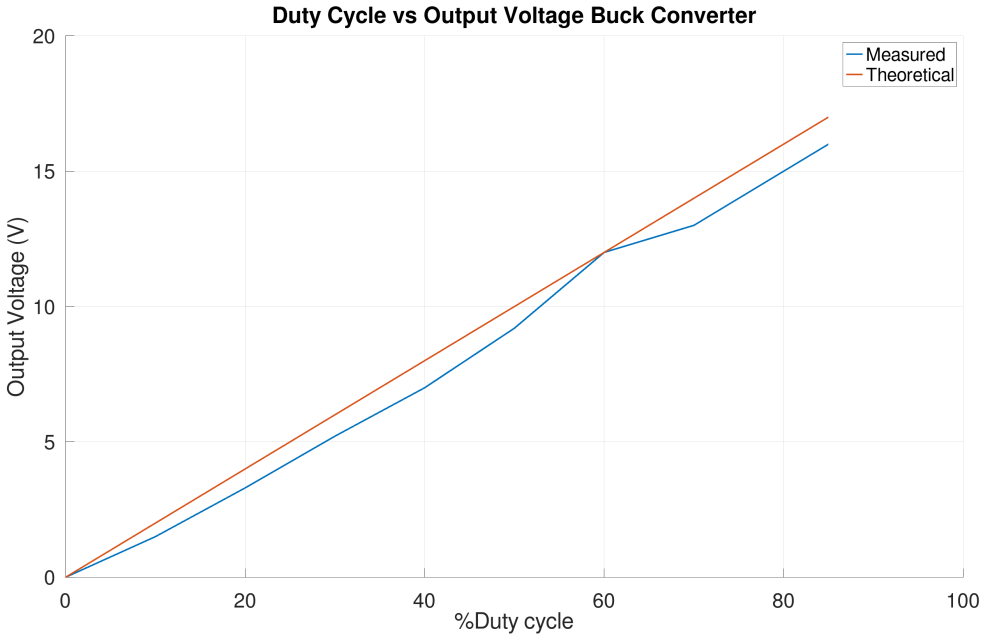

Figure 2: Theoretical and measured duty cycles compared

An output voltage versus duty cycle plot can be seen in Figure 2 and the code that produced it can be seen in Appendix A, it contains both measured and theoretical results. The theoretical plot was obtained by applying duty cycles ranging from 0% to 100% to the equation $V_o = V_d D$. It can be seen that the measured plot closely follows the theory, there is a noticeable constant negative drop for the measured values which is mainly due to losses in the MOSFET and diode as the theory does not account for this.

The voltage ripple at 20% duty cycle was measured to be: $\frac{\Delta V_o}{V_o} = \frac{3.4V}{3.7V} = 0.92$. Lets compare this to the theoretical value.

$$\frac{\Delta V_o}{V_o} = \frac{1}{8}\frac{T_s^2(1-D)}{LC}$$
$$\frac{\Delta V_o}{V_o} = \frac{1}{8}\frac{\left(15\times 10^3\right)^2(1-0.2)}{3\times 10^{-3}\cdot 100\times 10^{-6}}$$
$$\frac{\Delta V_o}{V_o} = 0.00148$$

This is obviously wrong, the value obtained is close to three orders of magnitude off. This is because of incorrect measurement during the lab, more specifically the change in output voltage (ΔV_o) is wrong. The oscilloscope should have been zoomed in so the triangular shape could be seen easier and the change in output voltage should have been manually recorded. However, a theoretical ΔV_o can be

calculated using the same equation, as seen in the following equation.

$$\Delta V_o = \frac{V_o}{8}\frac{T_s^2(1-D)}{LC}$$
$$\Delta V_o = \frac{3.4}{8}\frac{\left(15\times10^3\right)^2(1-0.2)}{3\times10^{-3}\cdot100\times10^{-6}}$$
$$\Delta V_o = 0.005\ V$$

This value is much more reasonable, giving us a voltage ripple of $\$\Delta V_o \frac{}{V_o=\frac{0.005}{3.7}=0.00135\$y}$

2.1 Doubling Inductance

Figure 3: Buck converter oscilloscope plot with two inductors in series. Ch1: inductor voltage, Ch2: inductor current, Ch3: output voltage and Ch4: capacitor current

looking at Figure 3 it can be seen that doubling the inductance the inductor current slope is lower, this is because it takes longer for the energy to charge and discharge, this can slightly be seen in Figure 3. The output voltage contains less ripple, the increased inductance allows a more constant current flow, reducing the ripple.

The required duty cycle for the new inductance can be calculated, as seen in the following.

$$L_{\min} = \frac{(1-D)R}{2f_s}$$
$$\Rightarrow D = 1 - \frac{2L_{\min}f_s}{R}$$
$$D = 1 - \frac{2\cdot6\times10^{-3}15\times10^3}{100}$$
$$D = -80\%$$

The required duty cycle for DCM is negative meaning the buck converter will never reach DCM for a non-zero duty cycle.

If it was not known what the inductance was it would be possible to calculate it by measuring the change in inductor current (Δi_L), the output voltage (V_o), the duty cycle (D) and the switching frequency (f_s). Knowing these values it can simply be put into the following equation and solving for L.

$$\Delta i_L = \frac{V_o}{L f_s}(1 - D)$$

3 Boost Converter

Table 2: Data collected from boost converter

Duty Cycle (%)	Input Voltage (V)	Input Current (mA)	Output Voltage (V)	Output Current (mA)	Calculated Efficiency (%)
0	10	87	8.7	87	87
10	10	111	9.6	96	83
20	10	140	10.8	108	83
30	10	167	11.7	117	81
40	10	233	13.6	136	79
50	10	325	15.7	157	75
60	10	438	17.8	178	72
70	10	773	21.8	219	61
80	10	1260	24.6	247	48
85	10	1600	24.8	249	38

Figure 4: Buck converter oscilloscope plot. Ch1: capacitor current

Figure 5: Boost converter oscilloscope plot. Ch1: inductor voltage, Ch2: inductor current

The inductor waveform for the boost converter is the same as the one for the buck converter. Increasing the duty cycle changes the on time and off time for the inductor voltage and the width of the triangles in the inductor current. It can slightly be seen in Figure 5 that the inductor current exhibits the expected triangular waveform, although the magnitude is small. It appears that the inductor is discharging for positive inductor voltages, however this is due to measuring the negative of the current which means that it the inductor is storing energy for positive voltages and releasing it for negative voltages, this aligns with the theory.

Using the following equation the plot in Figure 6 can be made, the code that produced it can be seen in Appendix B. It relates the duty cycle to minimum required frequency, we can then take the maximum value and that will be the minimum required frequency for all duty cycles. Looking at the plot it can be seen that the maximum is 2468.9 Hz.

$$f_s = \frac{D(1-D)^2 R}{2L_{\min}}$$

$$f_s = \frac{D(1-D)^2 100}{2 \cdot 3 \times 10^{-3}}$$

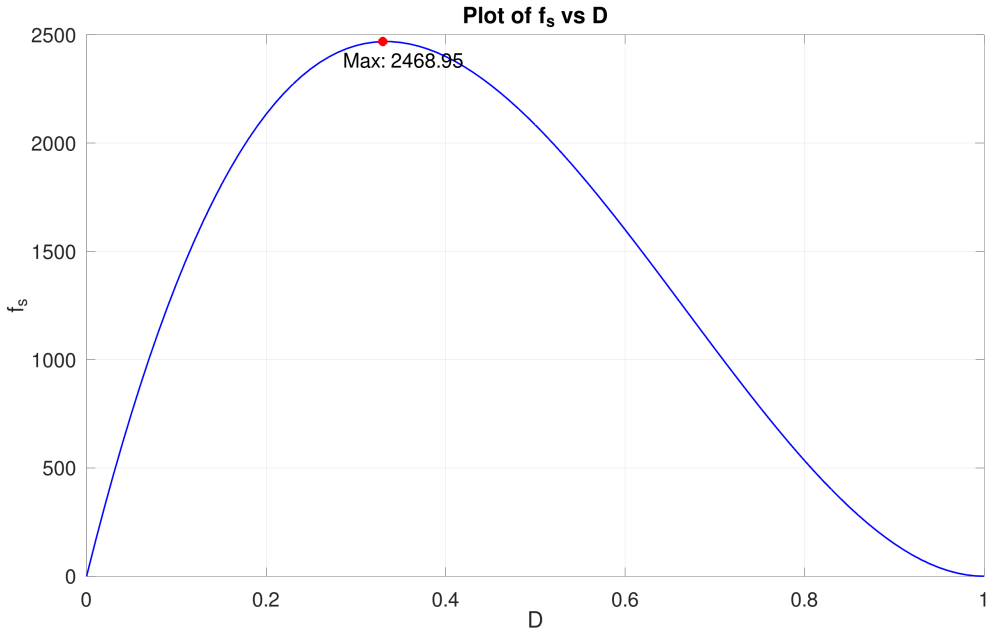

Figure 6: Boost converter switching frequency compared with duty cycle

4 Buck-Boost Converter

Table 3: Data collected from buck-boost converter

Duty Cycle (%)	Input Voltage (V)	Input Current (mA)	Output Voltage (V)	Output Current (mA)	Calculated Efficiency (%)
0	10	0	0	0.075	0
10	10	1	0.6	6	40
20	10	4	1.4	14	50
30	10	14	2.9	29	60
40	10	36	4.5	46	58
50	10	80	7.3	74	68
60	10	170	10.5	106	65
70	10	356	14.4	145	59
80	10	827	19.0	191	44
85	10	1300	20.2	203	32

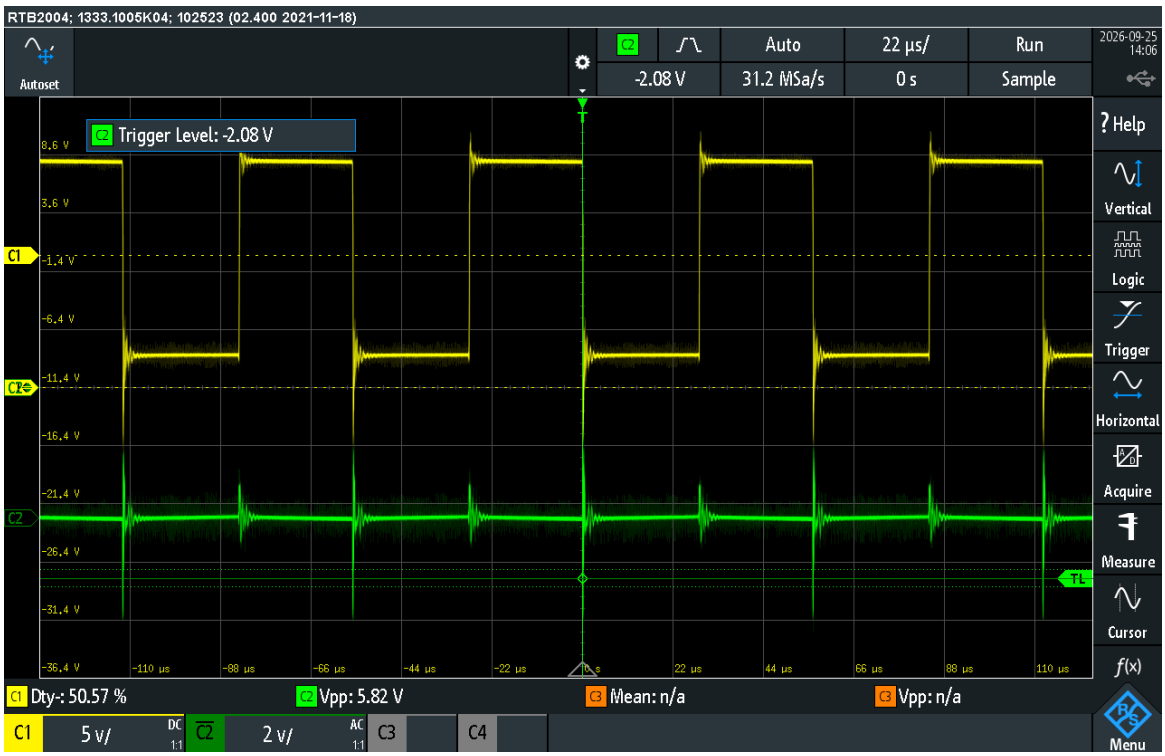

Figure 7: Buck-boost converter oscilloscope plot. Ch1: inductor voltage, Ch2: inductor current

Figure 8: Buck-boost converter oscilloscope plot. Ch3: output voltage, Ch4: inductor current

The measured output voltage at 50% duty cycle is -7.3V. To calculate a theoretical value use the formula, $V_0 = V_d \frac{D}{1-D} = -10V$. This error is likely caused by losses in the buck-boost converter. Sources of losses are discussed further in the later section.

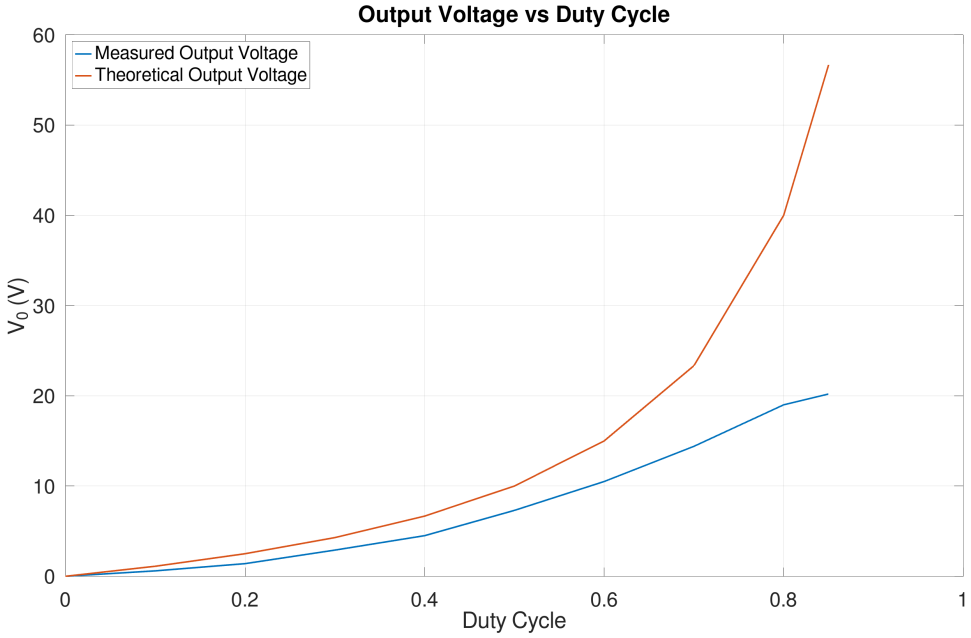

Figure 9: Measured output voltage compared to theoretical output voltage versus duty cycle

The plot of output voltage versus duty cycle, as seen in Figure 9 produced by the code in Appendix C, shows noticeable difference between the theoretical curve and the measured value. While both curves follow the expected nonlinear trend of the buck-boost converter, the measured output is consistently lower than the theoretical curve across the full duty cycle range. This shows that whilst the theoretical curve correctly describes the relationship between duty cycle and output voltage, real converter operation is affected by component non-ideality and practical losses. Sources of potential circuit loss are further detailed in the section below. This difference shows the importance of reviewing converter efficiency, as well as demonstrating issues in theoretical assumptions.

4.1 Buck-Boost Losses

1. Conduction Losses When the switch is on current flows through the MOSFET channel resistance $R_{DS(on)}$ causing I^2R losses. At higher duty cycles the switch conducts for longer so the conduction losses increase. When the switch is off current flows through the diode and energy is lost across its forward voltage. As duty cycle increases and the switch is on for longer the diode conducts for less time, lowering the forward voltage losses. The inductor winding has resistance R_L causing I^2R losses proportional to the average inductor current. At low duty cycles (buck mode) current is higher for step-down so losses are higher. At high duty cycles (boost mode) current stress also increases so losses rise again. Losses are minimal around the crossover duty cycle.

2. Switching Losses Energy is lost during voltage-current overlap when switching. Switching frequency remains constant with duty cycle but average inductor current changes with duty cycle. Higher duty cycle means higher inductor current, leading to higher switching losses.

3. Inductor Core Losses Hysteresis and Eddy Currents are caused in the inductor core by alternating flux. Loss depends on the ripple currents. At medium duty cycles ripple is large so core losses are maximised. At extreme high/low duty cycles the ripple current is smaller so losses are minimised.

4. Capacitor ESR Losses Capacitor Equivalent Series Resistance (ESR) causes $I^2_{C,ripple}R$ heating.

Ripple current depends on load and duty cycle. Near 50% duty cycle ripple is highest, so ESR losses increase.

5. Parasitic Losses Parasitic inductance and capacitance in wiring cause extra minor switching losses. Not strongly duty cycle dependant but worsens under higher current stress at high/low duty cycles.

Combining these sources of loss the theoretical highest efficiency duty cycle range should be around $D = 0.4 \leftrightarrow 0.6$ where diode and switch conduction losses balance and ripple current is not too high. Comparing this theoretical efficiency to the measured efficiency provides similar results, with the peak efficiency from $D = 0.3 \leftrightarrow 0.6$. Efficiency at extreme duty cycles are low as expected, due to high current stresses and other sources as mentioned previously.

5 Reflection

This lab task serves to emphasis key differences between DC-DC converter topologies. The buck converter stepping down voltage based on the MOSFET gate PWM signal duty cycle with high average efficiency, notably most efficient at higher duty cycles. The boost converter stepping up voltage again based on the MOSFET gate PWM signal duty cycle, with an average efficiency of 0.8%. The boost converter has high input current draw due to the relationship $P_{in} = P_{out}$. This means that for a constant input voltage, input current must increase when P_{out} increases. The buck-boost converter performs both voltage step down and up dependent on the MOSFET gate PWM signal duty cycle, however overall efficiency is lower due to higher conduction losses from increased RMS currents. The buck-boost converter also causes inverted output voltage as the ground because the inductor is fixed to ground, causing the inductor to switch between input and ground, discharging into the capacitor with reversed polarity.

Overall, this task was informative, highlighting major advantages and disadvantages with common DC-DC converter topologies.

6 Appendix A

```
clc
clear
close all;

if exist('OCTAVE_VERSION', 'builtin')
  set(0, "DefaultLineLineWidth", 2);
  set(0, "DefaultAxesFontSize", 25);
  warning('off');
end

V_d = 20;

D = [0, 10, 20, 30, 40, 50, 60, 70, 80, 85];
V_out = [0, 150e-3*10, 330e-3*10, 521e-3*10, 700e-3*10, 920e-3*10, 1.2*10, 1.3*10, 1.5*10,
↪  1.6*10];

D_theo = 0:0.1:85;
V_out_theo = V_d*D_theo/100;

figure;
hold on;
plot(D, V_out);
plot(D_theo, V_out_theo);

legend("Measured", "Theoretical");
xlabel("%Duty cycle")
ylabel("Output Voltage (V)")
title("Duty Cycle vs Output Voltage Buck Converter")
grid on;
print -dpng 'ENG306_D_vs_Vout_Buck.png'
```

7 Appendix B

```
clc
clear
close all;

if exist('OCTAVE_VERSION', 'builtin')
  set(0, "DefaultLineLineWidth", 2);
  set(0, "DefaultAxesFontSize", 25);
  warning('off');
end

D = 0:0.01:1;
f_s = (D .* (1 - D).^2 .* 100) / (2 * 3e-3);

[max_value, max_index] = max(f_s);
max_D = D(max_index);

figure;
plot(D, f_s, 'b-', 'LineWidth', 2);
hold on;

plot(max_D, max_value, 'ro', 'MarkerSize', 10, 'MarkerFaceColor', 'r');
text(max_D - 0.05, max_value - 50, sprintf(' Max: %.2f', max_value), 'VerticalAlignment',
↪  'top', 'HorizontalAlignment', 'left', 'FontSize', 25);

xlabel('D');
ylabel('f_s');
title('Plot of f_s vs D');
grid on;
hold off;
print -dpng 'ENG306_Frequency.png'
```

8 Appendix C

```
clc
clear
close all
if exist('OCTAVE_VERSION', 'builtin')
  set(0, "DefaultLineLineWidth", 2);
  set(0, "DefaultAxesFontSize", 25);
  warning('off');
end

Vin = 10;
D = [0, 10, 20, 30, 40, 50, 60, 70, 80, 85]*0.01;

Vo = [0, 0.6, 1.4, 2.9, 4.5, 7.3, 10.5, 14.4, 19.0, 20.2];
Votheory = Vin*(D./(1.-D));

figure;
plot(D,Vo)
hold on;
plot(D,Votheory)
title('Output Voltage vs Duty Cycle')
xlabel('Duty Cycle')
ylabel('V_0 (V)')
legend('Measured Output Voltage','Theoretical Output Voltage', 'location', 'northwest')
grid on;
print -dpng 'Part_4_Buck_Boost_V0.png'
```