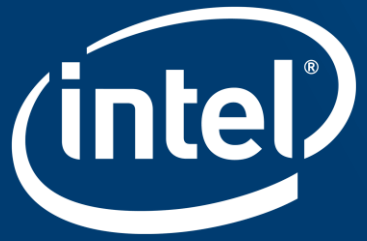
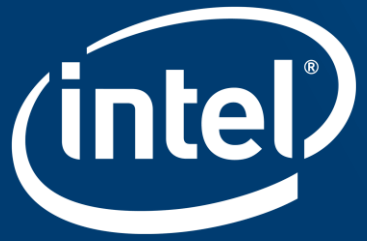


MAX 10 FPGAS → REVOLUTIONIZING NON-VOLATILE INTEGRATION!

November 2017

Speaker:
Marco Smutek – Arrow
Marco.smutek@arrow.com



MAX 10 FPGAS – ARCHITECTURAL DETAILS

MAX 10 FPGA – Architectural Sections

Analog Block

Configuration

- Instant-On
- Design Security
- SEU Mitigation

User Flash Memory

Core Fabric

- Core Architecture
- DSP
- PLL
- Clocking
- Internal Memory
- Power Savings

Power

- Voltage Regulator

I/O

- General Purpose I/O
- LVDS
- External Memory Interface (EMIF)

Internal Oscillator

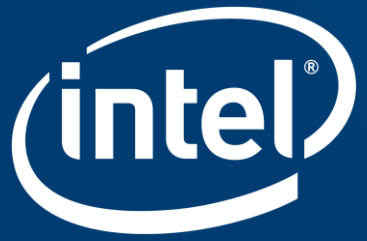
Target Applications

Power supply variant differences

Feature	Single Supply Variant	Dual Supply Variant
Core Speed	Fmax = 100 MHz	Fmax = 150+ MHz
DSP	Up to 198 MHz	Up to 234 MHz
LVDS	200 – 400 Mbps	380 – 830 Mbps
EMIF	Not Supported	DDR2 / LPDDR2 @ 200 MHz DDR3 @ 300 MHz
RAM Blocks	Up to 232 MHz	Up to 330 MHz
DSP Blocks	Up to 198 MHz	Up to 310 MHz
PLLs	Single PLL support	Up to 4
Analog Block	SNR: 54 dB SINAD: 53 dB	SNR: 62 dB SINAD: 61.5 dB

Single supply devices optimized for Simplicity

Dual supply devices offer increased Performance



MAX 10 FPGA – ANALOG BLOCK

Advantages of Hard IP Integration

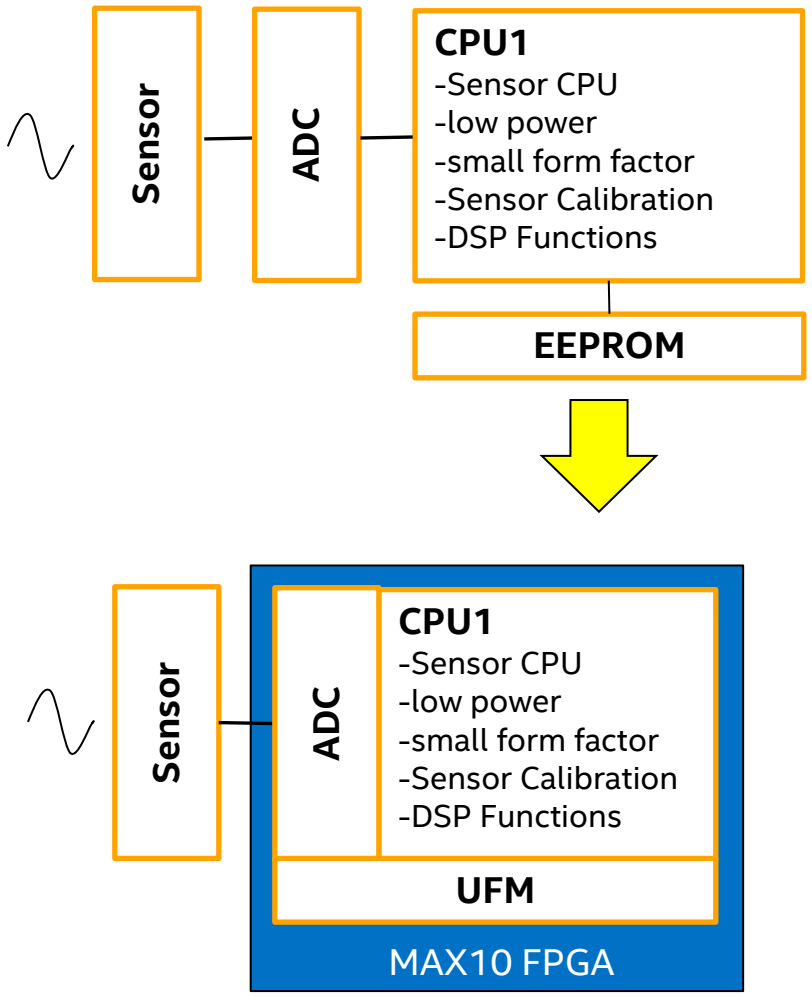
The real world is analog

- Integration of analog blocks allows direct mixed signal support
- Reduce components count at front end

Benefits of Integration

- Reduced device I/O count
- GUI based configuration
- Flexible sample sequence
- Faster data output
- Simultaneous Sampling

$$$ + space savings!



An Overview of ADC Technologies

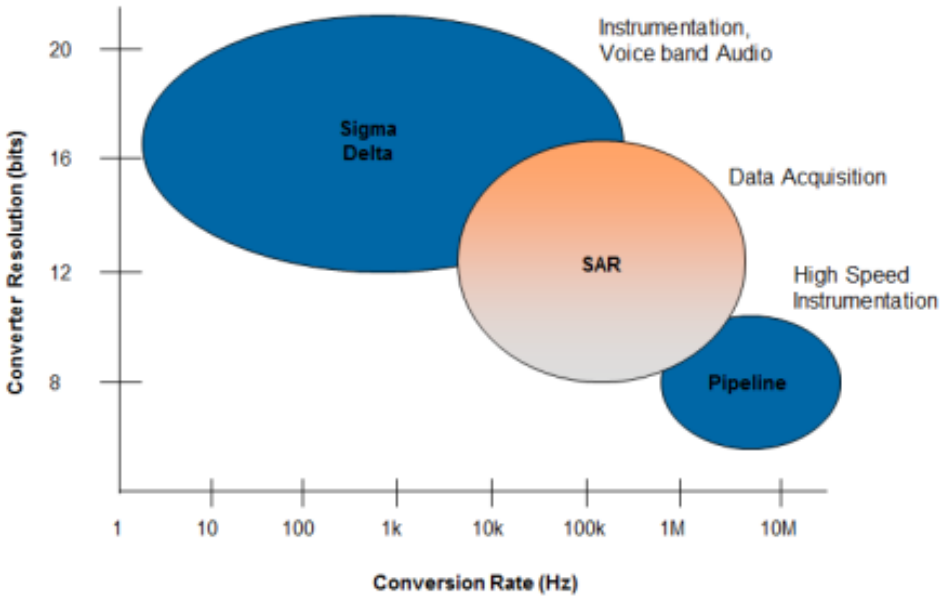
Three Main Types of ADC

- Sigma Delta
- Successive Approximation Register (SAR)
- Pipeline

The selection of the right architecture is a very crucial decision

ADC's are generally characterised in three ways

- Bandwidth / Conversion Rate
- Output Resolution
- Input Voltage Range
- Signal to Noise Ratio (SNR)



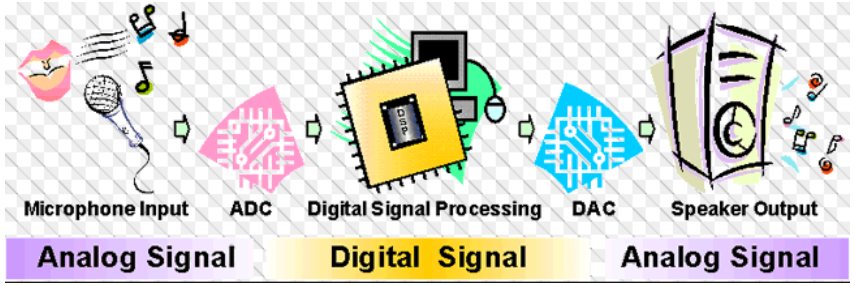
MAX10 ADC – Successive Approximation Register (SAR)

Advantages

- Zero-cycle Latency
- Low latency-time
- High Accuracy
- Low Power
- Easy to use
- Programmable alarm detection
- System simulation support

ADC (SAR) Applications

- Data Logging
  - Temperature sensors
  - Voltage sensors
  - Pressure sensors
- Motor Control
  - Bridge Sensors
- Displacement / Proximity measurement

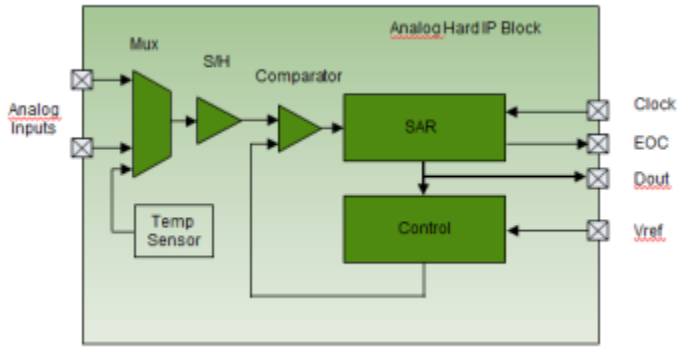


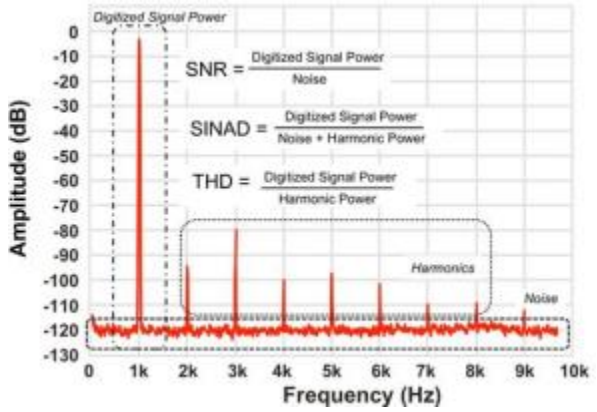
The Real World is analog

Analog Hard IP Block

12-bit SAR ADC

- Single or Dual mode operation
  - Supports simultaneous input sampling
- 18 Analog inputs
  - 1 Dedicated analog I/O per ADC
  - 16 Shared pads with GPIO
    - Includes pre-scaler channels
- ADC Performance
  - SNR 62dB*
  - SINAD 61.5dB*
  - THD 70dB*
- Variable sample rate
  - 25Ksps to 1Msps (per ADC)
- Temperature Sensing Diode
  - Operating Range -40°C to +125°C





ADC measurement criteria definitions

* Note: with prescalar enabled is 6dB less

ADC Megawizard

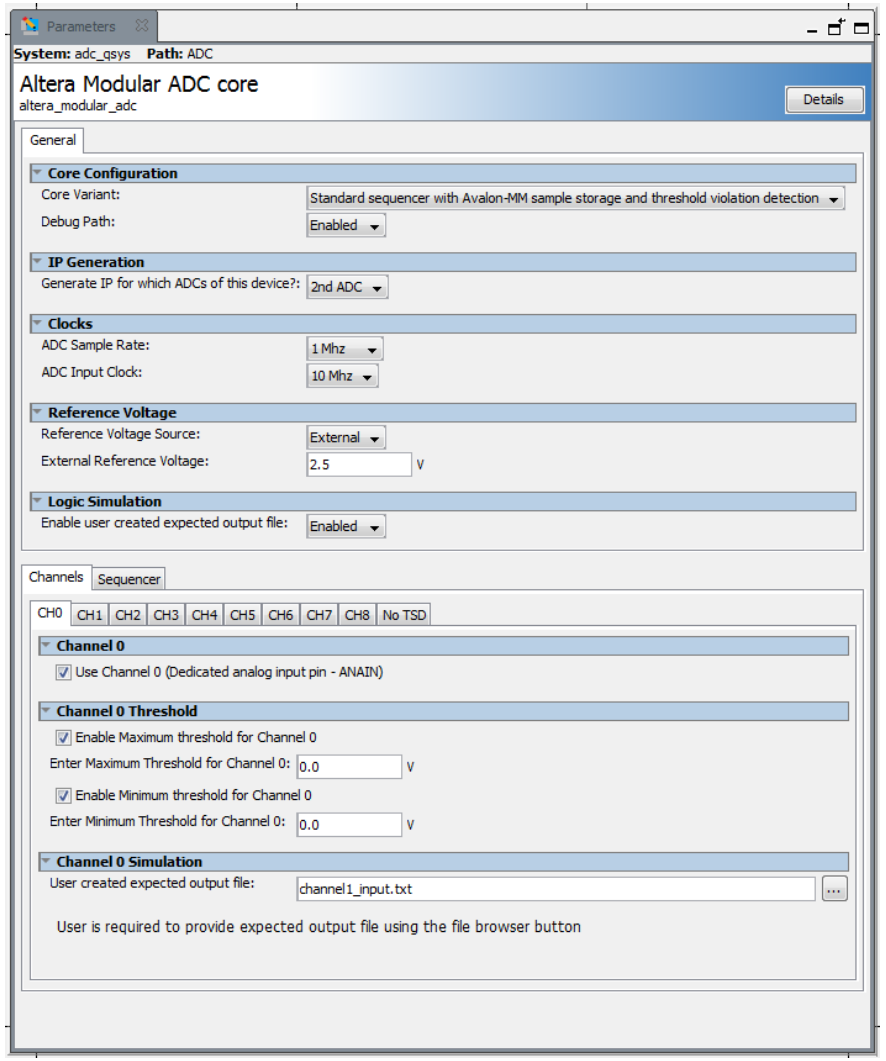
Modular Design

- ADC Block
- Sequencer
- Sample Store
- Debug Port (Analog Toolkit)
- Single or Dual ADC core

Input threshold detection

64 sample, fully programmable sequencer

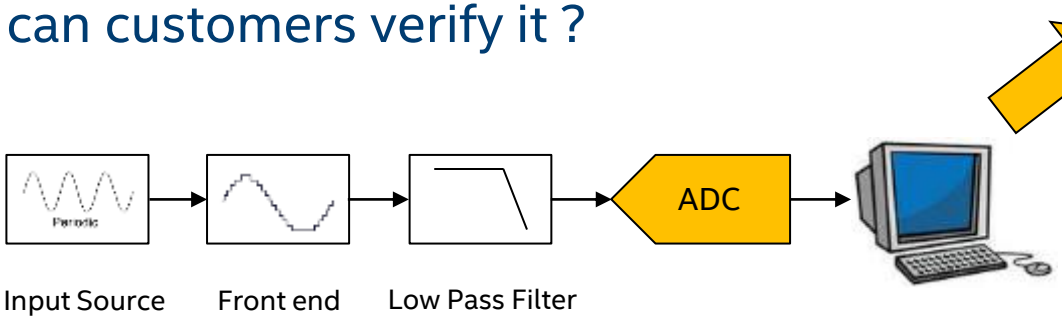
Internal or external reference



The Analog Toolkit - ADC Debug

What effects analog system performance ?

- Basic ADC architecture itself
- Signal integrity of the analog front end signal path
- But how can customers verify it ?



Analog Toolkit

- Select channel you wish to monitor
- Apply a clean sinewave
- Copy of each sample sent to pc
- FFT, INL, DNL analysis

No extra software, equipment or cost required

It works !

ADC Channel Count by Die / Package

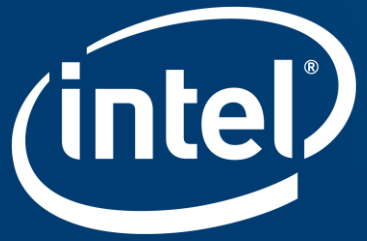
ADC Channel GPIO count per device / package option

- Additional Dedicated Analog input per ADC block
- Temperature Sensing Diode only available on ADC1
- Only 8 channels are migratable from 10M04 to 10M50 for ADC1

Package Details	Type	36-WLCSP	81-WLCSP	144-EQFP	153-MBGA	169-UBGA	256-FBGA	324-UBGA	324-UBGA	484-FBGA	672-FBGA
	Voltage	Dual	Dual	Single	Single	Single	Dual	Dual	Single	Dual	Dual
MAX 10 FPGA	10M04	-	-	8+0	8+0	8+0	16+0	16+0	16+0	16+0	-
	10M08	-	-	8+0	8+0	8+0	16+0	16+0	16+0	16+0	-
	10M16	-	-	8+0	-	8+0	16+0	16+0	16+0	16+0	-
	10M25	-	-	8+0	-	-	8+8	-		8+8	-
	10M40	-	-	8+0	-	-	8+8	-		8+8	8+8
	10M50	-	-	8+0	-	-	8+8	-		8+8	8+8

Note: ADC Channel Count = ADC1 + ADC2

- ***For example, 8+0 means 8 inputs from ADC1 and 0 inputs from ADC2***
- ***For example, 8+8 means 8 inputs from ADC1 and 8 inputs from ADC2***



MAX 10 FPGA – DEVICE CONFIGURATION

Configuration Flash Memory (CFM)

Instant On Configuration

Single or Dual Configurations

Less Board Space

Smaller Bill of Materials

- Reduces assembly costs
- Simplified inventory management

Increased Security

- No exposed external interface

Many Benefits of Integrated Configuration Flash

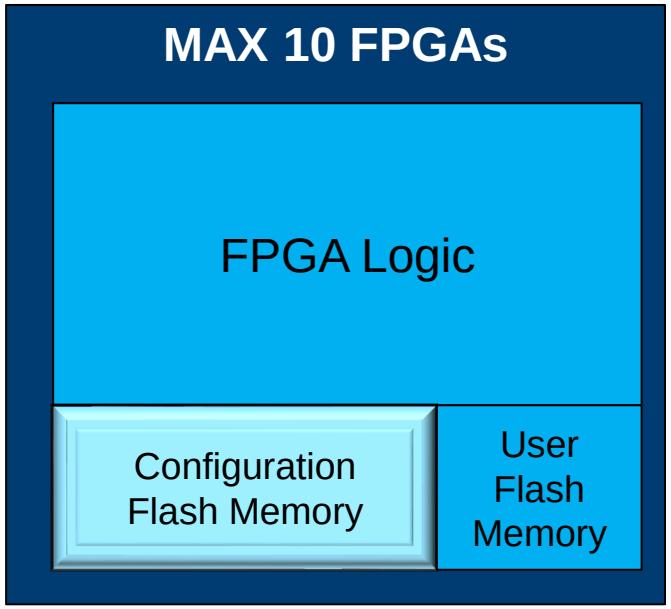
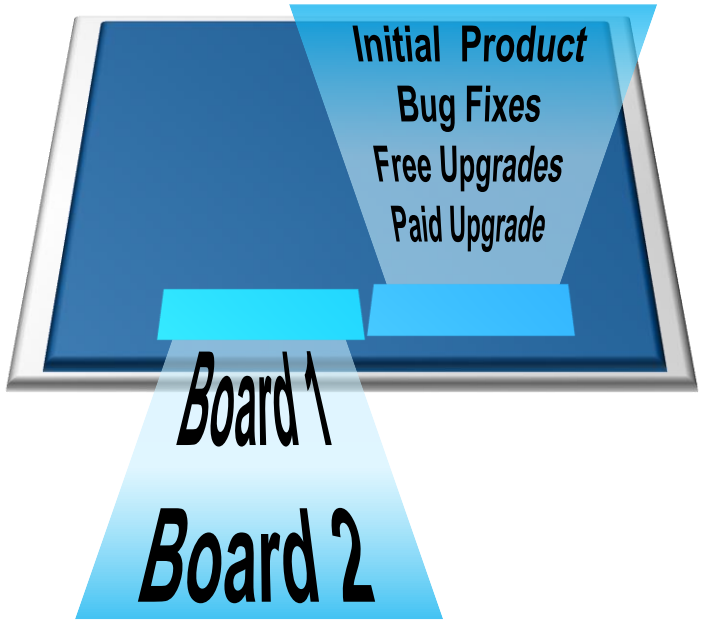


Figure Not to Scale

Dual Configuration Benefits

Infinite Possibilities with Dual Configuration

Capability	Use
Remote System Upgrade w/Fail-Safe Upgrade	Ship System Sooner
	Free Upgrades for Older Systems
	Paid Upgrades
Dual Personas	Reduce logic density by time multiplexing algorithms
	Reduce supply chain by combining multiple SKU's into one pre-programmed device



Dual Persona Configuration

CONFIG_SEL input pin selects one of two images from Configuration Flash Memory (CFM)

At design time, CONFIG_SEL pin can be disabled to provide configuration *anti-tamper* protection

Use Case	Example
Two configurations on the Same Board	Instantly switch between two image processing algorithms.
One Image Per Board, on Two Boards	Consolidate two different sockets into a single BOM line item.

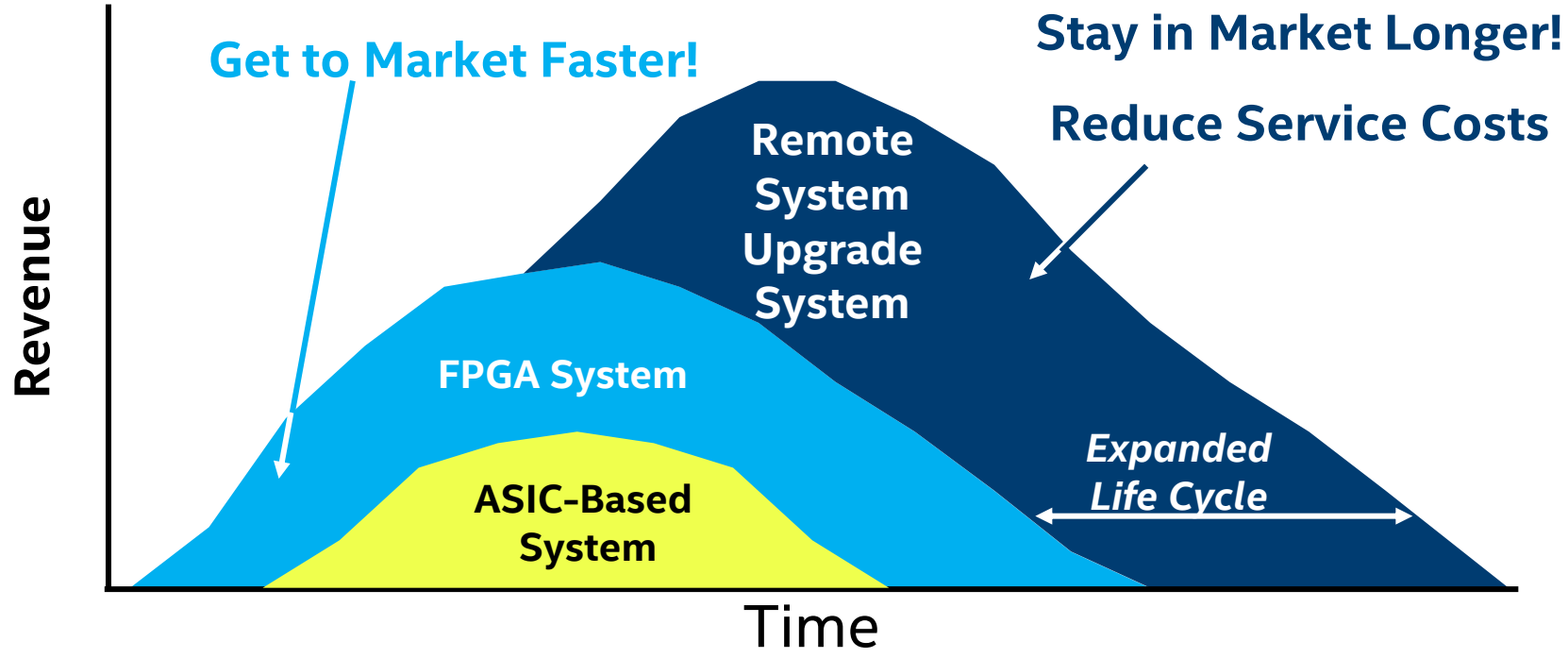
Dual Personas.

Endless Possibilities.

Remote System Update Benefits

Dual configurations with Remote System Upgrade

Adds Business Value At Every Phase



Minimum Device Configuration Times (max)

Without memory initialization (ms)

Device	uncompressed, unencrypted	uncompressed, encrypted	compressed*, unencrypted	compressed*, encrypted
10M02	1.7	5.4	5.2	5.2
10M04	2.7	15.0	10.7	10.7
10M08	2.7	15.0	10.7	10.7
10M16	3.7	25.3	17.9	17.9
10M25	3.7	38.1	26.9	26.9
10M40	6.9	112.1	66.1	66.1
10M50	6.9	112.1	66.1	66.1

***Assuming best case compression ratio (25% of original size)**

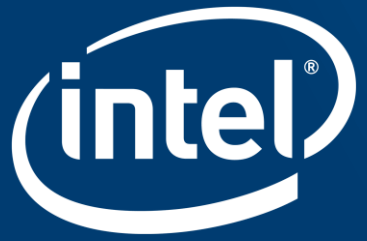
With memory initialization (ms)

Device	uncompressed, unencrypted	uncompressed, encrypted	compressed*, unencrypted	compressed*, encrypted
10M02	N/A	N/A	N/A	N/A
10M04	3.4	19.6	13.9	13.9
10M08	3.4	19.6	13.9	13.9
10M16	4.5	31.5	22.3	22.3
10M25	4.4	45.7	32.2	32.2
10M40	9.8	139.6	82.2	82.2
10M50	9.8	139.6	82.2	82.2

***Assuming best case compression ratio (25% of original size)**

Note: The internal configuration time measurement is from the rising edge of nSTATUS signal to the rising edge of CONF_DONE signal

1. Compressed mode times are the same because config time driven by decompression phase
2. Typically slowest mode because encryption performed on larger file size



MAX 10 FPGA – DESIGN SECURITY

Design Security – Deny the Counterfeiters!

Single chip solution with up to 2 secure configurations

Advanced Encryption Standard (128-bit AES) protection

- Non-volatile key for internal configuration

JTAG port security protection

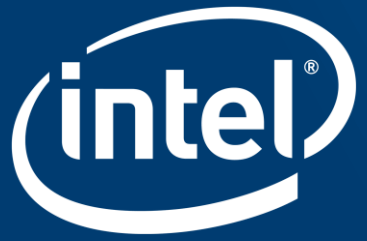
- Read disable or Read/Write disable (OTP)
- Prevents reverse engineering

Embedded unique identification (ID)

- 64 bit unique ID for traceability

Comprehensive Monolithic Design Protection

Click to return to Architectural Sections



MAX 10 FPGA – SINGLE EVENT UPSET (SEU) MITIGATION

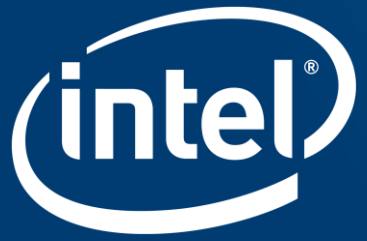
SEU Circuitry Features & Benefits

Function	Feature	MAX 10 FPGAs	Benefits
Detect	Configuration RAM (CRAM) CRC	✓ Embedded in silicon	Checking continuously in the background
	Error Detection Time	✓ Device density dependent	Fast
	User RAM SEU Detection	✓ Soft IP for M9K - ALTECC	Knowledge of data corruption
Fix	User RAM Correction	✓ Soft IP for M9K	ECC option

** CRC = Cyclic Redundancy Check circuitry*

SEU Detection Capability

Click to return to Architectural Sections



MAX 10 FPGA – USER FLASH MEMORY (UFM)

UFM Block Overview

User Flash Memory Block

- Up to 512 Kbits on largest device

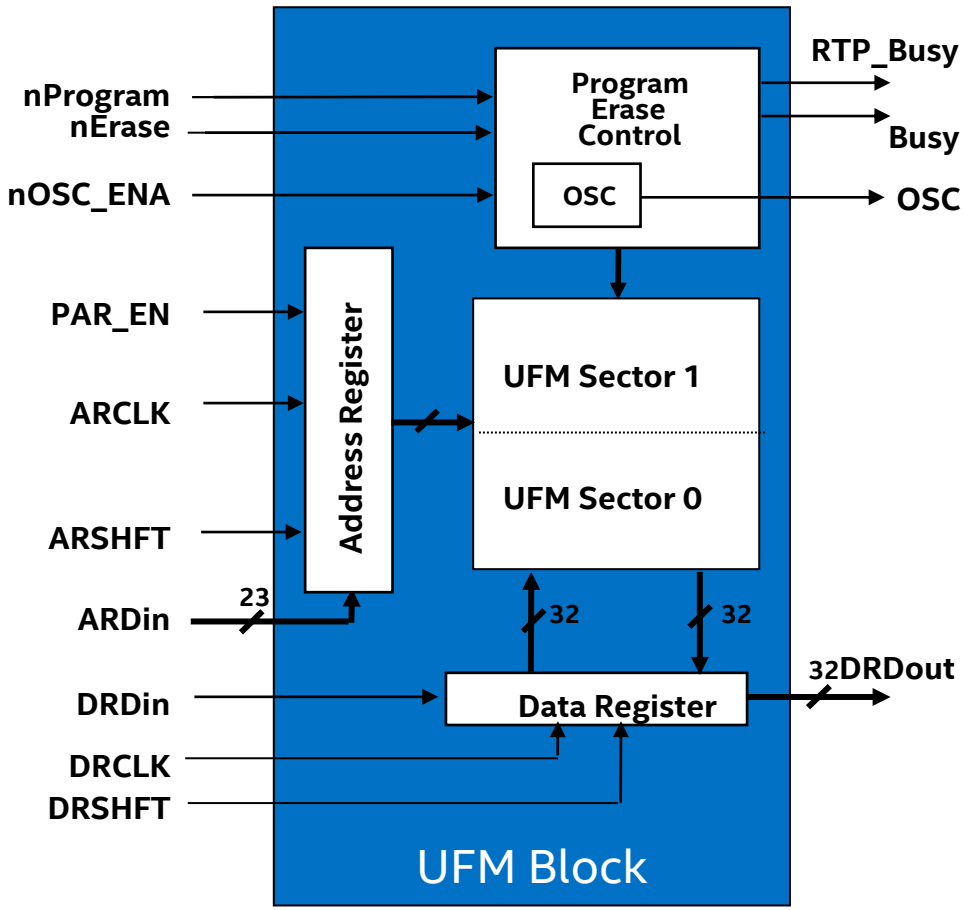
Supports native 32-bit parallel interface

- Enhancement over MAX II/V UFM
- Up to 320 Mbps read bandwidth

SPI and I2C soft interfaces supported in Quartus® Prime s/w

Page and Sector erase support

Integrated UFM oscillator available to core



User Flash Memory Organization

Device	Page Size (bits)	Pages / Sector	# of Sectors	Total UFM Size (bits)
10M02	16,384	3	2	98,304
10M04	16,384	8	1	131,072
10M08	16,384	8	2	262,144
10M16	32,768	4	2	262,144
10M25	32,768	4	2	262,144
10M40	65,536	4	2	524,288
10M50	65,536	4	2	524,288

Use-Models Include Scratch-Pad Memory for Nios II Processor Code

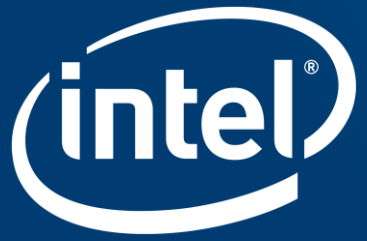
☞ ***Click to return to Architectural Sections***

Supported Configuration scenarios and associated CFM requirements

Supported Configuration Modes (1)	CFM2	CFM1	CFM0
Single image uncompressed, with RAM preload	Uncompressed configuration (w/RAM preload)		
Single image compressed, with RAM preload	Compressed configuration (w/RAM preload)		
Dual image configuration	Compressed Configuration 2		Compressed Configuration 1
Single image uncompressed, without RAM preload	UFM	Uncompressed configuration	
Single image compressed, without RAM preload	UFM		Compressed configuration

Note 1: 10M02 devices, support only CFM0 and therefore only support only single image, with and without compression

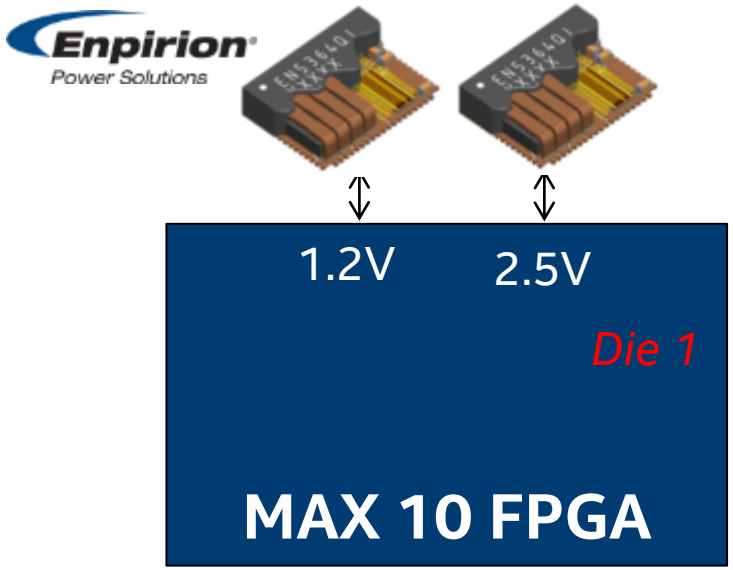
If desired, CFM can be reallocated as UFM



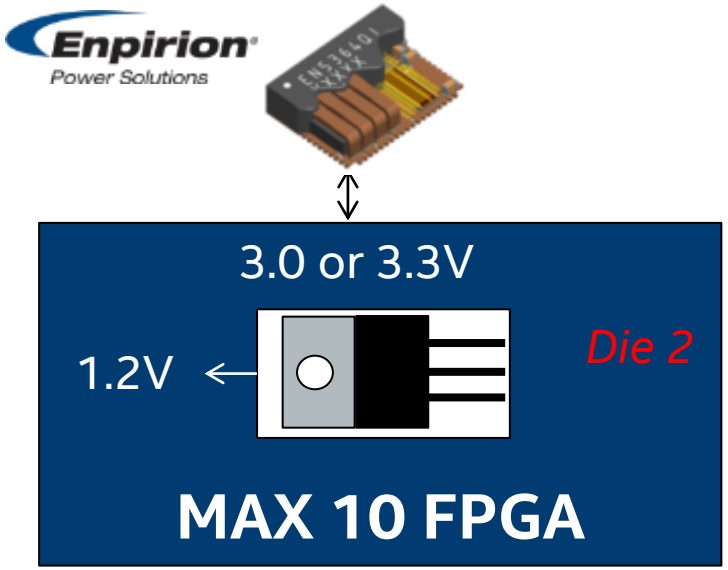
MAX 10 FPGA – VOLTAGE REGULATOR

MAX 10 FPGA – Optional Integrated Linear Regulator

Option 1 – Dual Supply



Option 2 – Single Supply

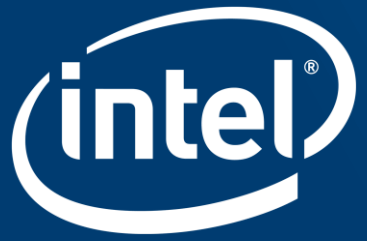


Higher Performance

Simple, compact PCB

More Features

Click to return to Architecture Section



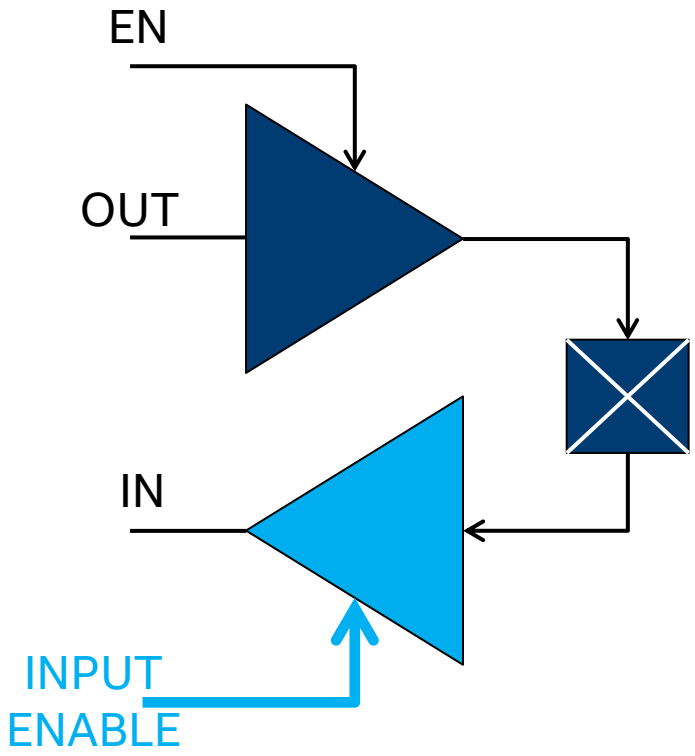
MAX 10 FPGA – POWER SAVINGS

Max 10 FPGA – Dynamic Input Buffer Disable (16k LE and higher)

Power down high performance input buffers

No FPGA reconfiguration needed

Automatic and/or User Control



I/O Type	Control Source
External Memory Interface	Memory Controller (during IDLE and WRITE)
LVDS	User Control

Saves Operating and Standby Power

Sleep Mode Capability & Ref. Design

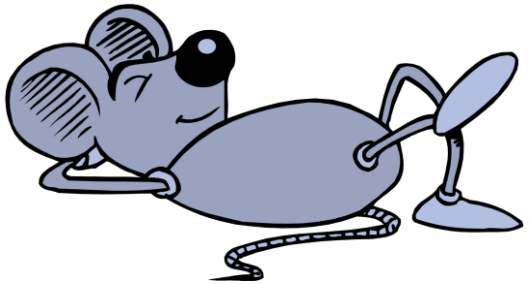
Low power mode without losing state

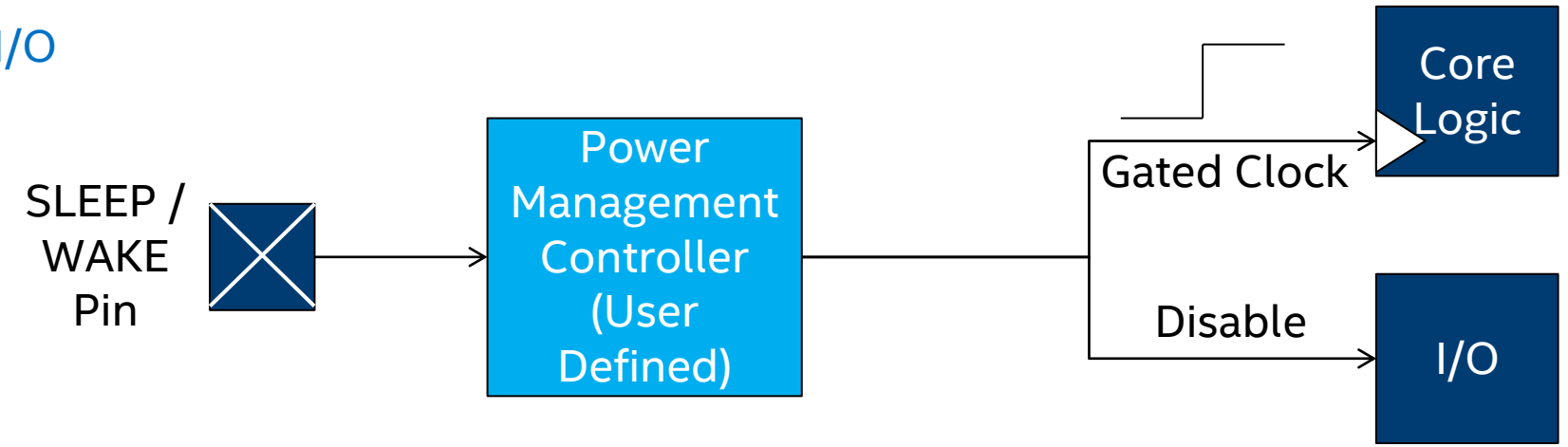
External control via single pin

Wake-up from sleep in < 1 ms

Gates clocks to internal logic

Disables I/O



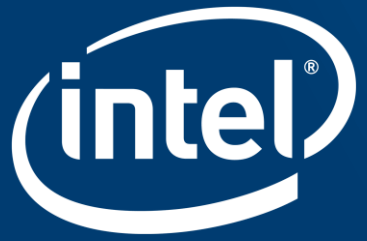


Reference Design Available

“Sleep” Mode

5%-95% Dynamic Power Reduction

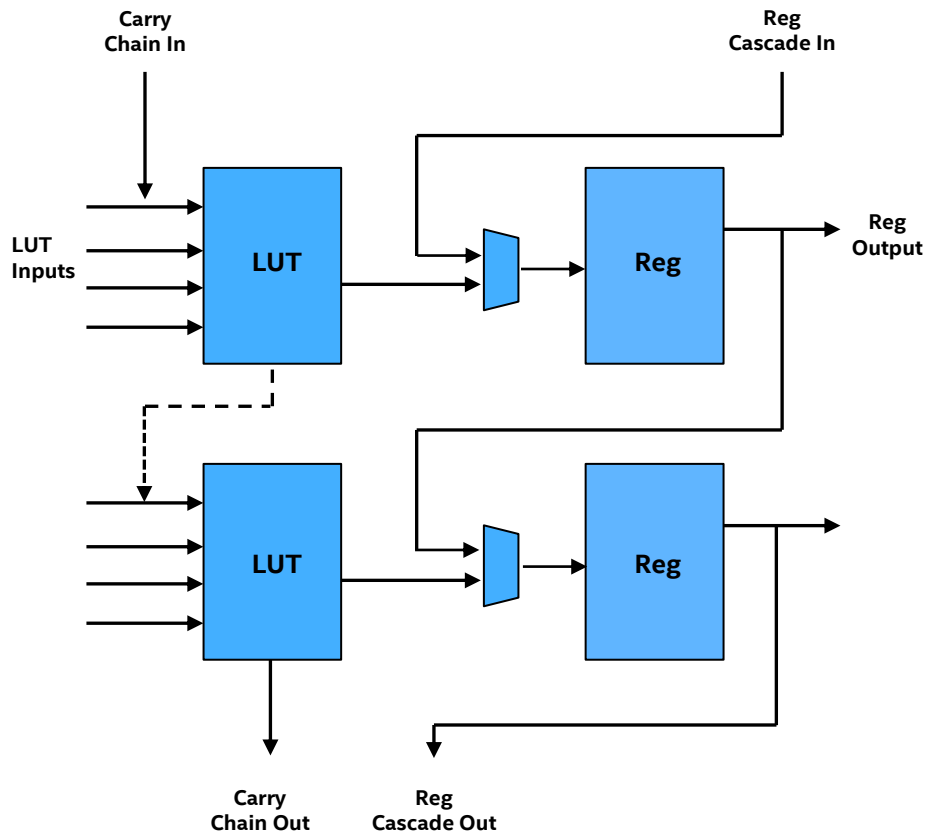
Click to return to Architectural Sections



MAX10 FPGA – CORE ARCHITECTURE

Logic Element (LE) and Interconnect

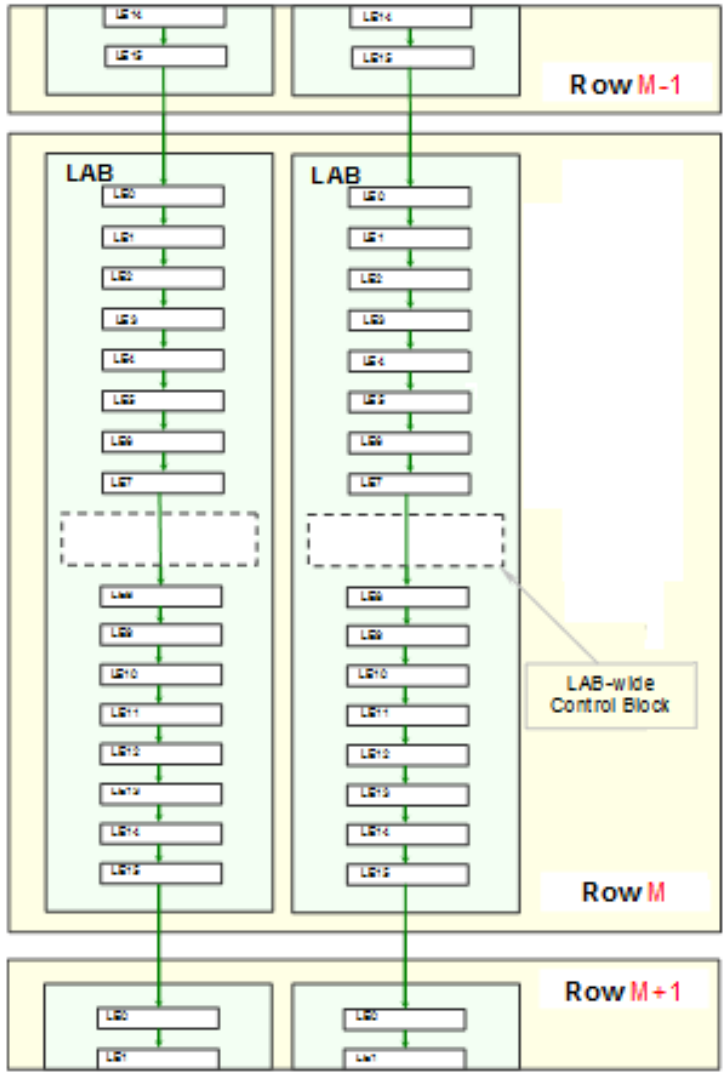
LE = 4-input Look Up Table (LUT) + Register



Two dedicated paths between LEs:

- Carry chain
  - Chain runs the entire length of a LAB Block Column
- Register cascade
  - Cascade chain can start & finish at any LE
  - Multiple chains supported
  - Register cascade between LAB blocks is not supported

Logic Array Block (LAB) Structure



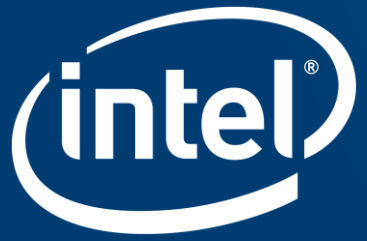
Logic Element

- Look Up Table + Register + Output Logic

Logic Array Block

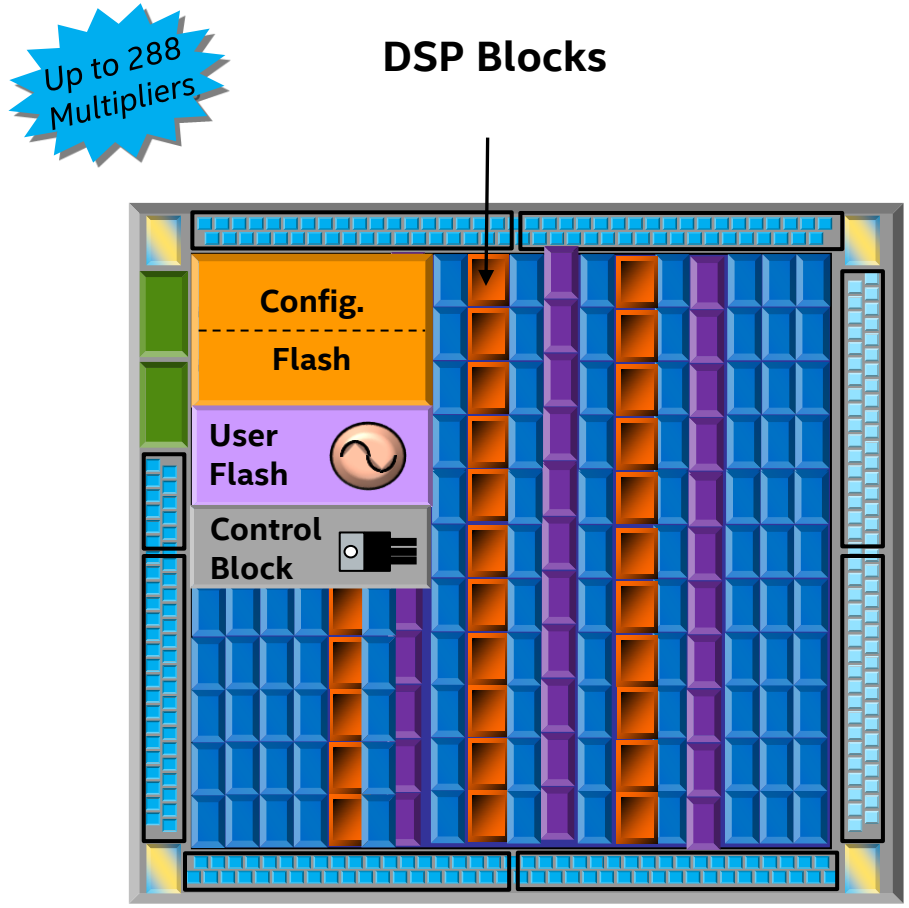
- 16 Logic Elements
- Control Block (middle of LAB)
- Lab-wide routing (not shown)

Click to return to Architectural Sections



MAX10 FPGA – DSP

Basic DSP Architecture



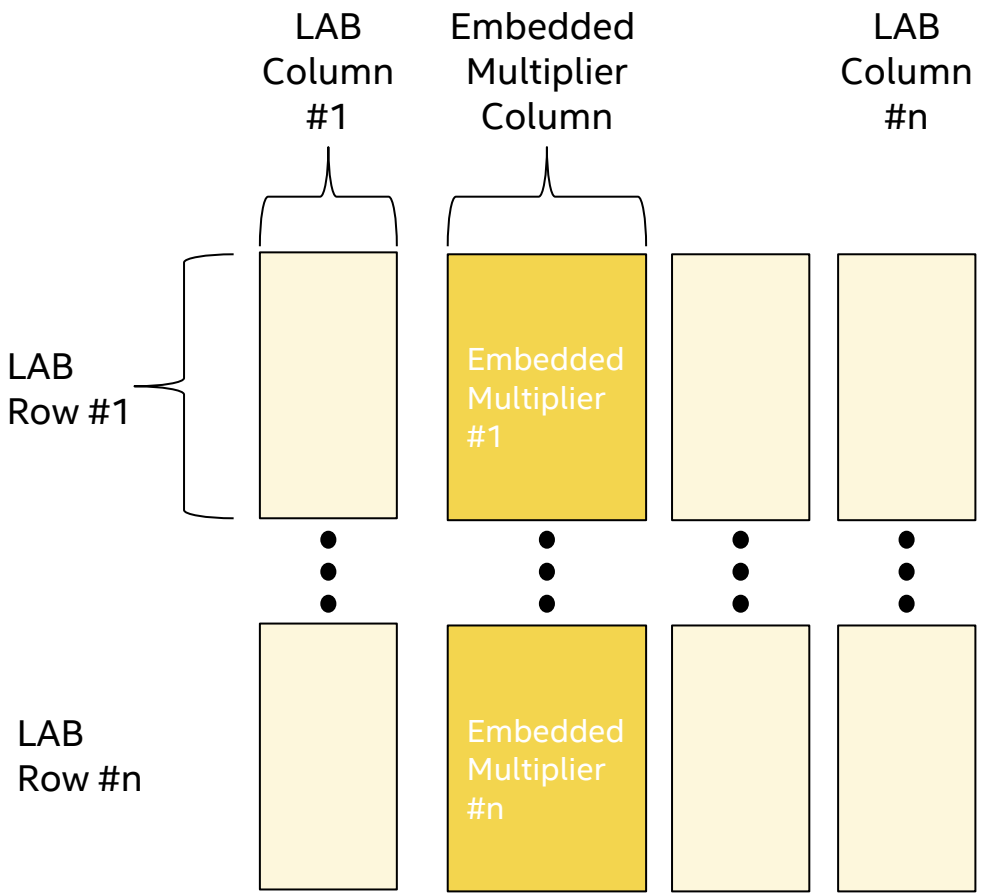
Only non-volatile, low-cost FPGA with dedicated hard multipliers

Supports Up To:

- 144 18x18 multipliers or,
- 288 9x9 multipliers

Maximum multiplier performance of 310 MHz

DSP Block Organization



Implemented as column elements in between LAB columns

Multiplications greater than 18-bits are supported via cascade chaining of DSP blocks

- Supports wide multiplication

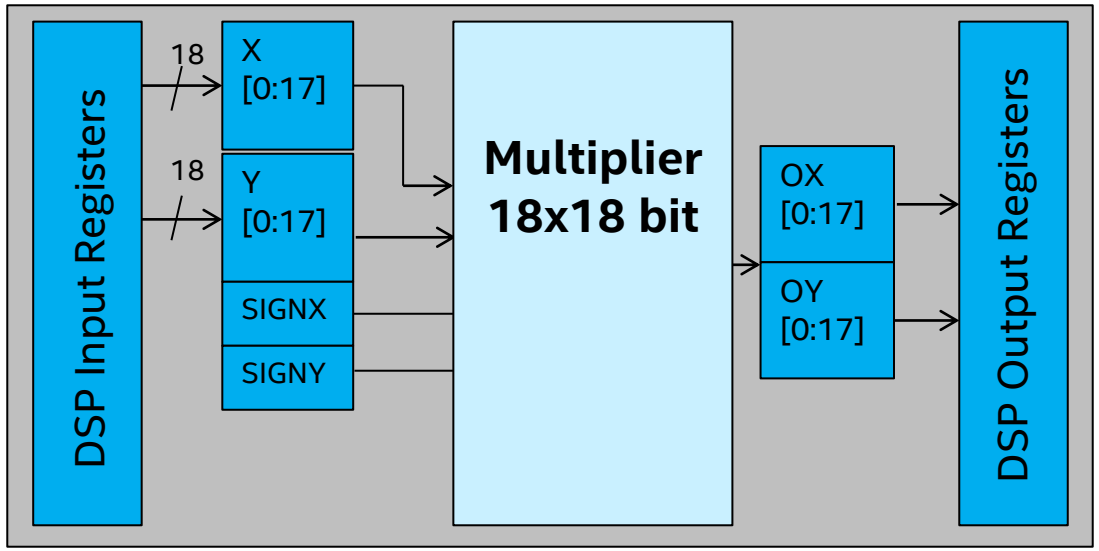
Automatically supported in Quartus® Prime software

DSP Block Architecture

41 inputs (max.)

- 36 data inputs
- 5 control signal inputs

36 outputs (max.)



Two modes of operation:

Modes	# Data Inputs	# Data Outputs
1 individual 18bx18b multiplier	36	36
2 individual 9bx9b multipliers	36	36

DSP Performance

9 × 9-bit multiplier

MAX 10 FPGA Supply Variant	Speed Grade		
	-6	-7	-8
MAX 10D - Dual Supply	310 MHz	260 MHz	210 MHz
MAX 10S - Single Supply	198 MHz	183 MHz	160 MHz

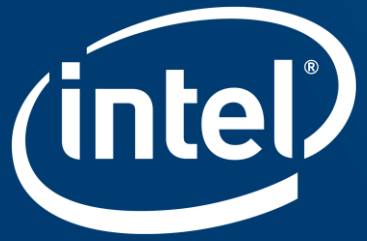
Note: performance numbers per speed grade all assume registered inputs and outputs

18 × 18-bit multiplier

MAX 10 FPGA Supply Variant	Speed Grade		
	-6	-7	-8
MAX 10D - Dual Supply	265 MHz	240 MHz	190 MHz
MAX 10S - Single Supply	198 MHz	183 MHz	160 MHz

Note: performance numbers per speed grade all assume registered inputs and outputs

Click to return to Architectural Sections



MAX10 FPGA – PHASE LOCKED LOOPS (PLLS)

Full Featured PLLs

Up to four full-featured PLLs

- Five programmable outputs per PLL
- Dynamically change both frequency and phase
- Up to 10 global clocks and 2 external clocks outputs from 1 clock source

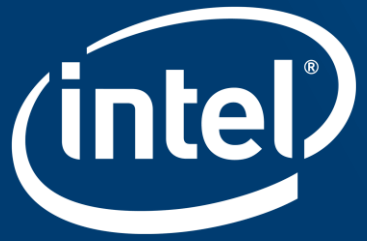
Flexibility

- Support multiple or unknown input frequencies using dynamic reconfiguration
- PLL counter cascading for finer clock synthesis resolution
- Single PLL supply device option

External interface support

- x16 DDR3 interfaces using a single PLL
- Support for LVDS interfaces up to 830 Mbps

☞ ***Click to return to Architectural Sections***



MAX10 FPGA – CLOCKS

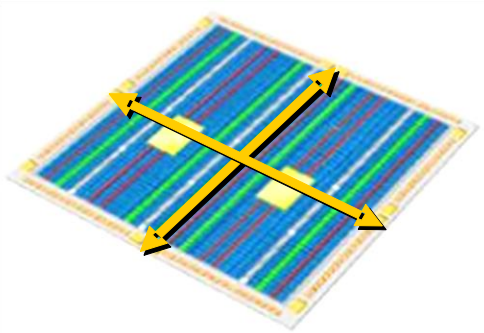
Low Power Clocking Architecture

Low power…when needed

- Dynamic enable/disable for power control/sleep
- Unused networks automatically powered down

High performance

- Up to 450MHz



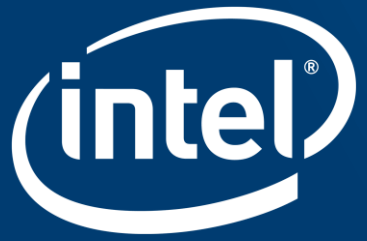
Abundant, flexible clocking resources

- Up to 20 global clock networks with dynamic user clock selection
- Oscillator for Self-running applications – sleep controller, watch-dogs, etc.

Up to 20 networks per device

Robust clocking resources to support system integration

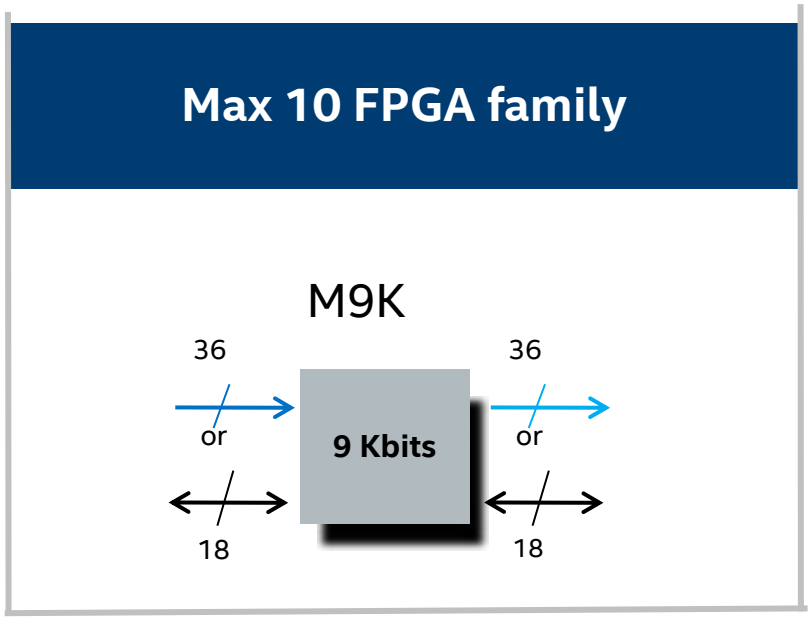
Click to return to Architectural Sections



MAX 10 FPGA – INTERNAL MEMORY

M9K Embedded RAM Blocks

Feature	M9K	Benefit
Block Size	9 Kbits	Optimizes Memory
Performance	Up to 330 MHz	Hi speed Performance
Dual-Port Read During Write Behavior	New Data or Old Data	Flexibility and Ease of Use
Parity Bit	Yes	Usability for High Reliability Apps
Clock Enables	4	Increased Flexibility and Reduced Power
Read and Write Enables	4	Increased Flexibility and Reduced Power



M9K Block Key features

9,216 RAM bits including parity bits

- Variable port width configurations of x1, x2, x4, x8, x9, x16, x18, x32 and x36
- Synchronous only operation operating up to 330 MHz
- Parity support by storing one extra bit per byte in x9, x18 and x36 modes.

Data options

- Byte enable support for data input masking during write
- Address stall for efficiency in cache-miss applications
- Same-port read-during-write to read out new data
- Same-port read-during-write to read out old data

Port options

- Single-port mode and simple dual-port mode supported for all port widths
- True dual-port operation in x1, x2, x4, x8 x9, x16 and x18 modes
- Pack mode in which 9k MEAB is split into two 4.5k single port RAMs
- Mixed-port same-clock read-during-write to read out old data.

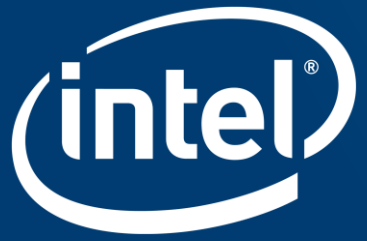
Control options

- total of 4 clock enable controls.
- Separate read enable and write enable for each port.
- Asynchronous clear for output latches
- Asynchronous clear for address registers.

ROM mode with preload supported for all port widths*

**** Feature available depending on configuration option used.***

Click to return to Architectural Sections



MAX 10 FPGAS – GENERAL PURPOSE I/O (GPIO)

I/O Features & Benefits

I/O features	Benefit
Multiple interfaces, standards, and features supported	■ Easily bridge between different devices having different voltage levels or protocols ■ Flexible I/O placements for easier PCB design and to reduce board area
Large number of I/O banks	Better granularity to mix and match different I/O requirements
Abundant I/O element registers	■ Increase external memory interface performance ■ Improve Tco performance
Dedicated differential output buffers	■ Eliminate external resistors for LVDS, RSDS, and mini-LVDS transmission ■ LVDS interfaces up to 720 Mbps (preliminary)
Selectable series OCT (some with calibration)	On-chip termination reduces external passive cost & calibration eliminates variations due to PVT
Adjustable slew rates	Improve signal integrity by slowing down edge rates on non-performance-critical I/O pins

I/O Bank Details

Interface to 3.3, 2.5, 1.8, 1.5, and 1.2V logic levels

3.3V PCI 32-bit, 33 MHz compatible

- PCI clamp diode on all pins

Output enable per pin

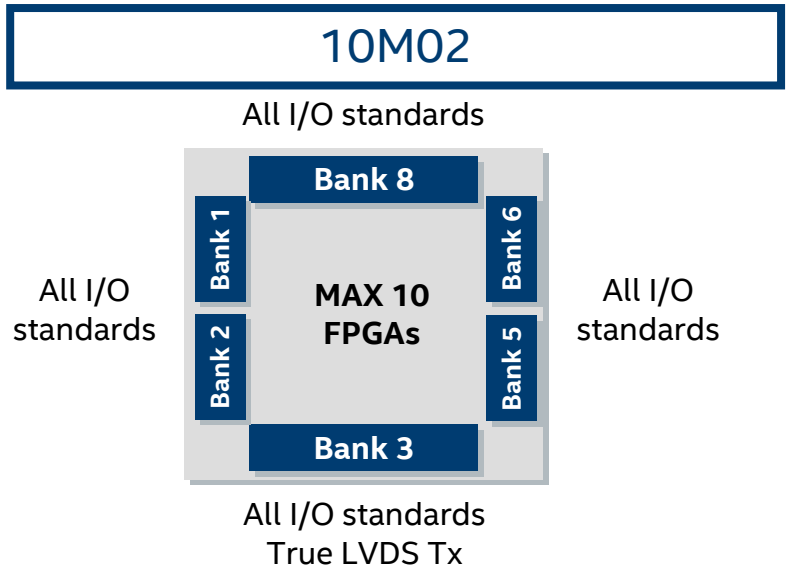
Noise control features

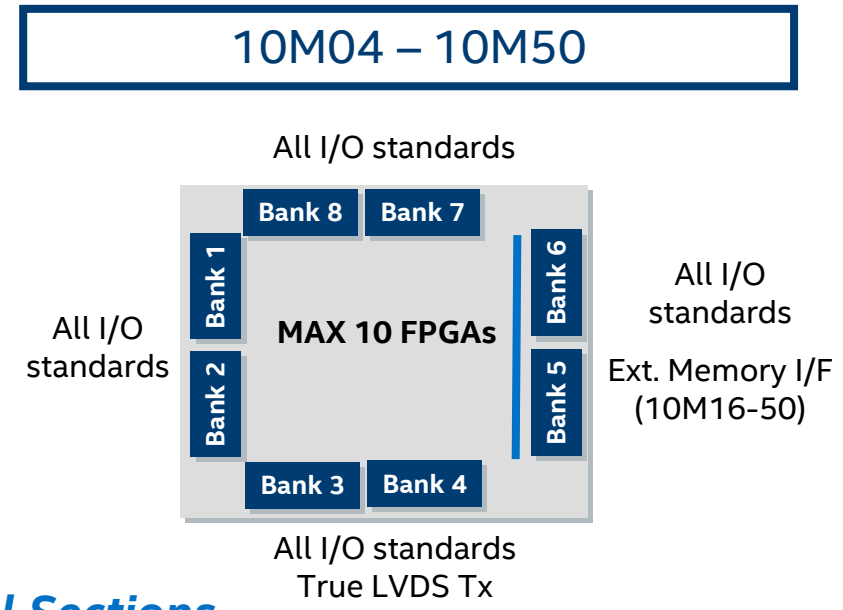
- Schmitt Triggers
- Three step slew rate
- Programmable output drive strength

Emulated-LVDS I/O on all banks

- True LVDS I/O, bottom banks only

On-chip series termination & Hot-Socket Compliant





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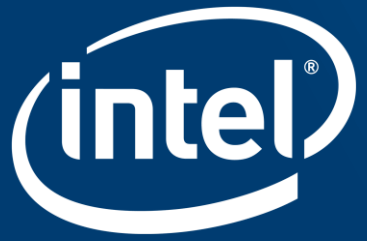


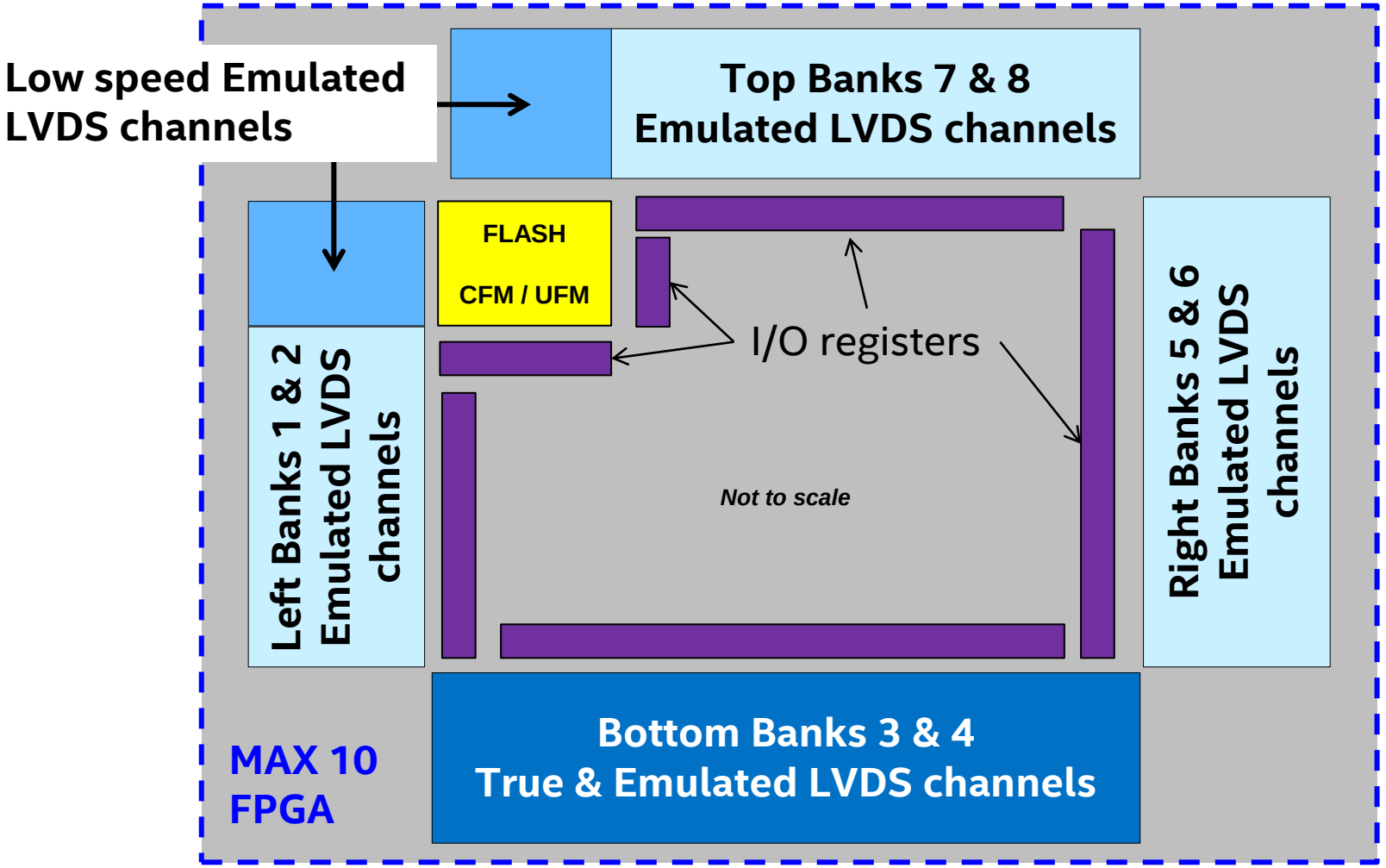
MAX 10 FPGAS – LVDS I/O

LVDS on Every I/O

Performance & Termination is Location/Bank Dependent

LVDS Type	Description	Performance	
		Single-Supply Voltage	Dual-Supply Voltage
True	Full differential matched channel Rx / Tx (Banks 3, 4)	Up to 400 Mbps	Up to 830 Mbps
Emulated	Requires external 3-resistors at Tx (Banks 2, 5, 6, 7)	Up to 285 Mbps	Up to 600 Mbps
Low speed Emulated	Requires external 3-resistors at Tx (Banks 1a, 1b, 8)	Up to 200 Mbps	Up to 380 Mbps

LVDS I/O Floorplan



LVDS Performance by Speed Grade
Dual-Supply devices

LVDS Type	I/O Signal Name	Direction & SERDES	Performance (Mbps)							
			C6[2,4]	A6[1]	A6[2]	i6[3]	c7	i7	a7	c8
True (Banks 3, 4)	DIFFIO_TX_RX (High_Speed)	Rx (x2, x4, x8) (x7, x10) (x1)	830	770	720 700 360	720 700 360	720 700 360	720 700 360	640 640 320	640 640 320
		Tx (x2, x4, x8) (x7, x10) (x1)	800		700 (x8, 720) 680 350	720 720 360	700 (x8, 720) 680 350	700 (x8, 720) 680 350	640 620 320	640 600 320
Emulated (3-resistor, Banks 2-7)	DIFFIO_RX DIFF_OUT (High_Speed)	Rx (max)	800		720	720	720	720	640	640
		Tx (max)	600		600	600	600	600	550	550
Emulated (3-resistor, Banks 1A, 1B, 8)	DIFFIO_RX DIFF_OUT (flash region) (Low_Speed)	Rx (max)	380		300	300	300	300	300	300
		Tx (max)	380		300	300	300	300	300	300

Notes:

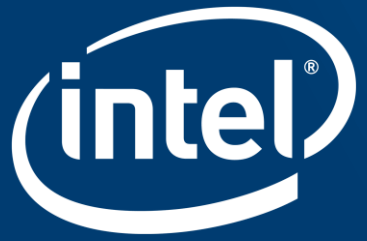
1. ***Requires design/Quartus restrictions/guidelines to achieve performance.***
2. ***Unrestricted performance but p/n is hidden or reactive in Quartus. File SR to request review & approval to unlock p/n.***
3. ***Industrial -6 speed grade p/n is 'hidden' in Quartus . File SR to request review & approval to unlock p/n.***
4. ***For C6 speed grade support, please contact the factory***

LVDS Performance by Speed Grade
Single-Supply devices

LVDS Type	I/O Signal Name	Data Direction	Performance (Mbps)				
			-i6 (1)	-c7	-i7	-a7	-c8
True	LVDS	Rx (input toggle rate)	380	290	290	200	200
		Tx (output toggle rate)	380	290	290	200	200
Emulated	LVDS_E_3R	Rx (input toggle rate)	285	290	290	200	200
		Tx (output toggle rate)	285	285	285	195	200
Low speed Emulated	LVDS_E_3R (flash region)	Rx (input toggle rate)	200	200	200	200	200
		Tx (output toggle rate)	200	200	200	200	200

Note:

1. ***Industrial -6 speed grade is 'hidden' in Quartus (visible but greyed out). File SR to request review & approval to unlock p/n.***
2. ***Preliminary performance numbers pending device characterization.***



MAX 10 FPGA – EXTERNAL MEMORY INTERFACE (EMIF)

EMIF Overview

Industry's Lowest Cost & Long-Life Memories

Device / Protocol	Configuration	Max Total DRAM Bandwidth (Gbps)	Max I/O Data Rate (MHz)	MAX 10 FPGA
SRAM	Up to x36	-	100	All
DDR3 / 3L	Up to 1 x16 (ECC option)	9.6	300	10M16 or larger densities (1)
DDR2	Up to 1 x16 (ECC option)	6.4	200	
LPDDR2	Up to 1 x16 (no ECC)	6.4	200	

4th generation Low-Cost I/F architecture

	MAX 10 FPGA	Higher-End Altera FPGAs
Objective	Low cost	Performance & flexibility
PHY	Soft IP: UniPHY – Proven solution Silicon features: Easy timing closure	UniPHY – NIOS-based solution for multiple protocols & high performance
Controller	Soft IP – no wasted device resources if design doesn't need EMIF	Soft/Hard- High speed, low latency, and high through-put

Note 1: EMIF only available on dual-supply voltage device/package options.

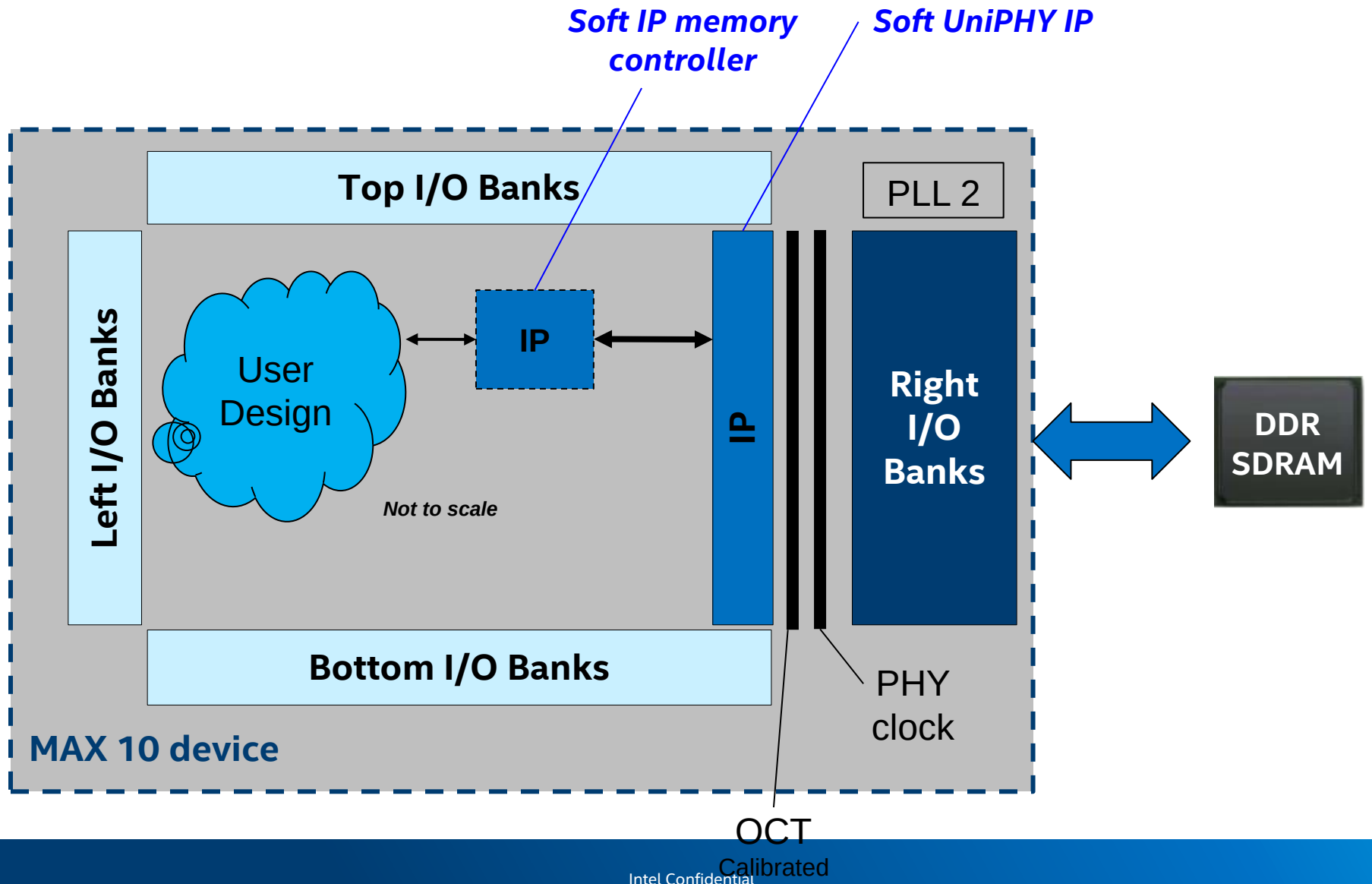
EMIF – Wide Range of Options in Low-Cost Families

Device	Altera Controller + PHY				Partner Controller + PHY
	DDR3 (MHz)	DDR2 (MHz)	LPDDR2 (MHz)	DDR (MHz)	Various
Cyclone® III	-	200	-	167	✓
Cyclone III LS	-	167	-	150	✓
Cyclone IV GX	-	200	-	167	✓
Cyclone IV E	-	167	-	133	✓
Cyclone V (HMC)	400	400	333	-	✓
MAX 10 FPGA	303	200	200	-	✓

Notes:

1. ***HMC = Hard Memory controller (part of die silicon). All other solutions use soft IP cores.***
2. ***Performance targets are for the fastest speed grade, not available in all speed grades.***
3. ***Memory solution partners include:***
   - ***Northwest Logic***
   - ***Microtronix***
   - ***CAST***

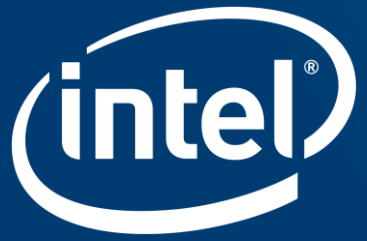
EMIF Solution Floorplan



EMIF Maximum Width Support by Package

Device	U324	F256	F484	F672
10M16	x8, x16 LPDDR2	x8 (no ECC), x16 LPDDR2	x8, x16 LPDDR2	-
10M25	-		x8, x16	x8, x16
10M40	-			
10M50	-			

Note: Only available in dual-supply package options and I/O Banks 5 & 6.



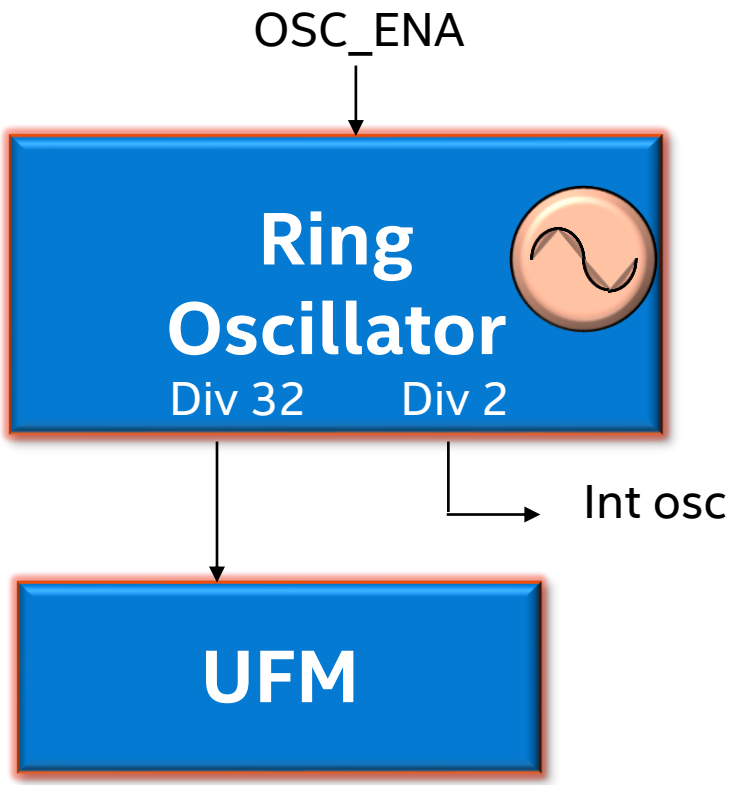
MAX 10 FPGA – INTERNAL OSCILLATOR

Integrated Oscillator Clock Source

Internal Ring Oscillator with clock multiplexers and dividers

- Maximum Freq 232MHz*

Uninterruptable clock source located within the UFM



Internal OSC Frequency (MHz)			
Device	Min	Typ	MAX
10M02 / 04 / 08 / 16 / 25	55	82	116
10M40 / 50	35	52	77

*10M40/50 144MHz

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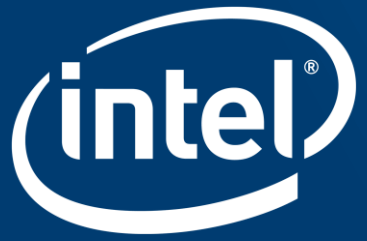


BROAD APPLICATION APPEAL!

MAX 10 FPGA Applications in Motor Control

Single chip solution = Drive-on-Chip (DOC)

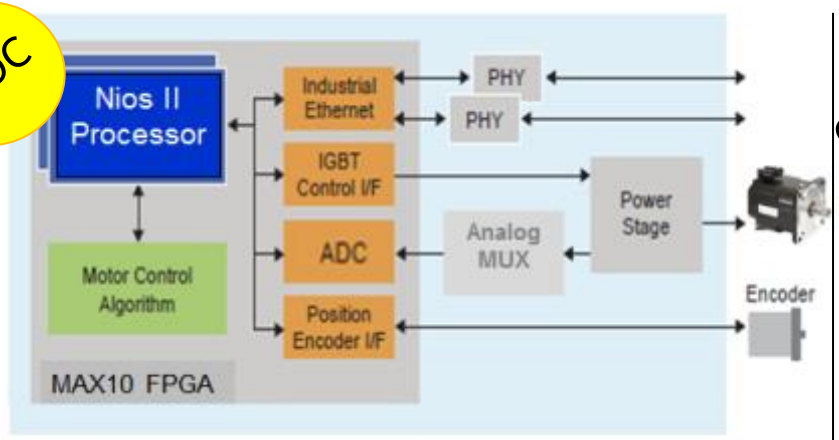
- Targets lower-voltage, lower complexity applications than existing Cyclone V SoC DOC
- Integrated ADCs reduce BOM cost in low voltage applications

Companion Chip, next to existing microprocessor

- Incremental integration of PLD into motor control (reduces risk)
- Augment existing design with new features / capabilities
  - Minimal or no change to existing motor-control algorithms
  - Design remains largely in designer comfort-zone of software-based control
  - Potentially lower cost than having to switch microcontrollers

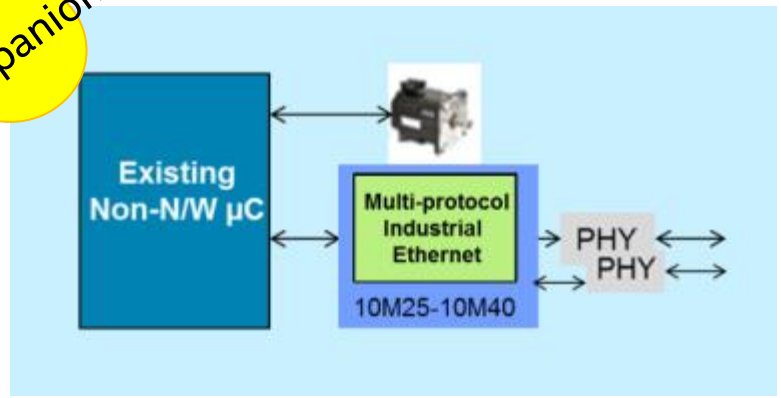
MAX10 in Motor Control Applications

DOC



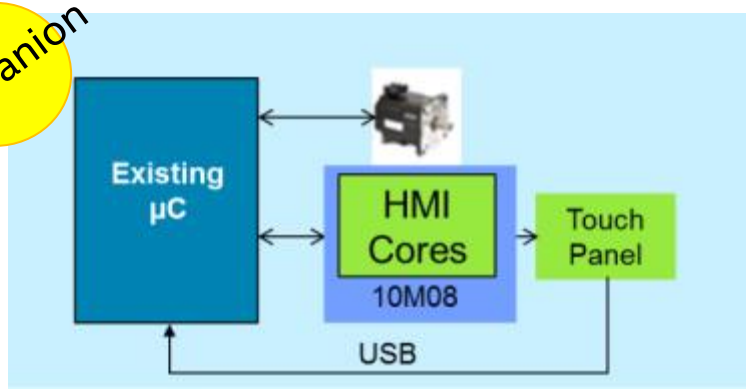
- DOC design will fit in 10M40; Simplest: 10M08
- Eliminating external ADC can save up to $5.00

Companion



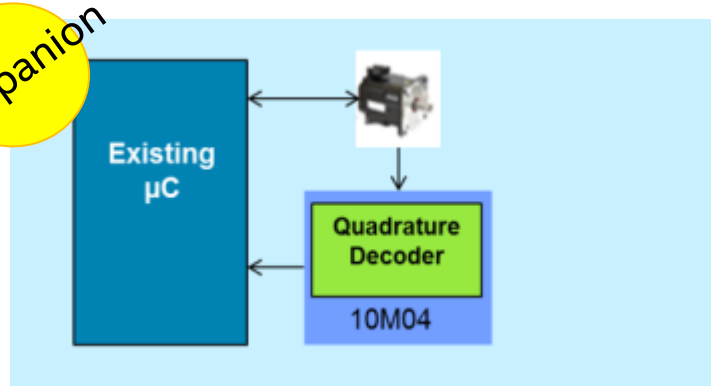
- 10M25 – 10M40 supports Industrial Ethernet
- Offers flexibility of multiple IE protocols

Companion



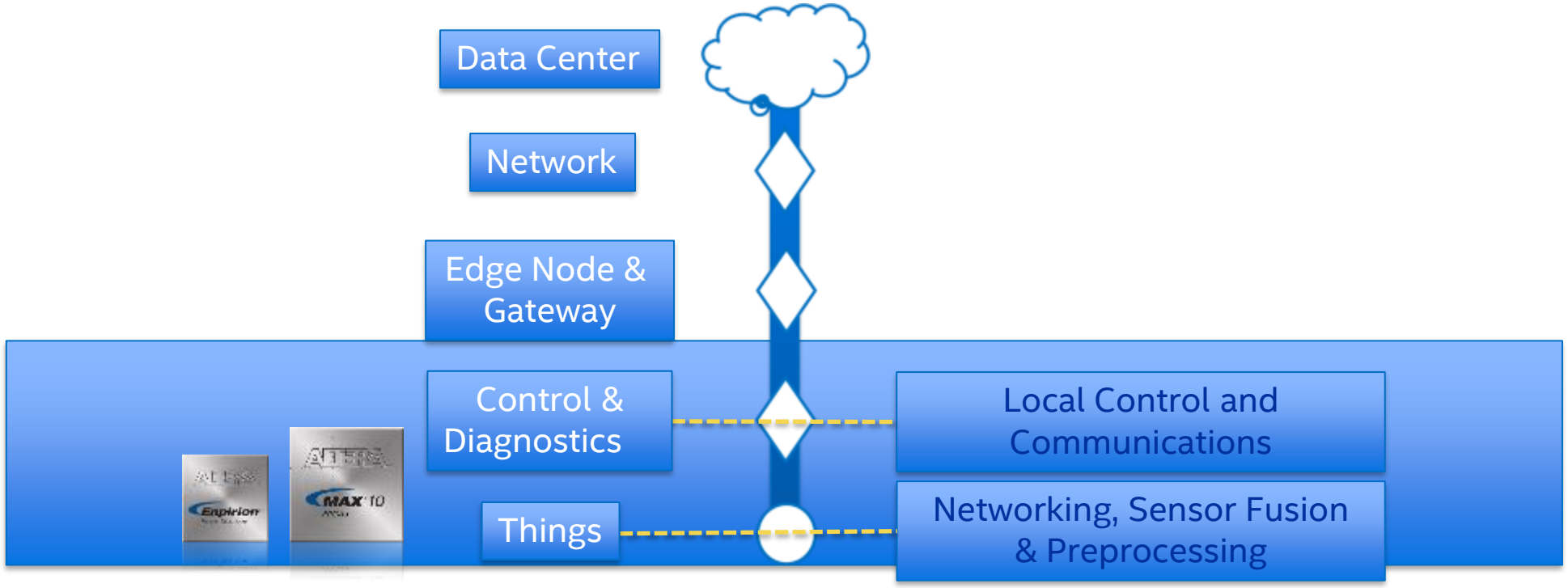
- 10M08 adds inexpensive touch panel HMI
- 7-8KLE (basic)*, 22 x M9K, 8 x Mult., ~80 I/O
  - * 15KLE, 55 x M9K for blended graphics (10M16)

Companion



- 10M04 adds encoder interface to existing microcontroller system

MAX 10 FPGAs in IoT Applications



Sensor Fusion with Max 10 FPGA + Sensor Daughter Cards

System Management Tasks and Functions

Power Rail Management

- Start up
- Configure
- Maintain
- Power down

Thermal Management

- Monitor thermal environment
- Evaluate environment data
- Mitigate conditions or initiate damage prevention

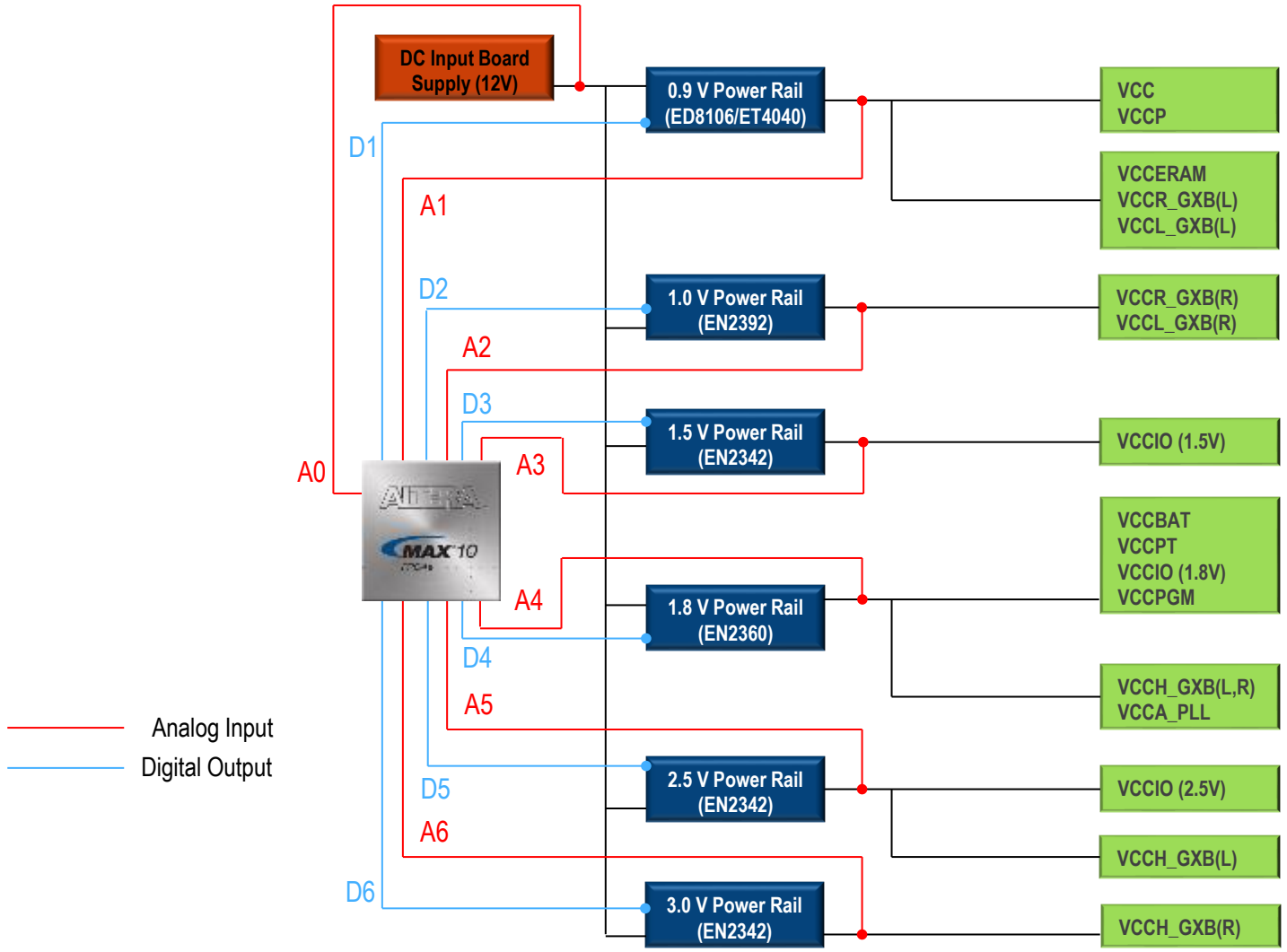
Diagnostics / Prognostics

- Record events
- Analyze data log
- Predict failure

Power Rail Management Functions

Power State	Description	Key Design Considerations
Off	No power applied.	Hot-socketing support: • Initialize upon insertion
Power On	• Main power supply on and stable • Power tree not initialized	• Monitor line-side power stability • Avoid brownout conditions
Power Up	Power rails initialized: • in prescribed sequence • at prescribed ramp rate	Out of sequence rails can cause: • high power consumption • unstable operation • reduce operating life • device damage
Run time	• Maintain power rail voltage and current • Communicate system health	Power rail drift and fluctuation can: • put devices into unknown or unstable states • undetected, reduce system reliability
Low-power / Sleep Option	Turn down / turn off system blocks: • reduce power consumption • reduce cooling / operating costs	Low-power / sleep states: • need specific voltage sequencing and control depending on desired state
Power Down	Power rails powered down: • in prescribed sequence	Uncontrolled power down can create: • internal potential differences reducing device operational life

MAX10 FPGA Power Sequencing of Arria 10 FPGA



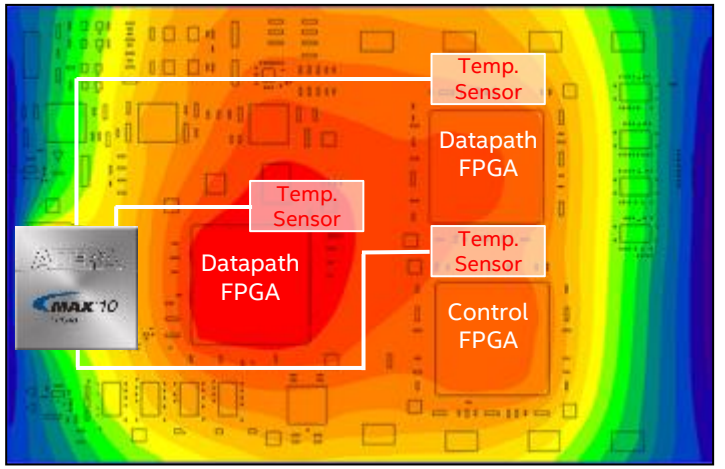
Thermal Management – Monitor Board-level Micro Climates

Temperature	Potential Action	Key Design Considerations
Rising. Within normal operating range	Increase active cooling (e.g. increase fan speed)	Temperature outside normal range can: • cause unreliable operation • lead to reduced device longevity
Rising. Approaching critical threshold	Any combination of: • increase active cooling • increase monitoring frequency • redirect data traffic • log event	
Reached critical threshold	• Shut down device or board • Log event	Prevent catastrophic device and / or system failure

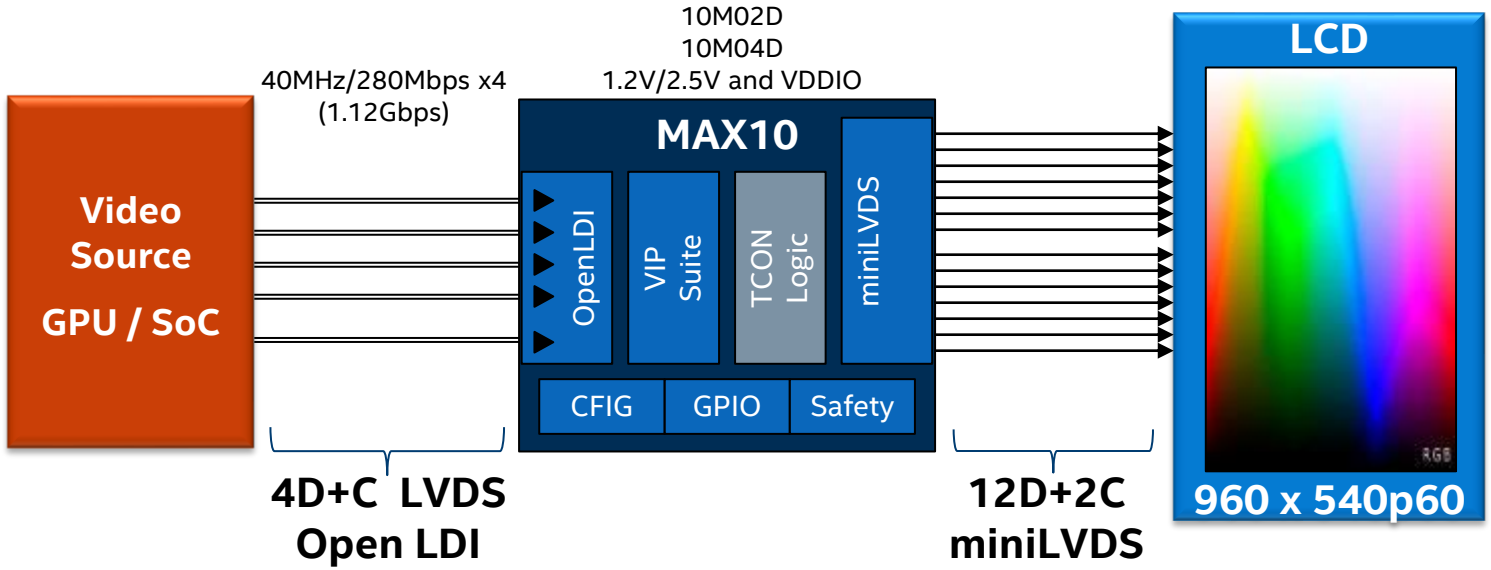
Typical temperature-sensor interfaces

- Analog / SPI / I^2C

With up to 18 analog inputs, Altera MAX10 supports all three types of sensors on the same device



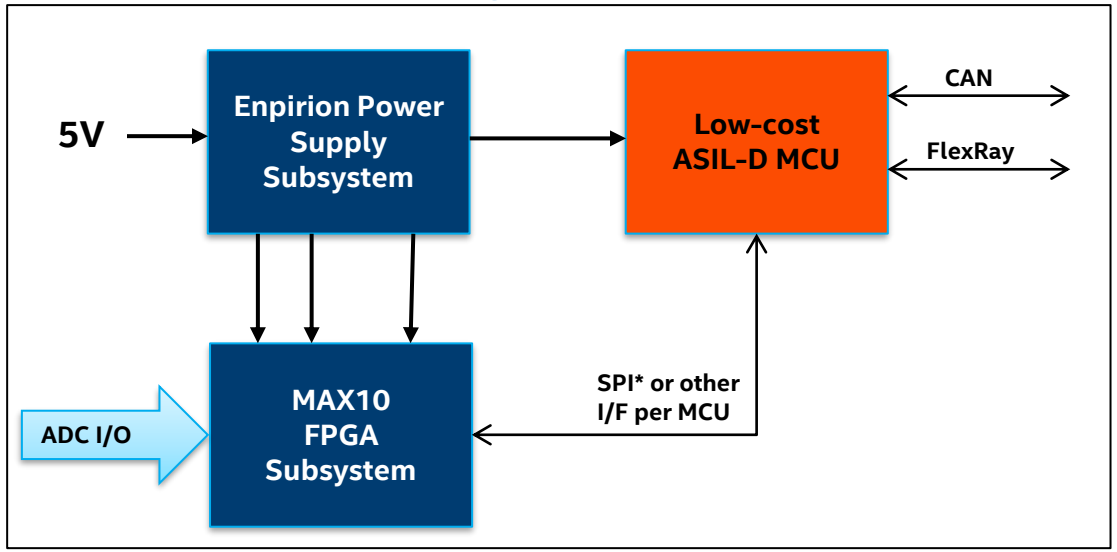
Automotive Infotainment Application:
Interface / Video Function & Timing Controller



IO Support: LVDS inputs, mini-LVDS outputs, and LVCMOS GPIOs
Altera IP: ALTLVDS MegaFunction, and VIP Suite
MAX10 FPGA: granular family, on-chip FLASH for reduced BOM

Small footprint with FLASH & ADC integration
The right IO and IP from Altera make MAX10
Ideal for Display Driving TCON applications

Automotive ADAS Application – MAX10:
Radar Processing Acceleration



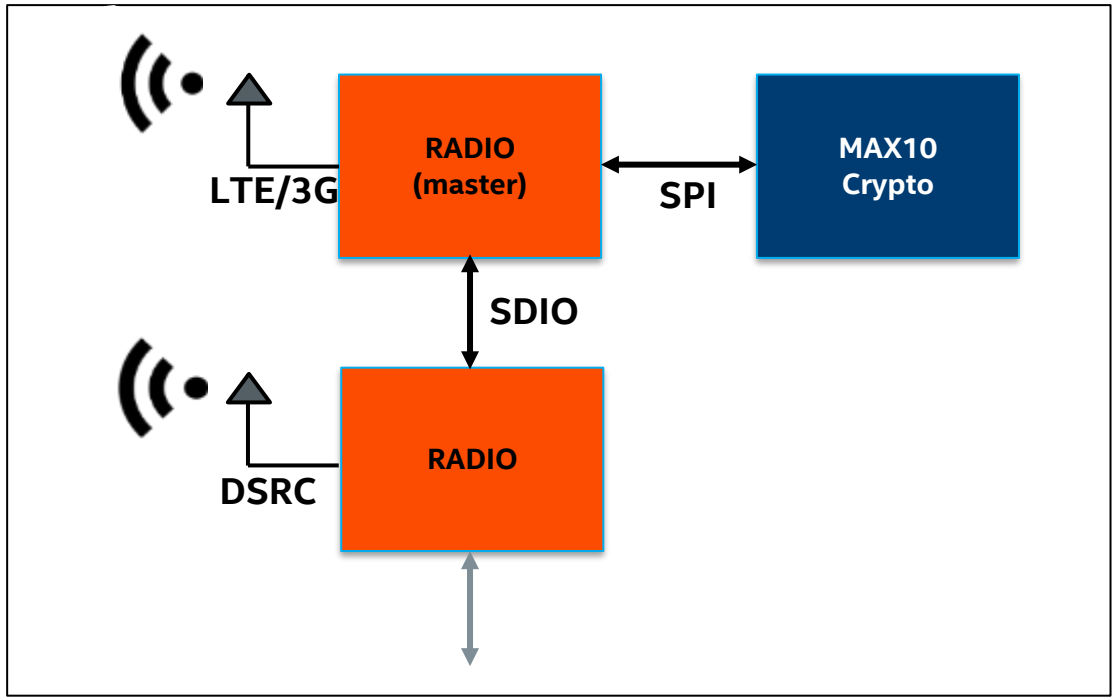
- Low System BOM due to integrated Configuration Flash
- MCU choice decoupled from Radar processing performance
- Flexible Package Options
- Complementary, small footprint integrated power solutions

- Performance to achieve high level of processing bandwidth through parallelism
  - 1.2 Tbits of memory bandwidth, >25GMACs
  - Implement CA & OS CFAR parallel processing
  - 25ms radar processing time
- Enhanced safety with BIST on every radar frame
- Fast TTM and balanced TCO using high-level design flow and tools

- *Lower System Costs*
- *Scalable Performance*
- *Small footprint*

} ***MAX 10 FPGA Companion Value***

Automotive ADAS Application – MAX10:
V2X DSRC Support



- Applications: V2V and V2I
- FPGA based security co-processor
- Dedicated short range communciations (DSRC)
- Application needs:
  - Security
  - High performance
  - Low Latency

- Single chip elliptic curve security algorithm accelerator
- Scalable from 25 to 1,440 operations / second
- MAX 10 density options from 8, 16, 25KLE

Scalable Performance

Lower system costs

Instant-on behaviour

MAX 10 FPGA companion benefits

PLD Benefits for Power Conversion

Altera Automotive-Grade Solutions for:

AC/DC

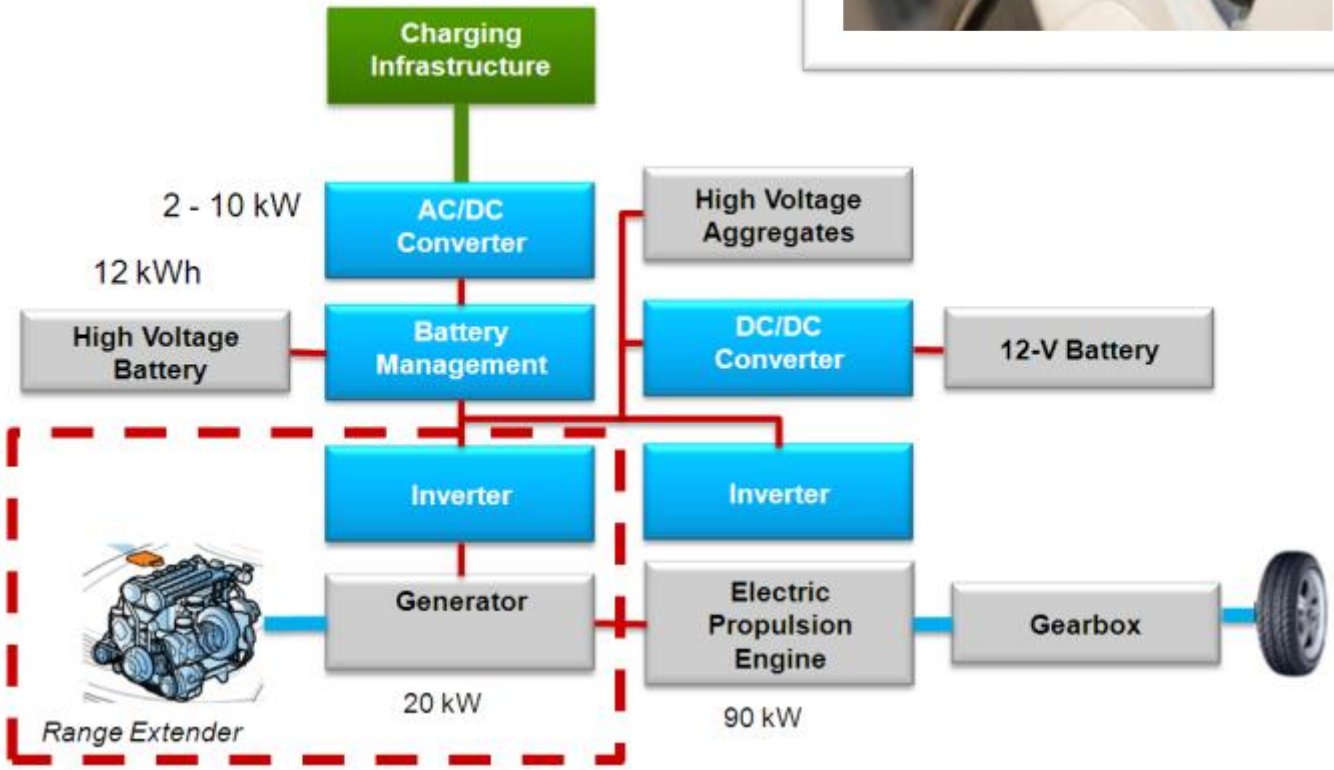
- Charging stations

Low power DC/DC

- HVAC
- Cooling

High power converter

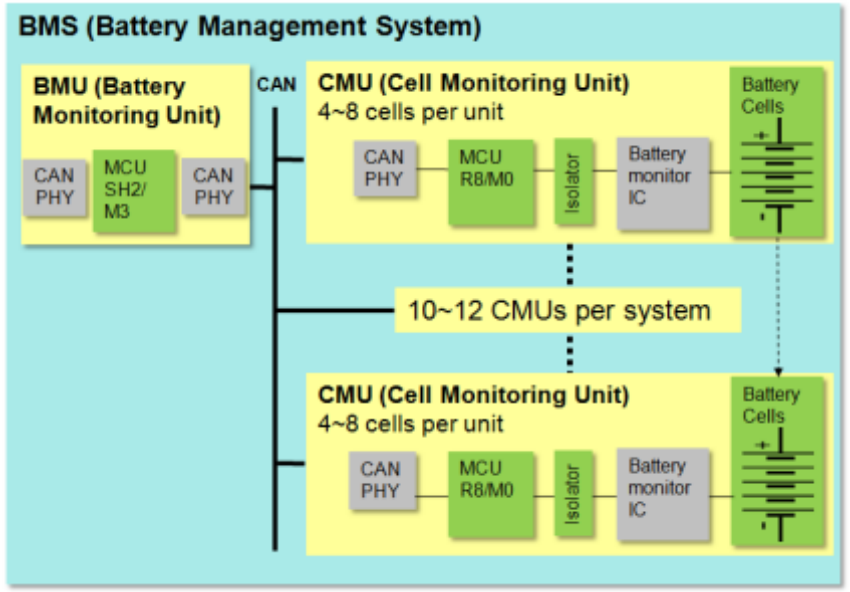
- Engine Inverter



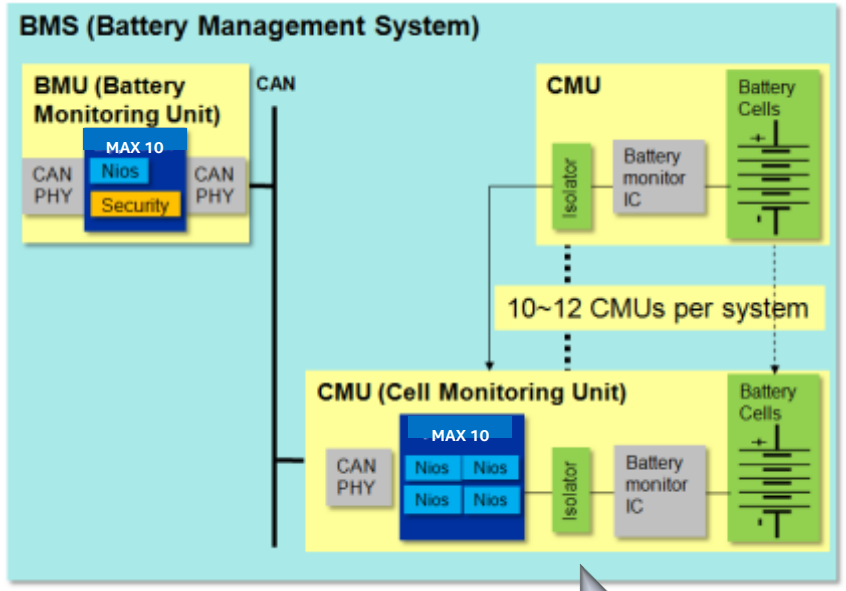
MAX 10 FPGA value = Integrate : DSP + ADC + PLD

FPGA Value as Battery Management "Evolves"

Current



Next Generation



FPGA Increase Differentiation, Cost Saving and Performance

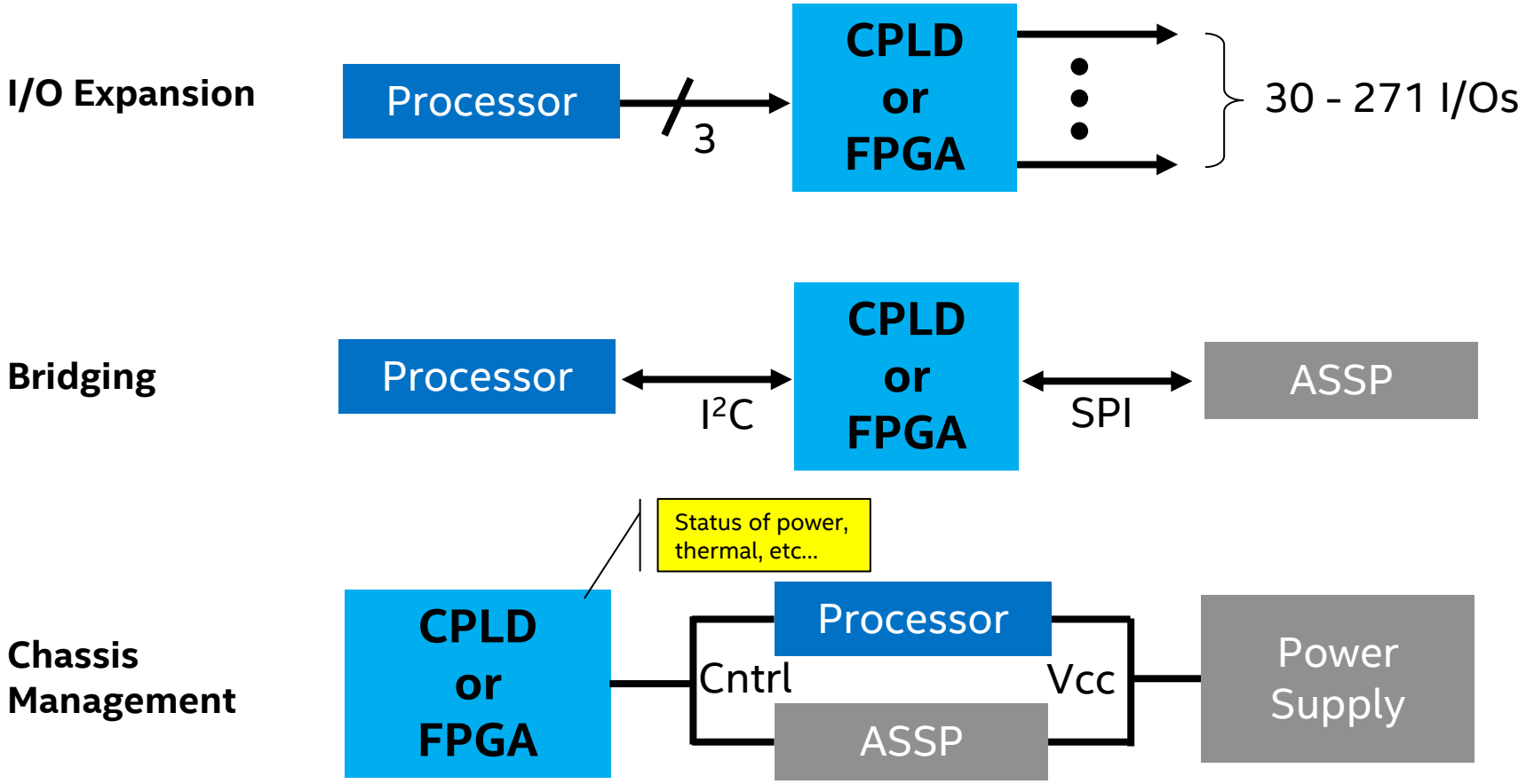
Few PLDs

- Low cost MCU (20MHz) on each CMU
- Simple battery State Of Charge measurement by MCU

Integration to MAX 10 FPGAs + Nios

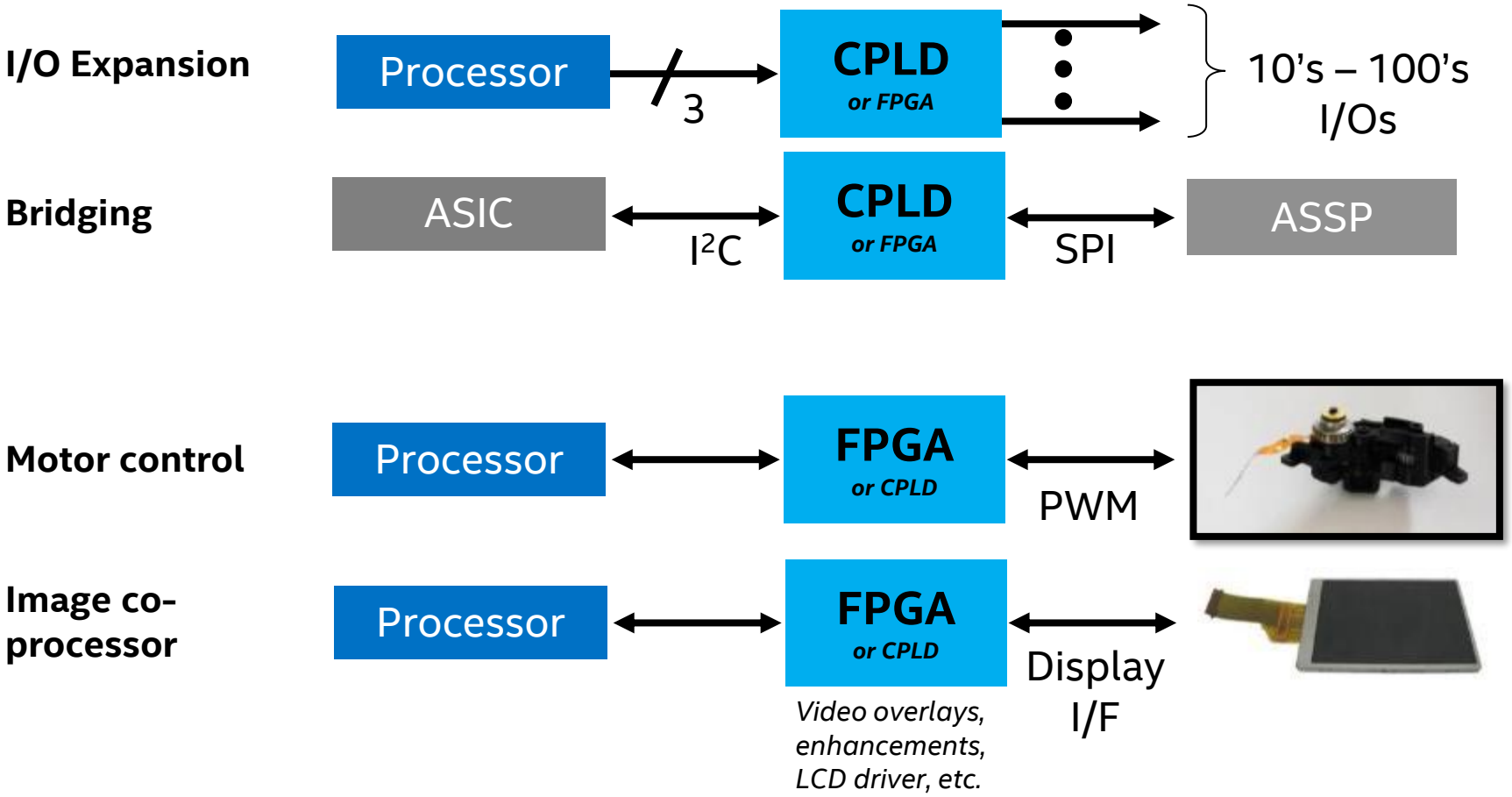
- Daisy-chain CMUs to reduce MCUs and CAN PHYs (~10 per system)
- Faster (~100MHz) and accurate SoC measurement by digital processing (Kalman filter etc.)
- Security for IP protection

Top Three Industrial Applications – More Density & I/O Options

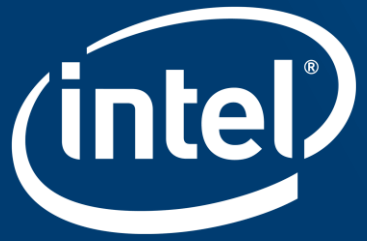


MAX 10 FPGA value = ADC, instant-on, higher density

Consumer functions: Simple → Complex

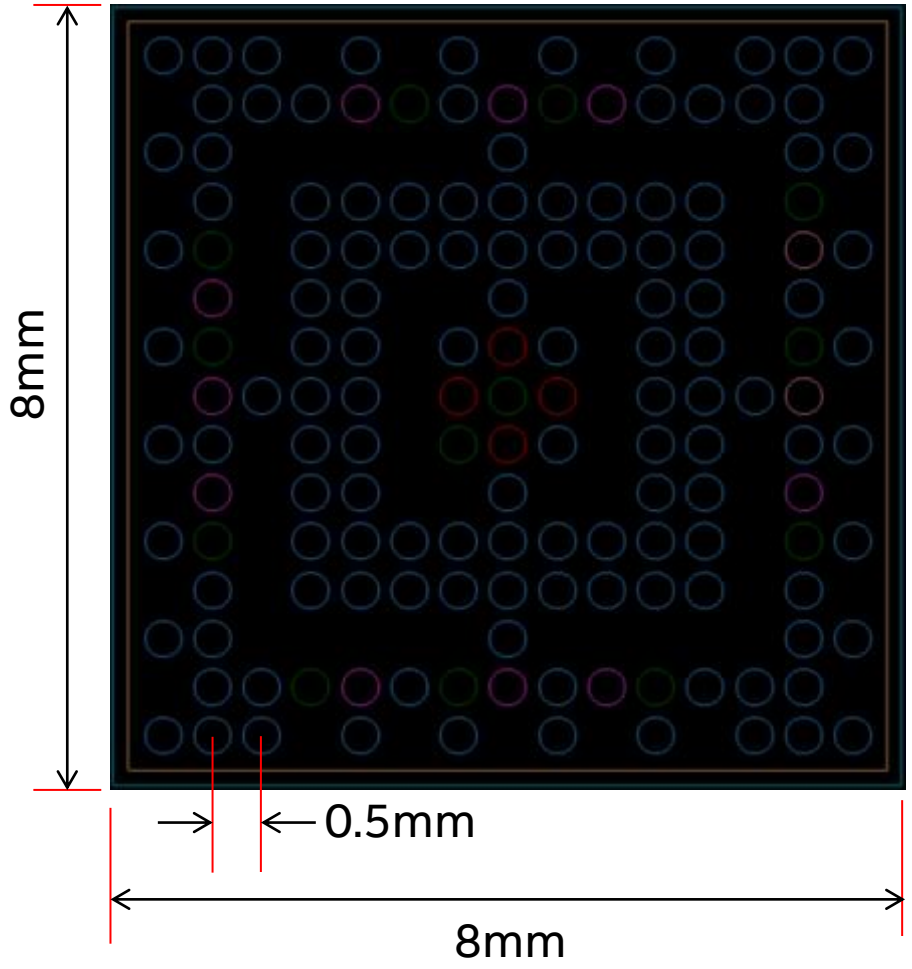


MAX 10 FPGA value = Flexibility, instant-on, small form factor packages



APPENDIX

MAX 10 FPGA M153 Package – "Easy PCB" Footprint



Note: Altera recommended PCB layout (preliminary) in 4Q 2013

Intentionally created gaps in ball grid array to allow space for PCB traces and/or through-hole via's.

Goal: **"Easy" PCB board design**

1. Use 0.8mm pitch design rules instead of 0.5mm rules.
   - 2 layer signal breakout (SMD on both component and PCB)
   - 3 mil line/space
   - 16 mil PTH
   - Shared P/G PTH
2. Avoiding use of blind or buried via's.
3. Minimize the number of PCB layers needed to route to all device pins.

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Intel PSG CPLD Advantages

MAX 10 Market Advantages

- Integrates multiple chips / functions into single chip
  - Single chip dual image configuration
  - User flash memory for data logging, MCU code, other…
    - Single chip soft processor platform
  - Real world interface with 12 bit SAR ADC with 8 – 16 inputs
- Security for IP protection and anti-tampering
  - Safe, secure, single chip remote system update
  - AES Encryption of bitstream secures IP
  - JTAG protection maintains system integrity
- Product line breadth
  - Foot print compatible solutions from 2 K LE to 50 K LE

Lattice Strongest ≤4 K LE density

- Aggressive price points
- Large IO counts in small density devices
- High IO drive strength (up to 16 mA)