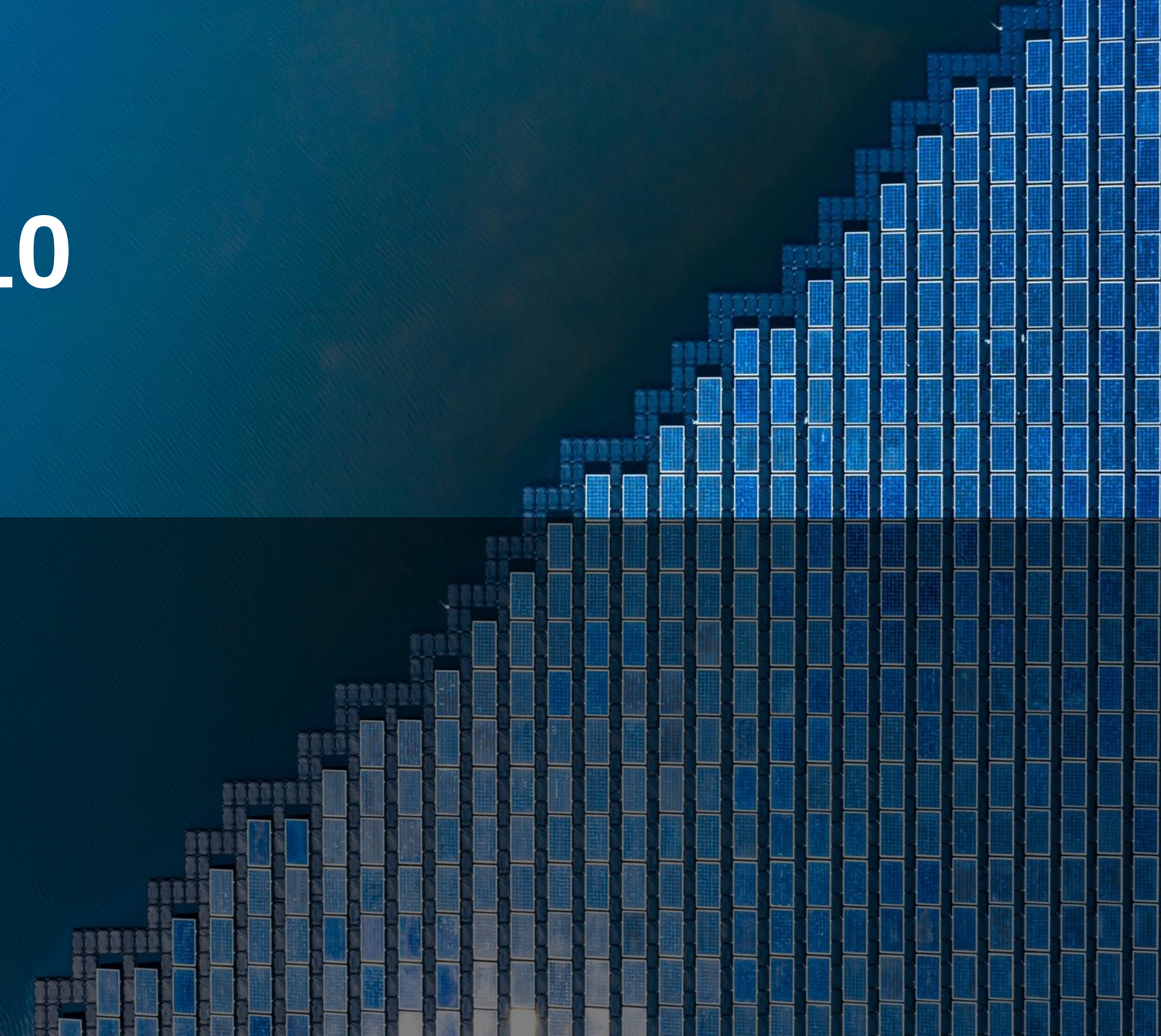
Intel MAX 10

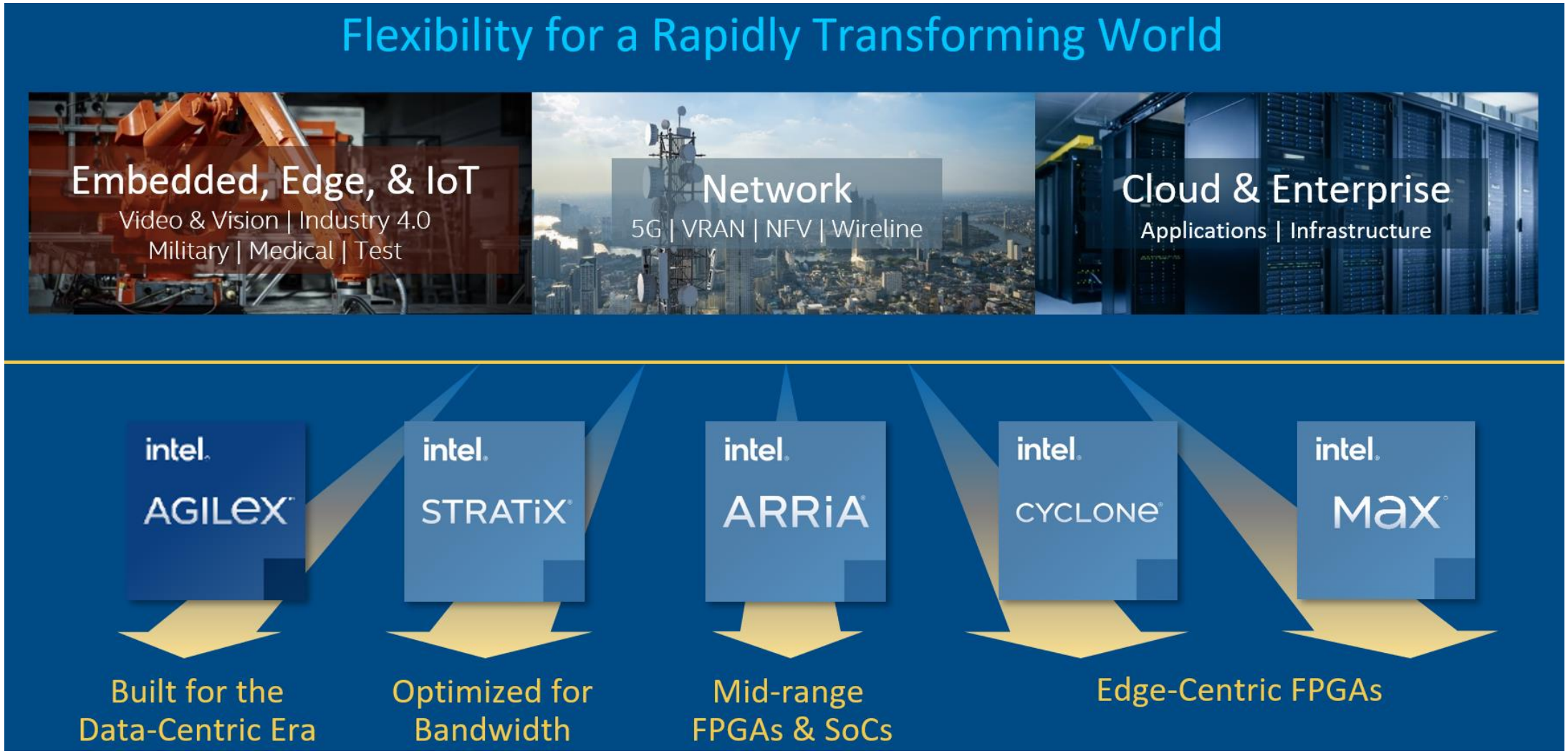
Marco Smutek, Arrow FAE

April, 2021



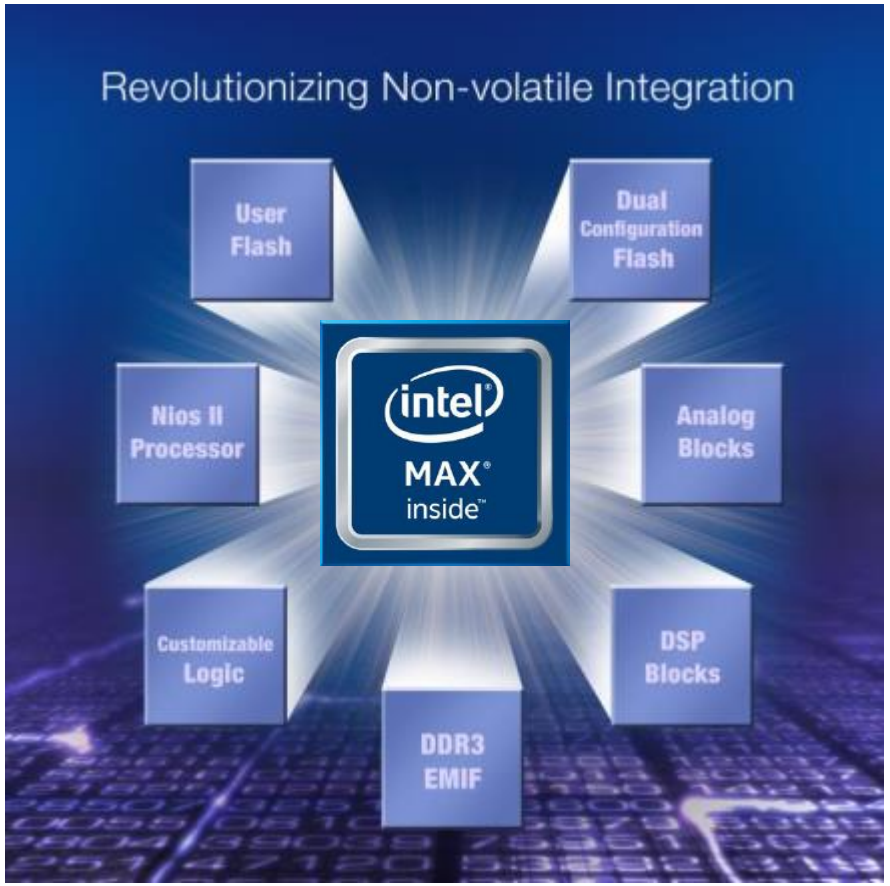
Five Years Out

Innovation Across the Board

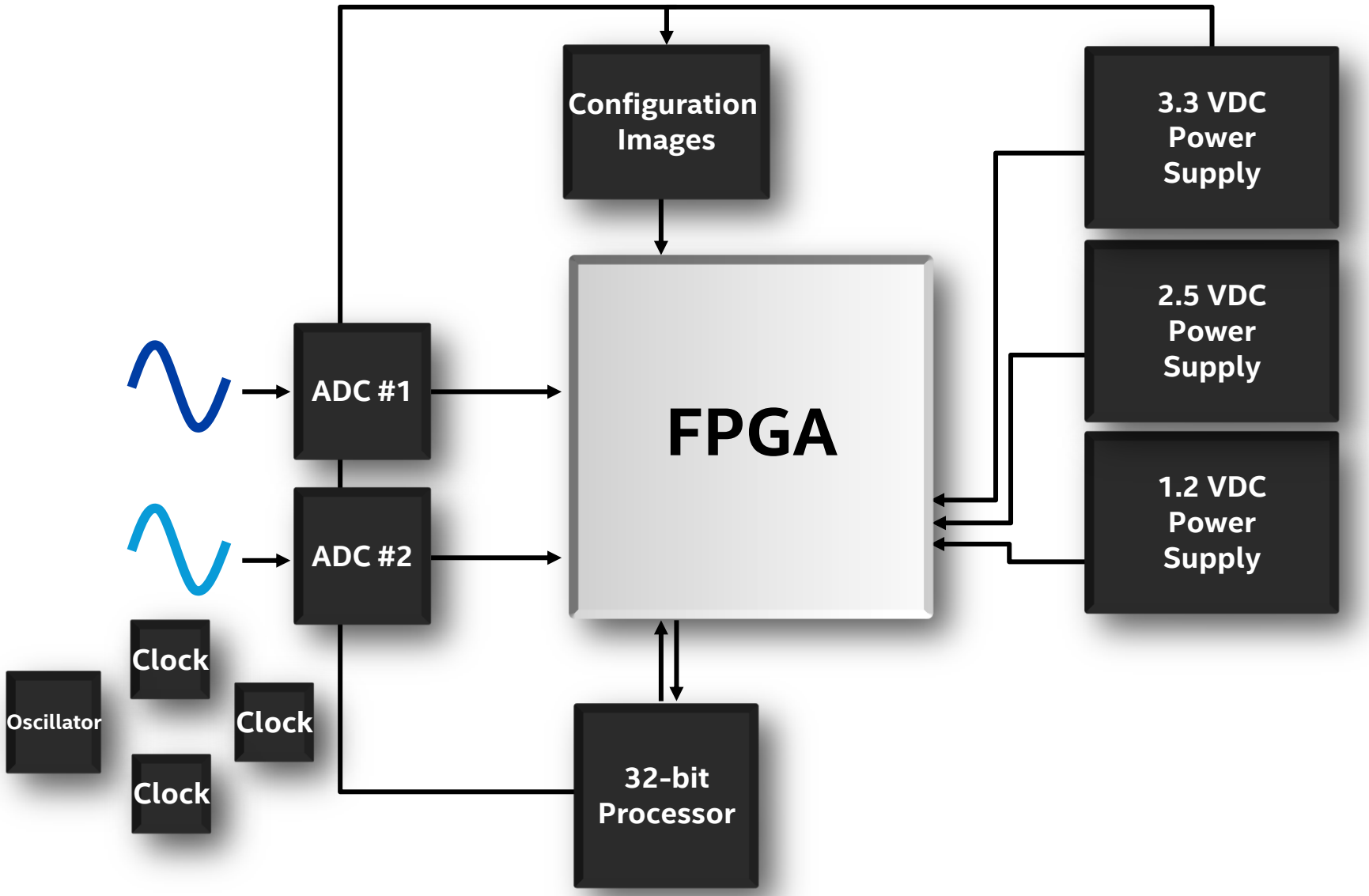


First Single-Chip FPGA to Combine…

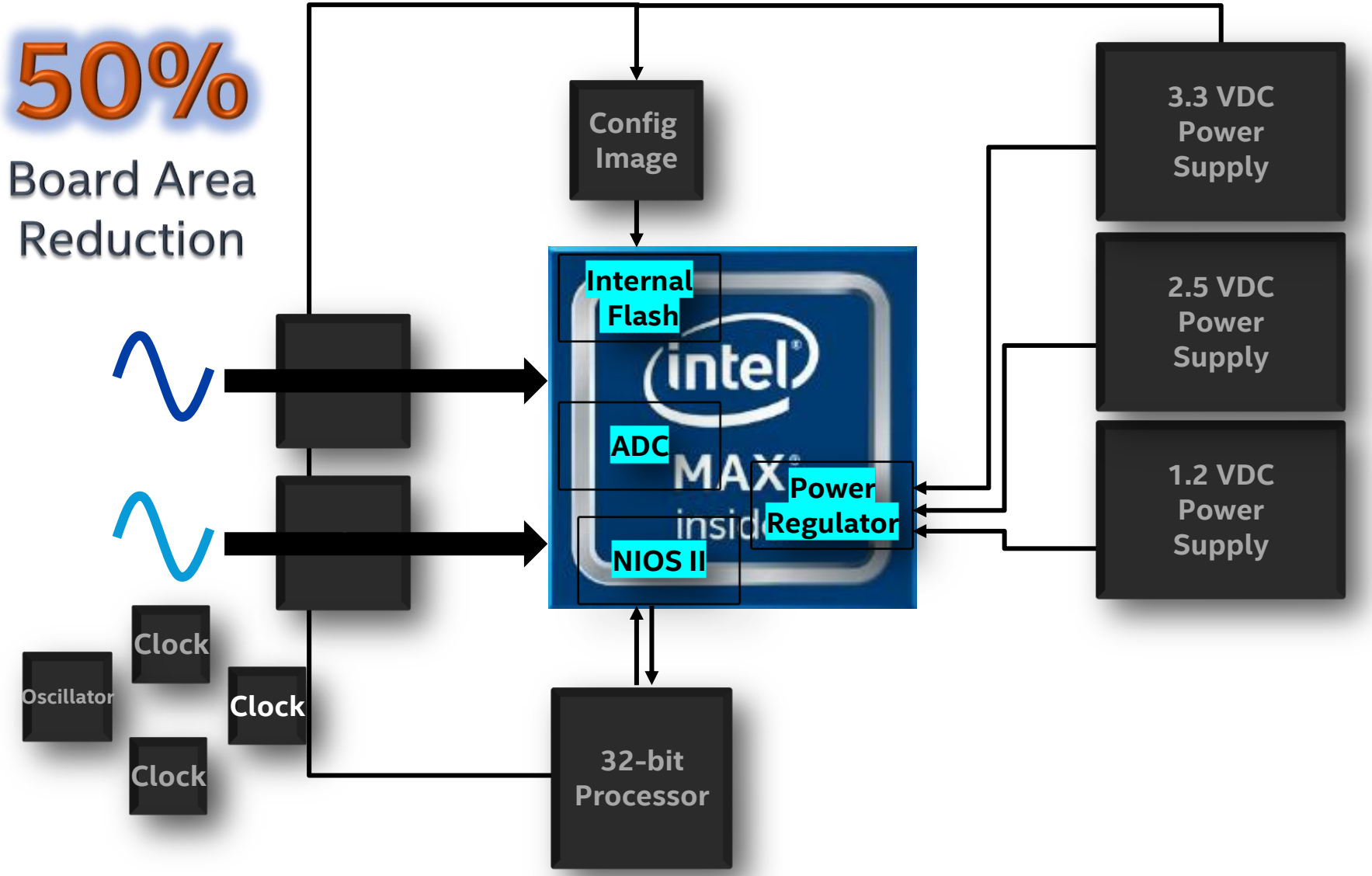
- Non-volatile, instant-on capabilities
- Dual-configuration support
- Embedded flash memory
- Integrated analog blocks
- Single chip soft processor support
- Integrated LDO’s
- Embedded RAM and DSP blocks
- DDR3 external memory interface



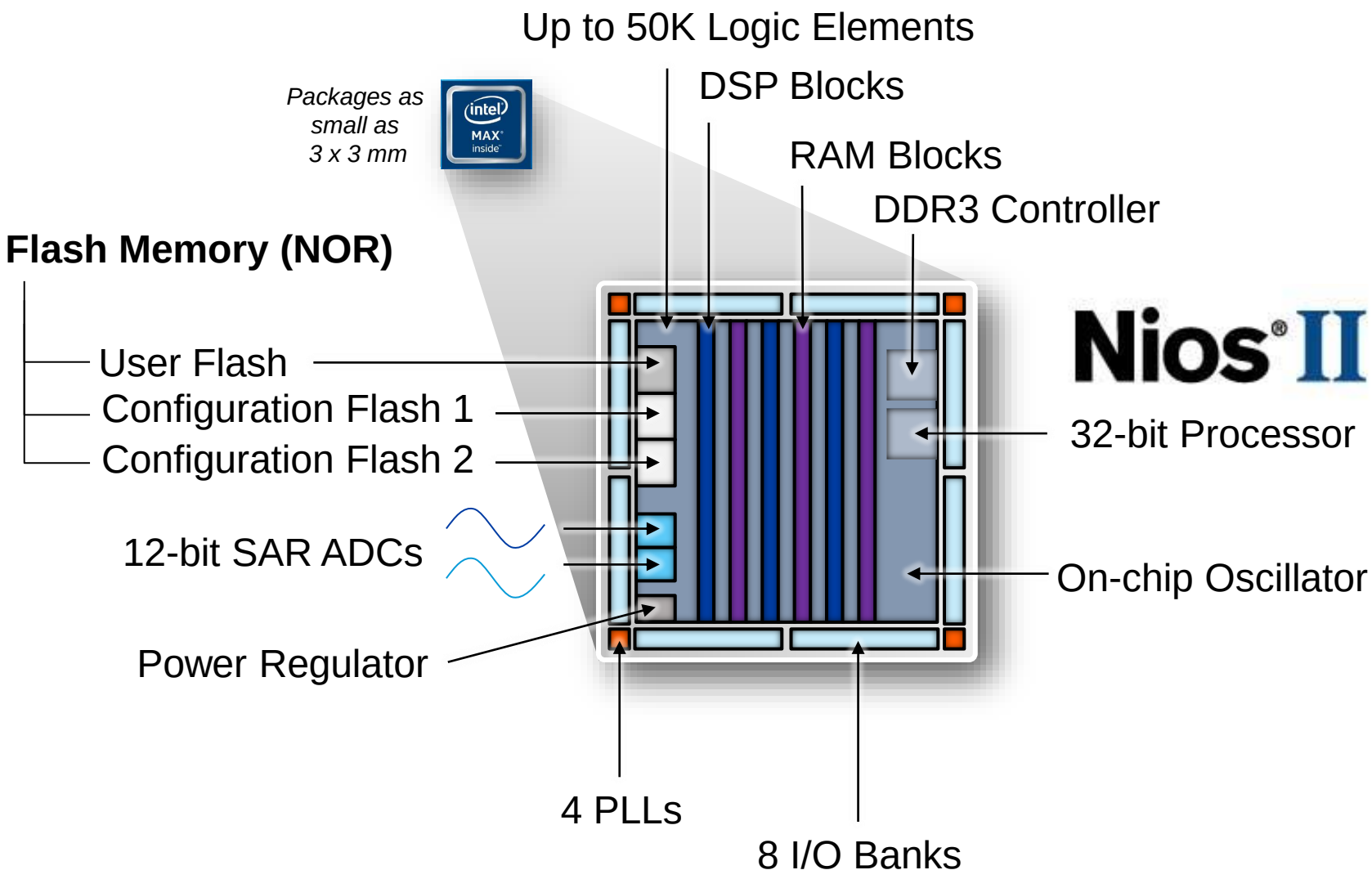
Traditional FPGA System Components



MAX 10 Simplifies Traditional FPGA Systems

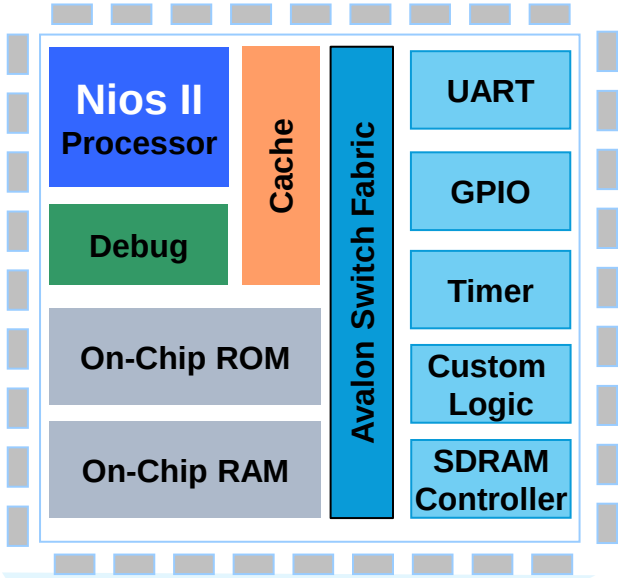


Lower BOM, Smaller PCB Area, Instant-on Configuration



Embedded Processing Capabilities Increase System Value

- Single-chip embedded processor system
  - Soft core Nios II processor support
  - Very small footprint
  - No external RAM or storage needed
- User-customizable processor
  - Flexibility MCUs don't offer
- Supports real-time applications
  - Configuration in under 10 ms
  - Meets automotive and industrial regulatory requirements
- Supports longer life cycles

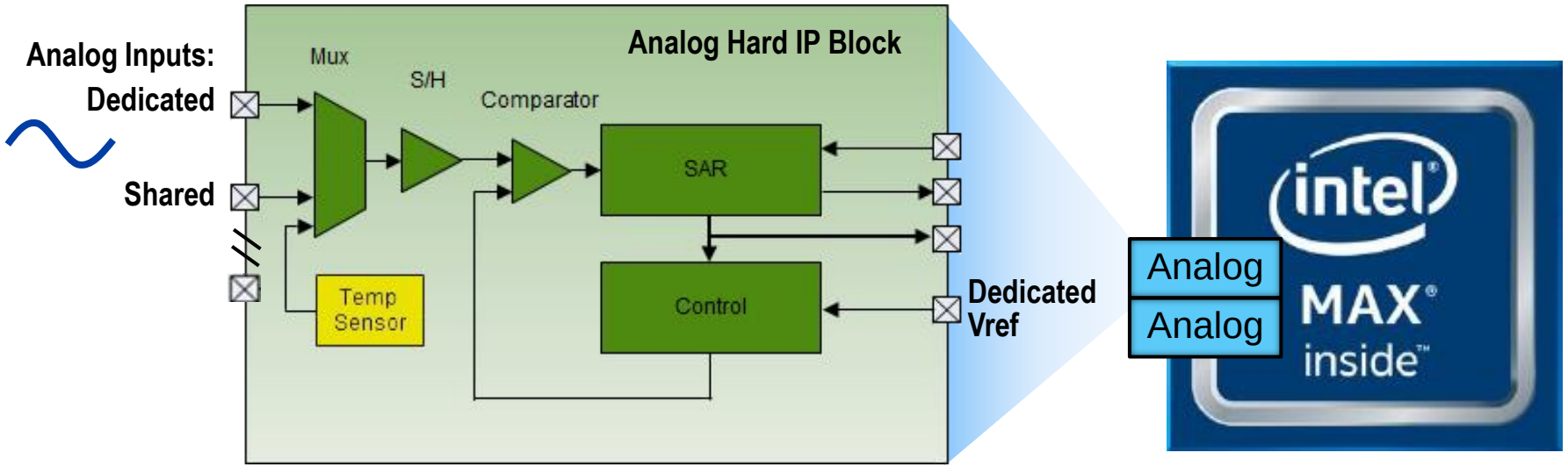


Customizable logic

Nios II

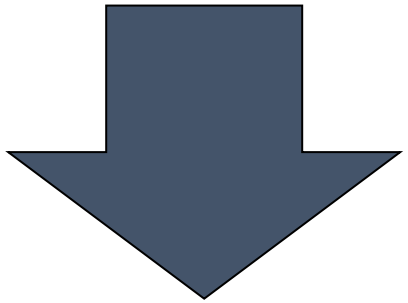
Increase System Value with Integrated Analog Blocks

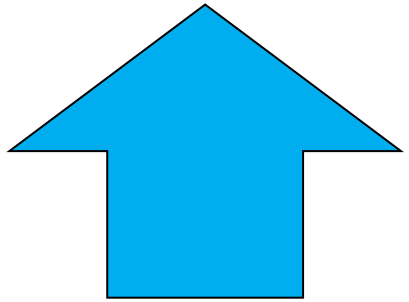
- In-chip system monitoring
  - Integrated ADCs
  - Reduce board space
  - Flexible sample sequencing
  - Lower latency
- Measure environmental conditions
  - Integrated temperature sensor



MAX 10 FPGA Customer Benefits

Lowers System Cost





Increase Board Reliability

Single-chip integration item	Customer Benefits
N-components → 1 component	Higher system reliability (less failure points)
	Reduced BOM/System Cost
Reduced PCB Footprint	Simpler PCB Design
	Fewer PCB layers → Lower PCB cost
Fewer Suppliers	Less vendors to manage
PLD have Longer Life-cycles	Avoids EOL vs. other technologies

MAX 10 Broad Application Coverage

- Industrial drives
- Motor control
- I/O modules

- Automotive infotainment
- Automotive driver assist
- E-vehicle

- Communications
- Computing
- Storage

MAX 10 FPGA – Family Plan

Device	LEs	Block Memory (Kbits)	18x18 Mults	PLLs	Internal Config.	User Flash [1] (KBytes)	ADC, TSD	External RAM I/F
10M02	2,000	108	16	1, 2	Single	12	-	Yes [2]
10M04	4,000	189	20	1, 2	Dual	16 – 156	1, 1	Yes [2]
10M08	8,000	378	24	1, 2	Dual	32 – 172	1, 1	Yes [2]
10M16	16,000	549	45	1, 4	Dual	32 – 296	1, 1	Yes [3]
10M25	25,000	675	55	1, 4	Dual	32 – 400	2, 1	Yes [3]
10M40	40,000	1,260	125	1, 4	Dual	64 – 736	2, 1	Yes [3]
10M50	50,000	1,638	144	1, 4	Dual	64 – 736	2, 1	Yes [3]

Notes:

1. ***User Flash depends upon configuration option.***
2. ***SRAM only.***
3. ***SDR SDRAM, SRAM, DDR3, DDR2, or LPDDR2.***
4. ***ADC blocks available on die but may not be available in low pin count packages.***

MAX 10 FPGA – Feature Set Options

Feature Set	C: Compact	A: Analog
Single configuration	Yes	Yes
Dual configuration w/Remote System Upgrade	-	Yes
Analog Features Block	-	Yes

“C” **“A”**

Two Feature Set Variants from which to order

Package Plan & Available I/O (all devices)

	Dual Power Supply: 1.2V/2.5V						Single Power Supply: 3.3V			
Device	36-WLCSP 3 x 3 mm² 0.4 mm	81-WLCSP 4 x 4 mm² 0.4 mm	256-FBGA 17 x 17 mm² 1.0 mm	324-UBGA 15 x 15 mm² 0.8 mm	484-FBGA 23 x 23 mm² 1.0 mm	672-FBGA 27 x 27 mm² 1.0 mm	144-EQFP 22 x 22 mm² 0.5 mm	153-MBGA 8 x 8 mm² 0.5 mm [1]	169-UBGA 11 x 11 mm² 0.8 mm	324-UBGA 15 x 15 mm² 0.8 mm
10M02	C (27)	-	-	C (160)	-	-	C (101)	C (112)	C (130)	C (246)
10M04	-	-	C/A (178)	C/A (246)	-	-	C/A (101)	C/A (112)	C/A (130)	C/A (246)
10M08	-	C/F* (56)	C/A (178)	C/A (246)	C/A (250)	-	C/A (101)	C/A (112)	C/A (130)	C/A (246)
10M16	-	-	C/A (178)	C/A (246)	C/A (320)	-	C/A (101)	-	C/A (130)	C/A (246)
10M25	-	-	C/A (178)	-	C/A (360)	-	C/A (101)	-	-	
10M40	-	-	C/A (178)	-	C/A (360)	C/A (500)	C/A (101)	-	-	
10M50	-	-	C/A (178)	-	C/A (360)	C/A (500)	C/A (101)	-	-	

Notes:

1 - "Easy PCB" utilizes 0.8mm PCB design rules

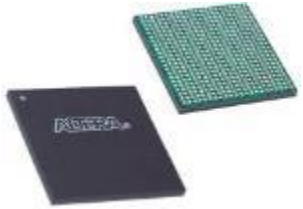
2 - A subset of p/n's will be available in Automotive grade.

Preliminary and subject to change without notice.

Bare Die

C: Compact features
F*: Dual configuration
A: Analog features

WLCSP



xBGA

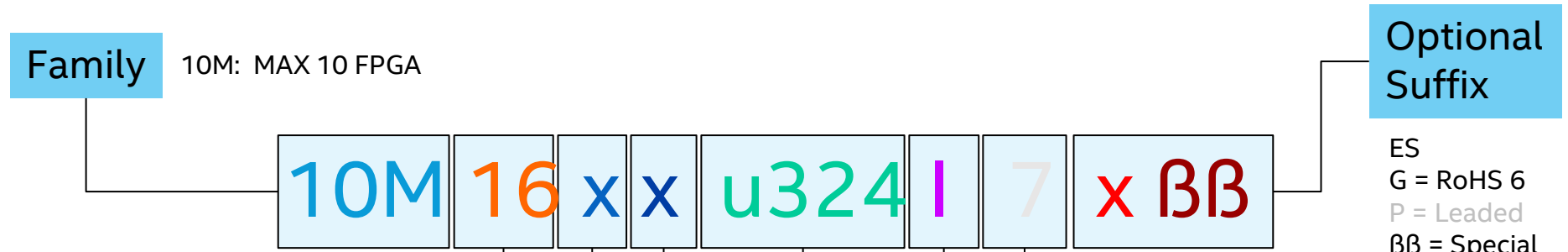
M = 0.5mm ball spacing
U = 0.8mm ball spacing
F = 1.0mm ball spacing

EQFP

MAX 10 FPGA I/O Standard Support

I/O Standard	Variant	Toggle Rate (MHz)	Max Strength	Load	Application
Single-Ended	LVTTL/LVCMOS 3.3V	250	2 mA	10 pF	General purpose
	LVTTL/LVCMOS 3.0V	250	16 mA	10 pF	General purpose
	LVTTL/LVCMOS 2.5V	250	16 mA	10 pF	General purpose
	LVTTL/LVCMOS 1.8V	250	12 mA	10 pF	General purpose
	LVTTL/LVCMOS 1.5V	250	8 mA	10 pF	General purpose
	LVTTL/LVCMOS 1.2V	250	8 mA	10 pF	General purpose
	PCI	250	-	10 pF	General purpose
	Schmitt Trigger (RX only)	200	-	-	General purpose
External Memory Interfaces (& Voltage Referenced I/O)	SSTL2 Class I	250	12 mA/50 Ω	7 pF	DDR1
	SSTL2 Class II	250	16 mA/25 Ω	7 pF	DDR1
	SSTL18 Class I	300	12 mA/50 Ω	7 pF	DDR2
	SSTL18 Class II	300	16 mA/25 Ω	7 pF	DDR2
	SSTL15 Class I	300	12 mA/50 Ω	7 pF	DDR3
	SSTL15 Class II	300	16 mA/25 Ω	7 pF	DDR3
	SSTL15	300	34 Ω	7 pF	DDR3
	SSTL135	300	34 Ω	7 pF	DDR3L
	HSUL12	200	34 Ω	7 pF	LPDDR2
	HSTL18 Class I	300	12 mA/50 Ω	7 pF	DDR2+/QDR2+/RLDRAM2
	HSTL18 Class II	300	16 mA/25 Ω	7 pF	DDR2+/QDR2+/RLDRAM2
	HSTL15 Class I	300	12 mA/50 Ω	7 pF	DDR2+/QDR2/QDR2+/RLDRAM2
	HSTL15 Class II	300	16 mA/25 Ω	7 pF	DDR2+/QDR2/QDR2+/RLDRAM2
	HSTL12 Cass I	200	12 mA/50 Ω	7 pF	General purpose
	HSTL12 Class II	200	14 mA/25 Ω	7 pF	General purpose
LVDS	Dedicated LVDS (RX/TX)	830/800 Mbps	-	6 pF	
	Dedicated Mini-LVDS (TX)	380 Mbps	-	6 pF	
	Dedicated RSDS (TX)	340 Mbps	-	6 pF	
	Dedicated PPDS (TX)	420 Mbps	-	6 pF	
	External Resistor LVDS (TX)	600 Mbps	-	6 pF	
	External Resistor Mini-LVDS (TX)	380 Mbps	-	6 pF	
	External Resistor RSDS (1R) (TX)	170 Mbps	-	6 pF	
	External Resistor RSDS (3R) (TX)	342 Mbps	-	6 pF	
	External Resistor PPDS (TX)	420 Mbps	-	6 pF	
	LVPECL (RX only)	830 Mbps		6 pF	
	BLVDS (RX/TX)	830/475 Mbps	16 mA	6 pF	

MAX 10 FPGA – Ordering Information



Family 10M: MAX 10 FPGA

Optional Suffix

ES
G = RoHS 6
P = Leaded
ßß = Special processing

Product Line

02: 2K LE's
04: 4K LE's
08: 8K LE's
16: 16K LE's
25: 25K LE's
40: 40K LE's
50: 50K LE's

Power Supply

S: Single Voltage
D: Dual Voltage

Feature Option

C: Compact features
A: Analog features
F*: Dual configuration

Package Type & Ball Count

V: Wafer level chip-scale
E: EQFP
M: MBGA
U: UBGA
F: FBGA

36, 81
144
153
169, 324
256, 484, 672

Speed

6, 7, 8
6 = fastest,
8 = slowest

Grade / Temperature

C: Commercial (T_J = 0°C to +85°C)
I: Industrial (T_J = -40°C to +100°C)
A: Automotive (T_J = -40°C to +125°C)

F*: Dual configuration (only available on V81 package)

Development Tools and Solutions

Quartus Prime Software and IP Support

QUARTUS® PRIME DESIGN SUITE

- Number one design software in performance and productivity
- MAX 10 FPGA compilation & EPE support
  - Flash and ADC Megawizards
  - Analog Tool Kits for ADC evaluation and debug

INCLUDES QSYS SYSTEM INTEGRATION AND DSP BUILDER FOR INCREASED PRODUCTIVITY

- Nios II support and DSP Builder + Advanced Block-set

ABUNDANT IP & REFERENCE DESIGNS

- Intel Design Store

Quartus Prime Lite Edition Software
Complete MAX 10 support at no Cost!

MAX 10 FPGAs App Notes & Design Examples

Available on Design Store

Design Examples
AN 496 - Using the Internal Oscillator in Altera MAX Series
AN 547: Putting Altera MAX Series in Hibernation Mode Using User Flash Memory
AN 425: Using the Command-Line Jam STAPL Solution for Device Programming
AN 502: Implementing an SMBus Controller in Altera MAX Series
AN 630: Real-time ISP and ISP Clamp for Altera MAX Series
AN 494: GPIO Pin Expansion using I2C Bus Interface in Altera MAX Series
AN 485: Serial Peripheral Interface Master in Altera MAX Series
AN 486: SPI to I2C Using Altera MAX Series
AN 488 - Stepper Motor Controller using Altera MAX Series
AN 294: Crosspoint Switch Matrices in Altera MAX Series
AN 501: Pulse Width Modulations Using Altera MAX Series
AN 500: NAND Flash Memory Interface with Altera MAX Series
AN 509: Multiplexing SDIO Devices Using Altera MAX Series
AN 490: Altera MAX Series as Voltage Level Shifters
AN 265: Using Altera MAX Series as a Microcontroller I/O Expander
AN 286: Implementing LED Drivers in Altera MAX Series
AN 498: LED Blink Using Power Sequencing in Altera MAX Series
AN 495: IDE/ATA Controller Using Altera MAX Series
AN 492: CF+ Interface using Altera MAX Series
AN 493: I2C Battery Gauge Interface using Altera MAX Series
AN 491: Power Sequence Auto-start Using Altera MAX Series

Thank You

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Five Years Out