Tyler Holland

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Lab 9A (Final)

**Alarm System**

**Purpose:**

The purpose of this experiment is to use all of our past experiments and combine them in a way to create a functional alarm system with an alarm state, armed state, and unarmed state, along with a 4 bit passcode.

**Setup:**

The only setup required was to download the D\_FF and ALARM\_FSM files from the course website and integrate them with our previous VHDL code. Then we just used ExPort to put the .bit file onto the Nexys2 board.

**Procedure 1:**

For this procedure we created a state transition diagram and PS/NS table for how we thought the ALARM\_FSM should work. These pages are included on separate pieces of paper.

**Procedure 2:**

For this procedure we analyzed the provided ALARM\_FSM code and created a testbench waveform to make the FSM go to every possible state given every possible input. The only problem we encountered at this point was getting ModelSIM to show the entire waveform. The results are included on a separate piece of paper.

**Procedure 3:**

For this procedure we created a new project in Xilinx and added all of our past VHDL code to the project. We then also added the provided ALARM\_FSM code and D\_FF code to the project. We then used the diagrams on the project handout and our previous thought diagrams to implement everything correctly as components and signals connecting those components.

The code is provided on a separate piece of paper.

**Conclusions:**

**Tyler**: In this final Lab I finally combined all of the work from the past labs to create a fairly functional alarm system. Using the AlarmFSM provided for us, I used VHDL and my past VHDL code to hook up the system as explained in the project handout. Using components and signals, I was able to easily incorporate my past projects into my new Lab9A code. Afterwards, all I had to do was simply assign the package pins correctly and I was good to go. This was a fun last experiment, because I can actually see all of the individual experiments working together correctly.

**Suzie:** In todays lab we combined all the VHDL code we created in previous labs in order to make an alarm system. The code for the finite state machine was given to us, but we had to analyze it in order to create proper test cases for the component and the whole machine. Once we were confident that all the components worked independently, we wrote more VHDL in order to combine the components. We had to assign the system with a secret code in order to turn the alarm off. Next we hooked it up tp the Nexys board and hand tested it. I enjoyed seeing all our work throughout the quarter and all that we had learned in lecture applied to this final project.