**Tyler Holland**

**--Upper Level (in bold)**

**library IEEE;**

**use IEEE.STD\_LOGIC\_1164.ALL;**

**Entity 4bit\_magcomp IS**

**Port(A, B : in STD\_LOGIC\_VECTOR(3 downto 0);**

**A\_equals\_B, A\_gt\_B : out STD\_LOGIC);**

**End 4bit\_magcomp;**

--Component Design for the Comparator (LOWER LEVEL)

entity Comparator2Bit is

Port ( A : in STD\_LOGIC\_VECTOR(1 downto 0);

B : in STD\_LOGIC\_VECTOR(1 downto 0);

AeqB : out STD\_LOGIC; -- True if A = B

AgtB : out STD\_LOGIC); -- True if A > B

end Comparator2Bit;

architecture DataFlow of Comparator2Bit is

begin

AeqB <= ( A(1) xnor B(1) ) and ( A(0) xnor B(0) );

AgtB <= ( A(1) and not B(1) ) or ( A(0) and not B(1) and not B(0) )

or ( A(1) and A(0) and not B(0) );

end DataFlow;

**Architecture struct OF 4bit\_magcomp IS**

**Component Comparator2Bit is**

**Port ( A : in STD\_LOGIC\_VECTOR(1 downto 0);**

**B : in STD\_LOGIC\_VECTOR(1 downto 0);**

**AeqB : out STD\_LOGIC; -- True if A = B**

**AgtB : out STD\_LOGIC); -- True if A > B**

**End Component**

**Signal eq1, eq2, gt: STD\_LOGIC;**

**Begin**

**C1: Comparator2Bit port map (A(3 downto 2), B(3 downto 2), eq1, open);**

**C2: Comparator2Bit port map (A(1 downto 0), B(1 downto 0), eq2, gt);**

**A\_equals\_B <= eq1 AND eq2;**

**A\_gt\_B <= gt;**

**End struct;**