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Entity hw20 is

Port (N, D : in std\_logic;

GiveToken, ChangeBack: out std\_logic);

End hw20;

Architecture brains of hw20 is

Type State\_type is (Got 0, Got5, Got10);

Signal PS, NS : State\_type := Got0;

Begin

Theprocess : process (PS, D, N) is

Begin

Case PS is

When Got0 =>

If(N = ‘0’) then

If(D = ‘0’) then NS <= got0; givetoken<=’0’; changeback<=’0’;

else NS <= got10; givetoken<=’0’; changeback<=’0’;

end if;

else

If(D = ‘0’) then NS <= got5; givetoken<=’0’; changeback<=’0’;

else NS <= got0; givetoken<=’0’; changeback<=’0’;

end if;

end if;

When Got5 =>

If(N = ‘0’) then

If(D = ‘0’) then NS <= got5; givetoken<=’0’; changeback<=’0’;

else NS <= got0; givetoken<=’1’; changeback<=’0’;

end if;

else

If(D = ‘0’) then NS <= got10; givetoken<=’0’; changeback<=’0’;

else NS <= got5; givetoken<=’0’; changeback<=’0’;

end if;

end if;

When Got10 =>

If(N = ‘0’) then

If(D = ‘0’) then NS <= got10; givetoken<=’0’; changeback<=’0’;

else NS <= got0; givetoken<=’1’; changeback<=’1’;

end if;

else

If(D = ‘0’) then NS <= got0; givetoken<=’1’; changeback<=’0’;

else NS <= got10; givetoken<=’0’; changeback<=’0’;

end if;

end if;

end case;

end process theprocess;

end brains;