ECE 467: Introduction VLSI Design

Project: Multiplication and Accumulation (MAC) Datapath for Neural Networks

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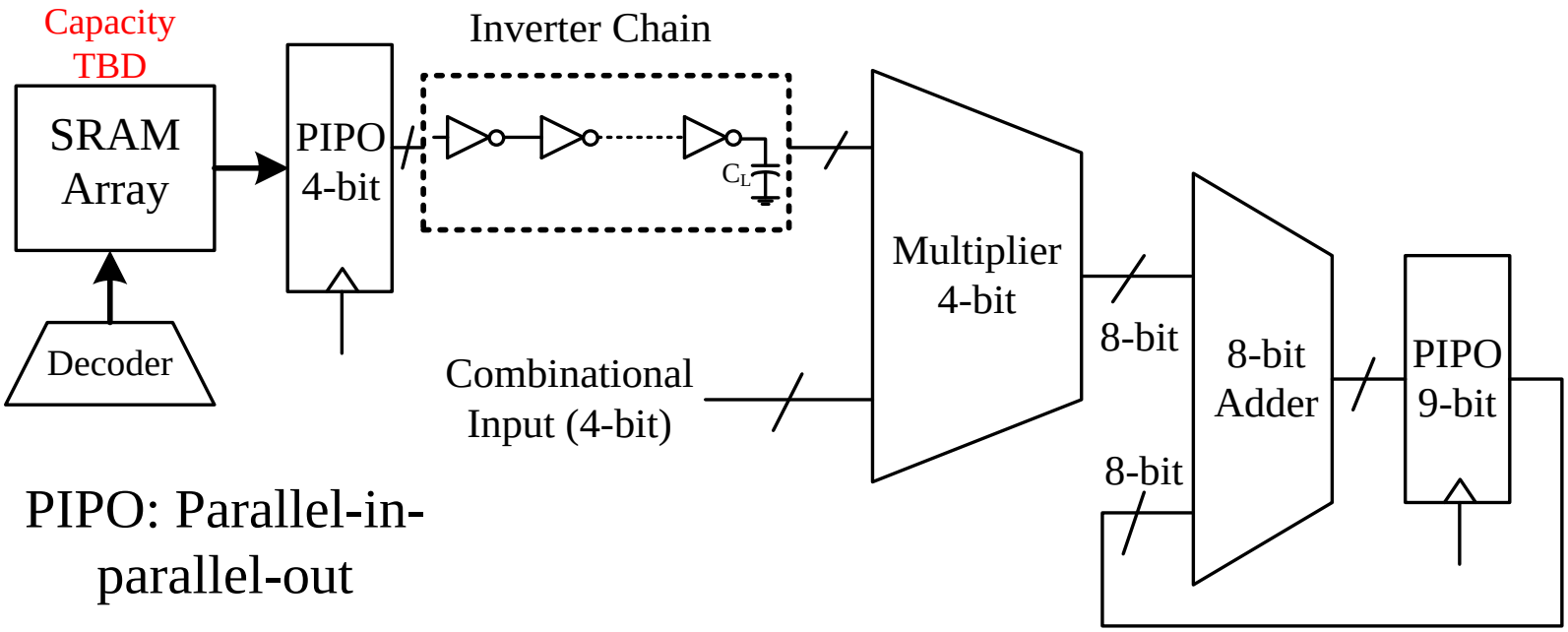
System Goal



PIPO: Parallel-in-parallel-out

System Level Components

- High level components
  - Inverter chain and universal gates
  - Adder
  - Multiplier
  - Register
  - SRAM

TBD based on sequence in which topics are covered in lecture

Specifications

- Technology: 45nm
- Nominal supply voltage: 0.9V-1.2V (choose appropriately to optimize the performance)
  - Targeted clock frequency: 1 GHz
- Aim-
  - Achieve functionality
  - Supply Voltage should be same for all the system blocks
  - Apply techniques learnt in the course to maximize frequency
  - **Low power design:** apply different power saving techniques to make your design energy efficient

Transistor Specifications

- VTG: Regular threshold voltage transistor should be used for project design

Submission Schedule

- Project Report I [5% of the total]: October 27th
- Project Report II [5% of the total]: November 17th
- Final Report [15% of the total]: December 9th
- Classroom Presentation [5% of the total]: Last week of classes

All report are due by the midnight of the due date

Tentative Project Plan

- Part-1 (Schematic Design)
  - Inverter chain design and NAND, NOR, XOR implementation (including symbols)
  - Adder
  - Flip/Flop design
  - Multiplier design
  - SRAM design
- Part-2
  - System level integration

Tentative Submission Dates

- Reports are due biweekly. Final grades for lab will be cumulative of these reports.
- Classroom presentations near the end of semester [TBD]
- This document will be updated biweekly. Please check this document regularly.

Project Report 1

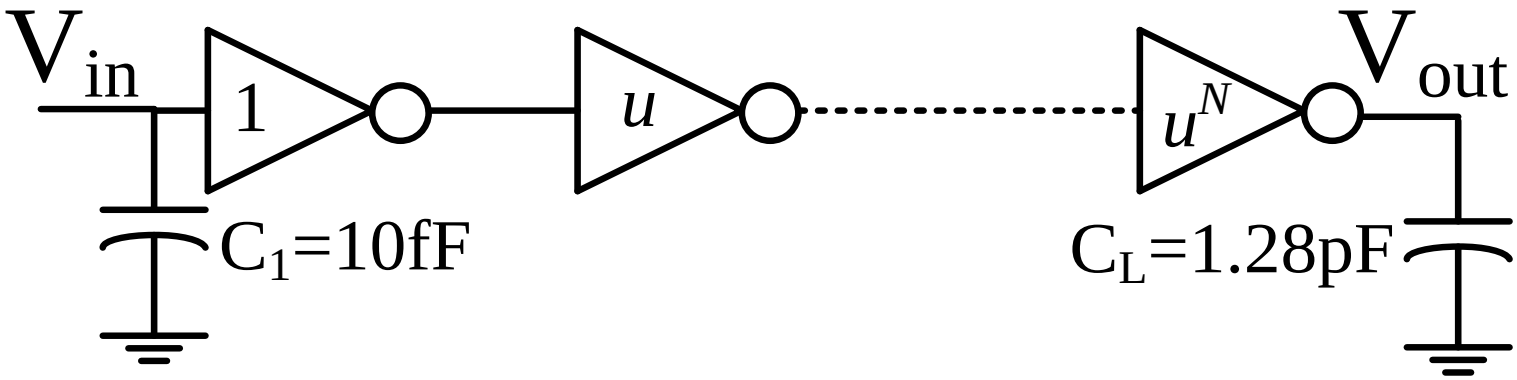
- *<u>Design of Inverter Chain to drive larger loads:</u>*
  - Memory blocks are often located far from the processing elements. Therefore, long interconnects are required for data transmission.
  - Using long interconnects leads to significant capacitive load at PIPO's output.
  - To drive larger loads efficiently, we use inverter chains

Project Report 1(contd..)

- In this sub-project, we will be designing an inverter chain to efficiently drive larger loads.

- *<u>Project Description:</u>*
  - Let the input capacitance of a minimum sized inverter be C1=10fF
  - Determine the number of appropriately sized inverter stages required to drive a load of 128C1=1.28pF
    - Refer to the lecture notes on sizing of inverter chain

Project Description(contd..)



Number of stages (N)	Upsizing Factor (*u*)	Propagation delay (t_p)
1		
2		
3		
4		
5		

Project Report 1

- Results required:
  - Delay characteristics for different N (Cadence plots) and complete the given table
  - Delay *vs.* Number of stages (N)
  - Delay *vs.* Supply Voltage (for optimal N)
  - Delay *vs.* Temperature (for optimal N)
  - Leakage current *vs.* Supply Voltage & Temperature (for optimal N)
  - Optimize the body biasing of all the NMOS transistors to minimize delay and plot Delay vs. V_{BS} (V_{BS} ranging -0.25 to 0.25) (for optimal N) [All the NMOS will have same V_{BS}]

Additional Assignment

- Create a library of standard cells including 2-input NAND & NOR, 3-input NAND & NOR and 2-input EXOR [size these gates to match t_{phl} and t_{plh} characteristics with that of a minimum sized inverter. For all designs, $L_p=L_n=L_{min}$=45nm. Minimum sized inverter: $W_{min}=2XL_{min}$, $W_n=W_{min}$, $W_p=2X\ W_{min}$]
- Create two more variants of the above setup as follows:
  - To match characteristics of an inverter upsized by a factor 2
  - To match characteristics of an inverter upsized by a factor 3

Some tips

- Label everything appropriately (nodes, wires, instances), no default labels
- Minimum size inverter can be named as INVx1, and twice strength one as INVx2. Use similar naming convention for the other gates too.
- Write one-line description of the circuit in the schematic view
- Schematic should be easy to follow

Additional Assignment (contd..)

- *<u>Results Required:</u>*
  - Delay *vs.* Supply Voltage
  - Delay *vs.* Temperature
  - Leakage current *vs.* Supply Voltage & Temperature
  - Optimize the body biasing of all the NMOS transistors to minimize delay and plot Delay vs. V_{BS} (V_B ranging -0.25 to 0.25)[All the NMOS will have same V_B]

Project Report 2

- Design 1-bit Full adder using
  - Architecture of your choice (design your schematic using expression in slides 6 & 7 of Adders lecture)
  - Static CMOS Full Adder architecture (Refer to slide 7)
  - Transmission Gate Based Full Adder architecture (Refer slide 11 & 12)

Project Report 2

- Results required for adder design
  - Compare the area and delay performance of different Full Adder architectures and select the best architecture to work with
  - Delay vs. Supply Voltage
  - Delay vs. Temperature
  - Leakage current vs. Supply Voltage and Temperature

Project Report 2 (contd.)

- Using the chosen Full Adder implementation style
  - Design an 8-bit Ripple Carry Adder (Refer Slide 15)
  - Design an 8-bit Carry Select Adder (Refer Slide 37)
  - Optimize one of the above designs to achieve a worst-case delay of <500ps (i.e, design to retain functionality when Cin is switched at a frequency > 1.5GHz)

Project Report 2

- Results required
  - Obtain proper functionality
  - Compare the area and delay performance of the two architectures
  - Determine and state the input combination for worst-case delay
  - Worst-Case Delay vs. Supply Voltage
  - Worst-Case Delay vs. Temperature
  - Leakage current vs. Supply Voltage and Temperature

Final Report

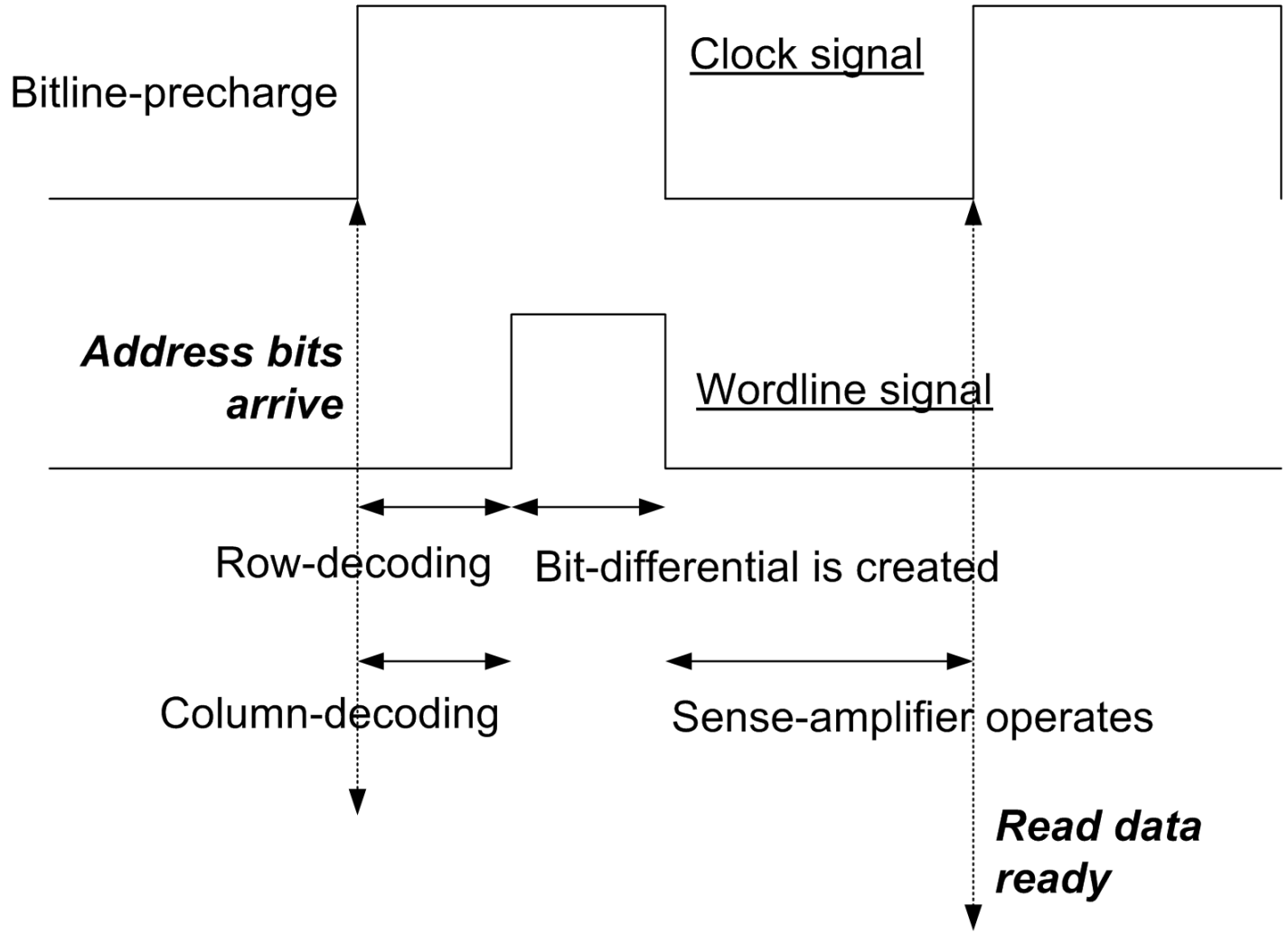
- Design an SRAM cell
  - Design an 6T SRAM cell
  - Read Noise Margin ≥ 30% of VDD
  - Write Noise Margin ≥ 30% of VDD
  - Required results
    - Clearly show the design steps
    - Power Consumption *vs.* VDD and Temperature
    - Read and Write Noise Margin *vs.* VDD
    - Read and Write Noise Margin *vs.* Temperature

Final Report

- Implement an array of 32x32 SRAM cells using 6T SRAM cells
- Design write circuitry and demonstrate data write ability of your design
- Design a row and column decoder to read 4-bit data while operating at clock frequency of >1GHz.
- Note: For read operation, initialize array contents randomly or to a fixed value.
- Consider bitline wire capacitance and word line wire capacitance to be 40fF (Does not scale with number of SRAM cells)
- Delay of the row and column decoder should be $<T_{CLK}/2$

Final Report

- SRAM timing considerations



Final Report

- Results Required:
  - Use the modular design and demonstrate reliable read functionality
  - Demonstrate reliable write functionality
  - Power Consumption *vs.* VDD & Temperature

Final Report

- You are free to adopt any multiplier architecture
- Report the chosen architecture
- Worst-case delay should be less than 1 ns
- Results Required:
  - Show the modular implementation of multiplier
  - Demonstrate proper functionality
  - Plot Delay vs. Supply voltage
  - Plot Delay vs. Temperature

Final Report

- You are free to choose any design style for D FFs
- Setup time < 15% of CLK period
- CLK-Q delay < 10% of CLK period
- Do not unnecessarily upsize the devices in the latch, it will increase power dissipation
  - Plot CLK-Q delay vs. Supply Voltage
  - Plot CLK-Q delay vs. Temperature
  - Plot Power consumption vs. Clock Frequency

Final Report

- Using the D FFs, implement parallel-in-parallel-out (PIPO) registers
- Implement 4-bit and 9-bit PIPO registers
- Report the modular design and demonstrate proper functionality for a CLK period <1ns
  - Plot Power Consumption vs. Supply Voltage
  - Plot Power Consumption vs. CLK period
  - Plot Max. operating frequency vs. Supply Voltage

Final Report Template

- Final report is the most critical part of this project
- Find the template of final report on BB
- Final report should combine the summary of the entire project
- Final report should be professionally written and should include properly drawn figure (no screenshots from Cadence, draw schematic figures manually)