ECE 467 Project #1

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Inverter Chain

$U^N = 128$; $t_p = 0.5(t_{HL} + t_{LH})$

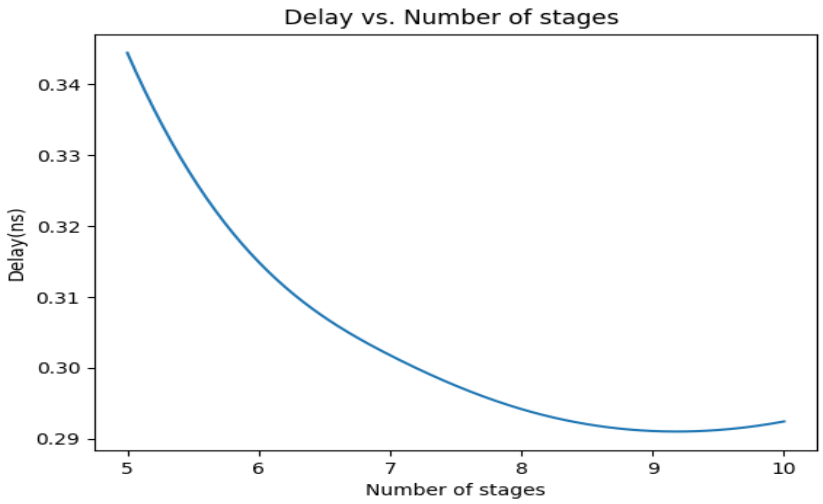
Delay characteristics for different N data table

N	U	t_p
5	2.63016	0.34445 ns
6	2.24492	0.31495 ns
7	2	0.3018 ns
8	1.83400	0.2942 ns
9	1.71449	0.2911 ns
10	1.62450	0.29245 ns

Optimal U= 1.71449

Optimal N= ln(128)/ln(1.71449)= 9

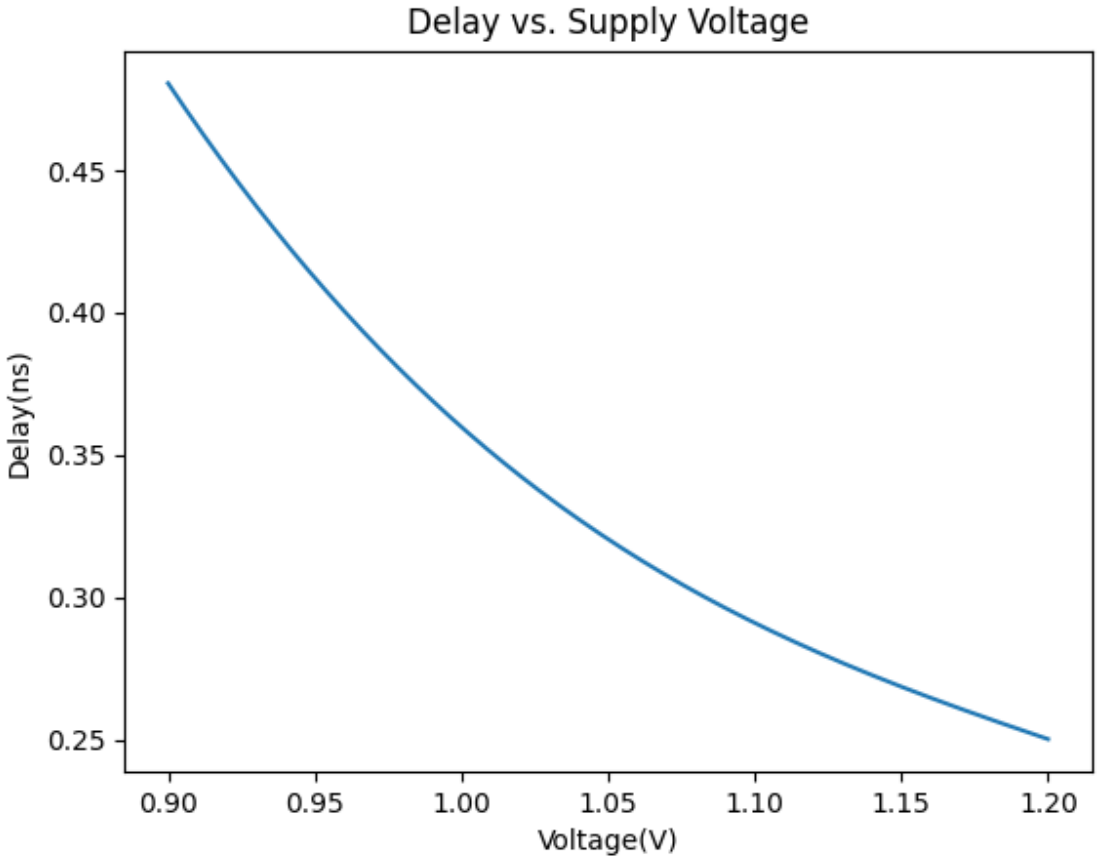
Delay vs. Number of stages (N)



Delay and Supply Voltage Data Table (for optimal N)

Voltage(V)	0.9	1.0	1.1	1.2
t_p(ns)	0.4806ns	0.3599ns	0.2911ns	0.2503ns

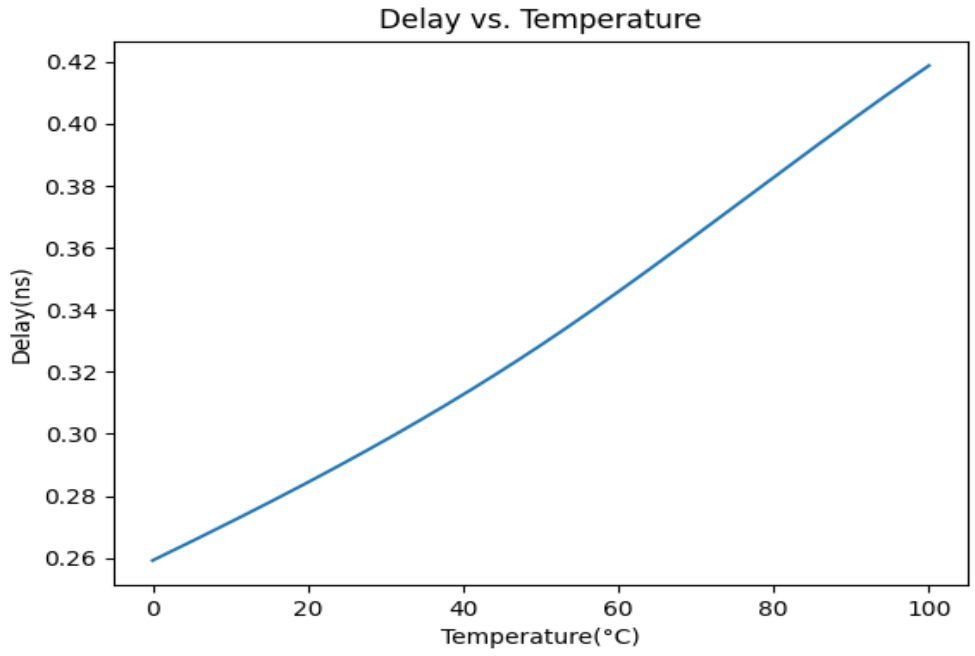
Delay vs. Supply Voltage Graph



Delay and Temperature Data Table (for optimal N)

Temperature(°C)	T_p(ns)
0°C	0.25920 ns
25°C	0.29110 ns
50°C	0.32860 ns
75°C	0.37340 ns
100°C	0.41875 ns

Delay vs. Temperature Graph

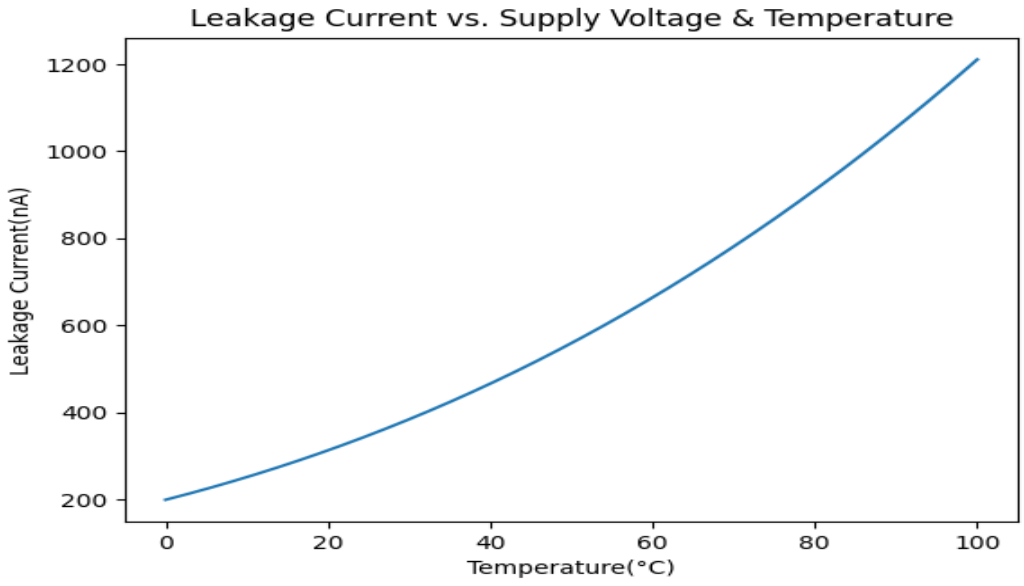


Leakage Current and Supply Voltage & Temperature Data Table (for optimal N)

Supply Voltage at constant 1.1V

Temperature(°C)	**Leakage current**
0°C	199.2405 nA
25°C	347.2131 nA
50°C	559.2233 nA
75°C	844.6916 nA
100°C	1211.098 nA

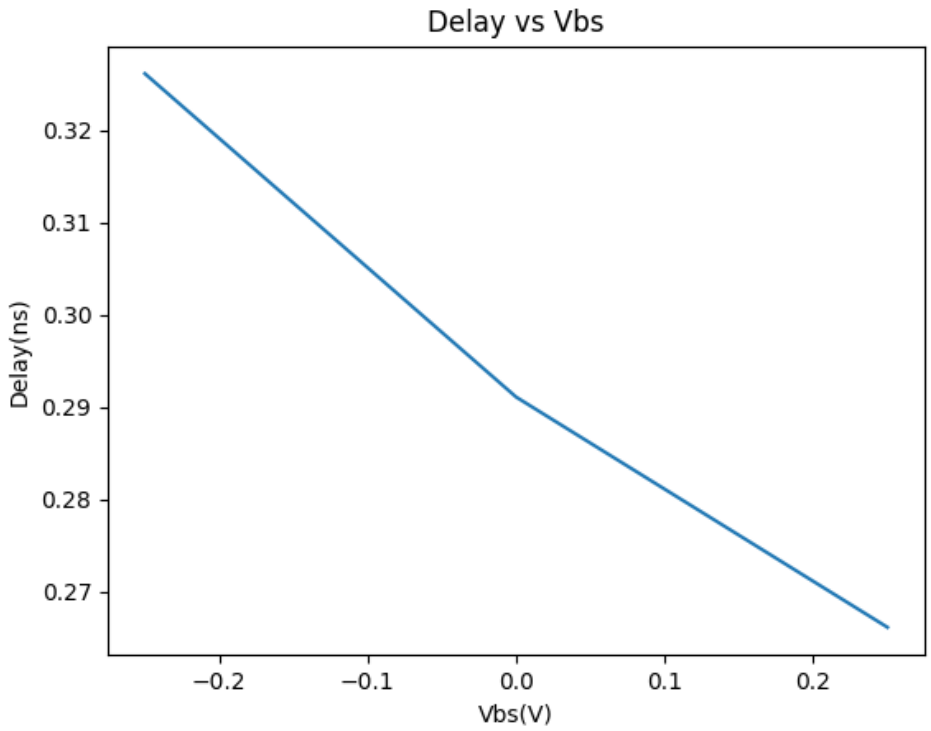
Leakage current vs. Supply Voltage & Temperature Graph



Delay and Vbs (all NMOS) Data Table

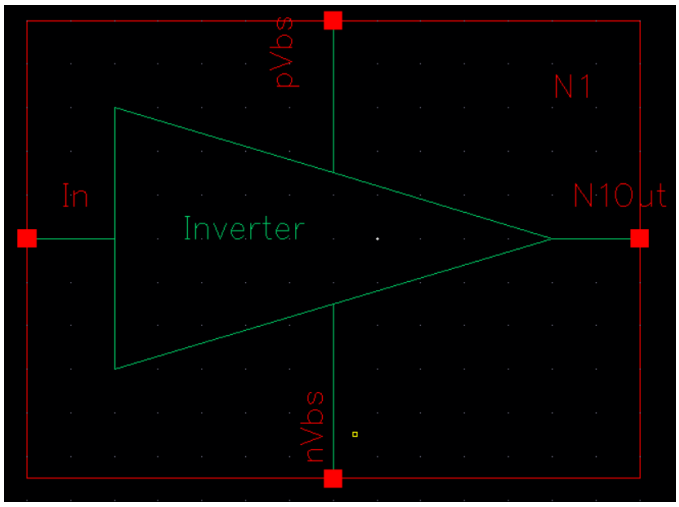
Vbs (V)	t_p(ns)
-0.25 V	0.32615 ns
0 V	0.29110 ns
0.25 V	0.26615 ns

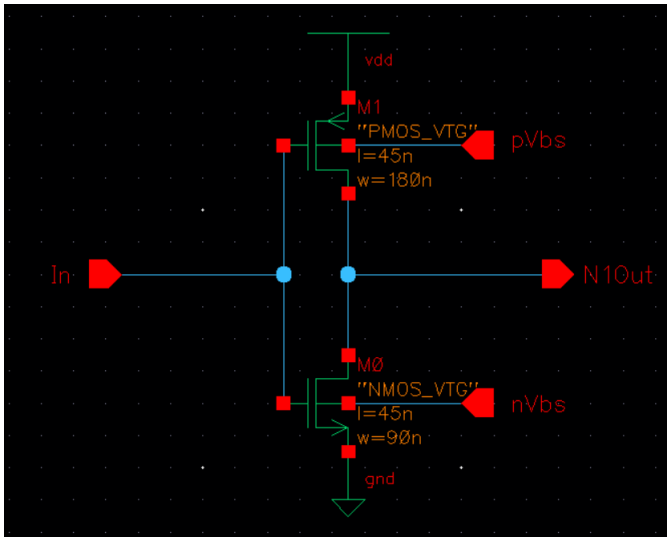
Delay vs Vbs Graph



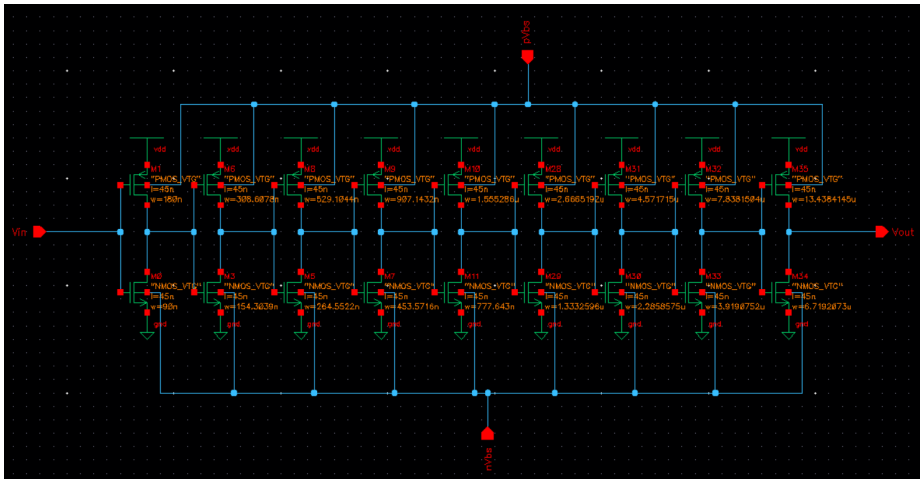
Schematics and Symbols

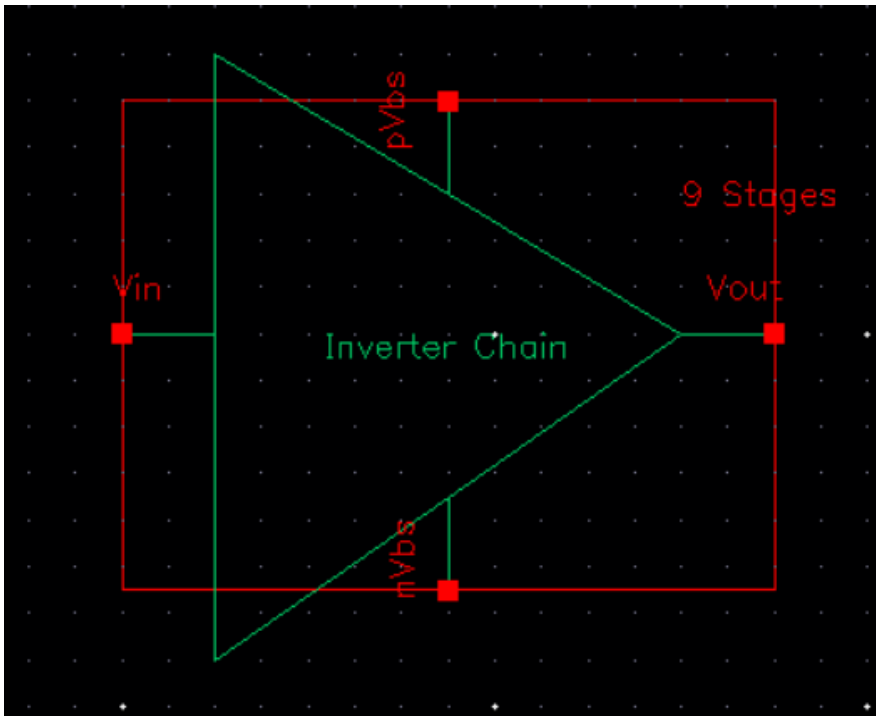
Inverter (minimum sized):

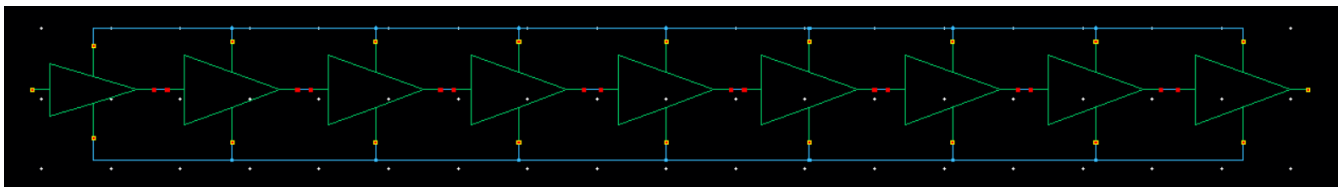




Inverter Chain (Optimal N=9):

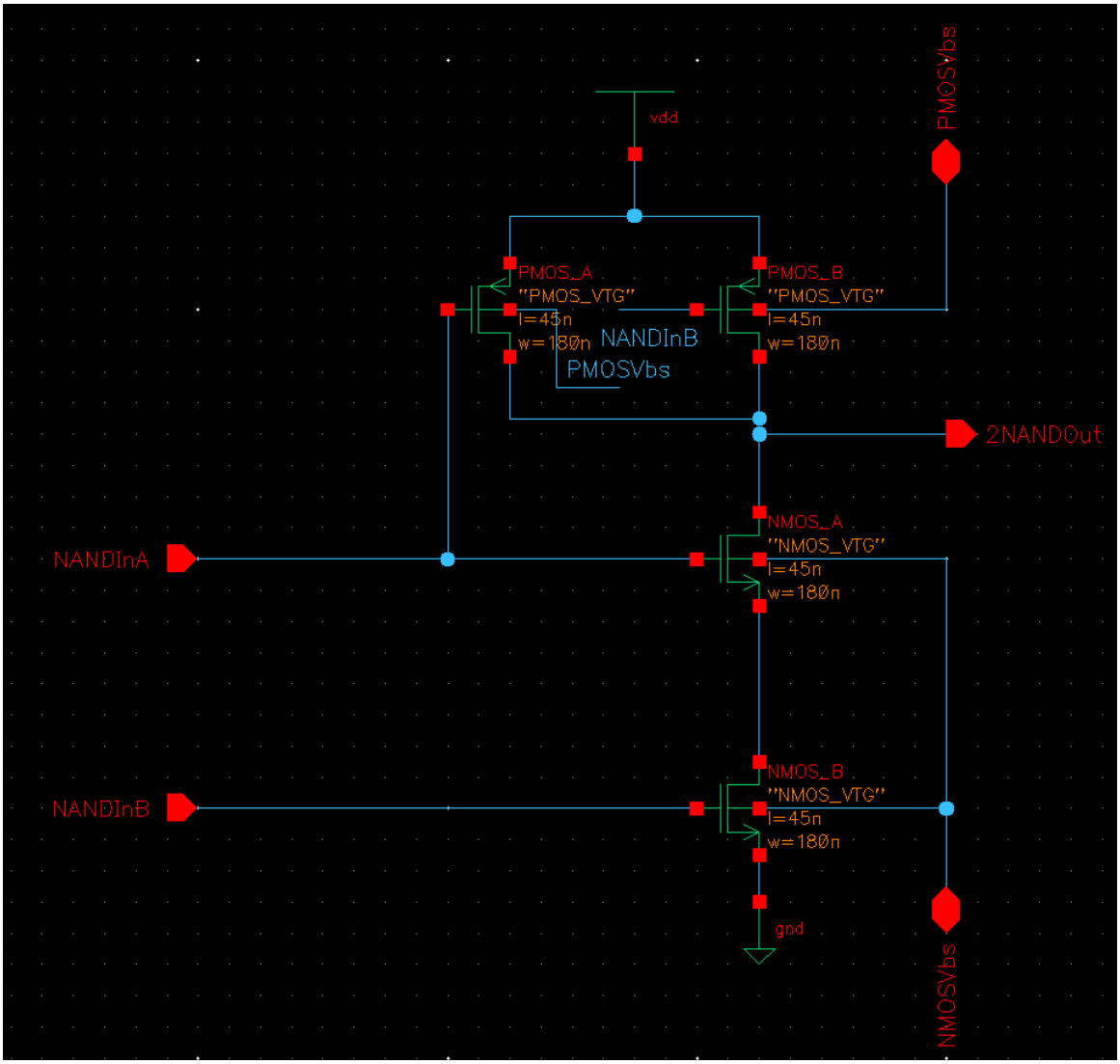






Two Input NAND

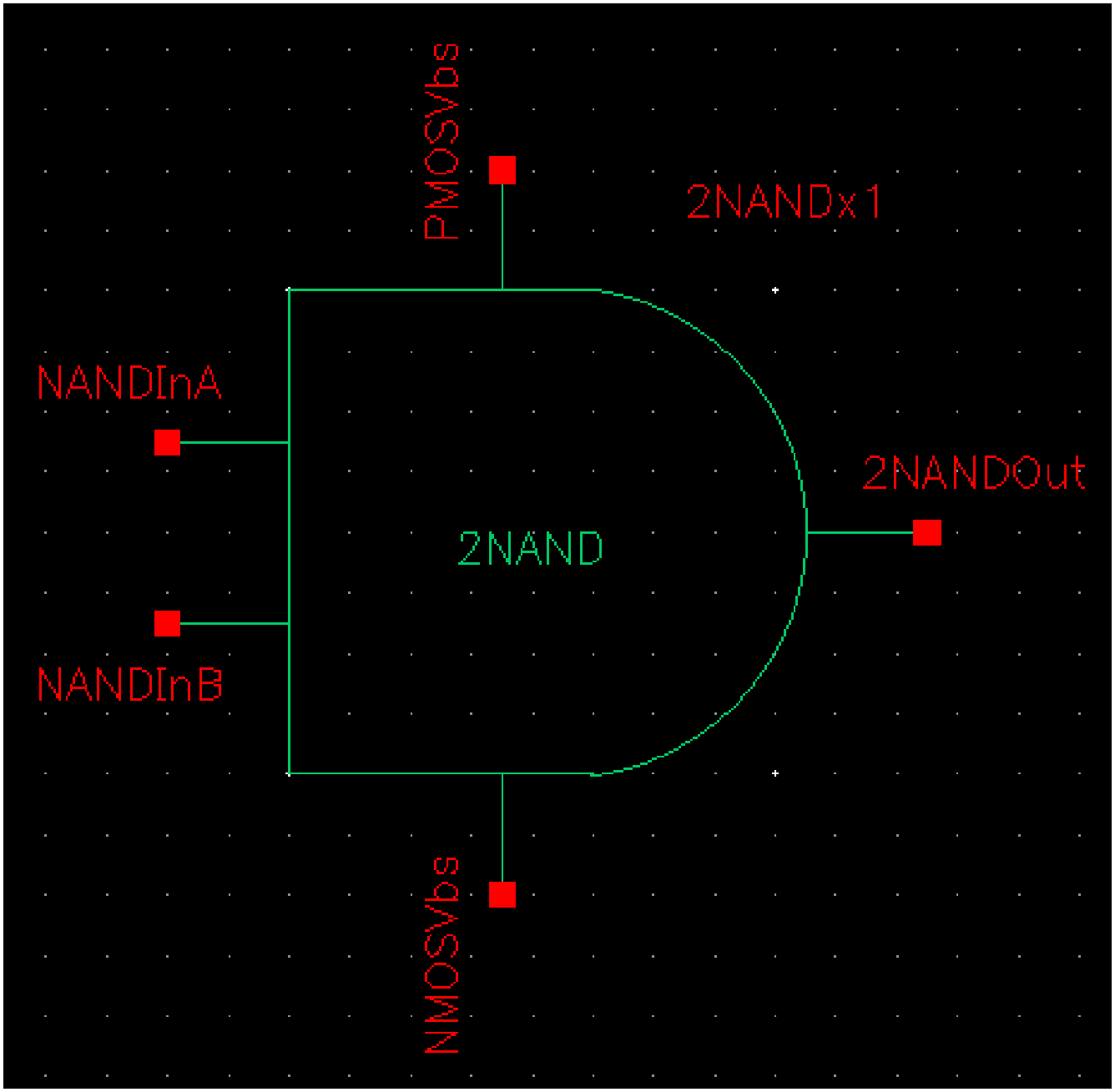
Schematic



Shown sizing is to match the delay of a minimum sized inverter. The transistor sizes for variants of the inverter are given in the below table.

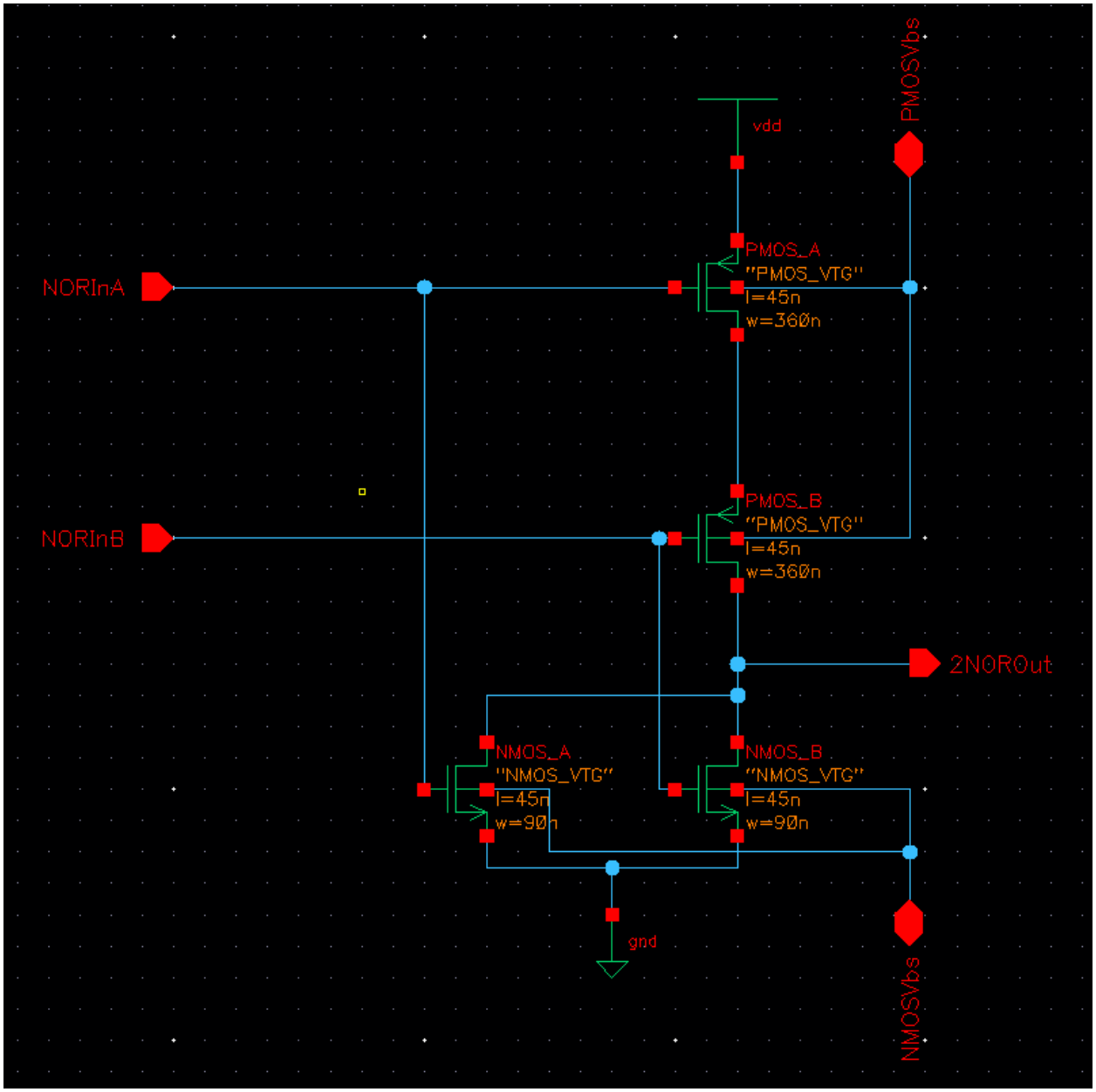
Inverter Upsize Factor	NMOS and PMOS lengths (nm)	PMOS Width (nm)	NMOS Width (nm)
2	90	360	360
3	135	540	540

Gate Symbol



Two Input NOR

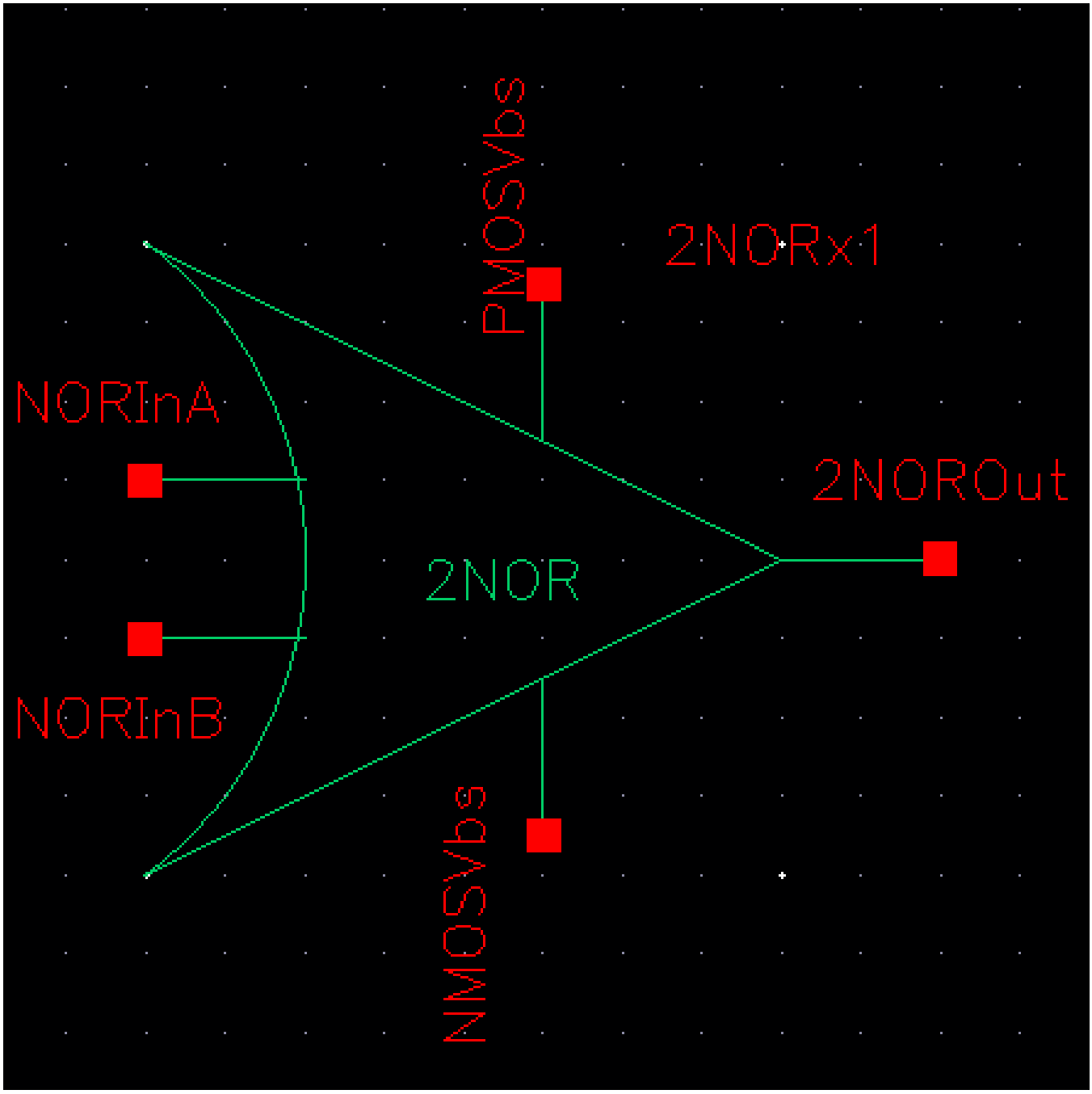
Schematic



Shown sizing is to match the delay of a minimum sized inverter. The transistor sizes for variants of the inverter are given in the below table.

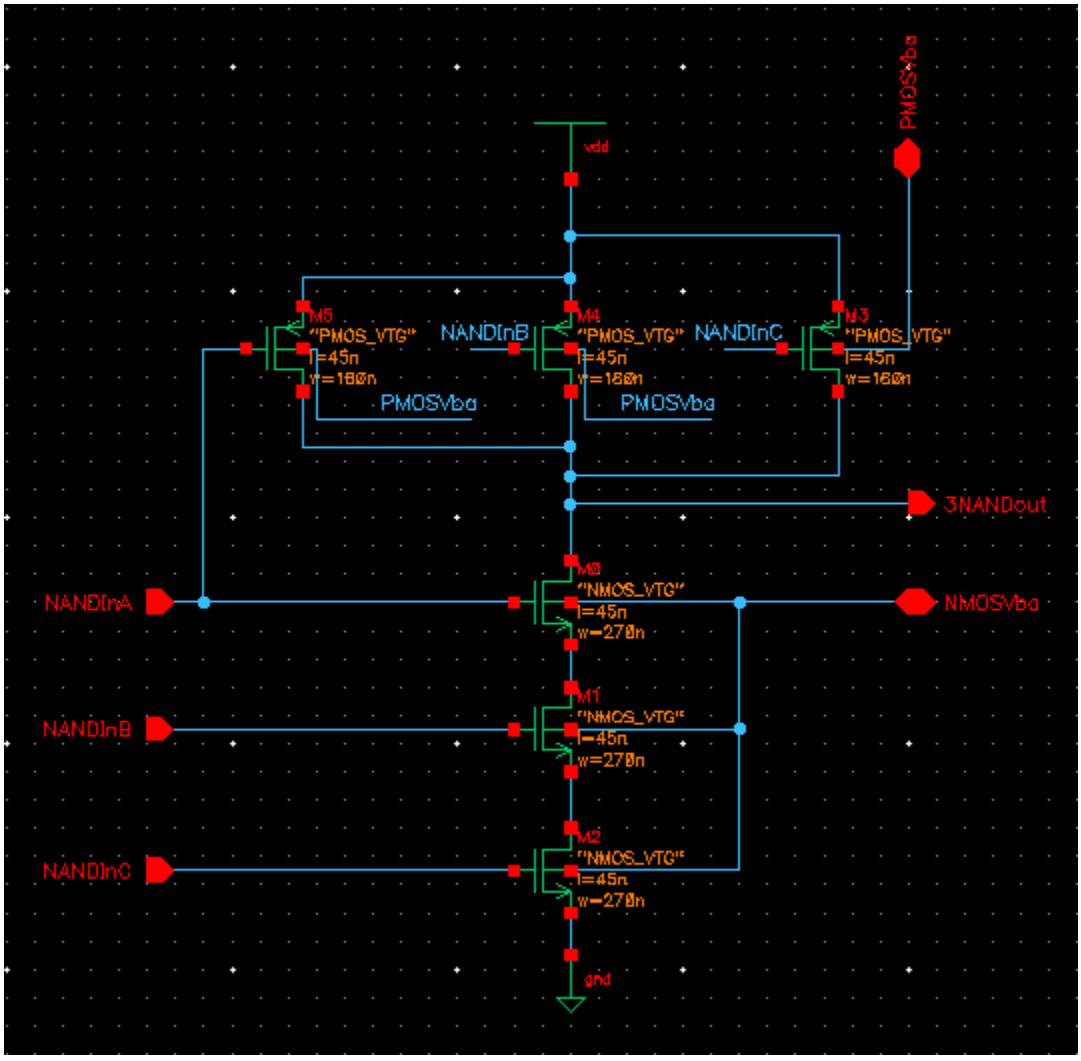
Inverter Upsize Factor	NMOS and PMOS lengths (nm)	PMOS Width (nm)	NMOS Width (nm)
2	90	720	180
3	135	1080	270

Gate Symbol



Three Input NAND

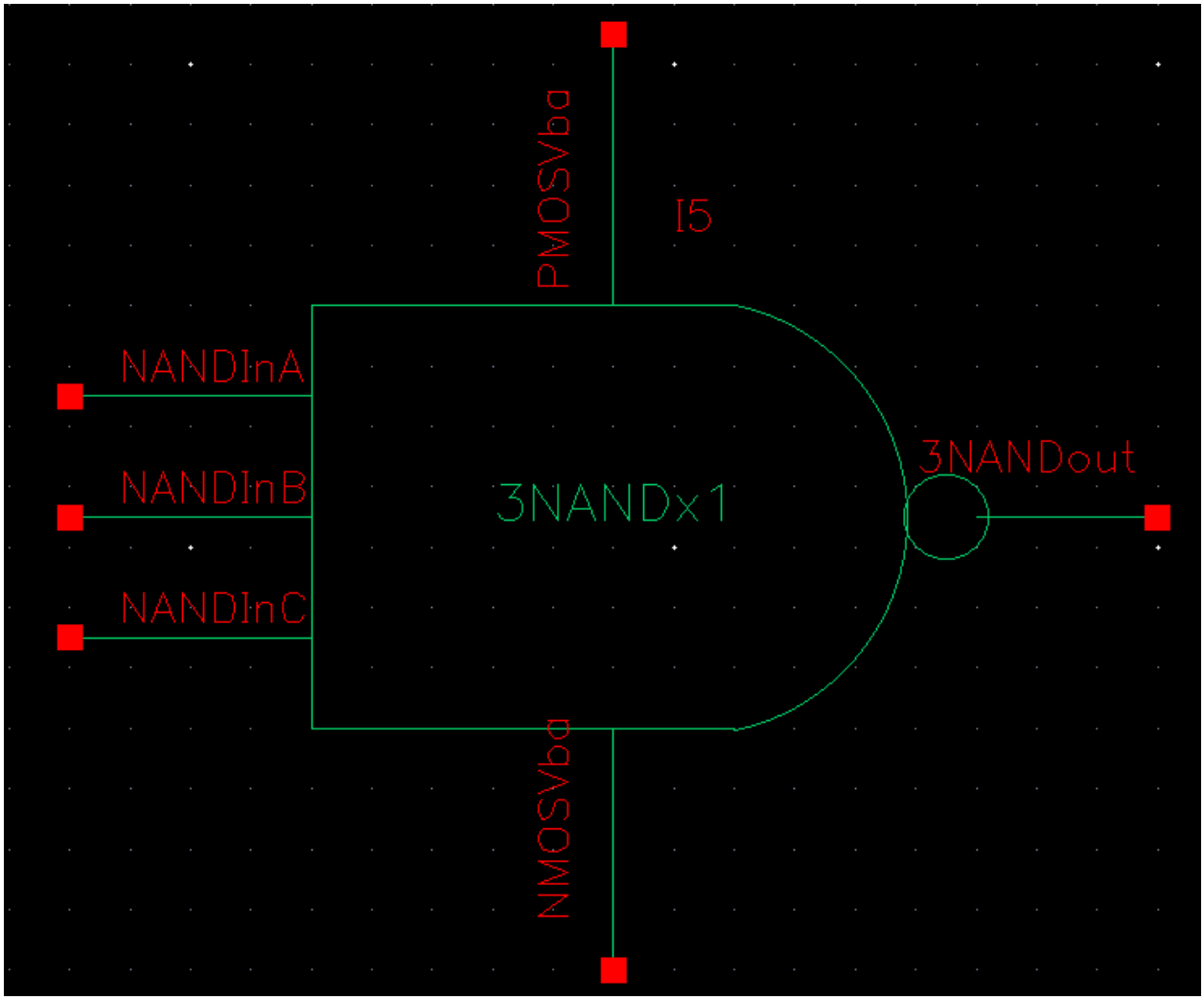
Schematic



Shown sizing is to match the delay of a minimum sized inverter. The transistor sizes for variants of the inverter are given in the below table.

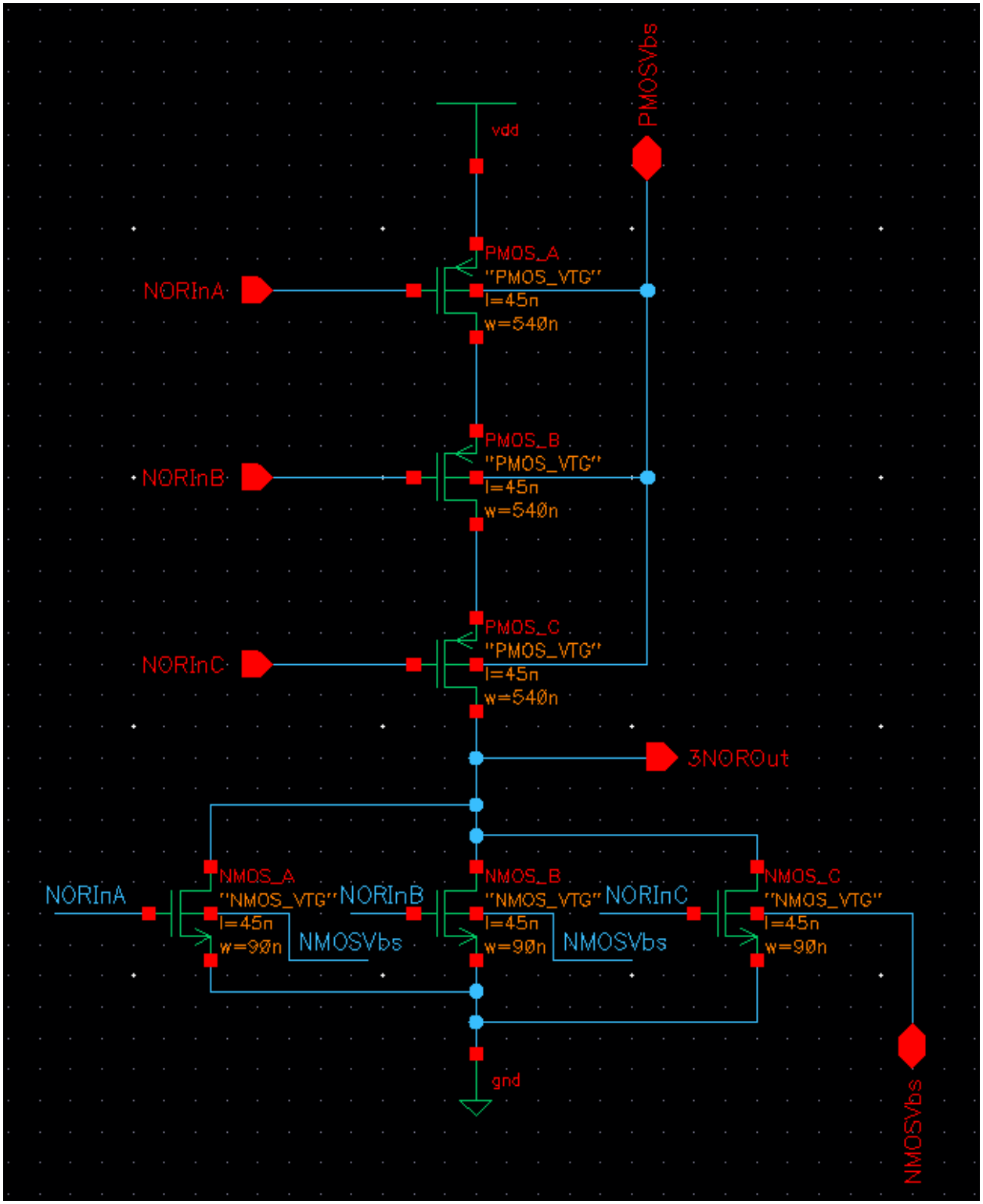
Inverter Upsize Factor	NMOS and PMOS lengths (nm)	PMOS Width (nm)	NMOS Width (nm)
2	90	270	540
3	135	540	810

Gate Symbol


PMOSVbp
I5
NANDInA
NANDInB
NANDInC
3NANDx1
3NANDout
NMOSVbn

Three Input Nor

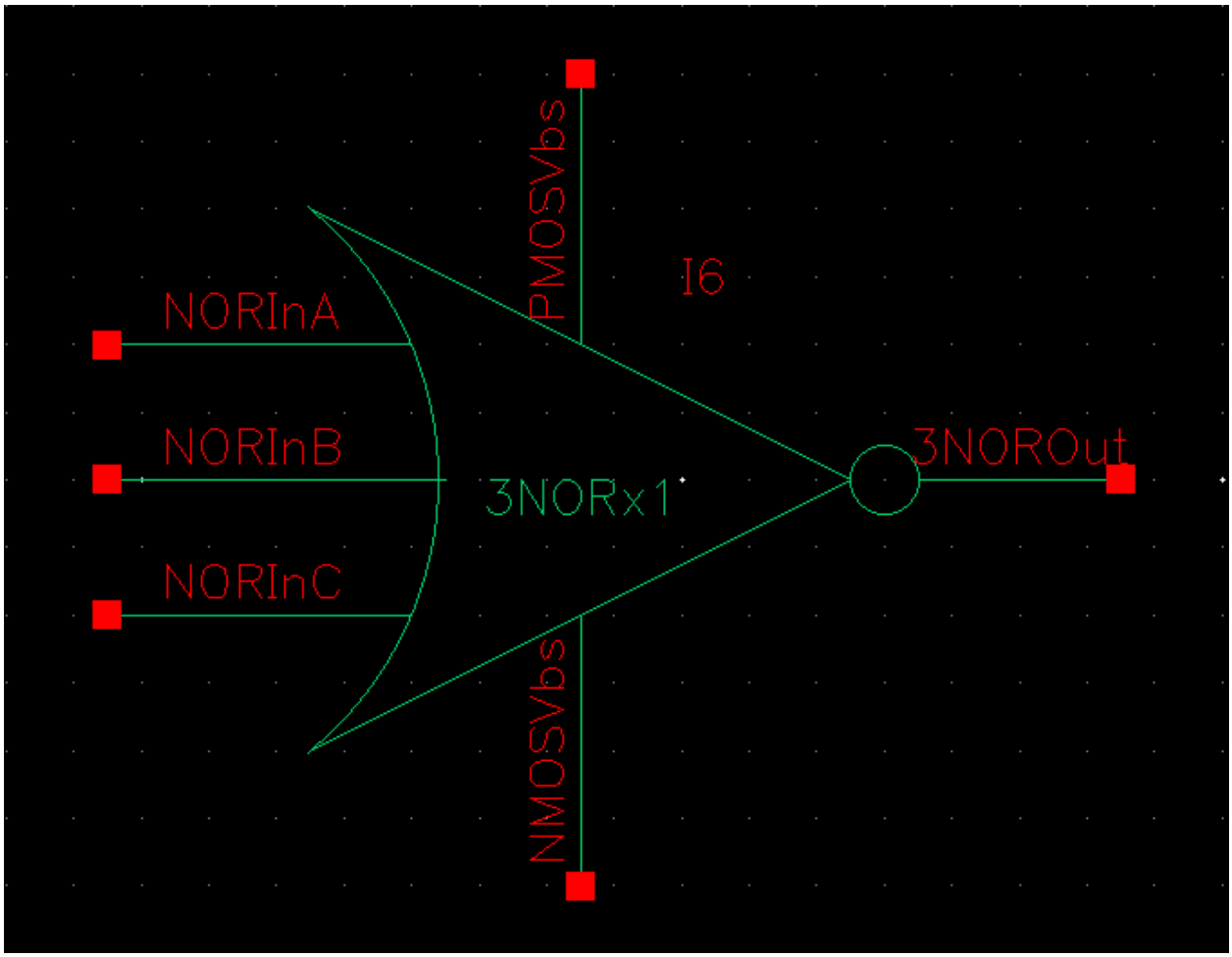
Schematic



Shown sizing is to match the delay of a minimum sized inverter. The transistor sizes for variants of the inverter are given in the below table.

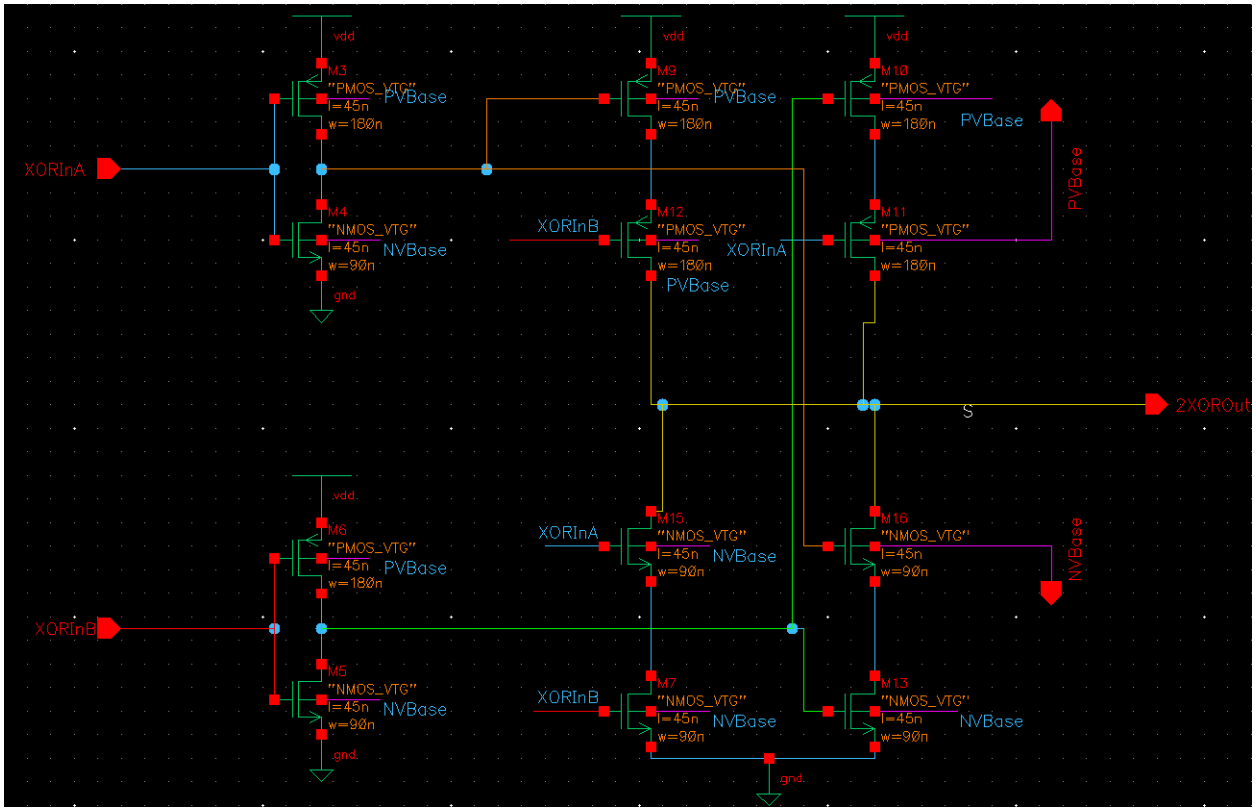
Inverter Upsize Factor	NMOS and PMOS lengths (nm)	PMOS Width (nm)	NMOS Width (nm)
2	90	1080	180
3	135	1620	270

Gate Symbol



Two Input XOR

Schematic

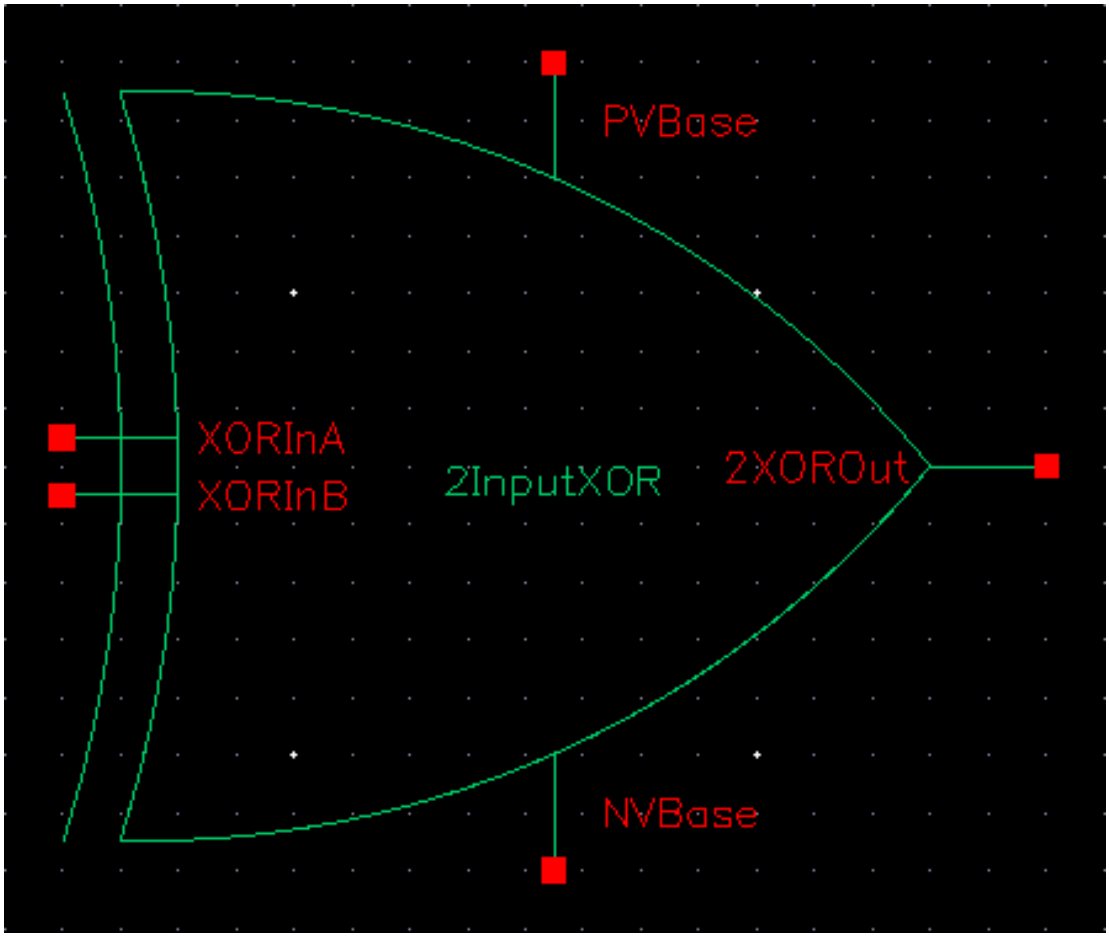


PMOS width = 180nm, NMOS width = 90nm, PMOS/NMOS Length = 45nm

Shown sizing is to match the delay of a minimum sized inverter. The transistor sizes for variants of the inverter are given in the below table.

Inverter Upsize Factor	NMOS and PMOS lengths (nm)	PMOS Width (nm)	NMOS Width (nm)
2	90	360	180
3	135	540	270

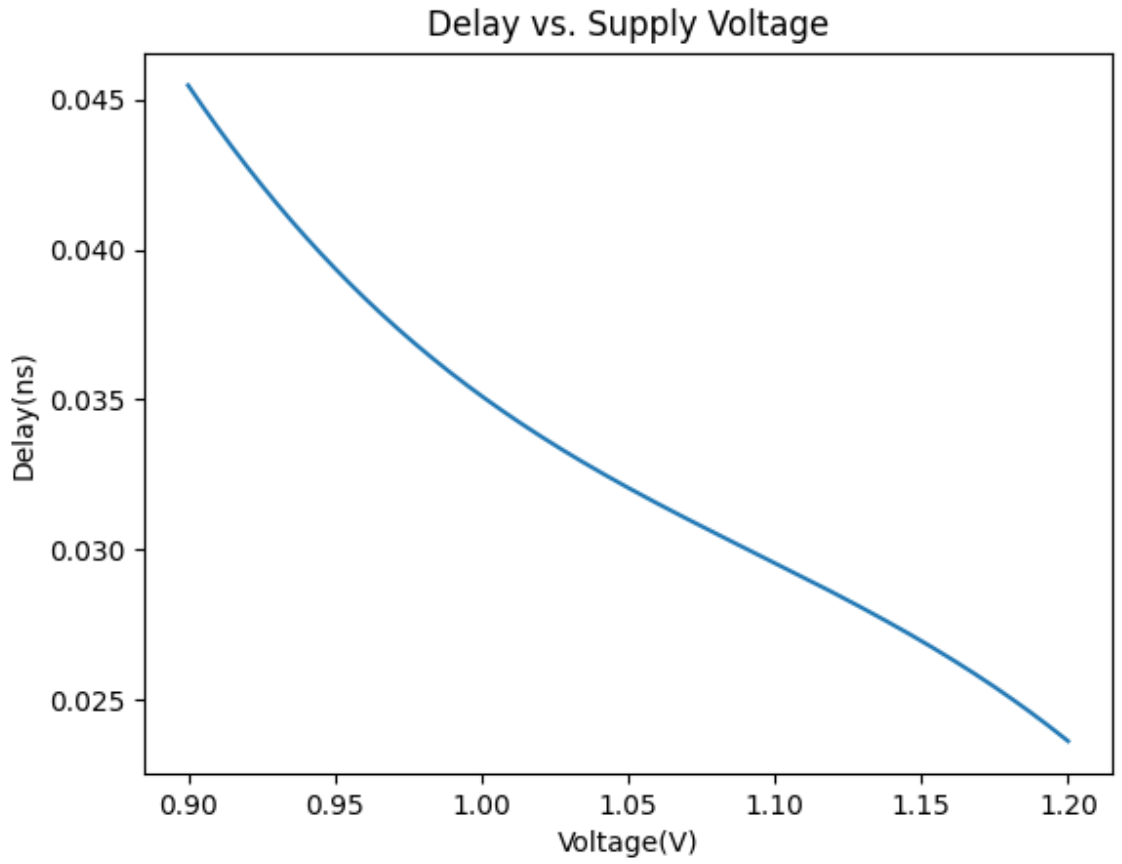
Gate Symbol



Gate Results(Testing with 2 Input NOR)

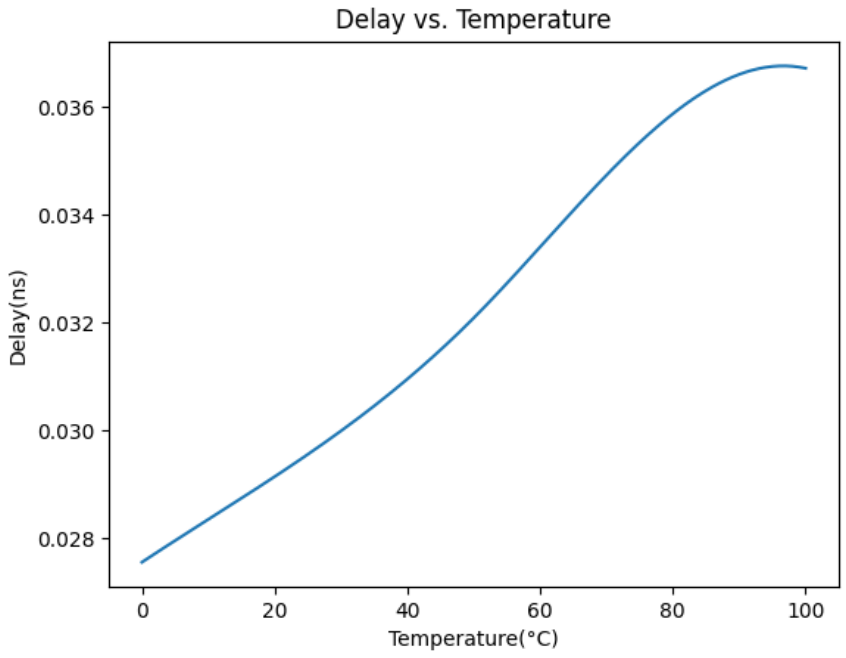
Delay vs. Supply Voltage(Tested at 25° C)

Voltage(V)	0.9	1.0	1.1	1.2
t_p(ns)	0.045475	0.035125	0.02956	0.023625



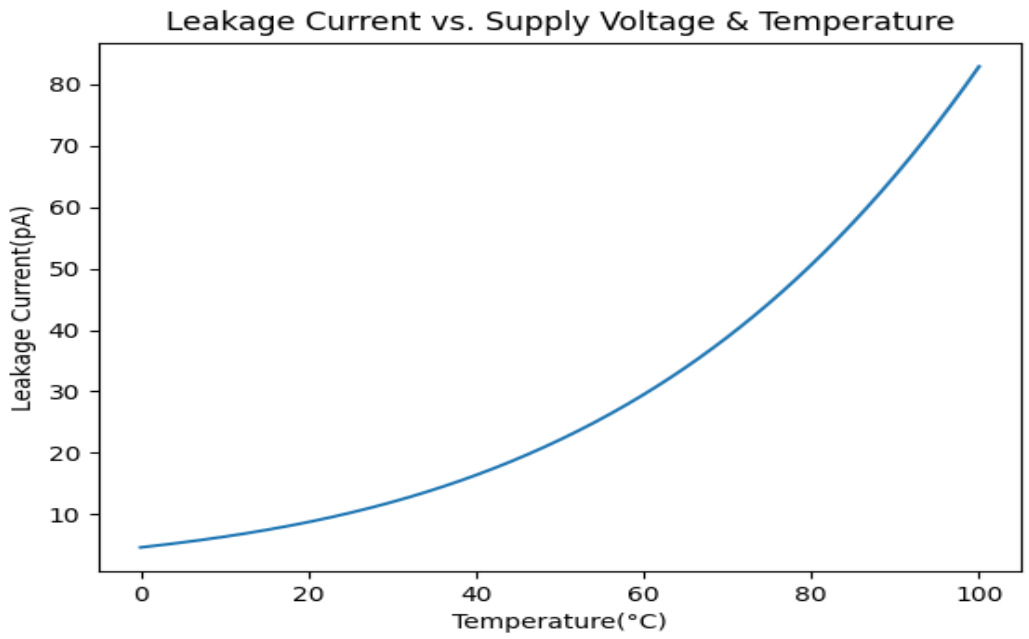
Delay vs. Temperature(Tested with VDD=1.1V)

Temperature(°C)	T_p
0°C	0.02756ns
25°C	0.02956ns
50°C	0.03209ns
75°C	0.035345ns
100°C	0.03672ns



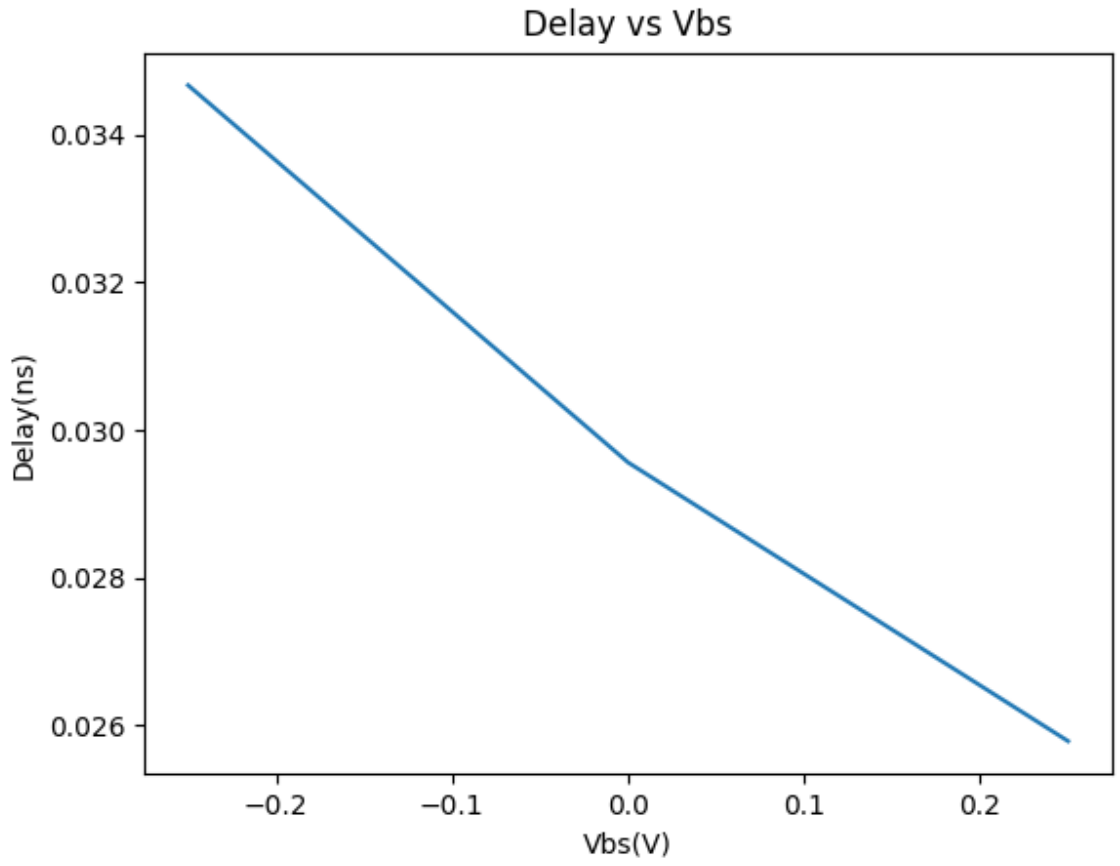
Leakage current vs. Supply Voltage & Temperature (Tested with VDD=1.1V)

Temperature(°C)	Leakage current
0°C	4.66317pA
25°C	10.2843pA
50°C	22.1507pA
75°C	44.4096pA
100°C	82.8285pA



Delay vs. NMOS Body Bias(Tested with VDD=1.1V at 25° C)

Vbs (V)	t_p(ns)
-0.25 V	0.03467ns
0 V	0.02956ns
0.25 V	0.025785ns



Appendix A

Work Distribution

Olivier Innocent	**Inverter Chain:** · **Schematic and Symbols** · **Inverter Chain Analysis Data**
Joseph Riem	**2-Input NAND and NOR Gates:** · **Schematic and Symbols** **Gate Analysis Data**
Ryn Stewart	**3-Input NAND and NOR Gates:** · **Schematic and Symbols** **Graphing Script**
Robert Ciesielski	**XOR Gate:** · **Schematic and Symbol**