ECE 467 Project #2

Olivier Innocent
Robert Ciesielski
Ryn Stewart
Joseph Riem

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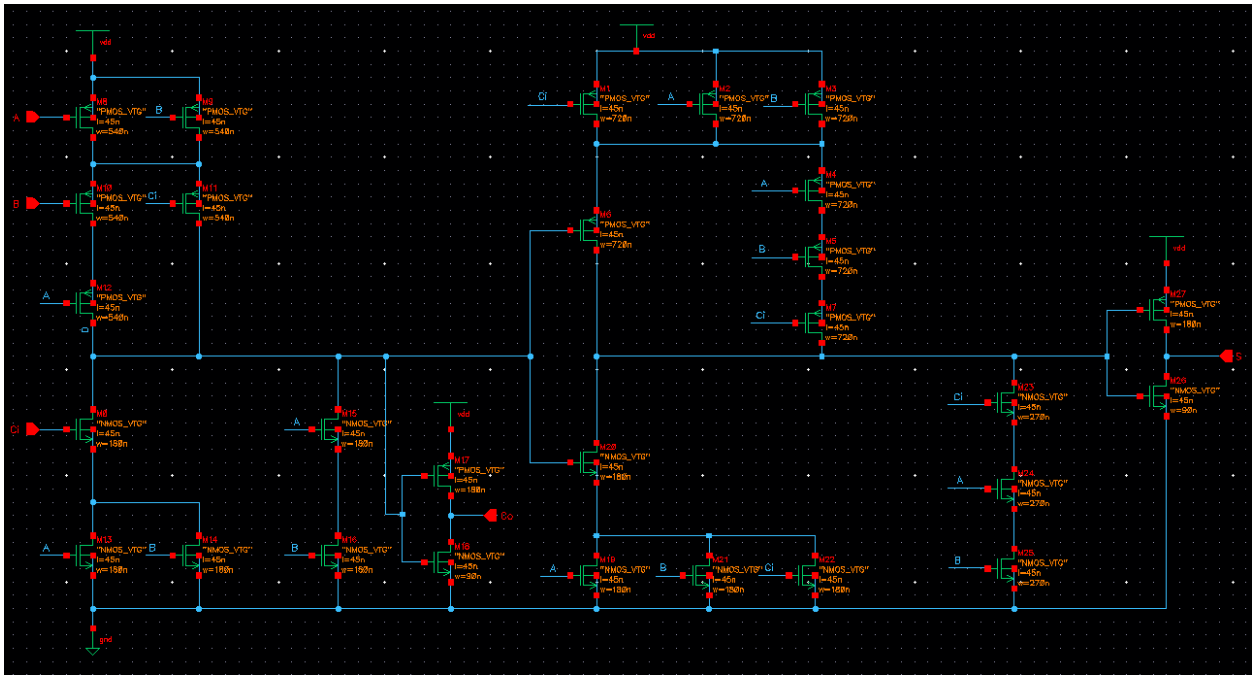
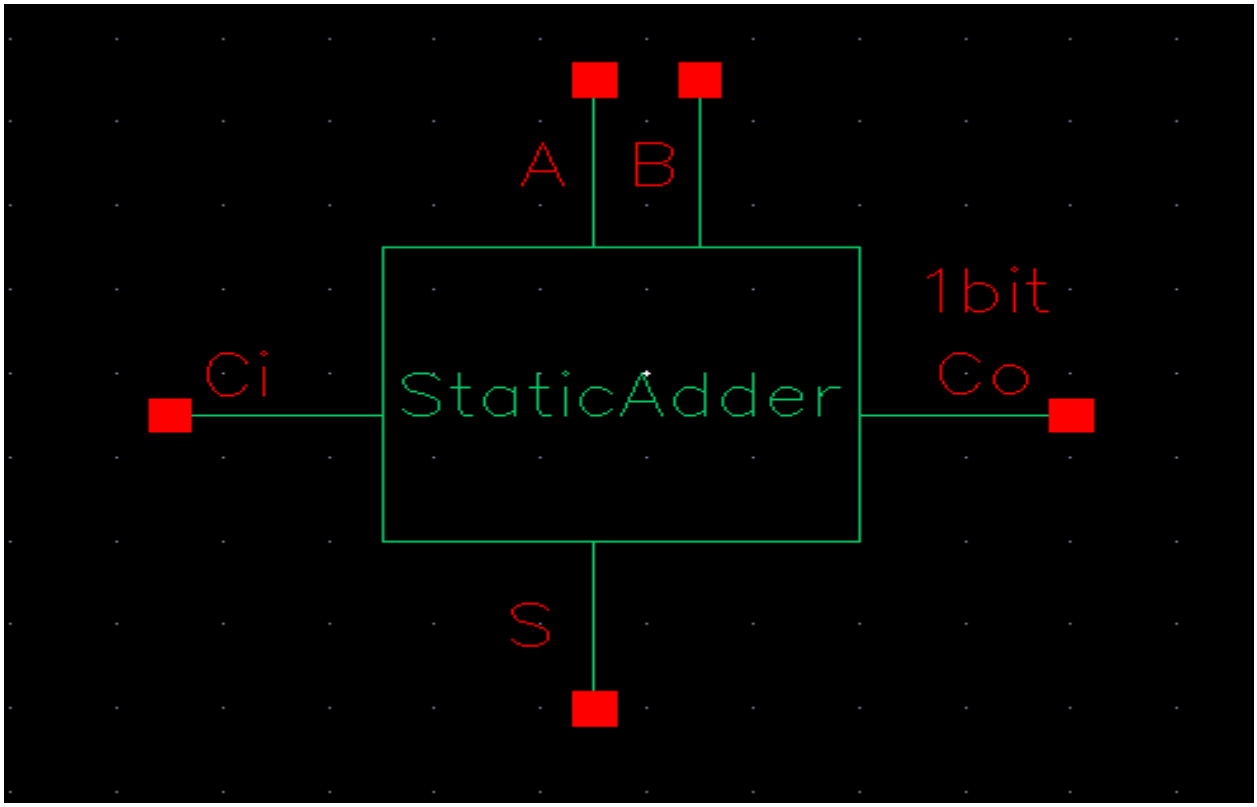
Static CMOS Full Adder

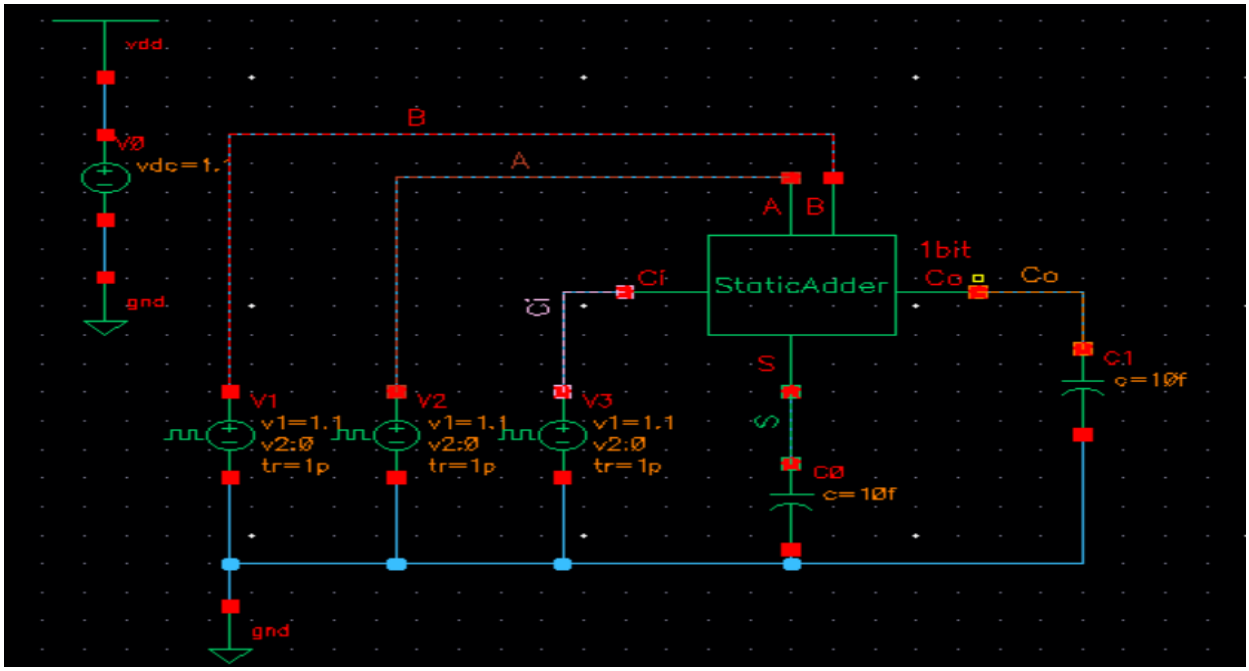
1. Implementation



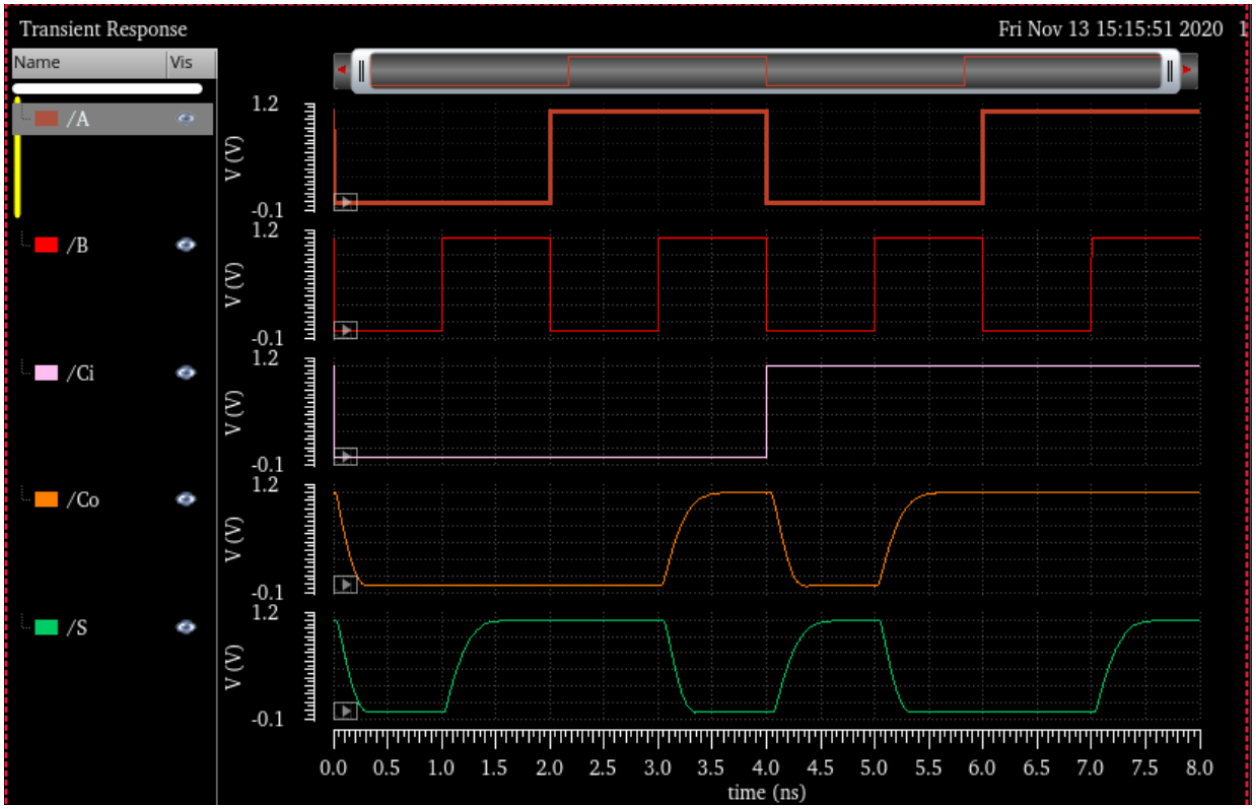


2. Functionality Verification

Test setup:



Simulation Results:

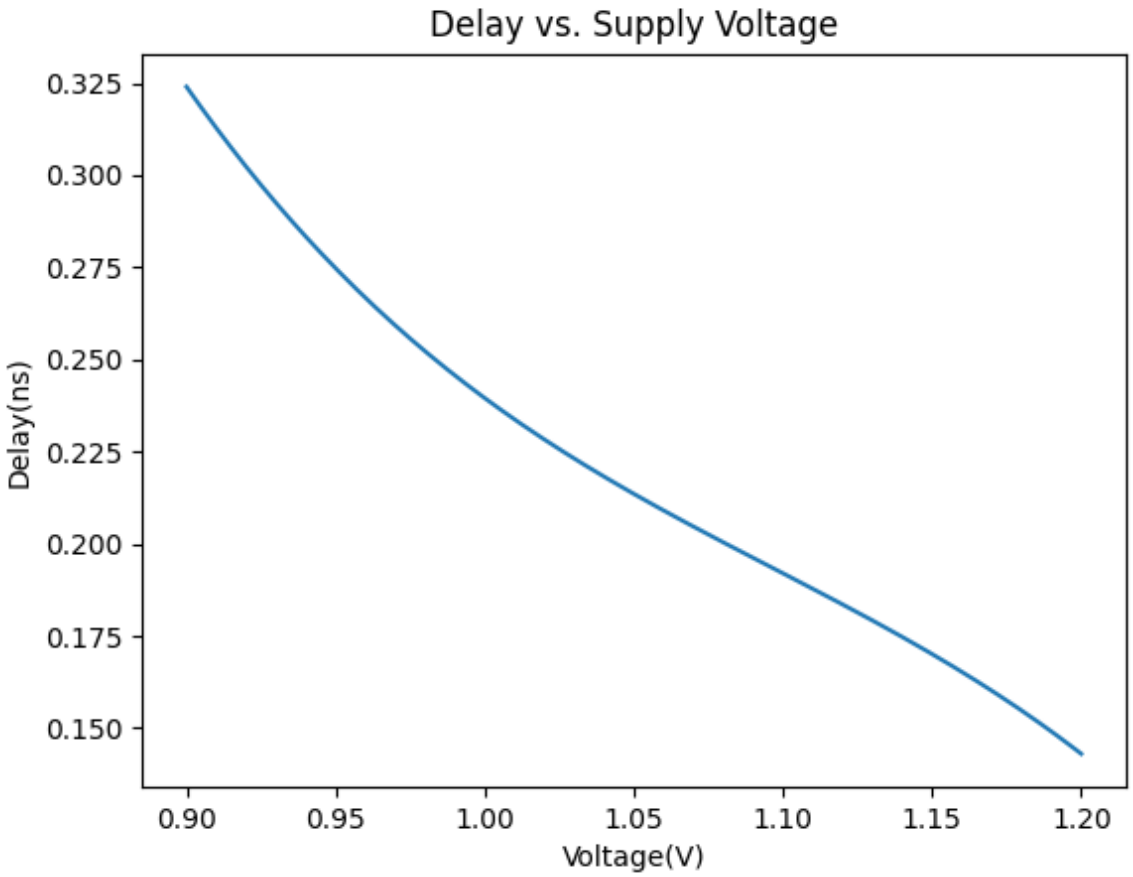


3. Required Tests

Worst case delay is found at S when A, B switch from high to low and Ci switches low to high.

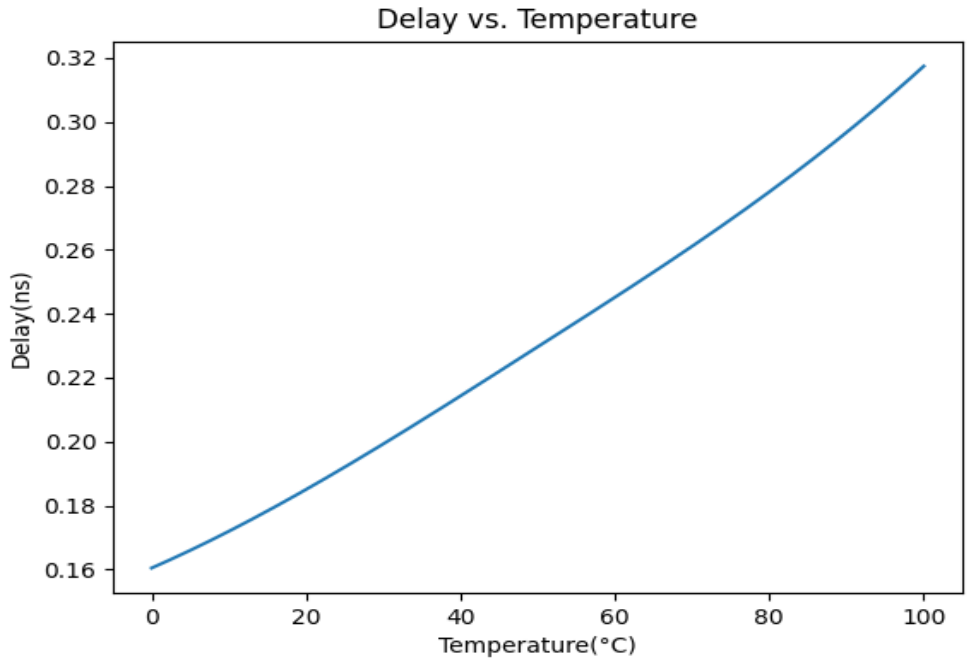
a. Delay vs. Supply Voltage (with 10f F capacitors)

Voltage(V)	**0.9**	**1.0**	**1.1**	**1.2**
t_p(ns)	0.324	0.23953	0.192	0.14304



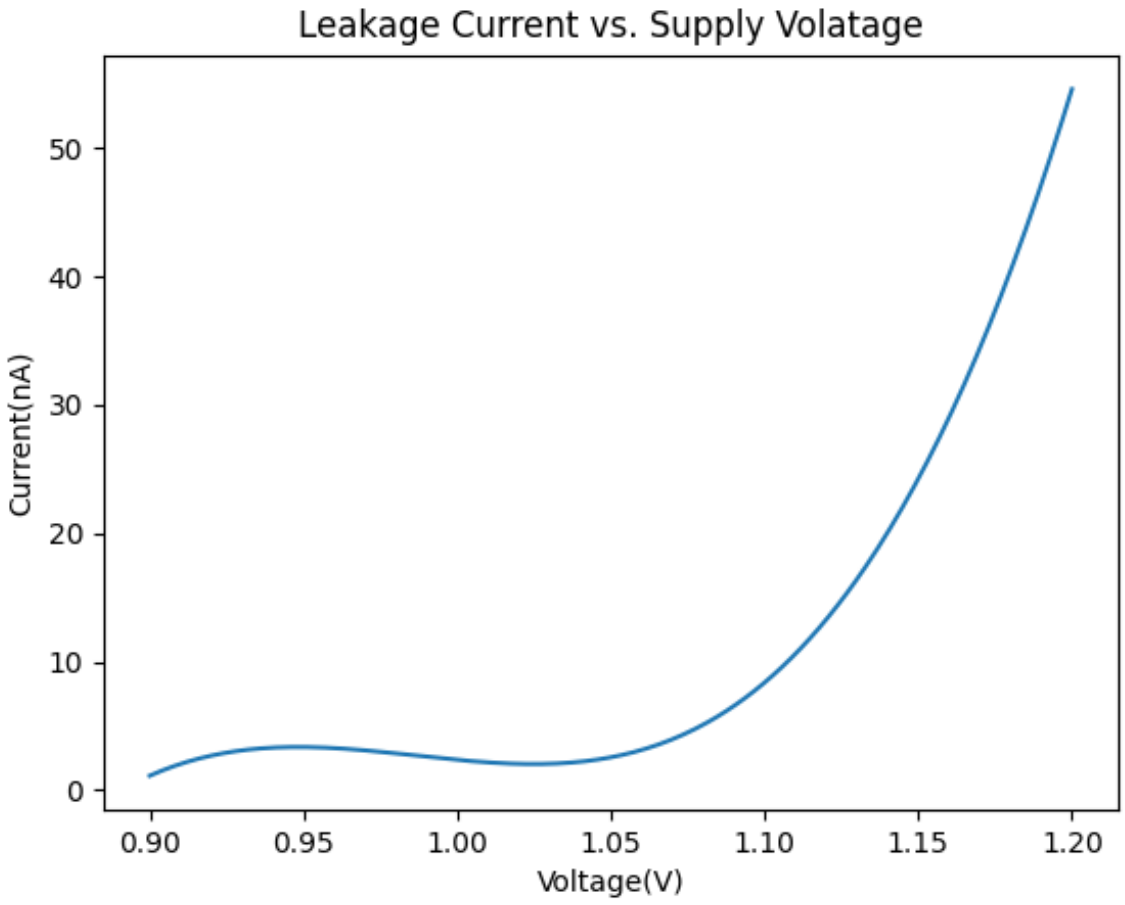
b. Delay vs. Temperature

Temperature(°C)	**t_p(ns)**
0°C	0.16043
25°C	0.192
50°C	0.22963
75°C	0.26945
100°C	0.31746



c. Leakage Current vs. Supply Voltage Change

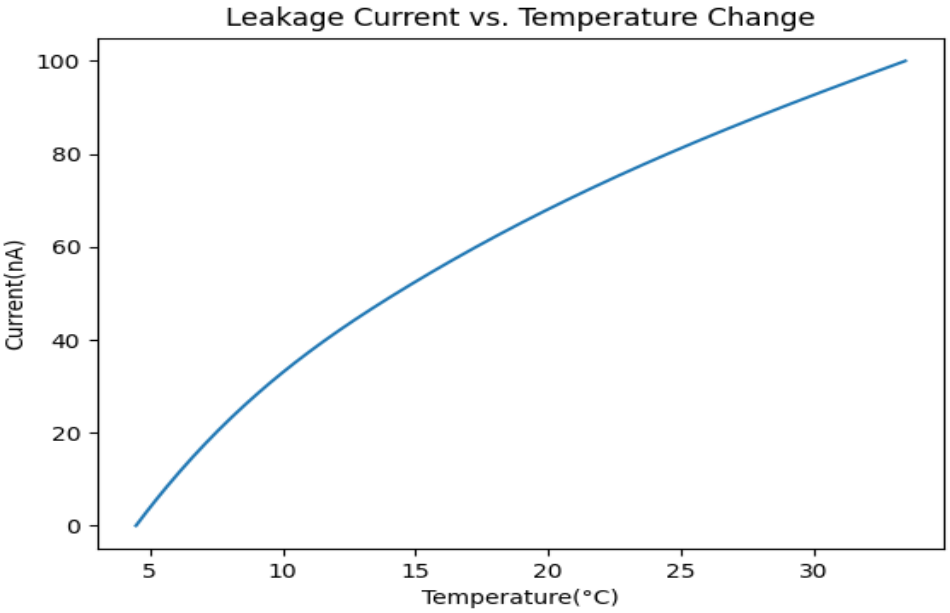
Voltage (V)	**0.9**	**1.0**	**1.1**	**1.2**
Leakage Current (nA)	1.12926	2.36784	8.38502	54.6038



d. Leakage Current vs. Temperature Change

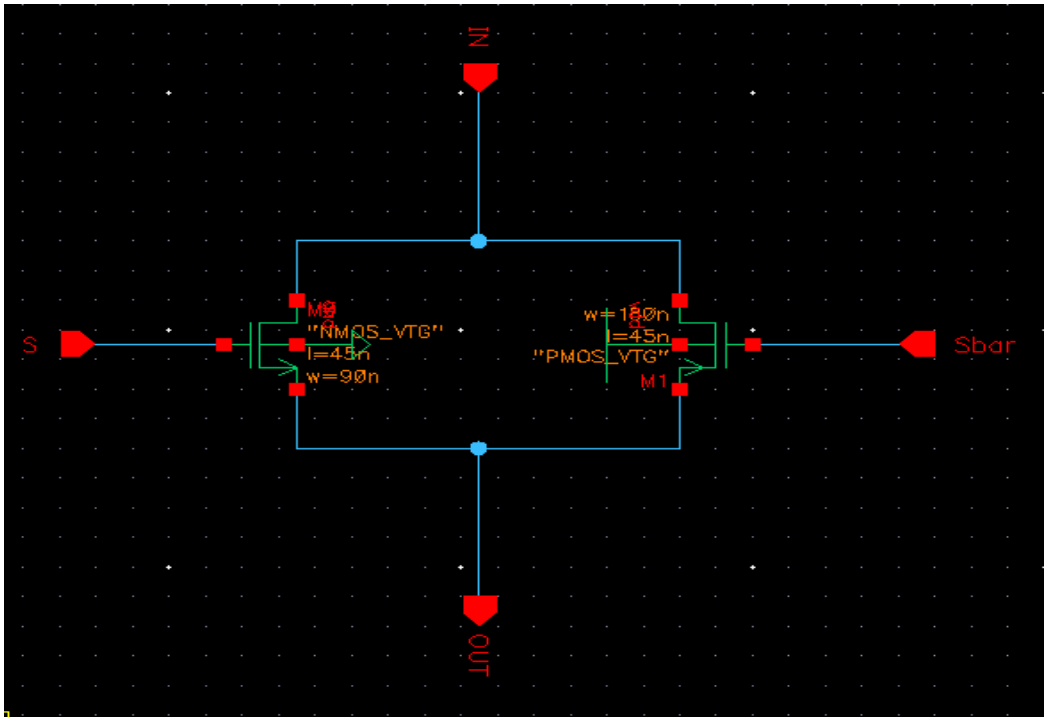
Supply voltage set to 1.1V

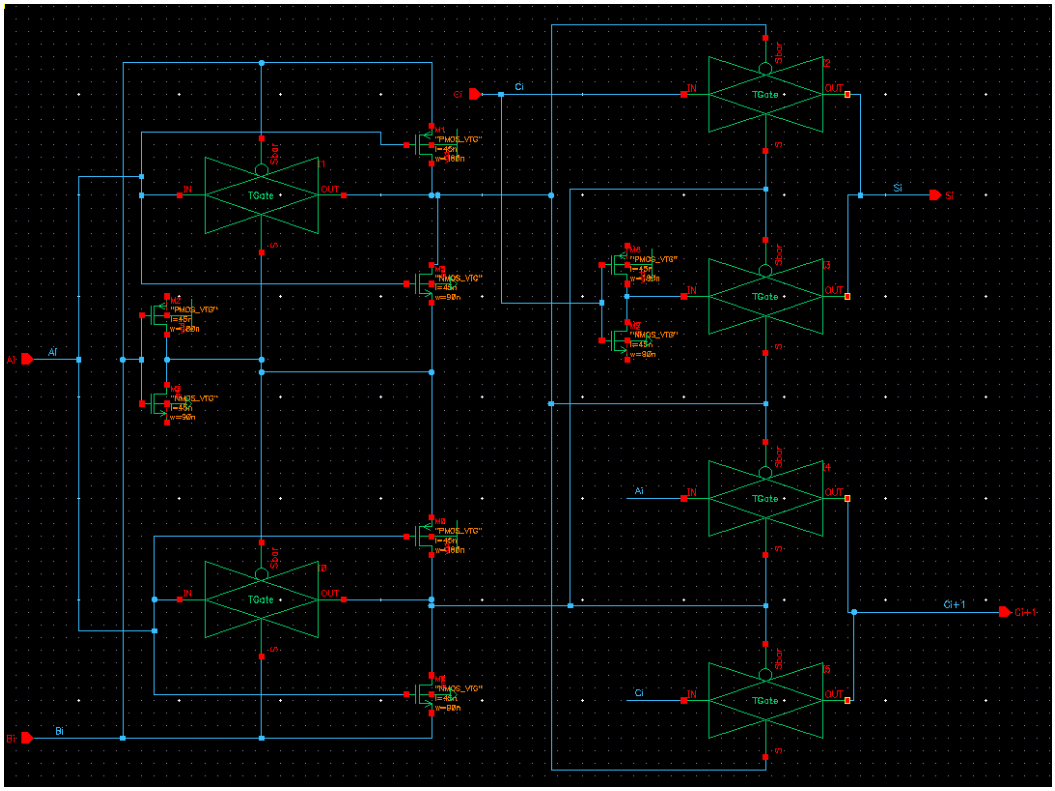
Temperature(°C)	Leakage current (nA)
0°C	4.46859
25°C	8.38502
50°C	14.2795
75°C	22.533
100°C	33.458


Leakage Current vs. Temperature Change
Current(nA)
Temperature(°C)
0
20
40
60
80
100
5
10
15
20
25
30

Transmission Gate Full Adder

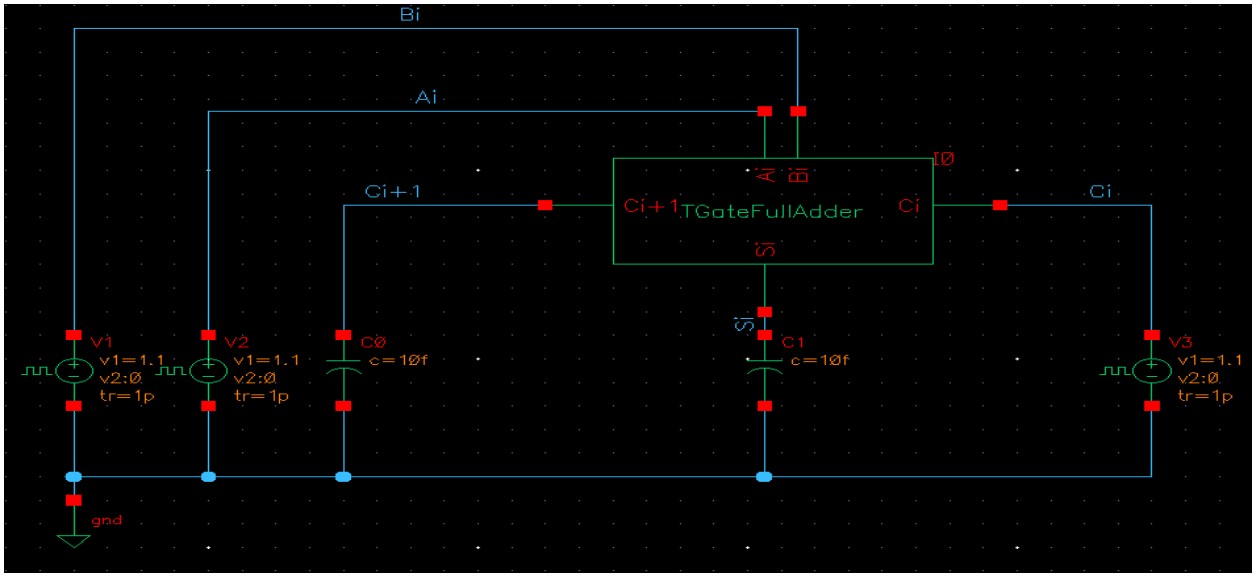
1. Implementation



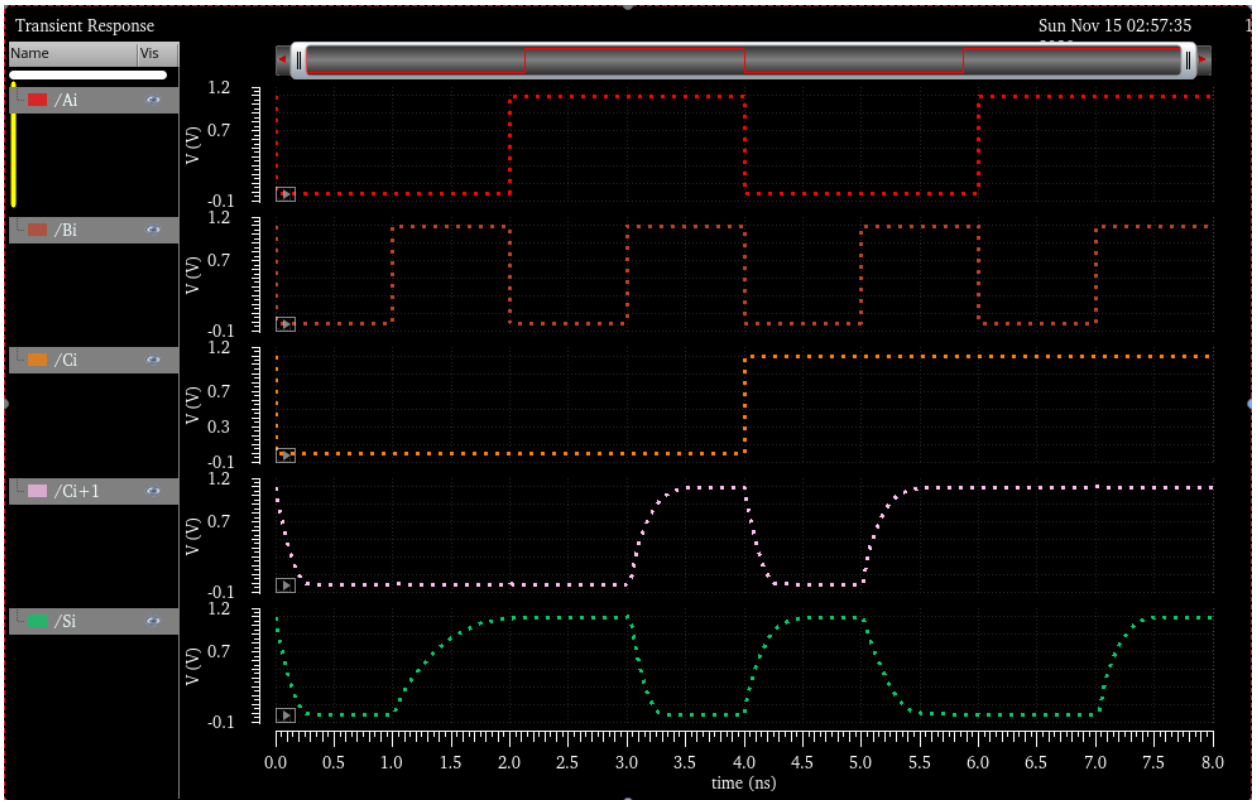


2. Functionality Verification

Test setup:

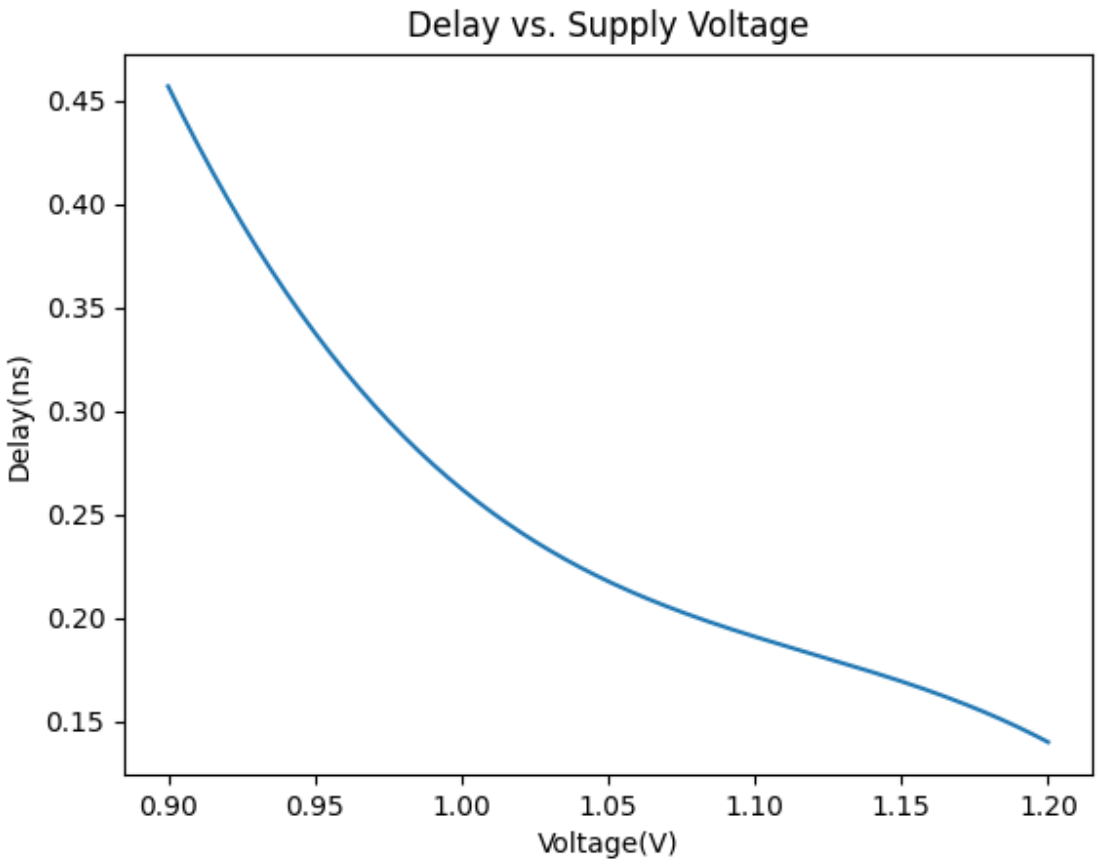


Simulation Results:



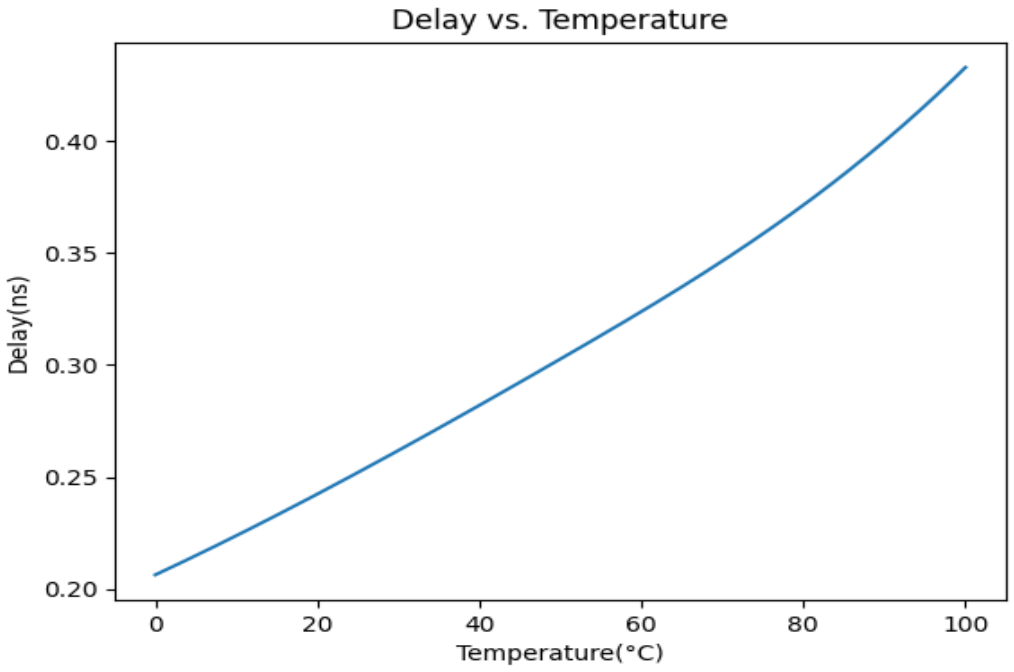
3. Required Tests
    a. Delay vs. Supply Voltage

Voltage(V)	**0.9**	**1.0**	**1.1**	**1.2**
t_p(ns)	0.45705	0.26228	0.19077	0.13973



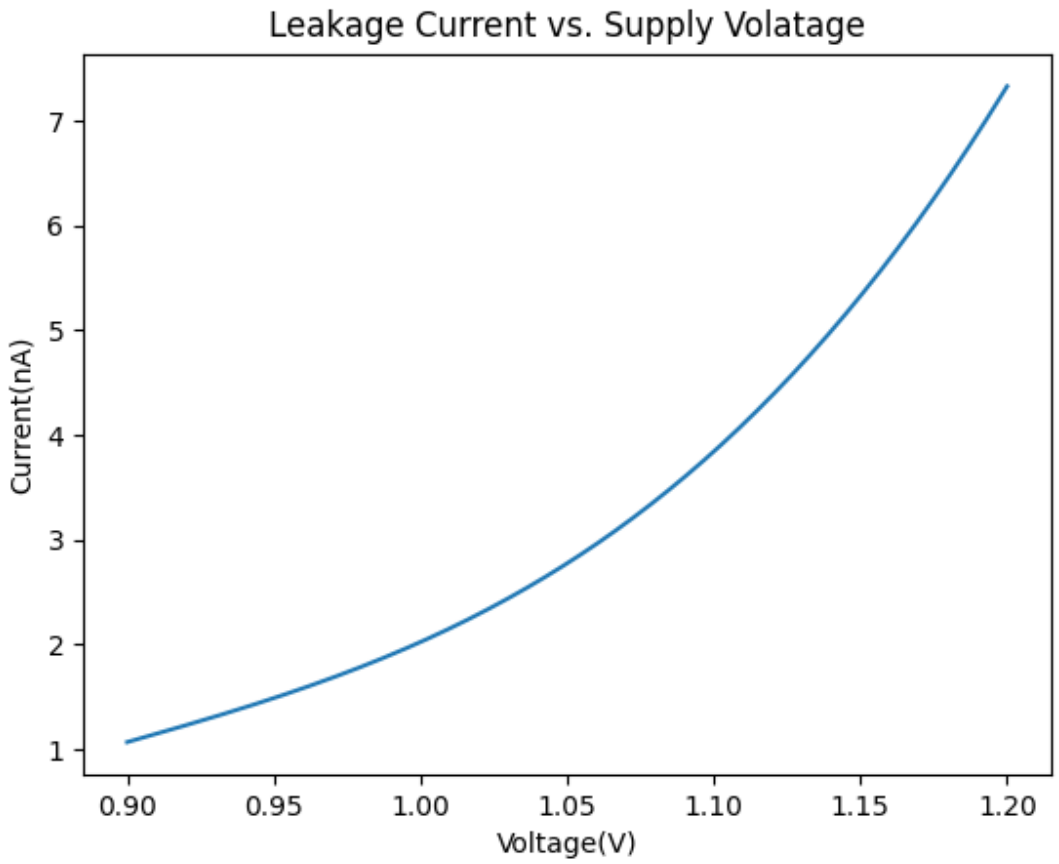
b. Delay vs. Temperature

Temperature(°C)	**t_p(ns)**
0°C	0.20623
25°C	0.25194
50°C	0.30262
75°C	0.35853
100°C	0.43288



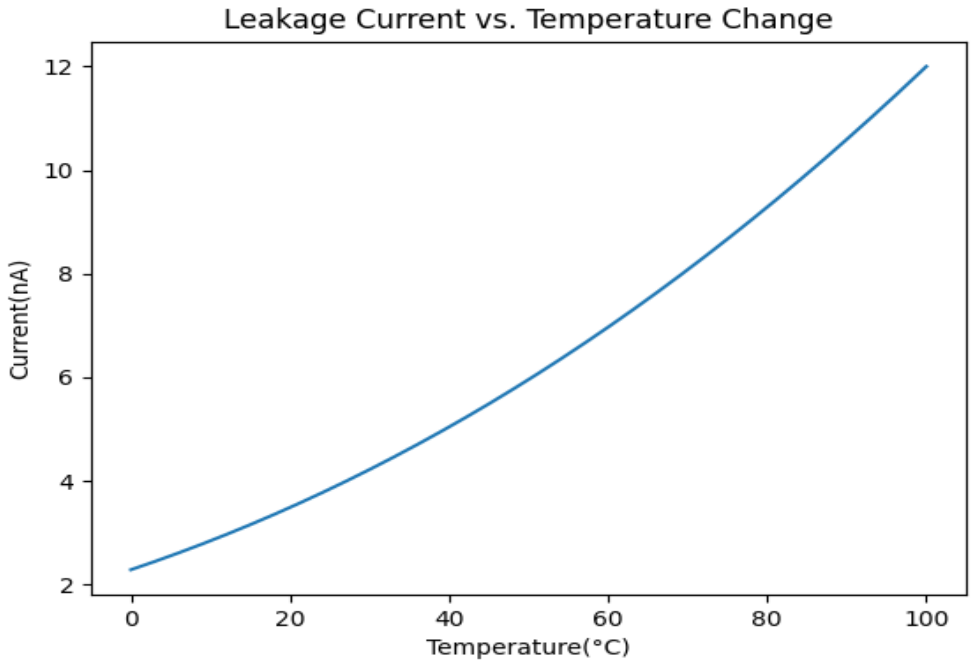
c. Leakage Current vs. Supply Voltage Change

Voltage(V)	0.9	1.0	1.1	1.2
Leakage Current	1.0689	2.0243	3.8423	7.3290



d. Leakage Current vs. Temperature Change

Temperature(°C)	Leakage current(nA)
0°C	2.2857
25°C	3.8423
50°C	5.9566
75°C	8.6686
100°C	11.9995



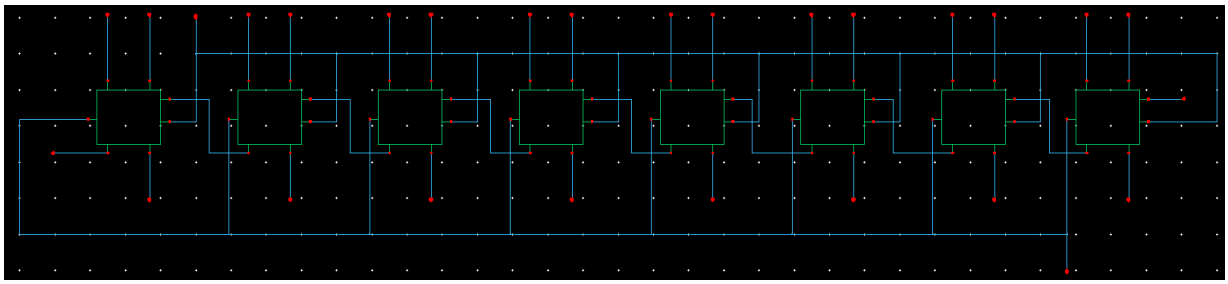
Choosing 1 Bit adder

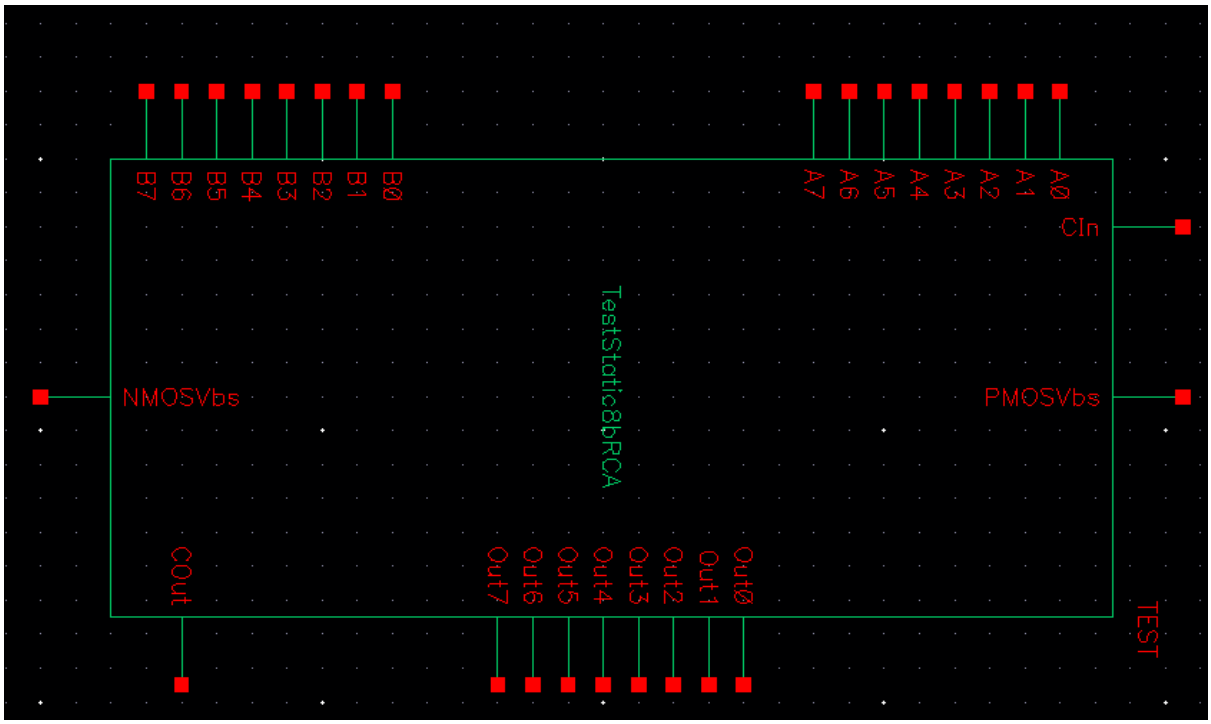
1. Area vs. Delay Analysis of 1 bit adders

TYPE	AREA	DELAY (ns)
Static CMOS FA	481.95 µm^2	0.192 (supply voltage of 1.1V)
Transmission Gate FA	121.5 µm^2	0.252(supply voltage of 1.1V)

8 Bit Ripple Carry Adder

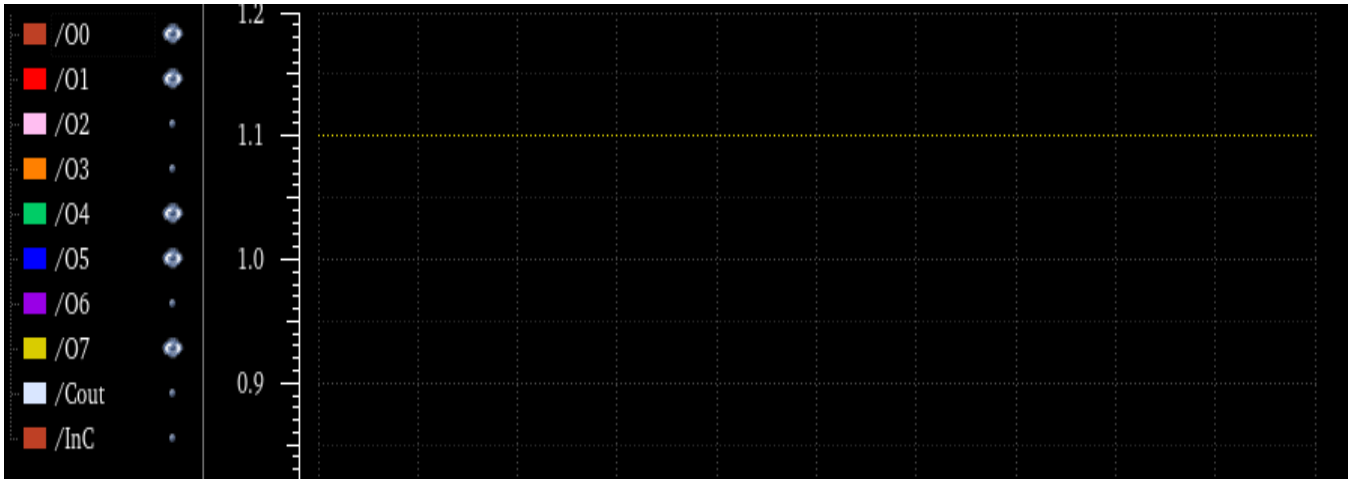
1. Implementation



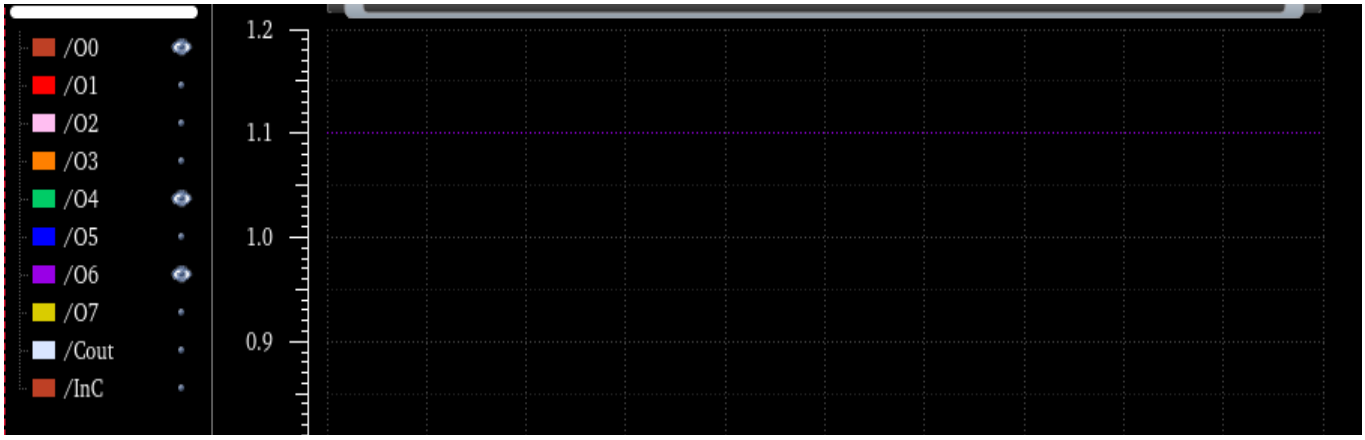


2. Functionality Verification(Marked as seen on graph)

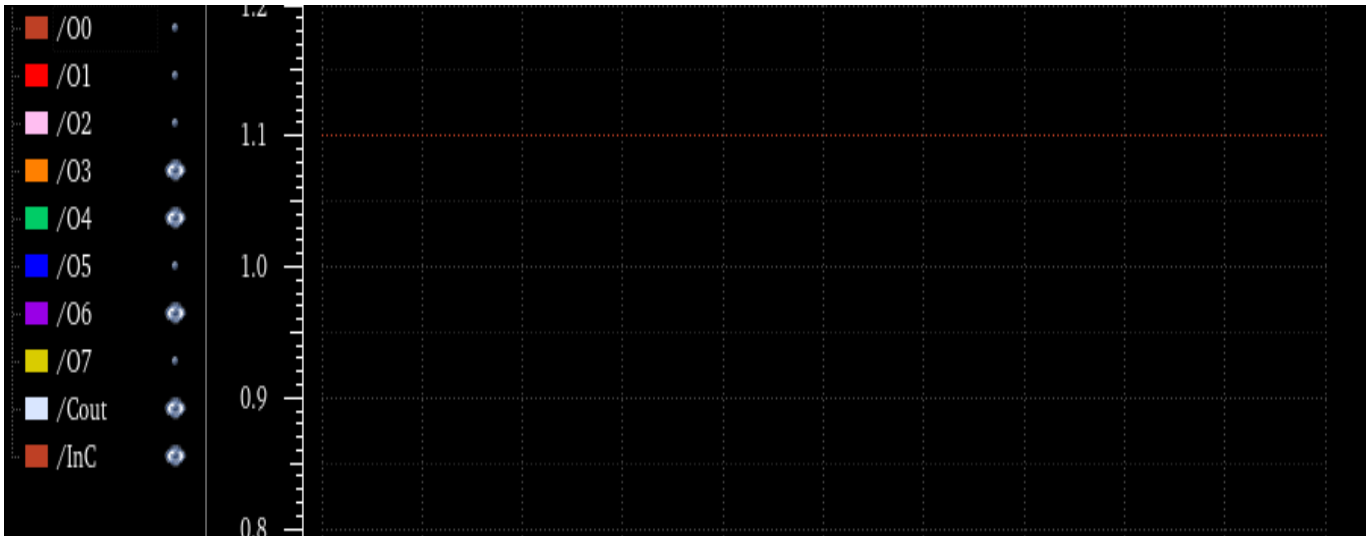
a. 82(01010010)+97(01100001)+0 = 010110011(179)



b. 48(00110000)+33(00100001)+0 = 001010001(81)



c. 214(11010110)+129(10000001)+1 = 101011000(344)

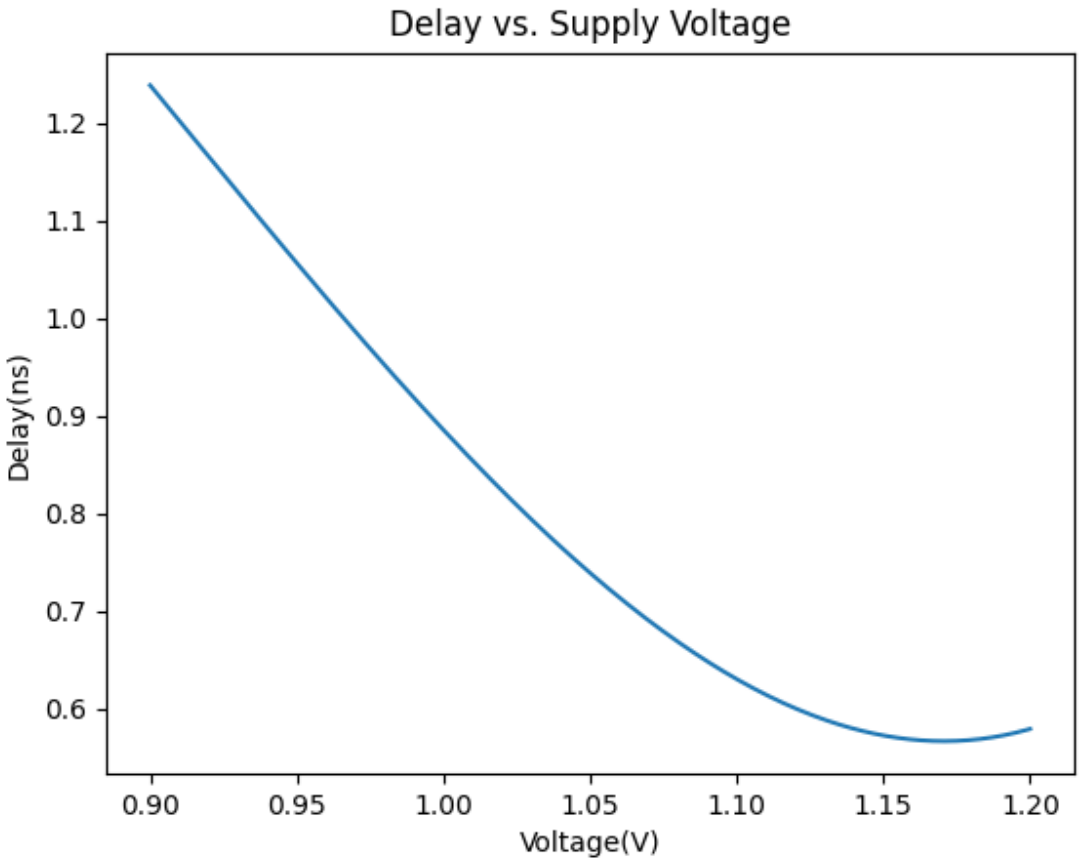


Worst case delay shown at the end of the report in the optimizing section.

3. Required Tests

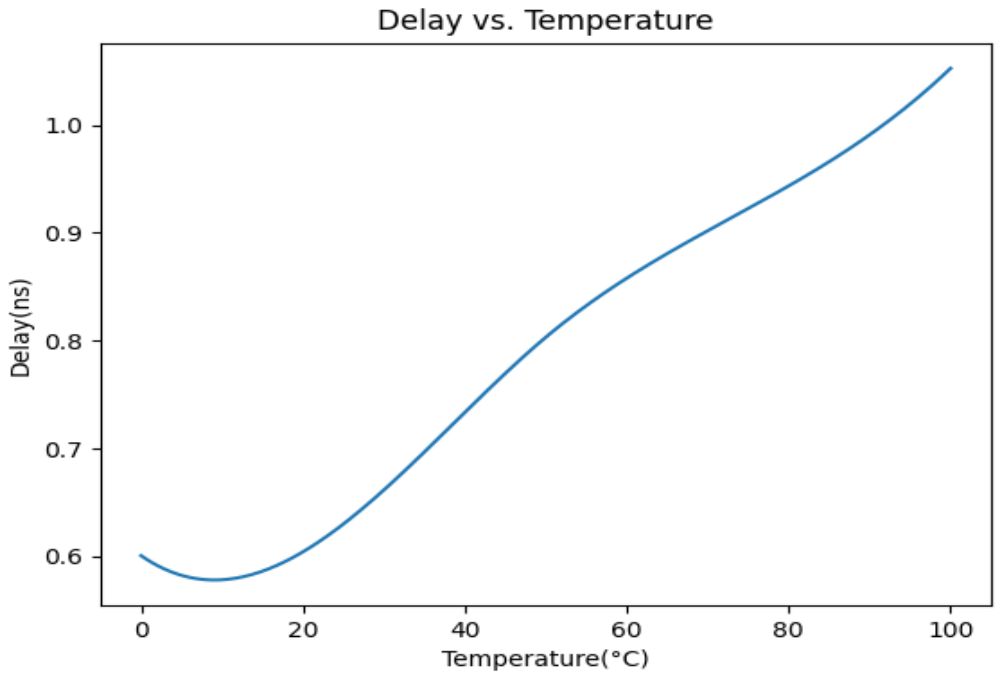
a. Delay vs. Supply Voltage

Voltage(V)	0.9	1.0	1.1	1.2
t_p(ns)	1.23922	.885655	.629955	.578895



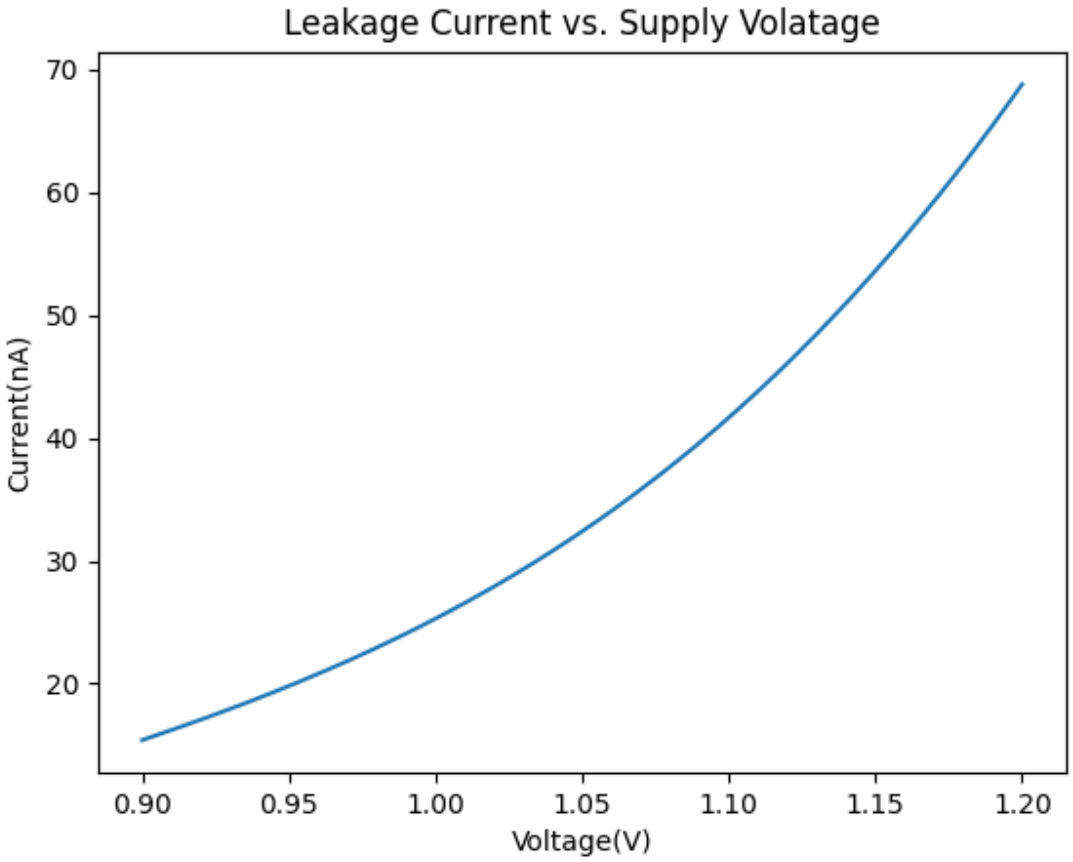
b. Delay vs. Temperature

Temperature(°C)	**t_p(ns)**
0°C	0.600575
25°C	0.629955
50°C	0.803205
75°C	0.92252
100°C	1.052595



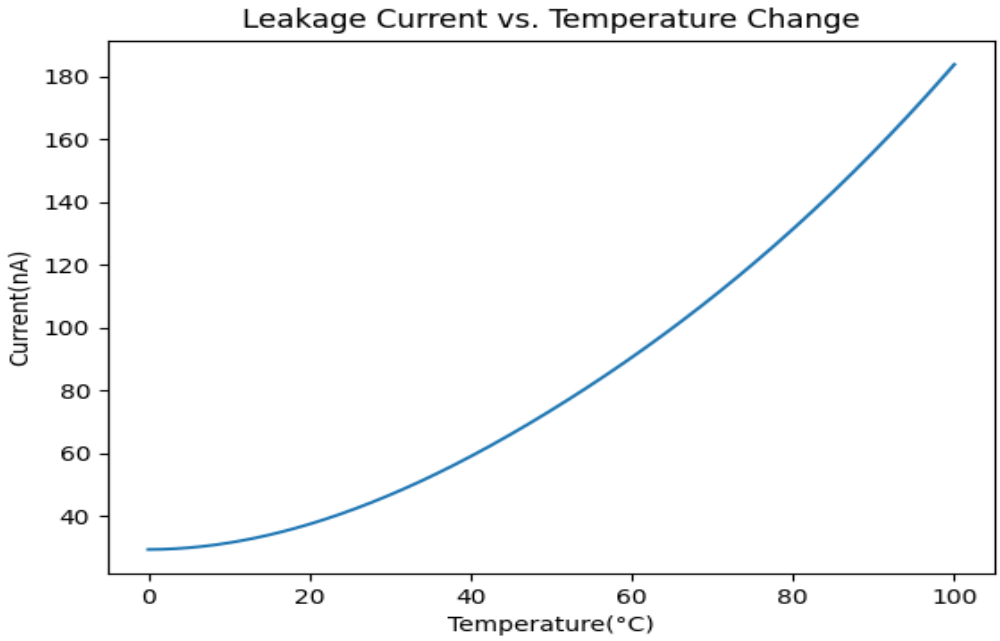
c. Leakage Current vs. Supply Voltage Change

Voltage(V)	**0.9**	**1.0**	**1.1**	**1.2**
Leakage Current(nA)	15.4	25.285	41.649	68.783



d. Leakage Current vs. Temperature Change

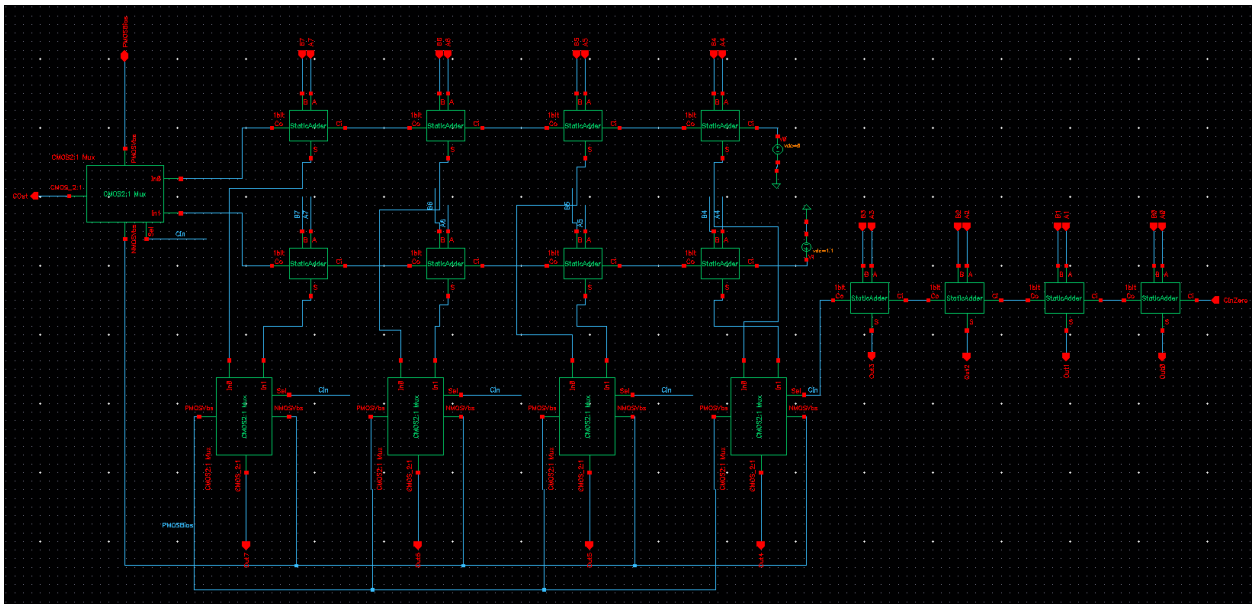
Temperature(°C)	Leakage current(nA)
0°C	29.296
25°C	41.649
50°C	73.651
75°C	120.155
100°C	183.746

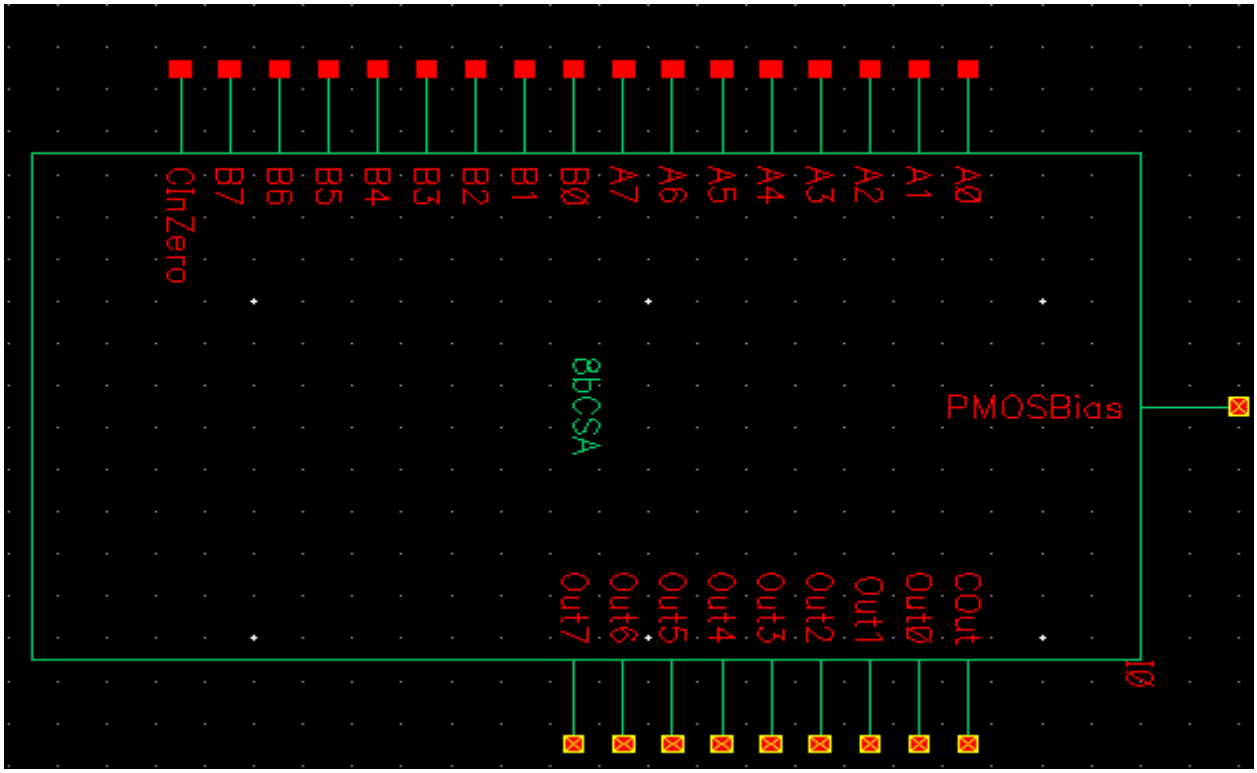

Leakage Current vs. Temperature Change
Current(nA)
180
160
140
120
100
80
60
40
0
20
40
60
80
100
Temperature(°C)

8 Bit Carry Select Adder

1. Implementation

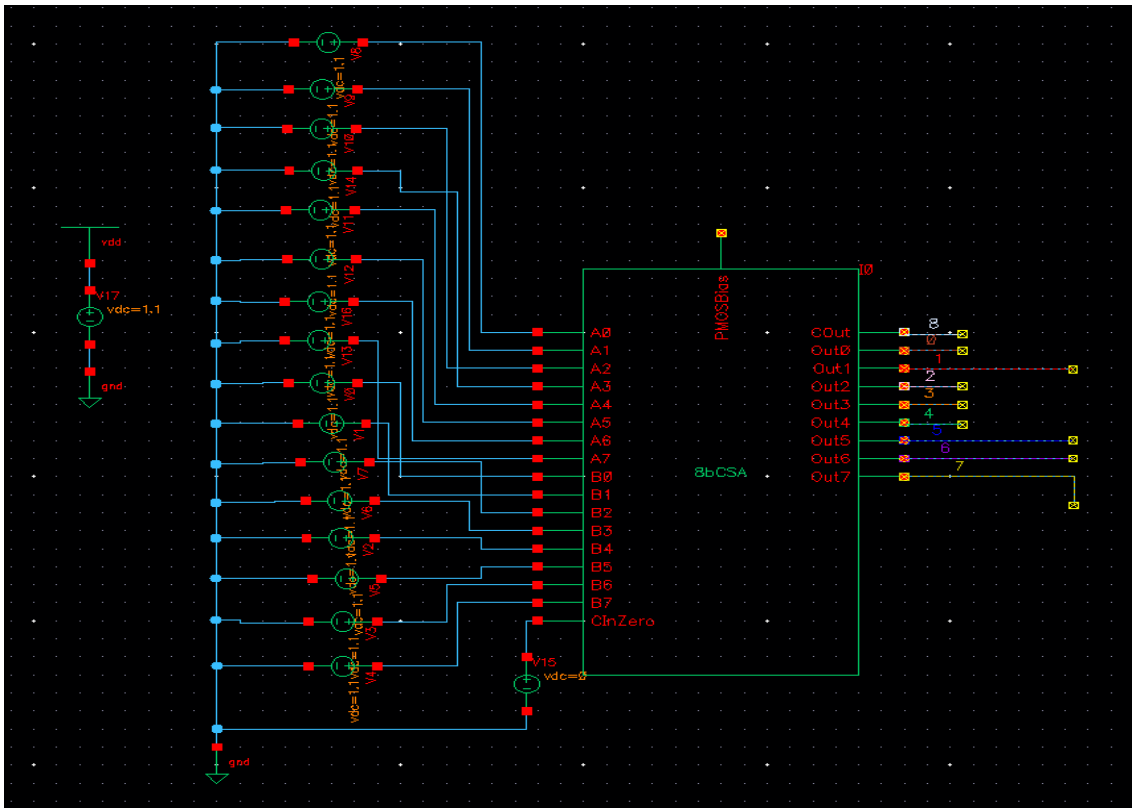
Done with Static CMOS implementation of a 1 bit full adder. There are a total of 12 full adders and 5 2:1 mux.



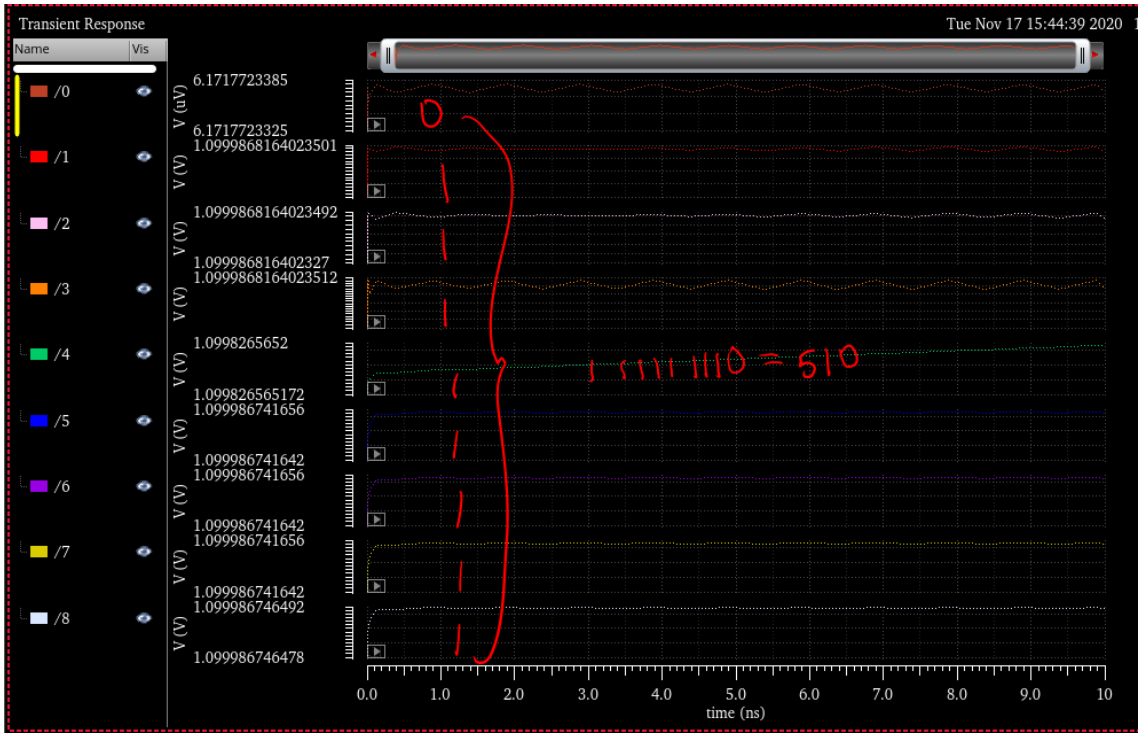


2. Functionality Verification

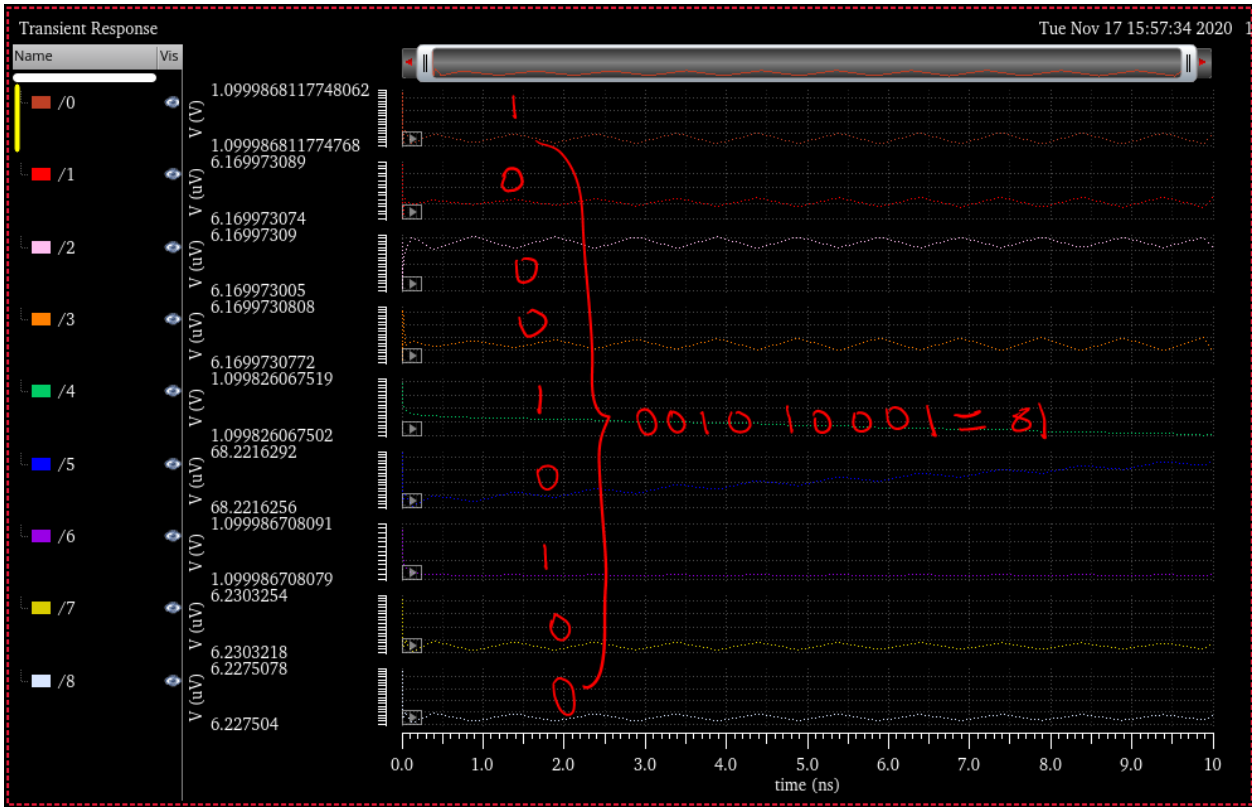
Testing setup:



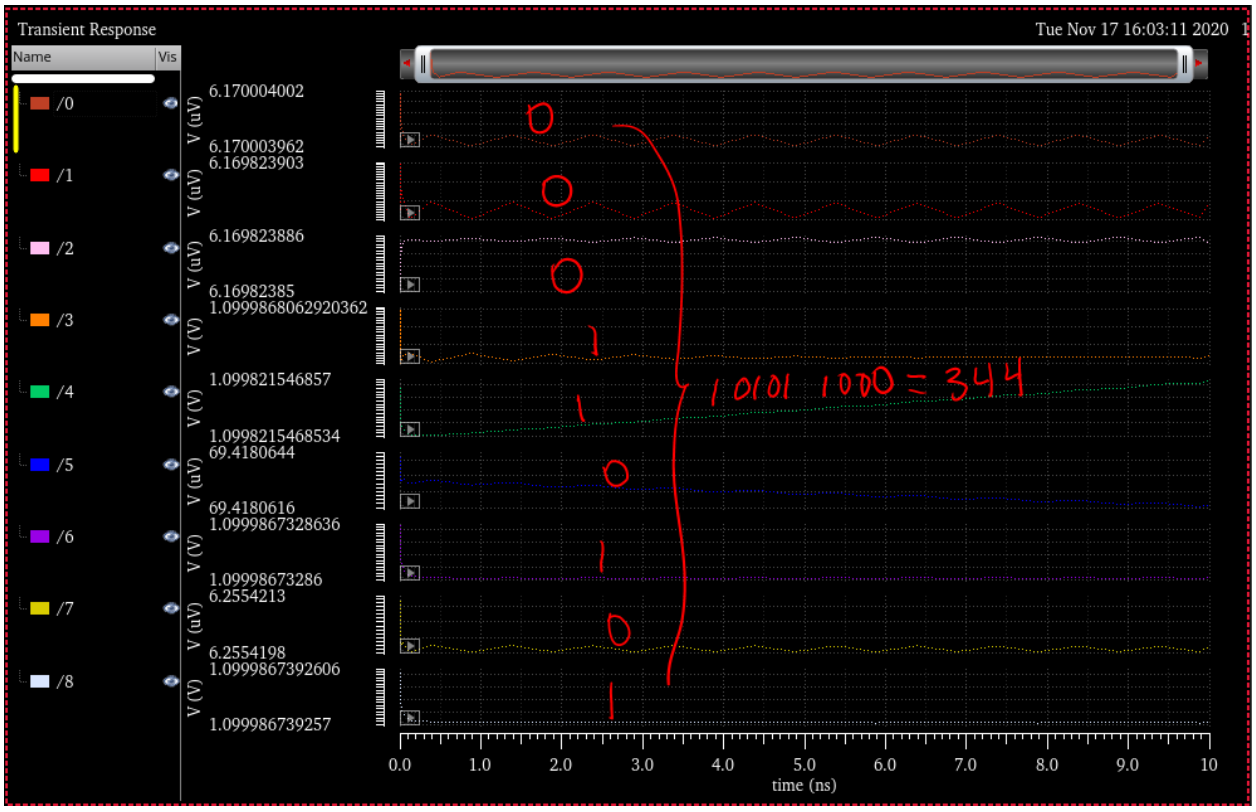
a. (255)11111111 + (255)1111111 + 0 = 111111110(510)



b. 48(00110000)+33(00100001)+0 = 001010001(81)



c. 214(11010110)+129(10000001)+1 = 101011000(344)

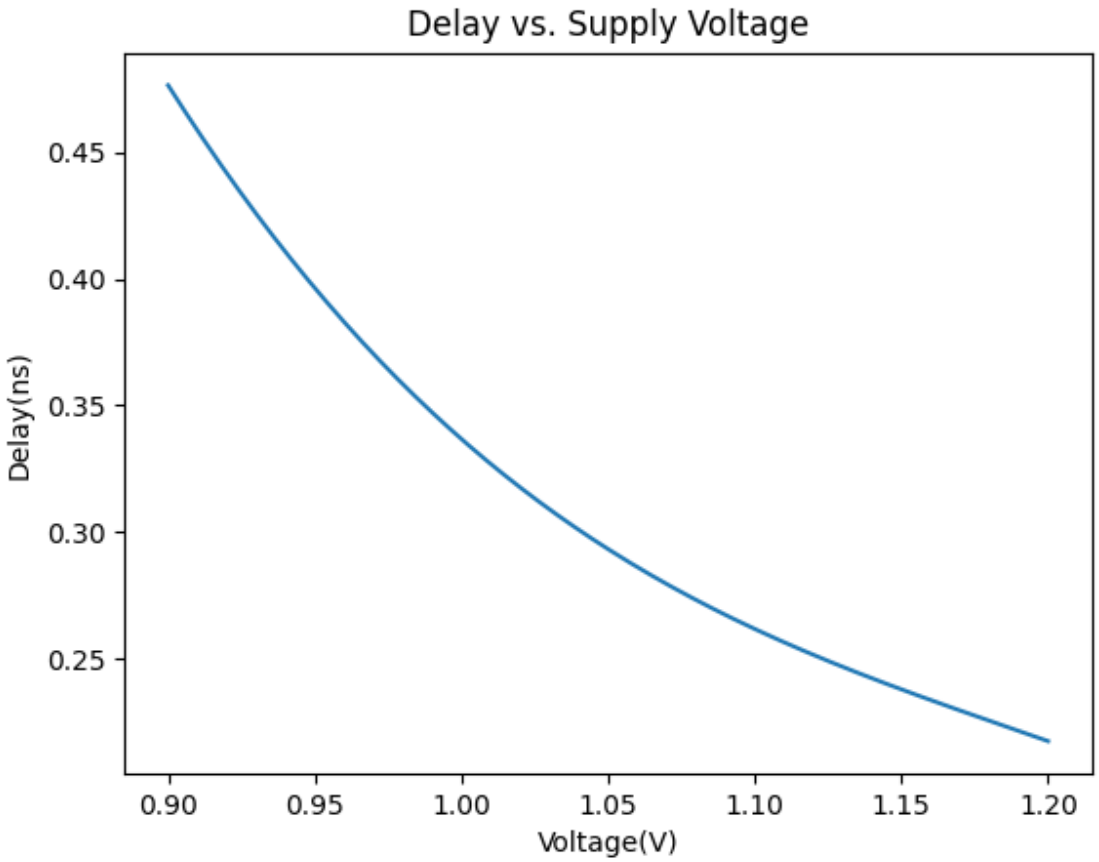


Worst case delay shown at the end of the report in the optimizing section.

3. Required Tests

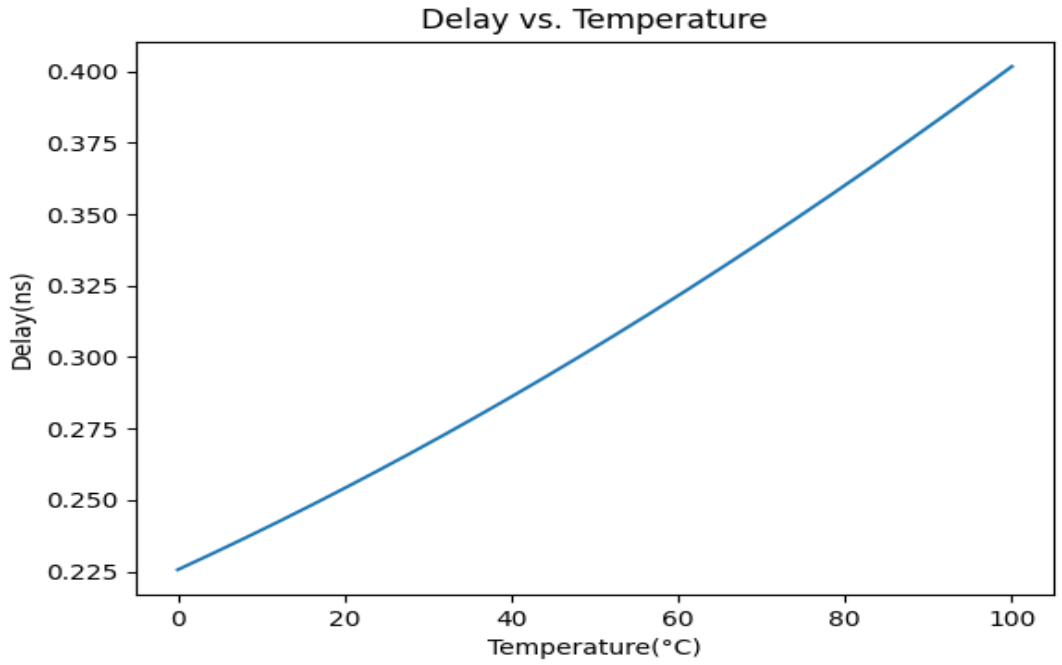
a. Delay vs. Supply Voltage

Voltage(V)	0.9	1.0	1.1	1.2
t_p(ns)	0.47643	0.33678	0.2618	0.21753



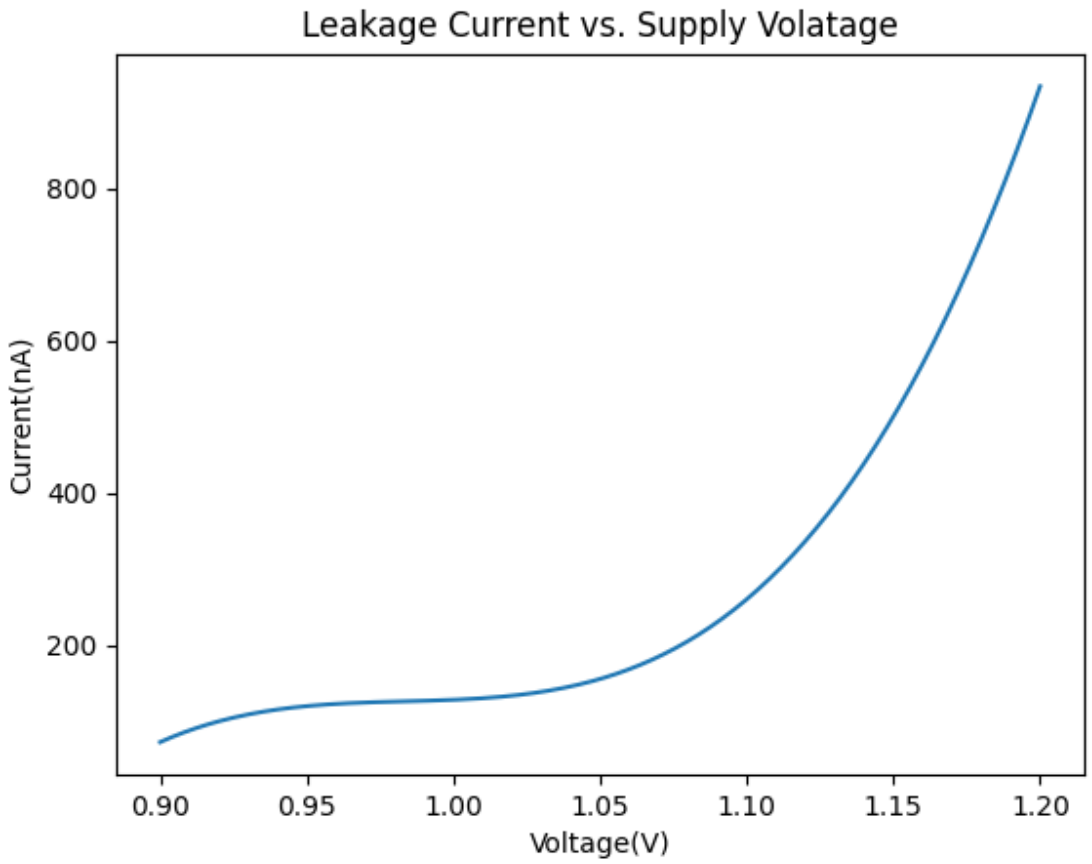
b. Delay vs. Temperature

Temperature(°C)	**t_p(ns)**
0°C	0.2256
25°C	0.2618
50°C	0.3034
75°C	0.3502
100°C	0.4017



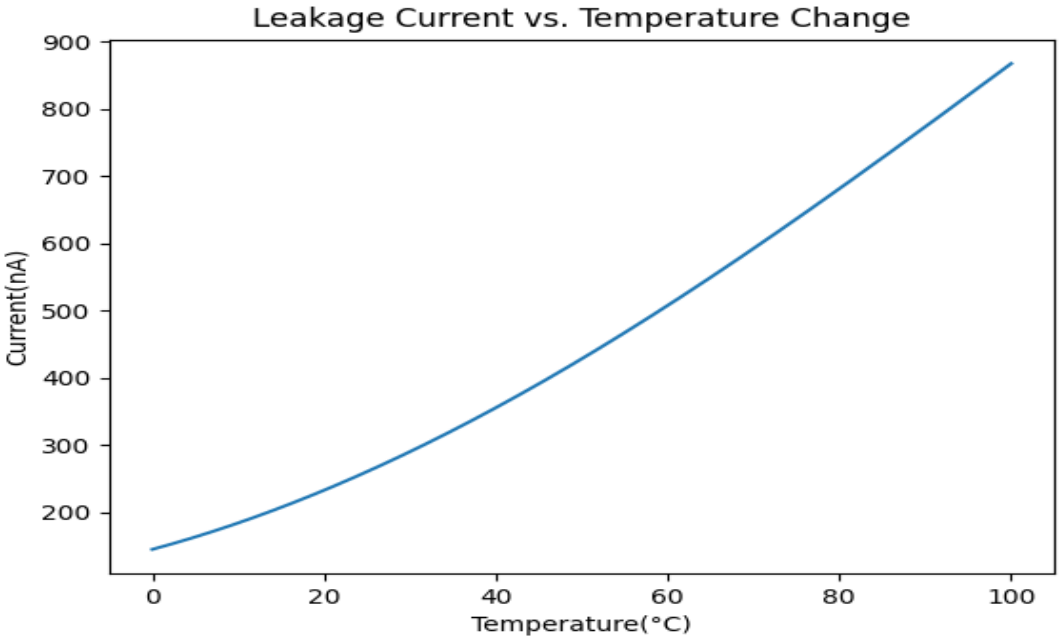
c. Leakage Current vs. Supply Voltage Change

Voltage(V)	**0.9**	**1.0**	**1.1**	**1.2**
Leakage Current(nA)	72.6	128.181	260.186	933.721



d. Leakage Current vs. Temperature Change

Temperature(°C)	Leakage current(nA)
0°C	144.5082
25°C	260.186
50°C	428.210
75°C	636.542
100°C	867.856


Leakage Current vs. Temperature Change
900
800
700
600
500
400
300
200
Current(nA)
0
20
40
60
80
100
Temperature(°C)

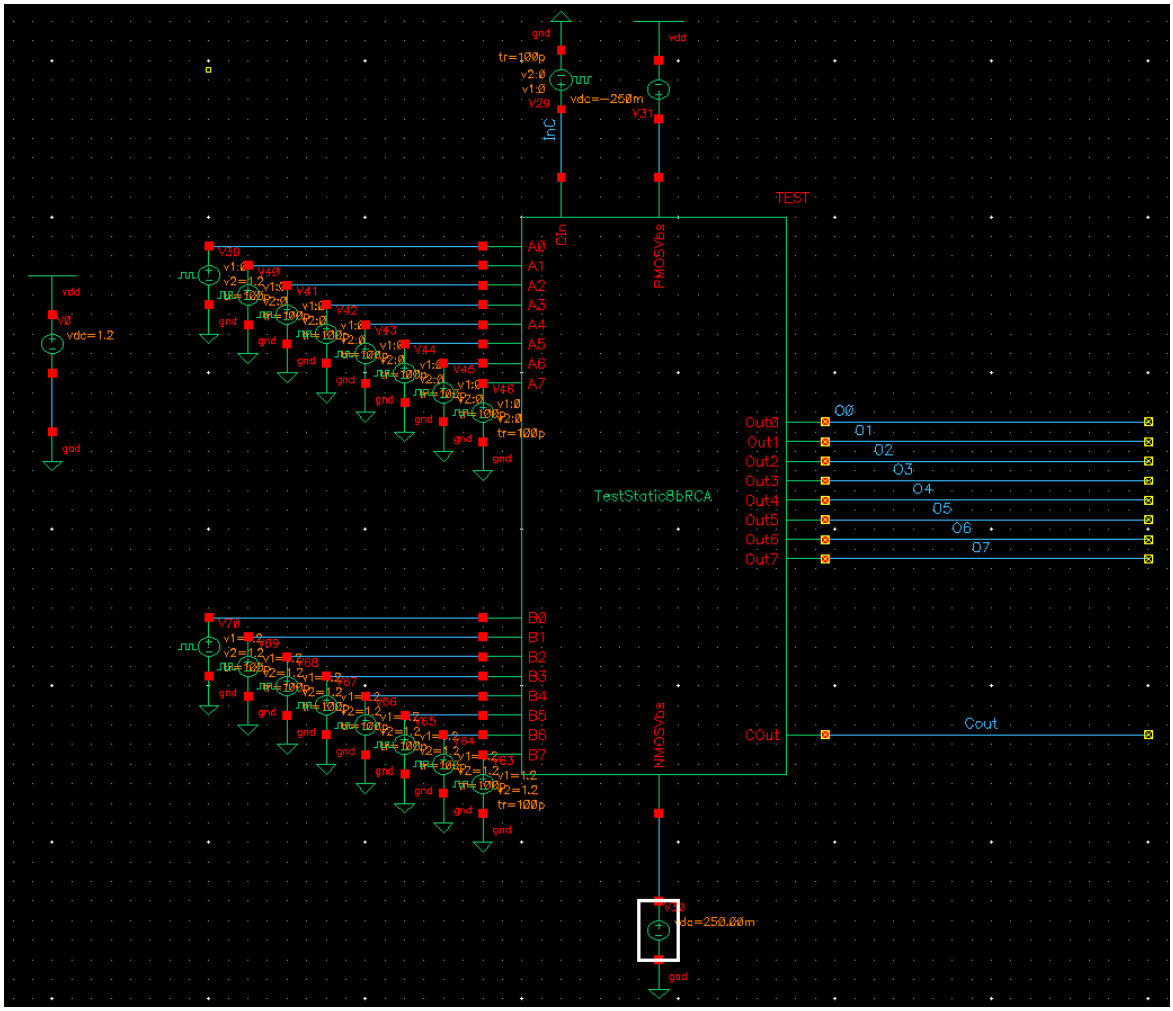
Optimizing One of the 8 Bit Adders

1. Area vs. Delay Analysis of 8 bit adders
    a. Delay is measured at the worst case which was when one input was 255 and the other flipped to one.

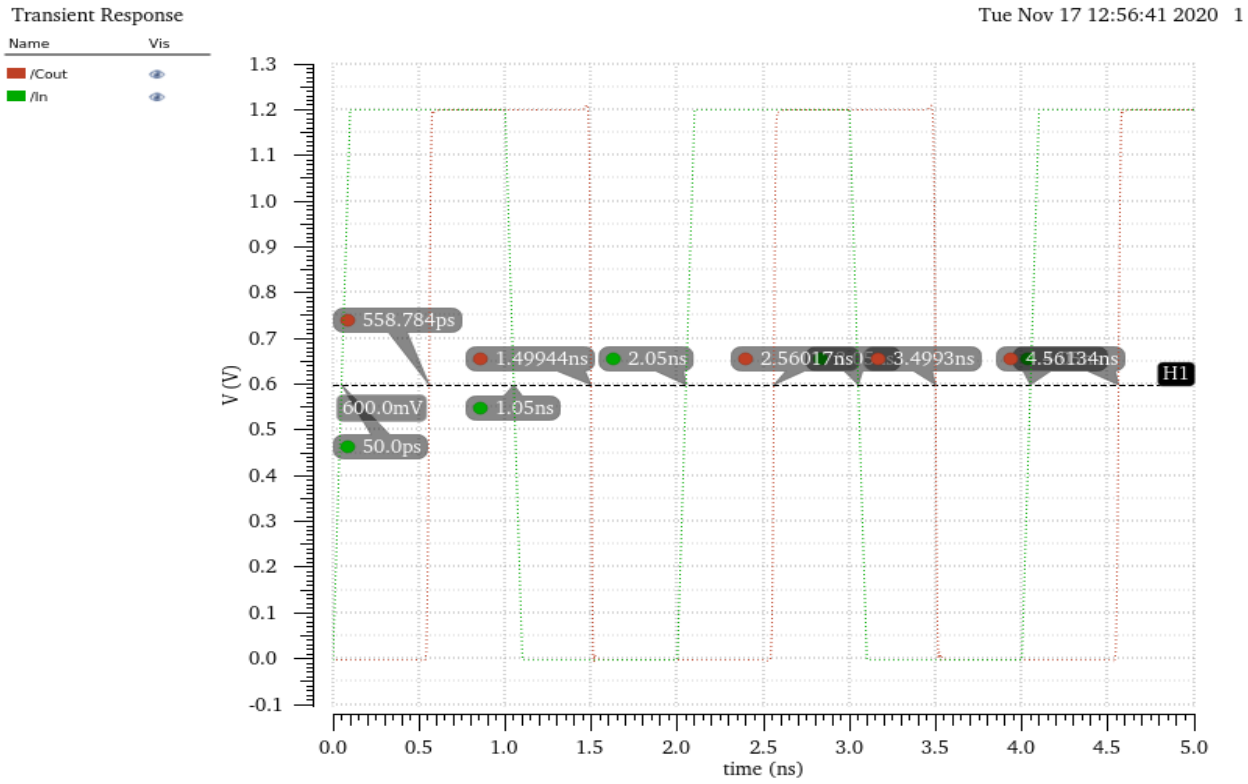
TYPE	AREA	DELAY(ps)
8 bit Ripple Carry Adder	3.8556 mm^2	479.805 (optimized at 1.2 V)
8 bit Carry Select Adder	5.9657 mm^2	260.186 (at 1.1V)

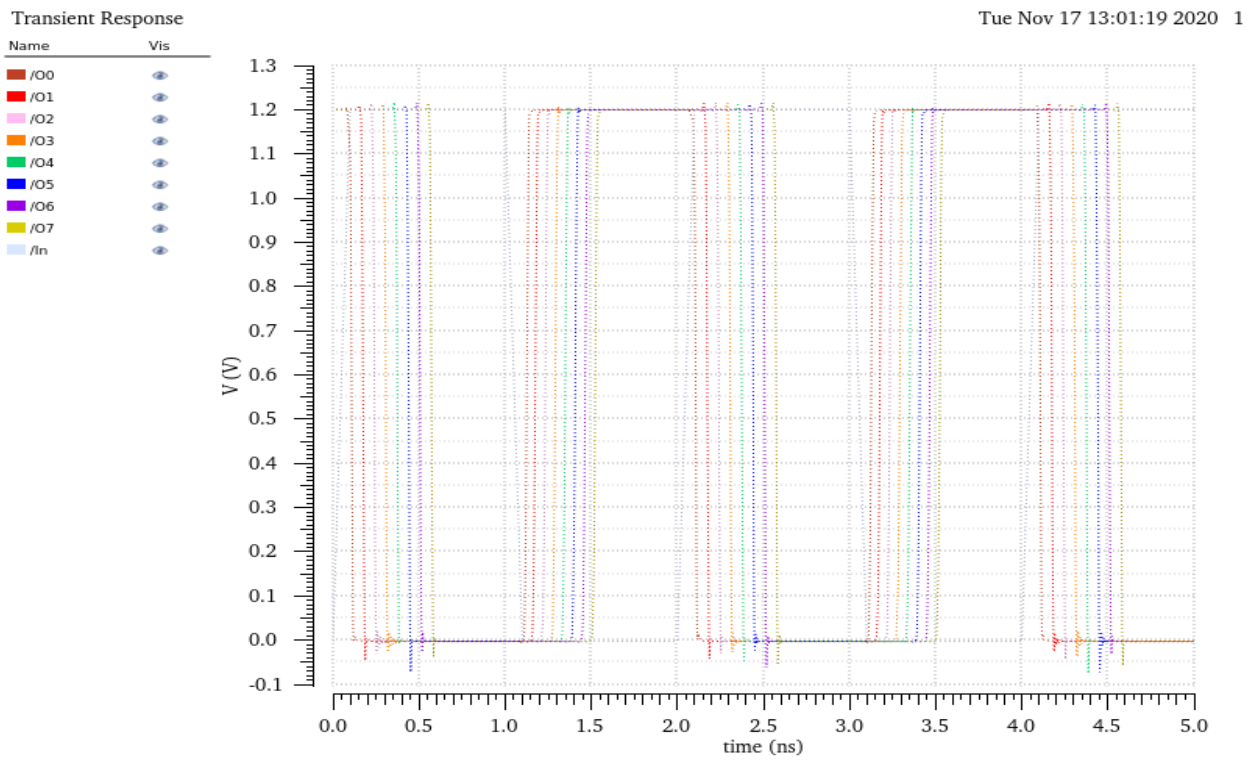
2. 8-bit adder set-up

Parameters: Vdd = 1.2V, PMOSVb = 0.95V, NMOSVb = 0.25V, A = 00000001, B = 11111111, CIn = 0, T = 25C



3. Simulation results





Appendix A

Work Distribution

Olivier Innocent	**Report formatting and graphs**
Joseph Riem	**Ripple Carry Adder:** • **All parts** **Carry Select Adder:** • **Initial design work** **Optimization of 8 bit adder**

Ryn Stewart	**Static CMOS Full Adder:** ● **All Parts** **Carry Select Adder:** ● **Implementation** ● **Functionality verification**
Robert Ciesielski	**Transition Gate Full Adder:** ● **All parts** **Carry Select Adder:** ● **All tests**