Wireless Communication IC

Topic of Final Projects

(06/20 17:00)

In the final project, you will implement either an algorithm or a hardware design for the algorithms of the homework. Two students form a group.

You can choose either one of the following 3 topics to implement. Upload all your programs (C/Matlab/Verilog) and reports to eeClass.

1. **K-best MIMO detector for 4x4 MIMO and 16-QAM** with K=8. The transmitted symbols belong to $\{\pm 1 \pm j, \pm 1 \pm 3j, \pm 3 \pm j, \pm 3 \pm 3j\}$. You need to generate your own test patterns. Besides, use the pattern provide in FinalProject1.mat to test your program and list the answer. Provide the simulation results of bit-error-rate (BER) v.s. signal-to-noise ratio (SNR) until BER below 10^{-3}. **Explain your design concept or flow chart of your program. Define your SNR. (Algorithm simulation only)**

2. **Depth-first MIMO detector for 4x4 MIMO and QPSK.** The transmitted symbols belong to $\{\pm 1 \pm j\}$. You need to generate your own test patterns for the BER and SNR curve. Besides, use the pattern provide in FinalProject2.mat to test your program and list the answer. Provide the simulation results of bit-error-rate (BER) v.s. signal-to-noise ratio (SNR) until BER below 10^{-3}. **Explain your design concept or flow chart of your program. Define your SNR. (Algorithm simulation only)**

3. Implement the hardware of delay correlator in Q3 of Homework 4 with parameter R and L chosen by yourselves. Please state the reason. Use the data in Homework 4 as test bench. In addition, you need to design the hardware of maximum search. Connect them together to ensure their simultaneous operation with serial input (one sample per clock cycle) and serial output. Compare the hardware outputs of delay correlator and maximum search with the Matlab outputs. **Illustration of hardware design concept is necessary.**

4. Design 6-best 3x3 MIMO detector for QPSK like in Homework 5. The transmitted symbols belong to $\{\pm 1 \pm j\}$. Use the pattern provide in FinalProject4.mat to test. Assume the input is $\mathbf{z}$ and $\mathbf{R}$. Determine the word-length of the hardware by providing some **quantitative results (shown by figures).** The error of calculated partial Euclidean distance should be less than 1×10^{-3}. Complete hardware simulation results. Compare the

hardware outputs with the Matlab outputs. **Illustration of hardware design concept is necessary.**

For 1 or 2, please upload

a. All your simulation codes in an RAR/ZIP file.
b. A WORD/PDF file of a report **explaining your design concept or flow chart of your program, simulation results and conclusion, and setting of SNR. If you have some new idea, please highlight it.**

For 3 or 4, please upload

a. Matlab codes and Verilog codes in an RAR/ZIP file.
b. A WORD/PDF file of a report illustrating **hardware design concept, Matlab simulation results, evaluation of quantization error, Verilog behavior and post-route simulation results, error comparison, and conclusion. If you have some new idea, please highlight it.**