





























## I. Overview

TM1640 is a LED (Light Emitting Diode Display) drive control circuit integrating MCU digital interface, digital latch, LED high voltage drive circuit, etc. The product has excellent performance and reliable quality, and is mainly applied in display drive for electronic scales and other small home appliances. In addition, it adopts the SOP28 packaging mode.

## II. Features

- Power CMOS technique
- Display mode (8 sections × 16 bits) supports common cathode digital tube output
- Brightness adjusting circuit (duty cycle adjustable among 8 levels)
- Dual-line serial interface (CLK, DIN)
- Mode of oscillation: built-in RC oscillation (450KHz±5%)
- Built-in power-on reset circuit
- Built-in auto blanking circuit
- Mode of packaging: SOP28

## III. Definitions of the pins

TM1640					
1		GRID12	GRID11		28
2		GRID13	GRID10		27
3		GRID14	GRID9		26
4		GRID15	GRID8		25
5		GRID16	GRID7		24
6		VSS	GRID6		23
7		DIN	GRID5		22
8		SCLK	GRID4		21
9		SEG1	GRID3		20
10		SEG2	GRID2		19
11		SEG3	GRID1		18
12		SEG4	VDD		17
13		SEG5	SEG8		16
14		SEG6	SEG7		15

#### ***IV. Functions of the pins***

Sign	Name	No.	Description
DIN	Data input	7	Serial data input; input data changed at low level and transferred at high level of SCLK
SCLK	Clock input	8	Input data at rising edge
SG1-SG8	Output (section)	9-16	Section output, P tube open drain output
GRID1-GRID11 GRID12-GRID16	Output (bit)	18-28 1-5	Bit output, N tube open drain output
VDD	Logic power supply	17	<b>5V±10%</b>
VSS	Logic grounding	6	Connect to system grounding

#### ***V. Electrical parameters***

**Limit parameters (Ta = 25°C, Vss = 0 V)**

Parameters	Sign	Scope	Unit
Logic power voltage	VDD	-0.5 to +7.0	V
Logic input voltage	VI1	-0.5 to VDD + 0.5	V
LED SEG drive output current	IO1	-200	mA
LED GRID drive output current	IO2	+20	mA
Power consumption	PD	400	mW
Work temperature	Topt	-40 to +85	°C
Storage temperature	Tstg	-65 to +150	°C

**Normal work condition (Ta = -40 to +85°C, Vss = 0 V)**

Parameters	Sign	Min.	Typical	Max.	Unit	Test condition
Logic power voltage	VDD		5		V	-
High level input voltage	VIH	0.7 VDD	-	VDD	V	-
Low level input voltage	VIL	0	-	0.3 VDD	V	-

**Electrical characteristics (Ta = -40 to +85°C, VDD = 4.5 to 5.5 V, Vss = 0 V)**

Parameters	Sign	Min.	Typical	Max.	Unit	Test condition
High level output current	Ioh1	-20	-25	-40	mA	GRID1~GRID16, Vo = vdd-2V
	Ioh2	-20	-30	-50	mA	GRID1~GRID16, Vo = vdd-3V
Low level output current	IOL1	80	140	-	mA	SEG1~SEG8 Vo=0.3V
Low level output current	Idout	4	-	-	mA	VO = 0.4V, dout
High level output current allowance	Itolsg	-	-	5	%	VO = VDD - 3V, GRID1~GRID16
Input value	II	-	-	±1	μA	VI = VDD / VSS
High level input voltage	VIH	0.7 VDD	-		V	CLK, DIN
Low level input voltage	VIL	-	-	0.3 VDD	V	CLK, DIN
Lagging voltage	VH	-	0.35	-	V	CLK, DIN
Dynamic current consumption	IDDdyn	-	-	5	mA	No load and display off

**Switching characteristics (Ta = -40 to +85°C, VDD = 4.5 to 5.5 V)**

Parameters	Sign	Min.	Typical	Max.	Unit	Test condition	
Oscillation frequency	fosc	-	450	-	KHz		
Transmission time delay	tPLZ	-	-	300	ns	CLK → DIO	
Transmission time	tPZL	-	-	100	ns	CLK → DIO CL = 15pF, RL = 10K	
Rising time	TTZH 1	-	-	2	μs	CL =	GRID1 to GRID16
Rising time	TTZH 2	-	-	0.5	μs	CL =	SEG1 to SEG8
Dropping time	TTHZ	-	-	120	μs	CL = 300pF, Segn, Gridn	
Max. clock frequency	Fmax	1	-	-	MHz	Duty ratio 50%	
Input capacitance	CI	-	-	15	pF	-	

**Time sequence characteristics (Ta = -40 to +85°C, VDD = 4.5 to 5.5 V)**

Parameters	Sign	Min.	Typical	Max.	Unit	Test condition
Clock pulse width	PWCLK	400	-	-	ns	-
Strobe pulse width	PWSTB	1	-	-	μs	-
Data setup time	tSETUP	100	-	-	ns	-
Data hold time	tHOLD	100	-	-	ns	-
Waiting time	tWAIT	1	-	-	μs	CLK↑→CLK↓

## VI. Description the interfaces

Data in microprocessor communicate with TM1640 through the bus interface. During data input, if CLK is at high level, the signal on DIN shall remain unchanged; it can only be changed if the clock signal on CLK is at low level. Low level of data inputs are always transmitted before high level. The starting condition of data input is: when CLK is high, the

DIN becomes low from high; the ending condition is: when CLK is high, the DIN becomes high from low.

Transmission process of command data is shown in the following figure:

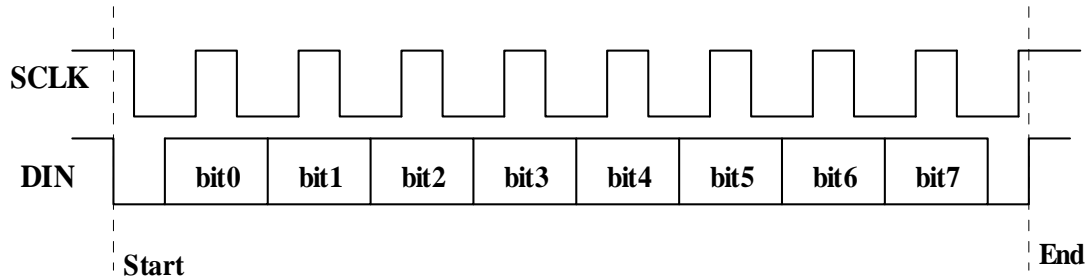


Figure 2: Command data transmission format

Writing SRAM data address auto + 1 mode:

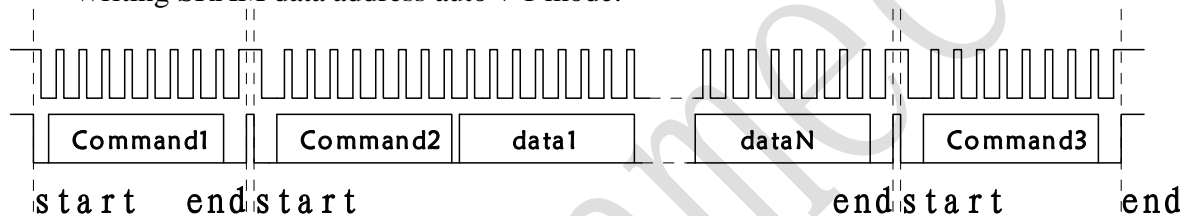


Figure 3: Format of auto address writing data

Command1: set data  
Command2: set address  
Data1-N: transmit display data  
Command3: control display

Writing SRAM data fixed address mode:

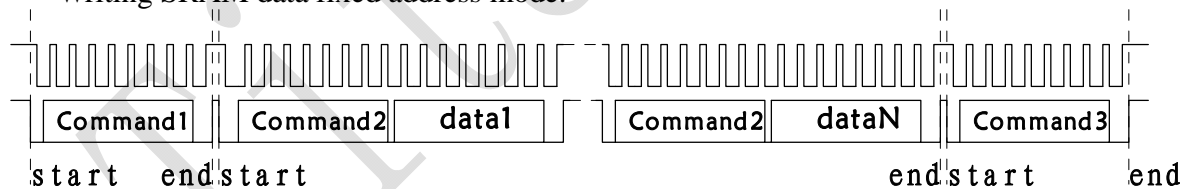


Figure 4: Format of fixed address writing data

Command1: set data  
Command2: set address  
Data1-N: transmit display data  
Command3: control display

## VII. Data command

Commands are used to set display mode and status of LED driver.

When START command becomes valid, the first byte input by DIN is taken as the first command. Through decoding, the highest B7 and B6 bits are adopted to distinguish different commands.

B7	B6	Command
0	1	Data command setting
1	0	Display control command setting
1	1	Address command setting

Table 7: Command setting classification

If END becomes valid during transmission of command or data, the serial communication will be initialized and the commands or data under transmission will become invalid (those completed transmission will remain valid).

**Data command setting:**

B7	B6	B5	B4	B3	B2	B1	B0	Description
0	1	Fill in 0 for items not applicable			0	Fill in 0 for items not applicable		Address auto + 1
0	1				1			Fixed address
0	1			0				Normal mode
0	1			1				Testing mode (internal use)

**Address command setting:**

B7	B6	B5	B4	B3	B2	B1	B0	Display address
1	1	Fill in 0 for items not applicable		0	0	0	0	00H
1	1			0	0	0	1	01H
1	1			0	0	1	0	02H
1	1			0	0	1	1	03H
1	1			0	1	0	0	04H
1	1			0	1	0	1	05H
1	1			0	1	1	0	06H
1	1			0	1	1	1	07H
1	1			1	0	0	0	08H
1	1			1	0	0	1	09H
1	1			1	0	1	0	0AH
1	1			1	0	1	1	0BH
1	1			1	1	0	0	0CH
1	1			1	1	0	1	0DH
1	1			1	1	1	0	0EH
1	1			1	1	1	1	0FH

Table 8: Display address command setting

When power-on, the default address is set as 00H.

The relationships between display data, chip pins and display addresses are shown in the following table:

SEG8	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1
B7	B6	B5	B4	B3	B2	B1	B0
Display memory address 00H							GRID1
Display memory address 01H							GRID2
Display memory address 02H							GRID3
Display memory address 03H							GRID4
Display memory address 04H							GRID5
Display memory address 05H							GRID6
Display memory address 06H							GRID7
Display memory address 07H							GRID8
Display memory address 08H							GRID9
Display memory address 09H							GRID10
Display memory address 0AH							GRID11
Display memory address 0BH							GRID12
Display memory address 0CH							GRID13
Display memory address 0DH							GRID14
Display memory address 0EH							GRID15
Display memory address 0FH							GRID16

Table 9: Relationship between display data, addresses and chip pins

#### Display control:

MSB				LSB				Function	Description
B7	B6	B5	B4	B3	B2	B1	B0		
1	0	Fill in 0 for items not applicable		1	0	0	0	Extinction Number setting (brightness setting)	Set pulse width to 1/16
1	0			1	0	0	1		Set pulse width to 2/16
1	0			1	0	1	0		Set pulse width to 4/16
1	0			1	0	1	1		Set pulse width to 10/16
1	0			1	1	0	0		Set pulse width to 11/16
1	0			1	1	0	1		Set pulse width to 12/16
1	0			1	1	1	0		Set pulse width to 13/16
1	0			1	1	1	1		Set pulse width to 14/16
1	0			0	X	X	X	Display switch setting	Display off
1	0			1	X	X	X		Display on

Table 10: Display mode control command

*VIII. Display cycle*

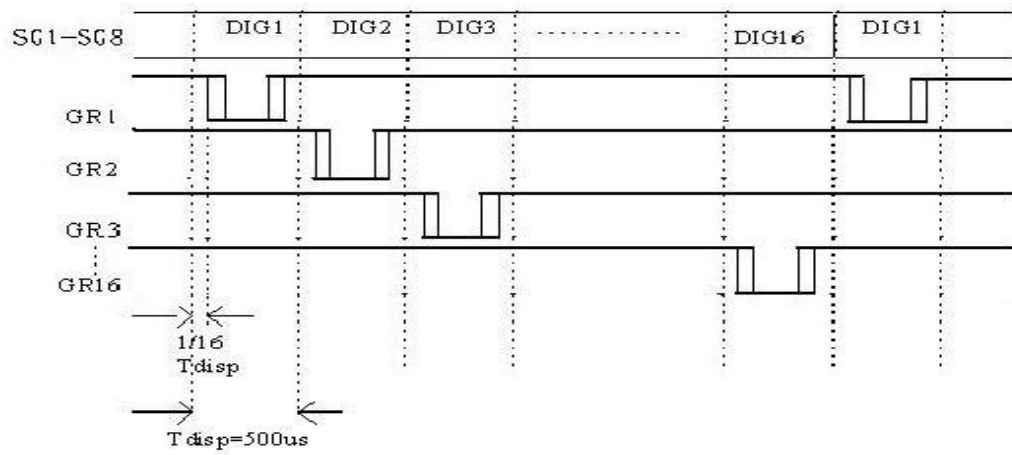
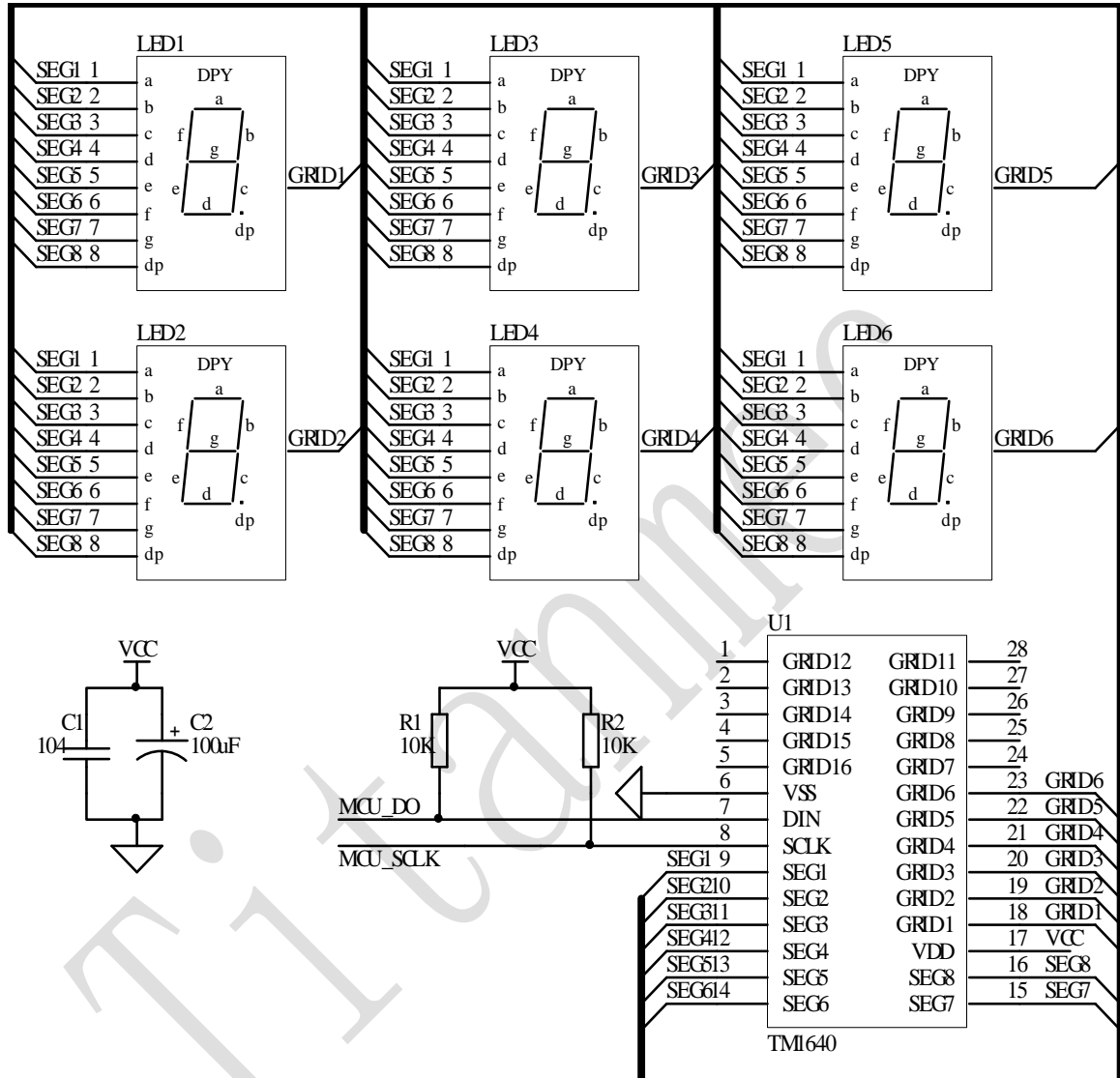


Figure 7: Data display cycle

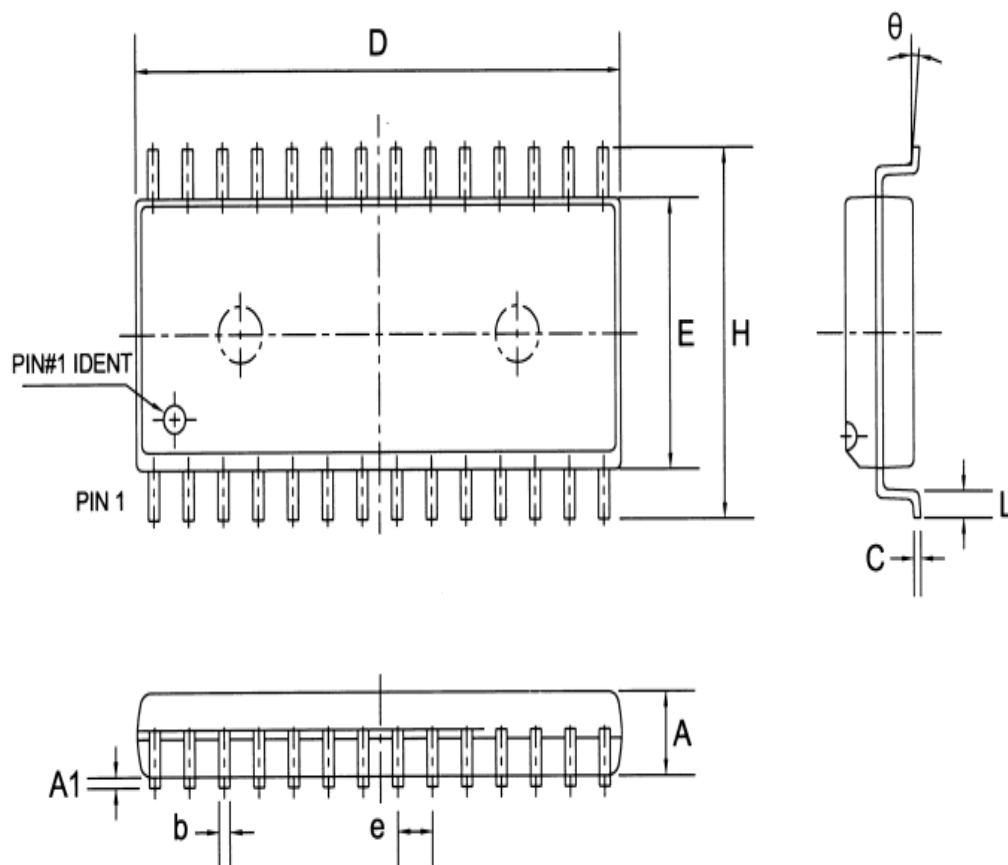


**IX. Hardware connection diagram**

Digital tubes shown in the diagram are common cathode digital tubes:



X. IC Packing drawing: (SOP28)



Symbol	Dimensions In Millimeters			Dimensions In Inches		
	Min	Nom	Max	Min	Nom	Max
A	2.15	2.35	2.55	0.085	0.093	0.100
A1	0.05	0.15	0.25	0.002	0.006	0.010
b	—	0.40	—	—	0.016	—
C	—	0.25	—	—	0.010	—
D	17.40	17.70	18.00	0.685	0.697	0.709
E	7.40	7.65	7.90	0.291	0.301	0.311
e	—	1.27	—	—	0.050	—
H	10.15	10.45	10.75	0.400	0.411	0.423
L	0.60	0.80	1.00	0.024	0.031	0.039
θ	0°	—	8°	0°	—	8°

- All specs and applications shown above subject to change without prior notice.