



UNIVERSITAT DE  
BARCELONA

A Master thesis for the degree of

**MASTER IN QUANTUM SCIENCE AND TECHNOLOGY**

---

# Characterization of Single Electron Transistors for Quantum Dot based Spin Qubits

---

Urtzi Jauregi Aberasturi

**Supervisors:** Francesc Perez, Gorka Aizpurua, Marius Costache

In collaboration with



*This page intentionally left blank*

# Characterization of Single Electron Transistors for Quantum Dot based Spin Qubits

Urtzi Jauregi Aberasturi

Supervised by: Francesc Perez, Gorka Aizpurua and Marius Costache

7th July 2024

High interest is placed on semiconductor devices to achieve scalable qubit technologies essential for the development of quantum computers. Nanowires and single-electron transistors (SETs) are fundamental in this pursuit due to their potential for electron confinement with long coherence times. This work contributes to the advancements of quantum technologies by developing SET characterization setups. Advanced techniques such as lock-in AC measurements and cryogenic temperature analysis have been employed to ensure precise evaluation of these devices. The demanding fabrication process and detailed characterization provide valuable insights into the electrical performance and stability of SETs, thereby supporting their potential applications in scalable quantum computing.

*Keywords:* SET, semiconductors, Coulomb oscillations, characterization setup, Spin qubits, Silicon, lock-in techniques.

# Contents

<b>1</b>	<b>Introduction</b>	<b>1</b>
<b>2</b>	<b>State of the Art</b>	<b>1</b>
2.1	Single Electron Transistors . . . . .	1
2.2	Silicon spin qubits . . . . .	5
<b>3</b>	<b>Objectives</b>	<b>7</b>
<b>4</b>	<b>Fabrication and architecture of Single Electron Transistors</b>	<b>7</b>
4.1	Non idealities . . . . .	8
<b>5</b>	<b>Measurement instrumentation</b>	<b>9</b>
5.1	Semiconductor Device Analyzer . . . . .	9
5.2	Opendacs DAC-ADC . . . . .	10
5.3	Lock-in amplifier . . . . .	10
5.4	Characterization setups . . . . .	11
5.5	Noise measurements . . . . .	12
5.6	MOSFET measurements . . . . .	13
5.7	Lock-in MOSFET measurements . . . . .	15
<b>6</b>	<b>SET characterization</b>	<b>17</b>
6.1	Barrier conductance . . . . .	17
6.2	Substrate current . . . . .	18
6.3	Coulomb peaks and diamonds . . . . .	19
<b>7</b>	<b>Conclusion</b>	<b>19</b>
	<b>Bibliography</b>	<b>21</b>
<b>A</b>	<b>Fabrication of SETs at the IMB-CNM cleanroom</b>	<b>23</b>
<b>B</b>	<b>Code for the characterization setup</b>	<b>27</b>

## 1 Introduction

Quantum technologies have made significant advancements in both industrial and research domains over the past few decades, thanks to their extraordinary potential for a wide range of technological applications. From the pursuit of the first practical quantum computer to the development of secure communication systems, the effort invested in this field is immense. However, the quantum realm presents both remarkable advantages and formidable challenges, such as scalability issues, short coherence times, and significant uncertainty regarding whether these technologies will eventually replace classical networks. Despite these challenges, significant investments from both private and public sectors around the world highlight the potential and promise of quantum technologies.

In this context, this project is situated within the Quantum Technology Ecosystem Platform (QTEP) of the Spanish National Research Council (CSIC), which gathers up to 35 different research groups. Among these is the NANONEMS group at the Institute of Microelectronics of Barcelona (IMB-CNM). The aim of this research is to develop silicon spin qubits for quantum technologies. Achieving this goal requires several preliminary steps, starting with the confinement of a single electron in potential wells, thereby creating a quantum dot. Given the extensive experience of the NANONEMS group in the semiconductor industry, we have fabricated single-electron transistors (SETs) to facilitate single-electron transport and subsequent electron confinement. However, characterizing these devices demands operation at cryogenic temperatures, which led to a collaboration with the University of Barcelona for low-temperature measurements.

The primary objective of this project is to design the experimental setup and conduct the necessary characterization of single electron transistors. This involves understanding their behaviour at low temperatures and evaluating their performance, which is a critical step toward the development of spin qubits in future research stages. SETs are chosen as a test vehicle to characterize the technology, as a preliminary step before attempting the fabrication of spin qubits

## 2 State of the Art

### 2.1 Single Electron Transistors

Single Electron Transistors (SETs) are nanoscale devices that control the transport of single elementary charges, leveraging the quantum mechanical properties of electrons. Based on the well-known technology of Metal-Oxide-Semiconductor Field-Effect-Transistors (MOSFETs), SETs replace the usual current-carrying channel with a small quantum dot, formed by two tunnelling junctions between the source and drain regions. A gate electrode regulates the flow of charges through the island, quantum dot, achieving a high level of sensitivity and precise control over electron flow. This allows SETs to exploit quantum effects to regulate electron transport at the single-electron level, representing a significant advancement in nanoscale electronics and quantum computing.

Single electron transport phenomena were first observed in the late 1980s through the work of Fulton and Dolan [1]. They observed the single-particle charging effect by fabricating a simple source-drain electrode configuration, metallic leads allowing electron transport, with two tunnel junctions and a gate electrode that modulated the charging effects. Parallelly, Likharev carried out a profound theoretical work on these type of de-

vices [2]. In his research, he proposed several methods to achieve single-particle transport, starting from the simple Electron Box of [1] and extending to Single Electron Transistors and electron traps (a generalization of the electron box) [2], which nowadays have great impact in nanowire devices.

A SET can be modelled using an equivalent circuit as the one in Figure 1. The small conducting island is connected to source and drain regions via tunnel junctions with capacitances  $C_s$  and  $C_d$ . Additionally, the island is capacitively coupled to a gate electrode with capacitance  $C_g$ .[3]

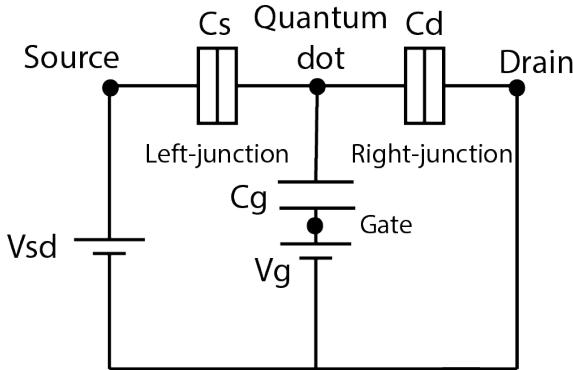


Figure 1: Equivalent circuit of a SET.

The fundamental operating principle of SETs involves the Coulomb blockade effect, where the transport of electrons is influenced by the energy required to add an additional electron to the quantum dot. This energy barrier ensures that electron tunnelling is highly controlled, dependent on the electrostatic environment defined by the gate voltage and the capacitive coupling of the island. Therefore, the Coulomb blockade effect inhibits electron tunnelling when the applied voltages do not provide sufficient energy to overcome the charging energy ( $E_C$ ), given by:

$$E_C = \frac{e^2}{2C_\Sigma} \quad (1)$$

where  $e$  is the elementary charge and  $C_\Sigma = C_s + C_d + C_g$  is the total capacitance of the quantum dot, the sum of the tunnel junctions and the gate capacitance.

The discrete nature of electron transport becomes apparent as the addition of even a single electron significantly alters the electrostatic potential of the island, leading to a blockade. This phenomenon is crucial for understanding the operation of SETs, as it dictates the conditions under which electrons can tunnel through the device. The Coulomb blockade effect ensures that electron transport is quantized, providing means to manipulate and control electron flow with high precision in nanoscale electronic devices. The transport is regulated by the electronic states of the quantum dot. In order to understand how different voltages might alter the conductance of the channel, a well-explained theoretical approach was made in [4]. This semiclassical approach, considers the Constant-Interaction model, the CI model, where the coulomb interactions between the electrons of the island and the rest are parametrized by the total capacitance  $C_\Sigma$ . Furthermore, the interactions within the dot are not considered, thus, the ground state of the  $N$ -electron dot is approximated

as:

$$U(N) = \frac{[e(N - N_0) - C_g V_g]^2}{2C_\Sigma} + \sum_{n,l} E_{n,l}(B) \quad (2)$$

where  $N_0$  is the number of electrons for gate voltage  $V_g = 0$  and  $C_g V_g$  is the charge induced by the gate voltage [5]. The last term is the energy sum of the single-particle states of the occupied states in the quantum dot, which in fact comes from solving the 2D Harmonic Oscillator Schrödinger equation, where  $n$  is the radial quantum number and  $l$  the angular momentum quantum number. On the other side, the electrochemical potential of the dot ( $\mu_{dot}$ ) is given by:

$$\mu_{dot}(N) = U(N) - U(N - 1) \quad (3)$$

This is an important physical factor as the electrons will only be able to flow through the channel when the electrochemical potential of the dot lies between the potentials of the source,  $\mu_s$  and the drain,  $\mu_d$ :

$$\mu_s > \mu_{dot} > \mu_d \quad (4)$$

Thus, a small voltage bias must be applied between source and drain, since  $eV_{SD} = \mu_s - \mu_d > E_C$ . From Equations (2) and (3), we get the GS of the electrochemical potential:

$$\mu_{dot}(N) = \left( N - N_0 - \frac{1}{2} \right) E_C - e \frac{C_g}{C_\Sigma} V_g + E_N \quad (5)$$

So the gate voltage has to fit the condition on Equation 4. Finally, the energy to add an electron to the island can be obtained:

$$\Delta\mu = \frac{e^2}{C_\Sigma} + \Delta E \quad (6)$$

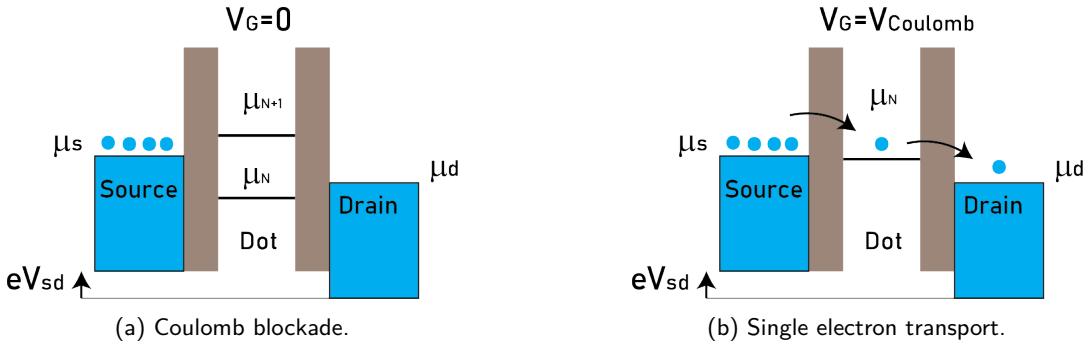


Figure 2: Electrochemical schemes of the quantum dot.

These conditions are observed with the Coulomb oscillations and diamonds. Coulomb oscillations are periodic variations in the differential conductance of a SET as a function of the voltage applied on the gate. Measuring differential conductance provides a more precise analysis of changes in the channel current. When the gate voltage aligns the electrochemical potential of the island with the one on the source or drain, the conductance of the device increases considerably due to electron transport in the channel. These increments, known

as Coulomb peaks, happen periodically as the energy levels of the island are continuously changing due to the gate voltage [6][7]:

$$eV_g = \left( n + \frac{1}{2} \right) E_C \quad (7)$$

These peaks show the addition of individual electrons to the quantum dot, and thus, conductance values are of the order of nanoSiemens. As previously explained, the source-drain voltage  $V_{sd}$  also plays an important role. Coulomb diamonds appear in a plot of conductance as a function of gate and source-drain voltages, showing the regions of the Coulomb blockade where electron transport is suppressed due to insufficient energy to add another electron to the quantum dot as in Figure 3.

When applying a source-drain voltage, for an electron to tunnel from source to dot the Inequality (8a) should occur and (8b) for an electron in the dot to reach the drain.

$$\mu_{\text{dot}}(N) < \mu_0 - \frac{eV_{sd}}{2} \quad (8a)$$

$$\mu_{\text{dot}}(N + 1) > \mu_0 + \frac{eV_{sd}}{2} \quad (8b)$$

These conditions define the boundaries of the Coulomb diamonds and information about the total capacitance of the island can be obtained, which typically reaches values as low as attofarads. Coulomb peaks and diamonds are the desired results of this thesis as it would be the first step towards silicon spin qubits fabricated at IMB-CNM.

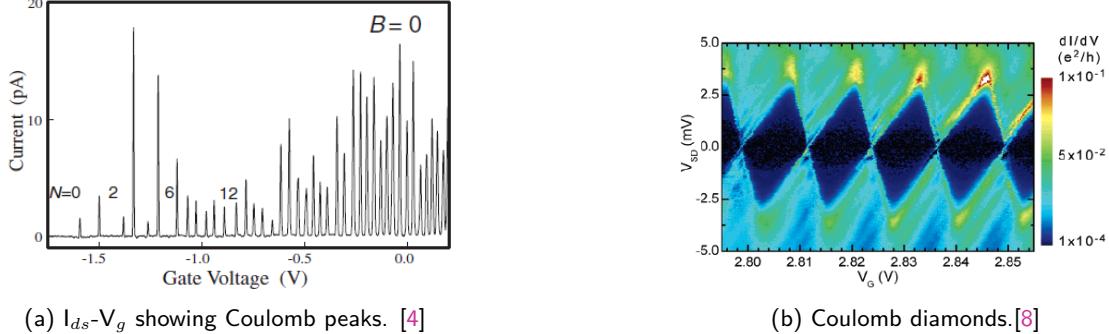
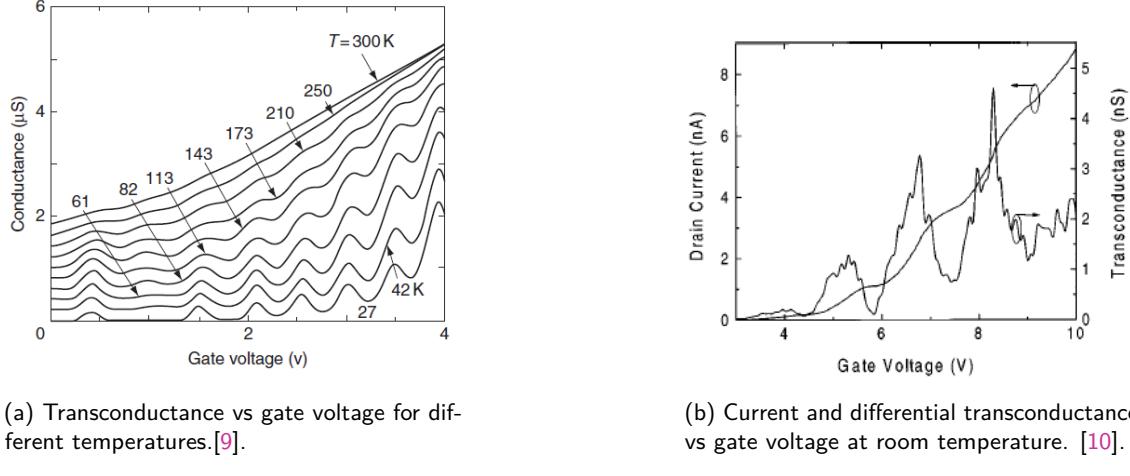


Figure 3: Coulomb oscillations and diamonds.

To visualize single electron transport in SETs, it is crucial to operate at low temperatures. At higher temperatures, thermal energy can exceed the charging energy  $E_C$ , making the energy levels less distinct and allowing multiple electrons to tunnel through the quantum dot. Therefore, to observe discrete electron tunnelling events, it is necessary that the charging energy greatly exceeds the thermal energy,  $E_C \gg k_B T$  typically requiring operation at cryogenic temperatures in the millikelvin range. However, it has been demonstrated that single particle transport can happen in higher temperatures, even at room temperatures, with careful design of the devices. Reducing the size of the quantum dot decreases the total capacitance, thereby increasing the charging energy. In 1995 Takashi et al. [9] increased the charging energy to about 70 meV, three times greater than the thermal energy at room temperature, achieving the impressive results shown in Figure 4a. Three years later, Zhuang, Guo, and Chou achieved 110 meV and showed sharper

peaks in the conductance of the channel, as observed in Figure 4b. Both works used Silicon nanowires as the conductive channel, making it easier to achieve smaller quantum dots.



(a) Transconductance vs gate voltage for different temperatures.[9].

(b) Current and differential transconductance vs gate voltage at room temperature. [10].

Figure 4: Single Electron phenomena measured at high temperatures.

Additionally, the tunnelling resistance  $R_T$  between the source and drain electrodes must be high enough so that the uncertainty of the charging energy is less than the charging energy itself [11]. According to the uncertainty principle and the time constant of the capacitor, given by  $\Delta t = R_t C_{dot}$ :

$$\frac{h}{R_t C_{dot}} < \frac{e^2}{2C_{dot}} \rightarrow R_t >> \frac{h}{e^2} = 25.813 \text{ k}\Omega \quad (9)$$

This value, known as von Klitzing resistance, indicates a lower boundary of the resistance necessary to observe the Coulomb blockade. Thus, the tunnel barriers must be fabricated ensuring that the quantum dot is well isolated to prevent unwanted tunneling.

## 2.2 Silicon spin qubits

The ability to control electron transport through quantum dots is essential for the creation of silicon spin qubits. Certainly, electrons can be confined in the dot between well-potentials with the following Hamiltonian [12][13]:

$$H = \frac{p^2}{2m^*} + V_{conf}(r) + H_Z \quad (10)$$

Where the first term is the momentum operator, the second term the confinement operator, which can be approximated as a 2D Harmonic Oscillator and  $H_Z$  is the Zeeman Hamiltonian that represents the interaction of the spin with an external magnetic field:

$$H_Z = g\mu_B \mathbf{B} \cdot \mathbf{S} \quad (11)$$

Where  $g$  is the Landé  $g$ -factor,  $\mu_B$  is the Bohr magneton and  $\mathbf{S}$  the spin operator. An external magnetic field,  $\mathbf{B}$ , splits the spin states up  $|\uparrow\rangle$  and down  $|\downarrow\rangle$ . Outstanding spin lifetimes have been measured lately getting qubits with coherence times in the millisecond range [14].

Loss and DiVincenzo first proposed theoretically how two quantum dots could be coupled to get a two-qubit quantum-gate operation by controlling the tunnelling barriers of the

quantum dots [15]. We could imagine it as a single electron transistor but with two quantum dots, created by adding more aluminium barriers in the conductance channel. This way, both islands would be separated by a single barrier whose potential is controlled by a high or low voltage. High voltages confine both electrons in their respective islands but low voltage allows interaction between both particles introducing time-dependent Heisenberg interaction:

$$H_s(t) = J(t)\mathbf{S}_1 \cdot \mathbf{S}_2 \quad (12)$$

$J$  is the interaction constant, modelled by the applied voltages. Thus, when the exchange interaction is on, the eigenstates of the system will be singlet and triplet states, obtaining a way to get a universal set of quantum gates for two-qubit systems.

In 2016 Maurand et al [16] created a double quantum dot system from 300 mm silicon-on-insulator wafers, p-doped source and drain regions and purified Si<sub>28</sub> channel with two gates above. At low temperatures, a double quantum dot system was formed in which one of them encoded a hole spin qubit and the other was used for qubit readout. This way, they could achieve electrical control of the hole spin qubit with microwave modulation. This work clearly demonstrated that by using silicon and standard CMOS processes, a high reliability and potential for larger-scale production can be ensured. Therefore, positioning these types of devices as a promising path toward scalable quantum computing architectures [17][18].

Moreover, the Intel research group has recently demonstrated a cutting-edge way to fabricate around 3700 quantum dots within a single 300 mm silicon wafer applying CMOS technology similar to the approach in [16], but introducing SiGe heterostructures to define a bidimensional electron gas in the substrate. This architecture enabled the electron confinement in the X and Y axes with gate electrodes. Thus, it was possible the formation of 12 quantum dot arrays, to obtain synchronous spin qubits as shown in Figure 5. The characterization methods were particularly innovative as they were able to cool the entire 300 mm wafer to 1.6 K. Moreover, it was demonstrated the possibility of controlling 16 quantum dot arrays at [19]. These works reinforce the capabilities of semiconductor qubits, demonstrating high uniformity and scalability and strengthening the debate over whether semiconducting technology might surpass superconducting technology in the realm of quantum computing hardware [20].

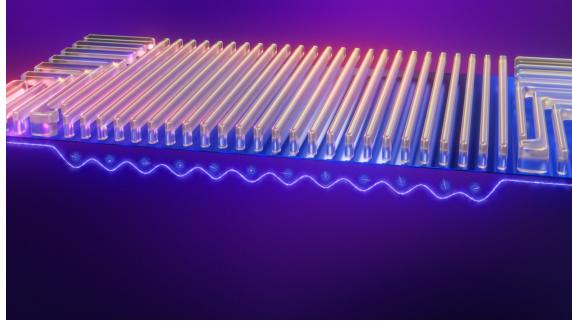


Figure 5: 1D array of 12 Quantum Dots. [21]

### 3 Objectives

As explained in the introduction, the objective of this thesis is the design and development of measurement systems for SET characterization. Yet, the characterization of single-electron transistors (SETs) involves complex processes due to their nanoscale dimensions and the sensitivity of their electrical properties. Thus, several previous steps must be taken before starting measuring the final devices:

- **Understanding the architecture of the devices:** This is the first essential step towards the successful management of Single Electron Transistors. This involves understanding the fabrication process, and reading state-of-the-art experimental setups and methodologies, explained in Section 5, to determine the most effective approaches for transport measurements. Developing a comprehensive understanding of SET devices includes their operational principles, structural composition, and the physical phenomena governing electron transport at the nanoscale.
- **Selecting the instrumentation:** instruments must be chosen carefully, considering the features we want to measure and the conditions under which these measurements will be taken. The instrumentation must be highly sensitive to detect the smallest changes in electron transport properties inherent to SETs. Analyzing similar experiments can help identify the necessary steps, which are vital for selecting the appropriate instrumentation.
- **Designing the experimental setups:** to measure the properties of SETs. Considering the lowest temperature we would reach with the UB cryostat was 24.5 K and 11 K at the ICMAB probe station, while the measurements at IMB-CNM would be conducted in room temperature.
- **Testing the setup:** It is necessary to test the good functioning of the setup with other semiconducting devices such as diodes and MOSFETs, as it also allows us to perform some noise analysis. This step includes learning how to communicate with the instrumentation via serial and GPIB connections for PC control.

After completing these steps we can proceed to measure the devices and analyze their properties to determine whether they are valid for creating silicon spin qubits. Additionally, we could identify the areas of improvement in the overall process, from fabrication to characterization.

### 4 Fabrication and architecture of Single Electron Transistors

The final layout of MOSFET and SET devices fabricated at IMB-CNM are displayed in Figure 6. These devices were designed based on the work by Angus et al. [8], trying to achieve a quantum dot diameter of  $\sim 50$  nm. An explanation of the fabrication process is available in Appendix A. Although I was not directly involved in fabrication, understanding this process is essential for interpreting the electrical characterization results.

Single Electron Transistors are fabricated on P-doped silicon wafers, serving as the substrate. As shown in Figure 6, the main difference between MOSFET and SET devices lies in defining two aluminium barriers, which create the quantum dot. This exploits one of the greatest advantages offered by semiconducting qubits: the extensive knowledge and

expertise of semiconductor technology, more specifically in fabrication processes and materials quality. Additionally, the semiconductor industry has demonstrated the capability to proper transistor scalability, Moore's Law [22], achieving billions of them in the same device.

The green regions of Figure 6 are the N-diffusion regions of the devices, the source and the drain, and have an ion concentration of  $N_D = 10^{19}\text{cm}^{-3}$ . The gate oxide is 6.5 nm thick, providing electrical insulation and acting as a dielectric between the gate and the substrate. The aluminium barrier gates are only 30 nm wide so precise EBL fabrication must be carried on. The length of the source-drain separation varies among different devices, with lengths of 4  $\mu\text{m}$ , 3  $\mu\text{m}$  or 2  $\mu\text{m}$ .

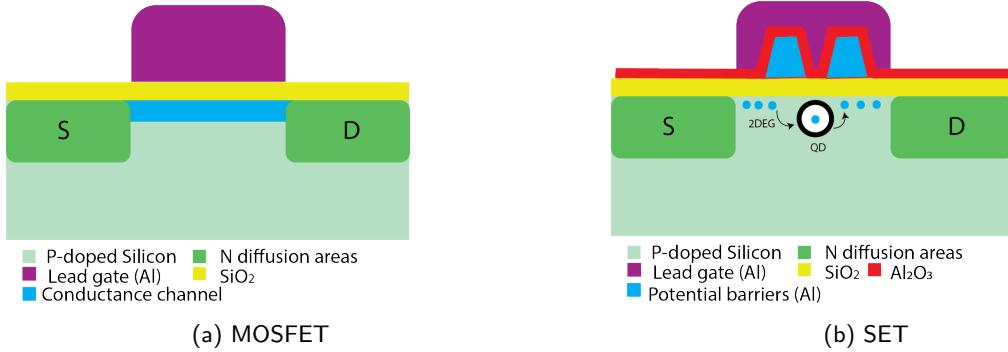


Figure 6: a) Scheme of the typical MOSFET and b) Scheme for the SETs we will characterize

Due to the doping differences, depletion regions form at the PN junctions in the substrate. When a positive gate voltage is applied, it attracts electrons from the N-diffusion regions just beneath the oxide layer, creating a 2D electron gas that forms a conductive path between the source and drain.

In SETs, the additional barriers introduce discretization of the electron transport, enabling single-carrier transport. This behaviour makes SET operation highly sensitive to voltage conditions, providing precise control over electron flow.

In Figure 7, we can take a closer look at the architecture of the devices with the images taken by scanning electron microscopy (SEM) and atomic-force microscopy (AFM).

#### 4.1 Non idealities

The devices might show non-ideal behaviours that could affect the proper functioning of the SETs. The most relevant issue is punch-through, a parasitic source-to-drain current caused by high doping differences at the PN junctions [23]. High doping differences create large depletion regions, which, due to the short channel length, could overlap, resulting in undesirable current and prohibiting single-electron phenomena. Usually, the punch-through effect is reduced by doping the silicon of the MOSFET channel with boron (P), but in order to get the lowest magnetic moment to increase the coherence times of the spin qubits, nearly-intrinsic silicon is employed. However, simulations and research indicate that this problem should be mitigated at lower temperatures, as the size of the depletion regions is directly temperature-dependent. Additionally, impurities may arise during the

fabrication process due to the challenges of achieving perfect operation at nanometric dimensions.

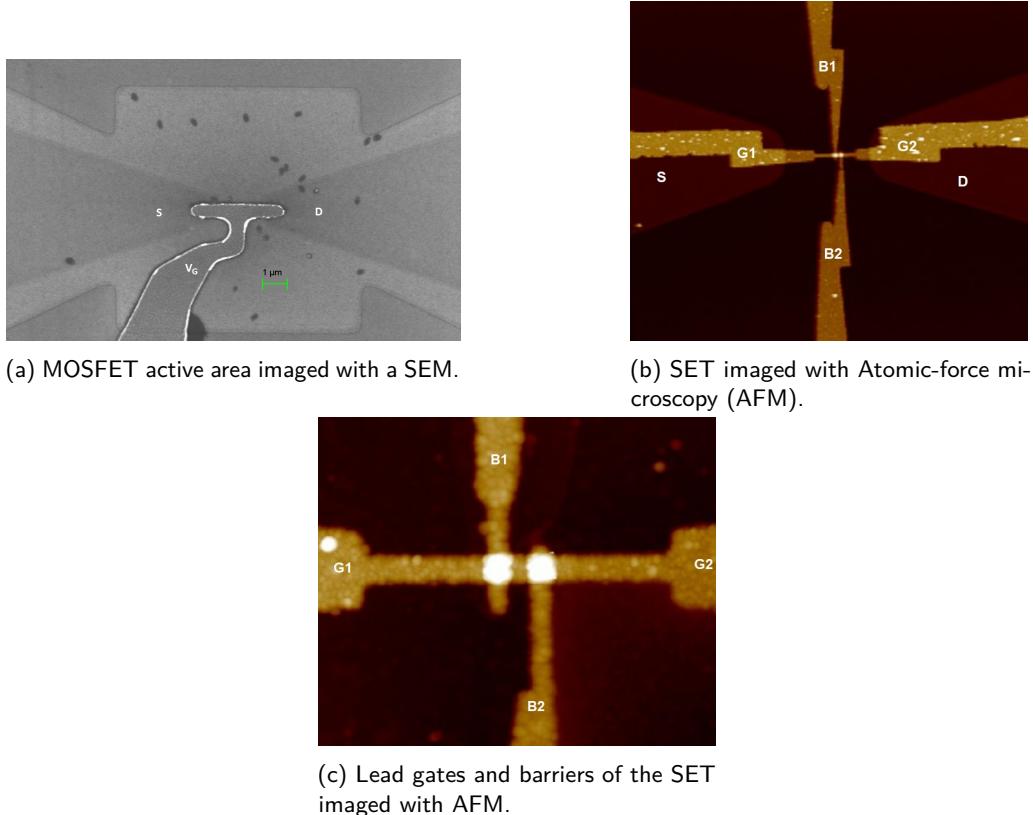


Figure 7: Active areas of a MOSFET and a SET.

## 5 Measurement instrumentation

Given the low current levels and variations to be measured, it is very important to use proper instrumentation and to pay attention to the smallest details. Handling the devices with grounded bodies and tools is essential to avoid unwanted static charging, and wearing gloves prevents contamination. Additionally, it is very useful to test the instrumentation with similar semiconductor devices to not only check everything is right but to provide some insight about the noise levels, in order to get more reliable data and have a more effective characterization.

Among other testing equipment, the main instruments that will help us properly characterize the SETs are a semiconductor device analyzer and a DAC-ADC system for performing voltage sweeps. Moreover, a lock-in amplifier will be employed to measure the differential conductance.

### 5.1 Semiconductor Device Analyzer

Semiconductor device analyzers are highly reliable devices used in the semiconductor industry for electrical characterization, as they allow voltage and current sweeps in 4 different terminals. In our case, we used the Agilent Technologies B1500A to measure trial devices

before measuring single electron transistors to make sure the equipment was functioning correctly. They operate with SMUs, source measurement units, making it possible to perform a voltage sweep and simultaneously measure the current within the same channel. This allows the establishment of compliance values to protect the devices and plotting the data for each channel.

## 5.2 Opendacs DAC-ADC

A DAC-ADC (digital-to-analog converter and analog-to-digital converter) device has been implemented for the characterisation at UB. Designed by [Opendacs](#), the device requires assembly from various components to complete the instrument. This assembly work was completed by Dr Matias Timmermans in 2019. The device operates with a central Arduino Due board, that sends signals through the evaluation boards. This DAC-ADC device uses a 16-bit DAC (AD5764) and ADC (AD7734) to achieve synchronized and fast measurements as shown in Figure 8. Communication with the DAC and ADC is facilitated by drivers written in the Arduino program and subsequently via a serial connection in a Python script. To simplify programming, I developed a DAC-ADC class in Python that includes the necessary commands. The general coding for the whole characterization setup is available on my [GitHub repository](#), but the general explanation is done in Appendix B.

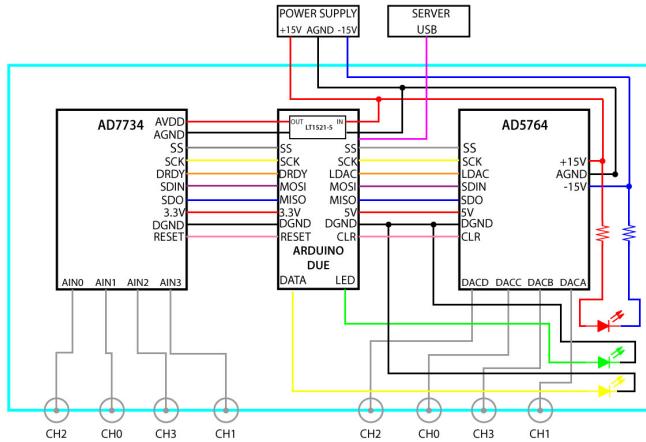


Figure 8: Opendacs DAC-ADC scheme.

## 5.3 Lock-in amplifier

Lock-in amplifiers are proper instruments for measuring low-amplitude signals, especially in a scenario like ours where precise differential conductance measurements are needed to capture the Coulomb peaks. These devices work by applying a low-amplitude AC signal through the sample at a certain frequency and measuring the resulting voltage or current. Lock-in amplifiers are particularly effective in filtering out unwanted noise signals at the same frequency or at a harmonic,  $f \pm \tau$ , where  $f$  is the measurement frequency and  $\tau$  is the time integration constant of the ADCs within the instrument. This effectively reduces the  $1/f$  noise, known as pink noise, that DC signals are typically exposed to, providing cleaner measurements.

Lock-in amplifiers use phase-sensitive detection with a dual-phase demodulation circuit shown in Figure 9. The input signal is split and multiplied with both the reference signal and a 90-degree phase-shifted copy. These mixed signals pass through configurable low-pass filters to obtain the in-phase and quadrature components. The amplitude and phase

of the signal are then derived by transforming these components from Cartesian to polar coordinates.

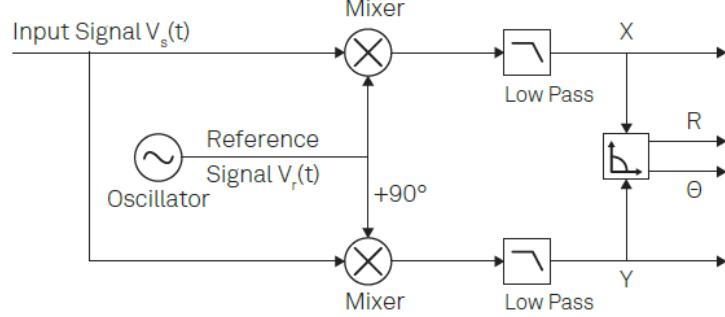
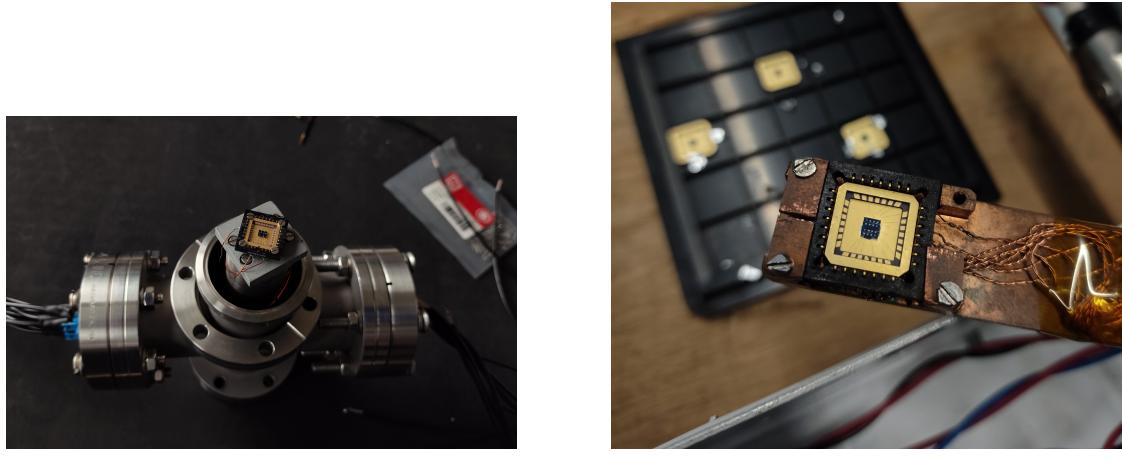


Figure 9: Dual-phase demodulation circuit of lock-in amplifiers.

Moreover, we needed to take good care when selecting the measurement frequency in order to obtain a good signal-to-noise ratio (SNR), as lower frequencies generally result in lower SNR. In our case, we measured the current through a resistor to fit the better frequency and finally selected 171 Hz. This selection was done by measuring the current through a  $100\text{ k}\Omega$  with different AC frequencies, choosing the value that better fitted with the real value. [24][25]

#### 5.4 Characterization setups

Considering that the resources for characterization varied between institutions, the work carried out at each location differed. Most of the thesis was conducted at IMB-CNM, where we undertook various tasks to prepare the setups. At IMB-CNM, we needed to prepare the measurement station to perform experiments on wire-bonded chips. The chips were bonded to a golden chip carrier, *LCC 28 pin ANDON chip carrier*, which was then screwed onto a chip carrier socket, *Kyocer 28 pin*. The pins of the socket had to be connected to the outer line of instrumentation with thin copper cables covered with Kapton, involving cable peeling and precise soldering to the socket pins, as shown in Figure 10.



(a) MOSFET chip at IMB-CNM.

(b) SET chip at UB.

Figure 10: Chip stations of IMB-CNM and UB.

The mechanical aspects of experimental physics can often be challenging and tedious. At UB these preparatory steps were already prepared for their previous experimental projects so it was ready to be used.

## 5.5 Noise measurements

Reducing the noise is one of the key aspects of nanodevice characterization. To get information about the environment we used the lock-in amplifier and measured the I/V characteristic curves of a commercial 1N4001 diode. Previously, we obtained the DC I/V curve with the SDA, as shown in Figure 11a. Then, by coupling a  $50 \mu\text{V}$  AC voltage to the DC, we measured the output differential current magnitude, illustrated in Figure 11b. The results are consistent, as the derivative of an exponential function is another exponential function, with positive values since the lock-in measures the magnitude. The differential conductance is obtained by dividing the measured current magnitude by the input AC amplitude.

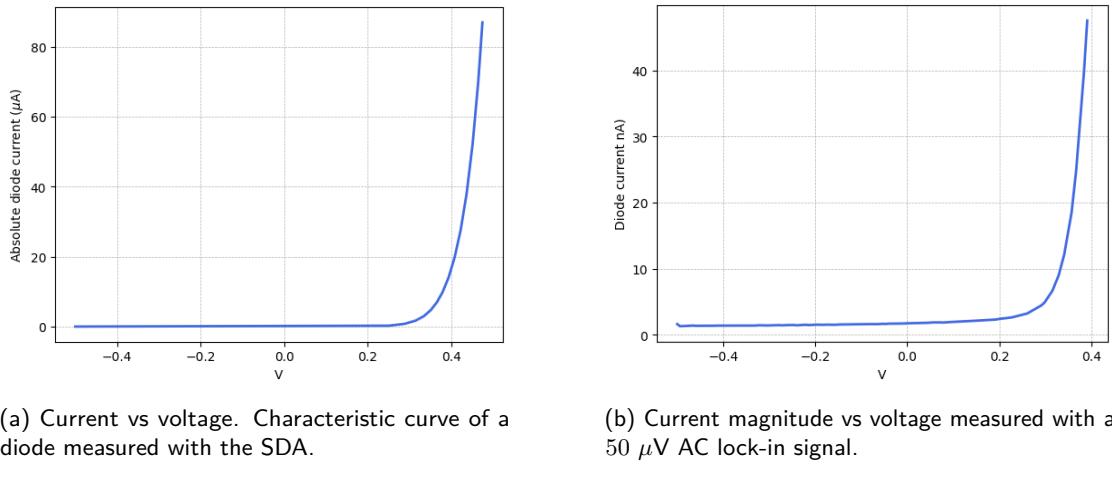


Figure 11: Characteristic curves of the MODEL diode in vacuum ( $4\text{e-}5 \text{ mbar}$ ).

After establishing the expected diode curve, we measured noise by maintaining the diode at specific working points and analyzing variations in conductivity using the lock-in with different integration time constants: 500 ms, 1 s and 2 s. Measurements were taken both outside and inside the vacuum chamber, providing substantial information.

Considering the Coulomb peaks are expected to have current magnitudes around a few picoamperes, the noise needed to be below these values. At atmospheric pressure, the noise values were 15 pA for 500 ms, 10 pA for 1 s and around 7 pA for 2 s. This was done by applying a DC offset smaller than the diode threshold voltage, which from Figure 11a is estimated to be around 300 mV, to get small magnitude values, reasonable enough to characterize the noise. These values significantly decreased when the diode was placed in the vacuum chamber and repeated the measurements. At ultra-high vacuum of  $10^{-6} \text{ mbar}$ , the noise effect was ten times smaller, making a time constant of 500 ms enough.

Additionally, at UB we checked the noise was even smaller, reaching values of a few femtoamperes with a  $\tau$  of 3 s. The lock-in amplifier at UB was a different model, thus the time constant values to consider were 300 ms, 1s and 3 s. At 25 K and a time constant of 300 ms, the noise values were 1.3 pA, which can be good enough to obtain Coulomb peaks.

To obtain more precise measurements  $\tau$  can be increased to 1 s. However, this would make the measurement run much more longer, as each new working point would require more than 3 seconds of stabilization time. Therefore, using integration times longer than 1 s is not practical, as the lock-in response time is in reality much longer than the stated  $\tau$ . Thus, an excessive delay would be needed for peak detection, due to their sharpness. It is a good approach, however, to use high integration constants once checking the specific voltage conditions for coulomb blockade. This way, longer measurement times could be applied to obtain much cleaner results.

## 5.6 MOSFET measurements

To further test the instrumentation, we measured MOSFET devices fabricated at IMB-CNM. We conducted three experimental runs on devices from three different wafers, which varied in some steps of the fabrication process and channel lengths, source to drain distance. The MOSFETs on the first wafer had channel lengths of the first wafer had channel lengths of 2  $\mu\text{m}$ , 1  $\mu\text{m}$  and 0.5  $\mu\text{m}$ , while those on the second and third wafer had longer channels of 4  $\mu\text{m}$ , 3  $\mu\text{m}$  and 2  $\mu\text{m}$ .

To verify the proper functioning of the transistors, we used the SDA to perform DC measurements to obtain the I/V characteristic curves. Figure 12 shows one of the devices, which clearly reflects an issue with the gate contact, as shown in Figure 12b shows no gate modulation as we only acquired a noisy signal.

To continue testing the instrumentation we measured MOSFET devices fabricated at IMB-CNM. We conducted three experimental runs for devices of different wafers, differing in the fabrication process and channel lengths. The MOSFETs measured on the first wafer had channel lengths of 2  $\mu\text{m}$ , 1  $\mu\text{m}$  and 0.5  $\mu\text{m}$  while the channel length of the devices of wafer 2 and 3 were designed to be 4  $\mu\text{m}$ , 3  $\mu\text{m}$  and 2  $\mu\text{m}$  long. To check their proper functioning, we used the SDA for DC measurements with the setup of Figure. During the first run, we discovered that the lead gate contact was not properly fabricated, as only noise was measured, see Figure 12b. The only considerable observation was the source-to-drain current due to the punch-through, Figure 12a.

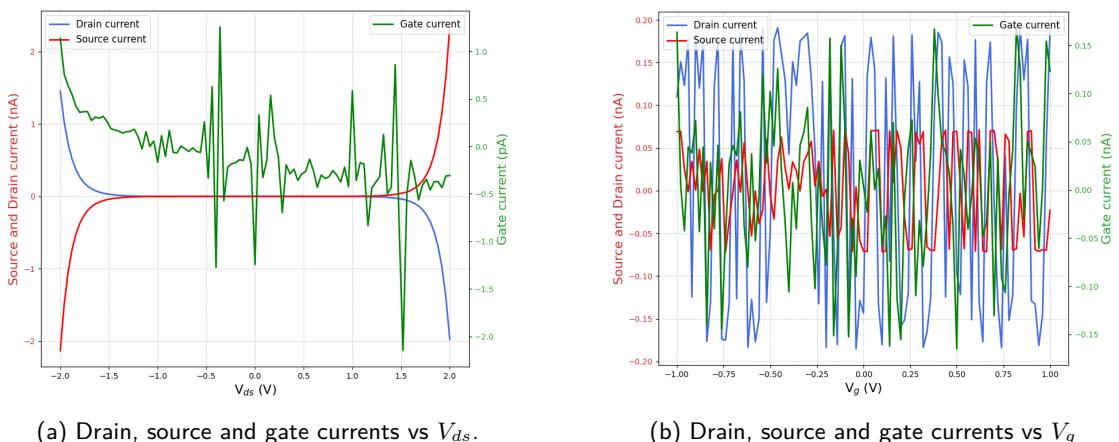


Figure 12: 1  $\mu\text{m}$  channel length MOSFET characteristic curves.

This tells the fabrication process of the lead gate was not correct, and as verified with a SEM, most of the devices of the wafer had no gate contact at the active area. The only significant observation was the source-to-drain current caused by the punch-through,

Figure 12a.

The samples from the second wafer exhibited a good lead gate contact, as current flows through the gate as observed in Figure 13. However, the gate did not properly modulate the current, as a significant amount of current was lost through the gate instead of the drain, as shown in Figure 13b. This could happen due to a perforation of the gate oxide, creating a path for the current flow. However, the most likely hypothesis is that the diffusion areas and the gate were short-circuited during the deposition of the aluminium for the lead gate via sputtering. This technique could leave unwanted metal residues that could not be taken away in the lift-off, creating the possibility of connecting the source and drain with the gate. Figure 13a also shows too high values for the gate current, which reaches the compliance limits set to prevent the device from burning.

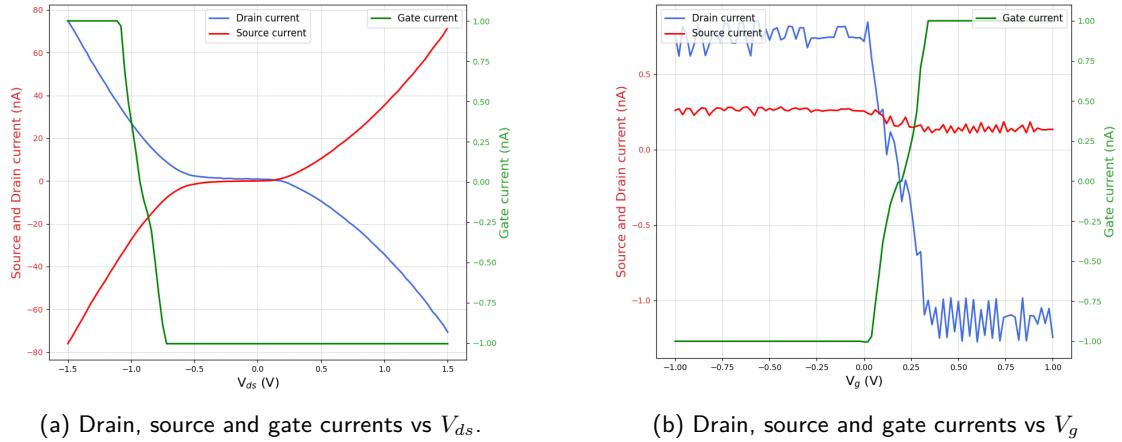


Figure 13: 3  $\mu\text{m}$  channel length MOSFET characteristic curves.

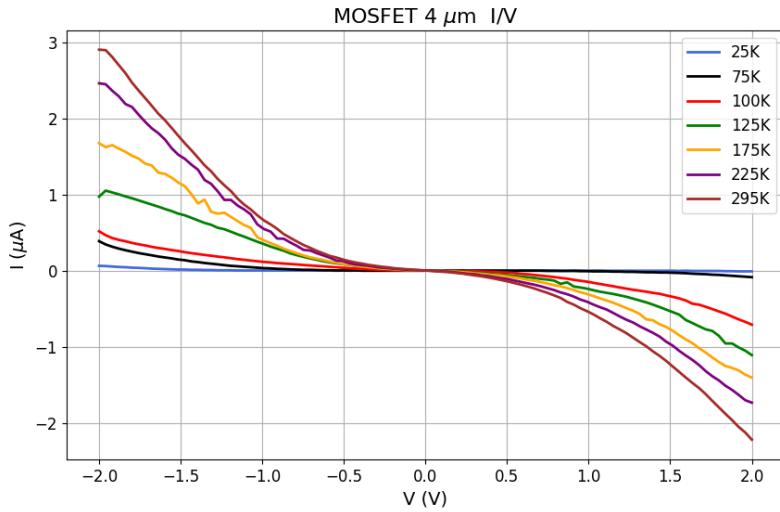


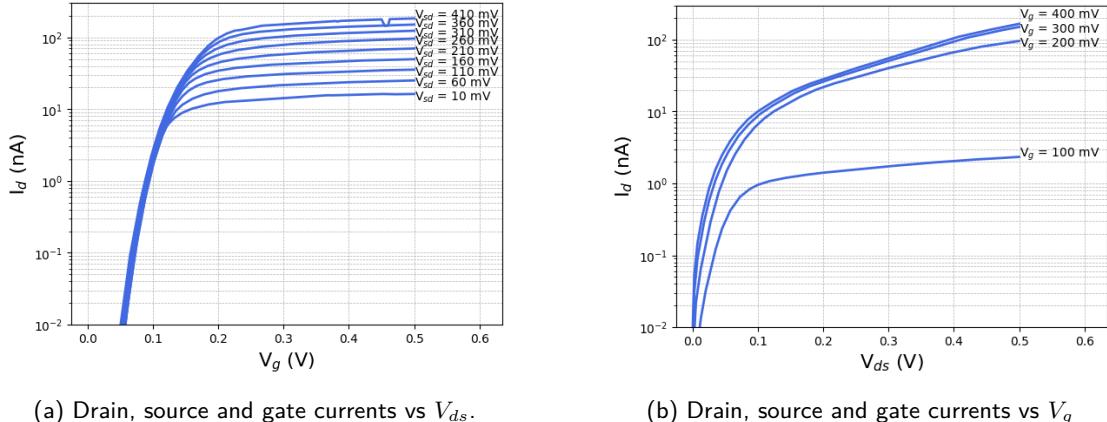
Figure 14:  $V_{ds}$  vs  $I_{ds}$  on a 4  $\mu\text{m}$  channel length MOSFET. The punch-through current is clearly reduced as temperature decreases.

Even though the MOSFETs did not show proper behaviour, they were useful for studying the variation of the punch-through with temperature. The cryostat at UB allows precise temperature control, enabling us to set temperature between 25 K and room temperature.

Using a  $4 \mu\text{m}$  channel MOSFET, we performed source-to-drain voltage sweeps to measure the current flow at the conductance channel. As expected, Figure 14 displays that the current values were significantly lower at low temperatures.

It is important to note that the gate contacts were left in open circuit, resulting in higher current values in comparison with previous measurements. This was due to the socket chip carrier at UB having different pin connection soldering compared with the ones at IMB-CNM. However, this didn't have any effect on our qualitative analysis as the gate does not alter the punch-through.

Considering the observed fabrication errors, another technique was used to place the lead gate, replacing the sputtering with evaporation among other changes. This way, better characteristic curves were measured at the probe station at room temperature. However, due to time constraints, we were unable to get them wire-bonded and conduct the measurements in low temperatures at UB. Consequently, we went to ICMAB, the Institute of Material Sciences of Barcelona, and used their low-temperature probe station, which can be cooled down to 10 K. We performed cryogenic measurements at 13 K. Figure 15 shows the I/V curves for a MOSFET with a  $2 \mu\text{m}$  channel length, operating at low temperatures. The turbomolecular pump to generate the ultra-high vacuum for cryogenization affected the points of the probe station and therefore, placing the points at the pads correctly was not straightforward. Therefore, the collaboration with UB to run cold experiments with wire-bonded chips was crucial to avoid vacuum impurities.



(a) Drain, source and gate currents vs  $V_{ds}$ .

(b) Drain, source and gate currents vs  $V_g$

Figure 15:  $2 \mu\text{m}$  channel length MOSFET characteristic curves.

Taking noise into consideration, the I/V characteristics show good functionality with lead gate sweeps (Figure 15a). When performing  $V_{sd}$  sweeps for different gate voltages, saturation was achieved for low  $V_{gs}$ . For higher values, it could happen that due to punch-through still being too high at low temperatures, caused the device to remain in the ohmic region.

## 5.7 Lock-in MOSFET measurements

Once checked that functional devices were available, we measured the differential conductance with the lock-in to validate the setups for SET characterization. To do so, we prepared the setup at Figure 16. This way, we introduced a small amplitude AC voltage coupled with a varying DC to perform sweeps at the lead gate while maintaining a constant

source to drain voltage.

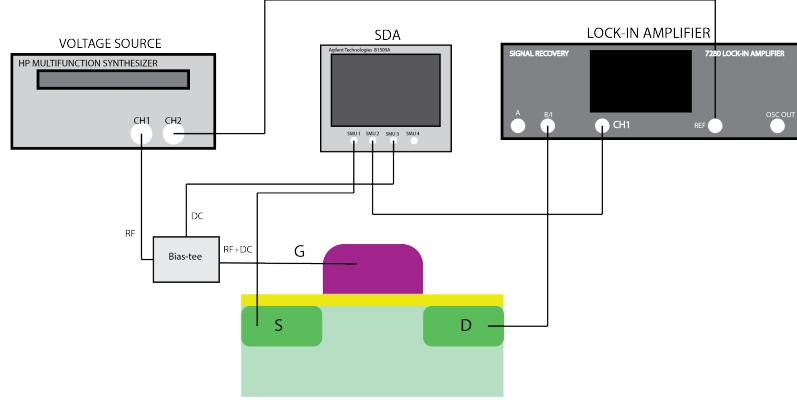


Figure 16: MOSFET characteristics measurement setup.

With this setup, small variations on the gate working point were measured while doing a gate sweep. Ideally, the instrumentation would be connected with a GPIB connection, but there was no time to download the necessary drivers and prepare the corresponding programs, as this was only done for the characterization at UB with different instrumentation. Therefore, even though the function generator allowed setting an offset to the AC signal, it could not be programmed for sweeping. Thus, the AC signal had to be combined with a sweeping DC signal from one of the SMUs of the SDA. This was done using a bias-tee, which could only couple RF signals with frequencies higher than 100 kHz, greatly exceeding the frequency we had probed for low noise. This compromised the measurements slightly, but still provided us with useful information. Figure 17 shows the measured differential current amplitude for gate sweeps with different AC amplitudes. As can be seen, the green plots, representing the DC source currents, are very noisy due to bad contacts of the probes. Figure 17a follows the setup of Figure 16, while the plot in Figure 17b is acquired with a manual gate voltage sweep, set from the HP function generator for  $V_g = [0, 50, 100, 150, 200, 250, 300, 350, 400, 450, 500]\text{mV}$ , to remove the bias-tee and measure the differential current at 171 Hz. In this second case, HP CH1 was directly connected to the gate leaving the corresponding SMU unconnected.

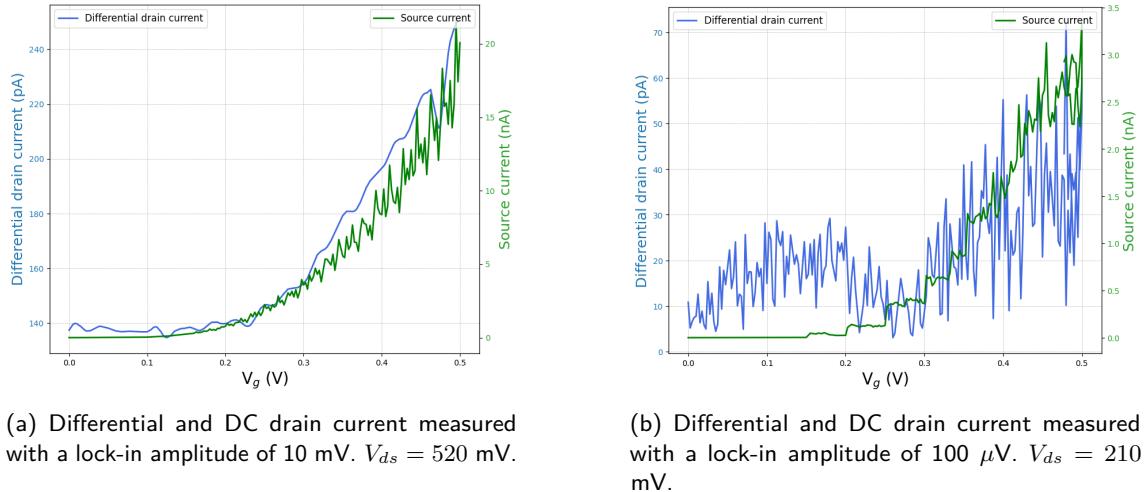


Figure 17: 2  $\mu\text{m}$  channel length MOSFET differential characteristic curves.

The noise levels were too high to properly apply lock-in techniques, as the noise level exceeded the differential slope for small gate voltages. This is why we can see a proper differential plot of the exponentially increasing source current when applying 10 mV amplitude in the AC signal. However, for a lock-in amplitude of 100  $\mu$ V, the noise level is too high, and the increase in current can vaguely be observed. Despite this, the behaviour is expected, with the current increasing with the gate voltage. To solve this issue, better points should be used in the probe station, but since this problem should occur with wire-bonded chips, it does not concern us for the future characterization of SETs.

## 6 SET characterization

The main objective of this master thesis was to prepare the setup for SET characterization, which was achieved and tested with Diode and MOSFETs. However, due to limited time, we were unable to measure a functional single-electron transistor. The SETs based on the architecture of the wafer 3 MOSFETs were not wire bonded before the end of the master thesis. Consequently, the measured SETs, from wafer 1, might not be properly working due to different reasons, and there was time for only measuring six of them. Based on the work done by Angus et al, at [8], we prepared different experimental setup to apply lock-in techniques in order to measure the differential conductance values of the Coulomb peaks.

### 6.1 Barrier conductance

Once the MOSFET architecture of the SETs is confirmed to be functional through DC measurements, the next step is to verify the additional components of the new devices, specifically the barrier gates. This can be done by measuring the conductance through the channel as a function of the barrier voltages to determine the threshold voltages, thereby setting proper barrier voltages for single-electron measurements. We should observe an increase in the conductance once reaching threshold values while setting the lead gate and the other barrier at high voltages to see how the barrier under test modulates the current through the channel. The setup for this test is shown in Figure 18 and the codes can be found on [GitHub](#).

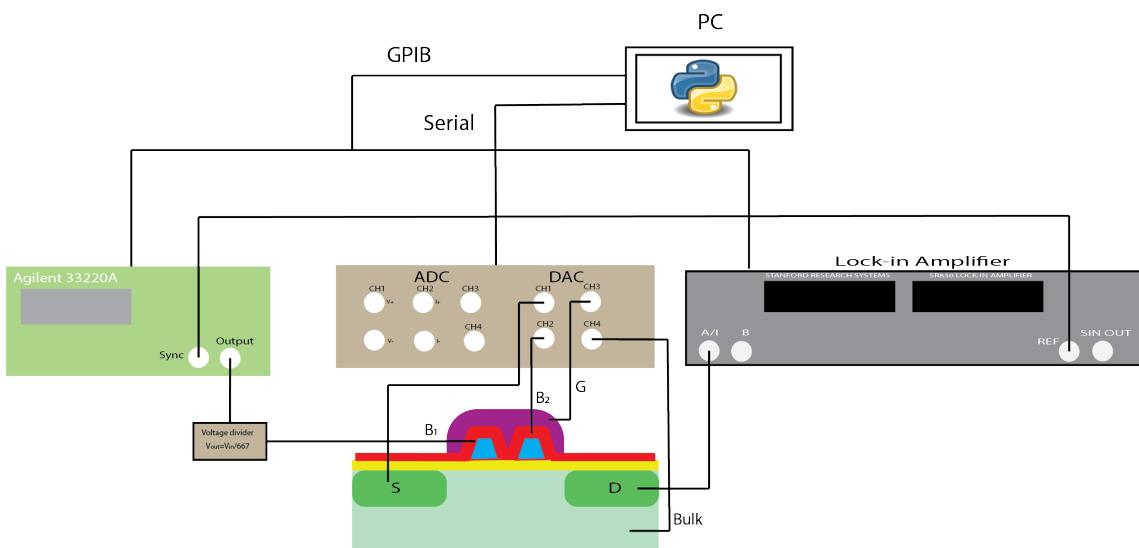


Figure 18: Set-up to measure the barrier conductance.

A  $100 \mu\text{V}$  amplitude and 171 Hz frequency lock-in signal was used to measure the channel conductance while the gate and the other barrier were set at 1.5 V, a voltage higher than the expected threshold but still below levels that could damage the sample. The source-drain voltage was established at 100 mV and the bulk was connected to the ground. However, only noise was measured as observed in Figure 19.

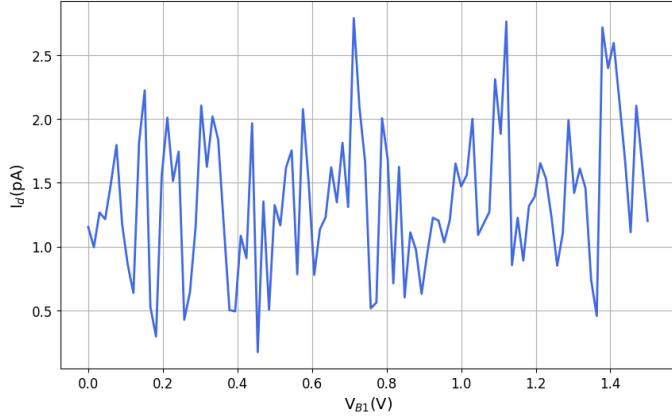


Figure 19: Conductance through the SET dependent on the barrier voltage.

The same run for the other barrier showed nothing but unwanted noise. This indicates that either the barrier contact is not good, possibly due to oxidation processes, or the current is being lost through the substrate or another terminal.

## 6.2 Substrate current

Considering the previous conclusions, we examined the effect the substrate might have on the device and found that most of the current was lost through the substrate. We performed a gate sweep while connecting the barriers and the drain to the ground, setting  $V_s = 100 \text{ mV}$ , and measuring the conductance through the bulk. The setup was similar to Figure 18 but with the AC signal introduced through the gate and the bulk output connected to the lock-in input.

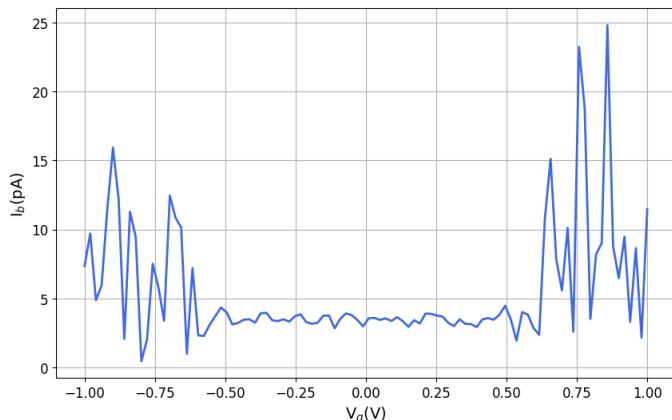


Figure 20: Bulk current as a function of gate voltage.

An interesting result was obtained, as it looked like the current only flowed through the bulk for absolute voltage values higher than 0.6 V. Figure 20 apparently shows a correlation

with the silicon band gap, which for 25 K is 1.169 eV, as approximated by the method proposed in [26]. Considering the non-conducting gap extends approximately from -0.6 V to 0.6 V, this could indeed mean the gate and the semiconductor are short-circuited. It is possibly either because the gate oxide was broken or the gate pads didn't reach the active area, as it happened with the MOSFETs of wafer 1. Additionally, it might happen that the wire bonding was not correct, damaging the field oxide and short-circuiting gate and bulk, observing this semiconducting behaviour.

### 6.3 Coulomb peaks and diamonds

Finally, we designed the setup to try to measure Coulomb peaks and diamonds. First, we established the barrier gates at 400 mV, below the expected threshold voltage that should be obtained from barrier conductance analysis. Then, we configured the setup in Figure 18, but with the AC signal connected to the lead gate and the barrier to the DAC. This way, we performed a 2D voltage sweep, the lead gate was controlled by sweeping the AC offset voltage from 1 to 1.5 and the source voltage with a sweep from -5 mV to 5 mV using the DAC, again based on the experimental runs of [8].

As it can be observed in Figure 21, the initial values at 25 K appeared as noise signals, with no significant changes nor modulation. However, due to an error at the cryostat, which unexpectedly reached 60 K, we observed the magnitude of the current increased some picoamperes. This observation indicated the punch-through effect, considering it was a  $2 \mu\text{m}$  channel length SET, this was completely reasonable.

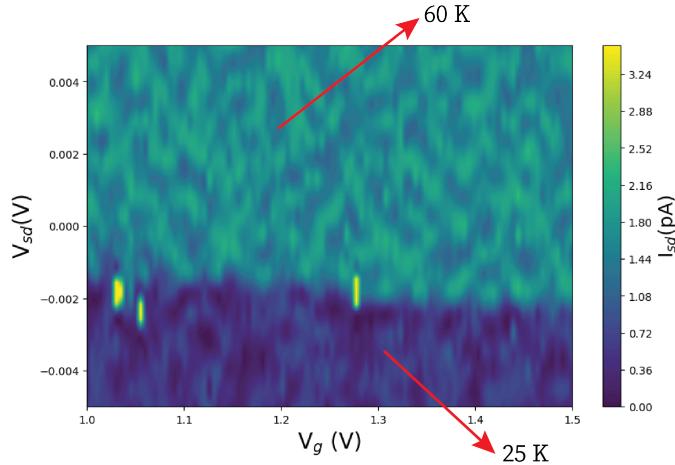


Figure 21: Conductance through the SET dependent of the barrier voltage.

## 7 Conclusion

The proper functioning of the setup has been demonstrated through measurements with diodes and MOSFETs. The setup at UB was proven to be useful, with a noise level around a picoampere, lower than the Coulomb peak height measured at [8], where the magnitude of the differential current was around 6 pA. Moreover, the tests with the diode indicated good noise levels and detection sensitivity. The GPIB and serial connections have also been shown to work properly, as the instrumentation can create and measure signals remotely programmed. Therefore, once the new SETs with good current modulation are fabricated and wire-bonded, the setup will be ready to be used with the programs I wrote in Python. These programs and setups are well documented, so even in my absence, setting up and

running the measurements should not pose a significant problem.

Finally, we were unable to measure a functional SET, which it was expected given that only six samples were tested and the MOSFET architecture of that wafer was not operational. However, this has highlighted the importance of designing and preparing characterization for very sensitive devices. Not getting the expected results might sometimes feel disappointing, as it may seem like a lot of work has been done for nothing. However, throughout the process of my master's thesis, I have realized how important is sometimes to obtain negative results in order to develop well-working devices, especially when dealing with nanodevices, where the fabrication is much more challenging. Observing the MOSFETs we measured, we can see the progress in fabrication: the first wafer didn't even have a proper gate in the active area, the second had it but it was deficient, and finally, the third one showed behaviour close to that of a good MOSFET. In the coming months, similar progress is expected with the SETs. It is already possible to obtain SETs with good gate modulation, but introducing 30 nm thick barriers and oxidizing is not straightforward to achieve on the first try. Nonetheless, by characterizing them properly and correctly identifying which fabrication step can be improved, there is hope to obtain single electron devices fabricated completely at CNM. It is possible that Coulomb peaks may not be observed at 25 K. Nonetheless, some insight into discretization might be gained by comparing the differential conductance at different temperatures, ranging from room temperature down to 25 K. Additionally, I realized that even unexpected errors can provide valuable information, no matter how insignificant it might be seen. For instance, when the cryostat accidentally heated up, I was able to unintentionally observe an increase in the channel current of the SET.

Experimental physics is a fascinating field, particularly for those with a passion for both physics and electronics. The journey, though challenging and sometimes disappointing, is immensely rewarding. It is through these meticulous processes that we gain a deeper understanding and appreciation of the complex details involved. I hope that the setup will eventually measure the Coulomb Diamonds, demonstrating the high-level work done at IMB-CNM and highlighting its potential as a cornerstone for future quantum technologies.

## Bibliography

- [1] Theodore A Fulton and Gerald J Dolan. Observation of single-electron charging effects in small tunnel junctions. *Physical review letters*, 59(1):109, 1987.
- [2] Konstantin K Likharev. Single-electron devices and their applications. *Proceedings of the IEEE*, 87(4):606–632, 1999.
- [3] MA Bounouar, F Calmon, A Beaumont, M Guilmain, W Xuan, S Ecoffey, and D Drouin. Single electron transistor analytical model for hybrid circuit design. In *2011 IEEE 9th International New Circuits and systems conference*, pages 506–509. IEEE, 2011.
- [4] Leo P Kouwenhoven, DG Austing, and Seigo Tarucha. Few-electron quantum dots. *Reports on progress in physics*, 64(6):701, 2001.
- [5] Carlo WJ Beenakker. Theory of coulomb-blockade oscillations in the conductance of a quantum dot. *Physical Review B*, 44(4):1646, 1991.
- [6] Marc A Kastner. The single-electron transistor. *Reviews of modern physics*, 64(3):849, 1992.
- [7] U Meirav, MA Kastner, and SJ Wind. Single-electron charging and periodic conductance resonances in gaas nanostructures. *Physical review letters*, 65(6):771, 1990.
- [8] Susan J Angus, Andrew J Ferguson, Andrew S Dzurak, and Robert G Clark. Gate-defined quantum dots in intrinsic silicon. *Nano letters*, 7(7):2051–2055, 2007.
- [9] Yasuo Takahashi, M Nagase, H Namatsu, K Kurihara, K Iwdate, Y Nakajima, S Horiguchi, K Murase, and M Tabe. Fabrication technique for si single-electron transistor operating at room temperature. *Electronics Letters*, 31(2):136–137, 1995.
- [10] Lei Zhuang, Lingjie Guo, and Stephen Y Chou. Silicon single-electron quantum-dot transistor switch operating at room temperature. *Applied Physics Letters*, 72(10):1205–1207, 1998.
- [11] Ben Rogers, Jesse Adams, and Sumita Pennathur. *Nanotechnology: understanding small systems. Chapter 6*. Crc Press, 2007.
- [12] Yosuke Kayanuma. Quantum-size effects of interacting electrons and holes in semiconductor microcrystals with spherical shape. *Physical Review B*, 38(14):9797, 1988.
- [13] Wenfang Xie. Potential-shape effect on photoionization cross section of a donor in quantum dots. *Superlattices and Microstructures*, 65:271–277, 2014.
- [14] Maud Vinet. The path to scalable quantum computing with silicon spin qubits. *Nature nanotechnology*, 16(12):1296–1298, 2021.
- [15] Daniel Loss and David P DiVincenzo. Quantum computation with quantum dots. *Physical Review A*, 57(1):120, 1998.
- [16] R Maurand, X Jehl, D Kotekar-Patil, A Corna, H Bohuslavskyi, R Laviéville, L Hutin, S Barraud, M Vinet, M Sanquer, et al. A cmos silicon spin qubit. *Nature communications*, 7(1):13575, 2016.
- [17] M Veldhorst, JCC Hwang, CH Yang, AW Leenstra, Bob de Ronde, JP Dehollain, JT Muhonen, FE Hudson, Kohei M Itoh, A t Morello, et al. An addressable quantum dot qubit with fault-tolerant control-fidelity. *Nature nanotechnology*, 9(12):981–985, 2014.
- [18] Floris A Zwanenburg, Andrew S Dzurak, Andrea Morello, Michelle Y Simmons, Lloyd CL Hollenberg, Gerhard Klimeck, Sven Rogge, Susan N Coppersmith, and Mark A Eriksson. Silicon quantum electronics. *Reviews of modern physics*, 85(3):961–1019, 2013.
- [19] Francesco Borsoi, Nico W Hendrickx, Valentin John, Marcel Meyer, Sayr Motz, Floor van Riggelen, Amir Sammak, Sander L de Snoo, Giordano Scappucci, and Menno

- Veldhorst. Shared control of a 16 semiconductor quantum dot crossbar array. *Nature Nanotechnology*, 19(1):21–27, 2024.
- [20] Marco De Michielis, Elena Ferraro, Enrico Prati, Louis Hutin, Benoit Bertrand, Edoardo Charbon, David J Ibberson, and Miguel Fernando Gonzalez-Zalba. Silicon spin qubits from laboratory to industry. *Journal of Physics D: Applied Physics*, 56(36):363001, 2023.
  - [21] Samuel Neyens, Otto K Zietz, Thomas F Watson, Florian Luthi, Aditi Nethewewala, Hubert C George, Eric Henry, Mohammad Islam, Andrew J Wagner, Felix Borjans, et al. Probing single electrons across 300-mm spin qubit wafers. *Nature*, 629(8010):80–85, 2024.
  - [22] Gordon E Moore. Cramming more components onto integrated circuits. *Proceedings of the IEEE*, 86(1):82–85, 1998.
  - [23] Fabien Dubois, Hervé Morel, Dominique Bergogne, and Régis Meuret. Modeling of the punch-through effect in normally-on sic jfet used in high temperature inverter for aerospace application. In *IMAPS, High Temperature Electronics Conference (HITEC)*, pages 154–161, 2012.
  - [24] Michiel de Moor GuanzhongWang, Jouri Bommer. Notes on transport measurements using a lock-in. 2023.
  - [25] Zurich Instruments. Principles of lock-in detection and the state of the art. *White Paper*, 2023.
  - [26] W Bludau, A Onton, and W Heinke. Temperature dependence of the band gap of silicon. *Journal of Applied Physics*, 45(4):1846–1848, 1974.

## A Fabrication of SETs at the IMB-CNM cleanroom

The devices were designed by the Nanonems group and fabricated at the IMB-CNM cleanroom, the largest facility of its kind in Spain. The entire process takes several months, with each step performed at the nanoscale, requiring great precision and complexity. A brief overview of the complete process is provided in Appendix A.

The SETs are fabricated on P-doped silicon wafers, each large enough to accommodate 90 chips, which can be fabricated to be measured at a probe station or by wire bonding. The remaining devices can be measured at a probe station. Figure 29 shows the final aspect of the chips in a simulation performed with KLayout.

The fabrication process begins by defining the alignment marks on the P-doped silicon substrate ( $N_A = 10^{15} \text{ cm}^{-3}$ ) using photolithography and dry etching (2)-(3). These marks are essential for aligning every single lithography level of the process. The next step involves defining the active area. With this objective, a pedestal oxide layer is grown on the substrate (5) to protect it and increase the adhesion of the  $\text{Si}_3\text{N}_4$  layer deposited (6). Afterwards, it will enable to define the active area in the second stage of optical lithography (7). This ensures that part of the  $\text{Si}_3\text{N}_4$  layer protects the active area during the growth of the field oxide through wet thermal oxidation in the next step (10). The field oxide, initially 200 nm thick, will be reduced to 100 nm by the end of the process, providing proper protection for the substrate and isolating it from external electrical stimulus. Finally, the nitride and oxynitride are removed (11)-(12)-(13) of Figure 23. This is a standard semiconductor industry process called LOCOS.

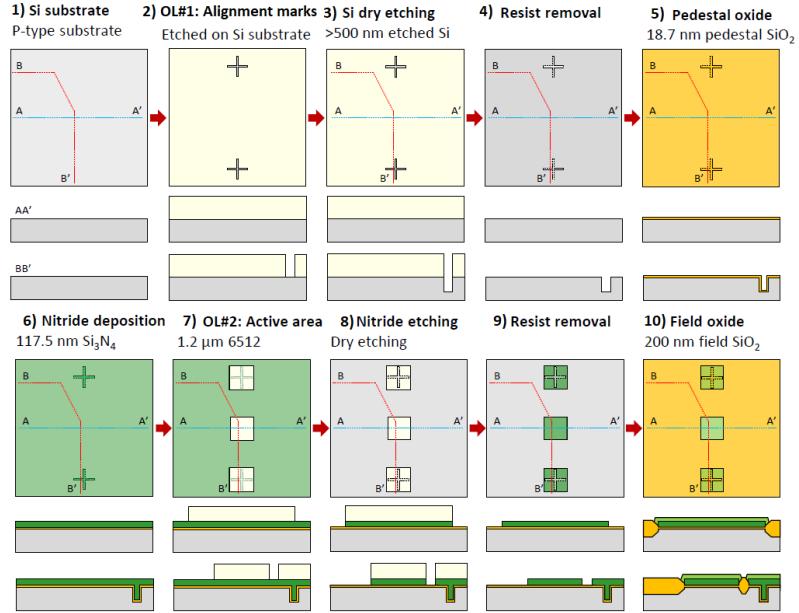


Figure 22: Steps 1-10 of the fabrication process

The next steps involve implanting phosphorus ions ( $N_D = 4.2 \cdot 10^{15} \text{ cm}^{-3}$ ) at 50 keV. To achieve a homogeneous N region around the MOS oxide, a sacrificial oxide layer is grown before (14). This layer modulates the scattering of the phosphorus ions, preventing them from penetrating too sharply into the semiconductor and protecting the silicon from a

chaotic etching by ion bombardment. Photolithography is used again to define the regions of interest (15), protecting the rest of the device with optical resist. This lithography is very important as the length of the S-D channel is defined before the implantation (16). The sacrificial oxide is then removed (18) to allow for the growth of a thinner 6.5 nm gate oxide (19). This oxidation is also used to activate the implanted dopants.

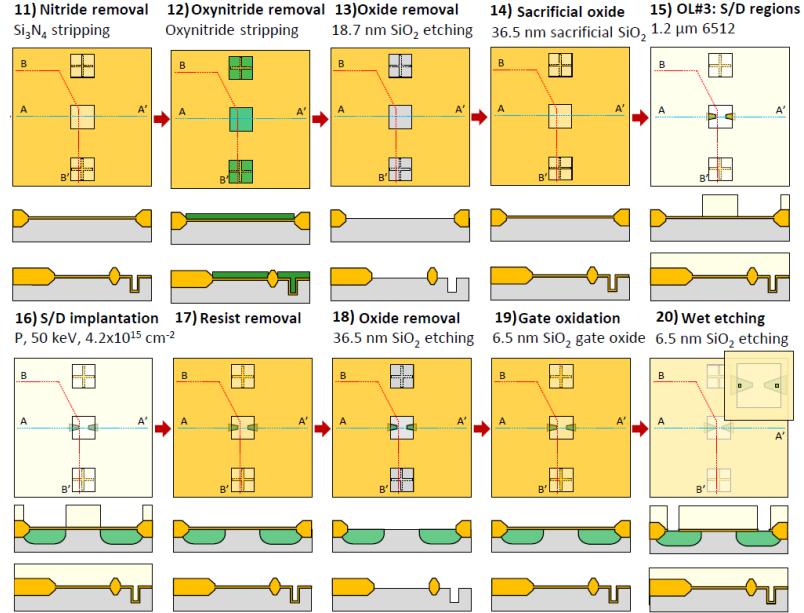


Figure 23: Steps 11 to 20 of the fabrication process

Next, the source/drain (S/D) contacts are opened by photolithography and wet etching (20), followed by the deposition of aluminium through evaporation. This process is performed twice: first, the contact windows are opened at the S/D regions and afterwards, these contacts are connected to the fabricated pads, far from the gate oxide. The aluminium that remains on the optical resist is removed by lift-off (21)-(22)-(23).

At this stage, a decision must be made whether the final device will be a MOSFET or a SET. For MOSFET devices, only the final metallic gate needs to be added, which is done using photolithography and aluminium evaporation (24)-(25).

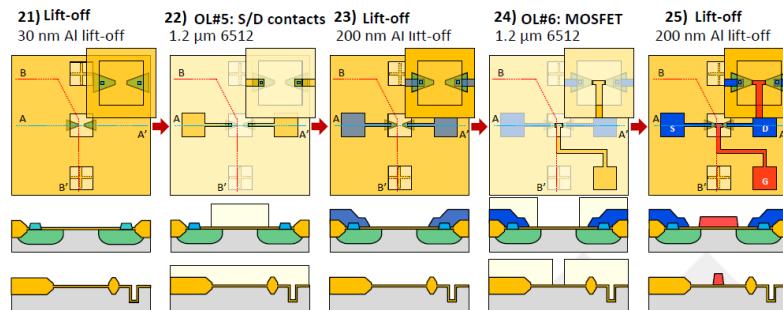


Figure 24: Steps 21 to 25 of the fabrication process

On the other hand, additional steps are required to create a SET. The potential barriers

are too thin to be defined through photolithography, so EBL techniques are applied. This involves depositing two 30 nm thin layers of aluminium via evaporation on top of the S-D channel (27)(28)-(29). These barriers need to be electrically isolated, which is achieved by covering them with an Atomic Layer Deposition (ALD) of 5 nm of  $\text{Al}_2\text{O}_3$  as a dielectric (30). A second metal deposition is then used to create the lead gate of the device (31)-(32)-(33). Finally, a third EBL process takes place (34), as the ALD step grows oxide in the source and drain contacts and over the pads of the barrier contacts. The oxide is taken out by reactive ion etching (RIE) (35) and finally, a third metal deposition is performed on the pads to ensure metallic contacts are the proper ones and to fit with the wire bonding requirements as a thicker metal layer is needed (36)-(37).

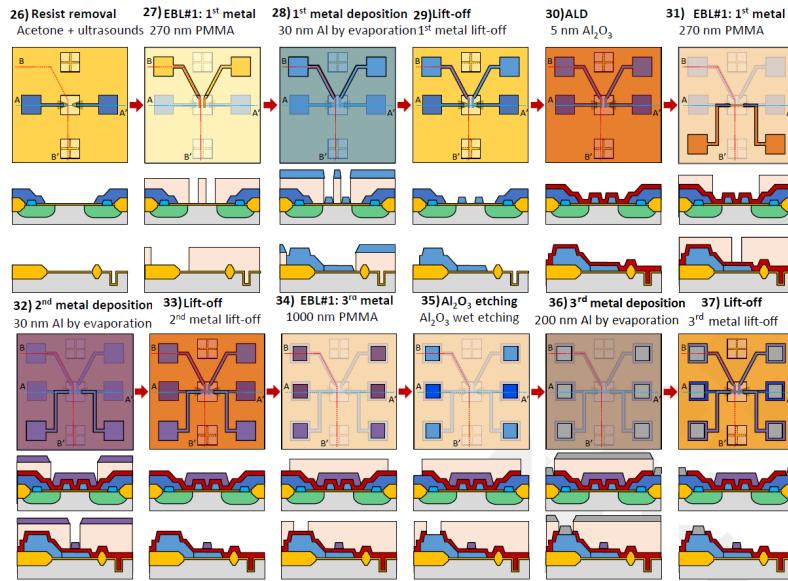


Figure 25: Steps 26 to 37 of the fabrication process

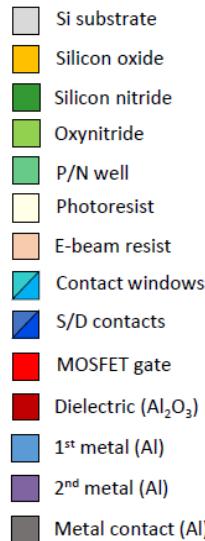


Figure 26: List of the corresponding materials with their colors in Figures 22, 23, 24, 25.

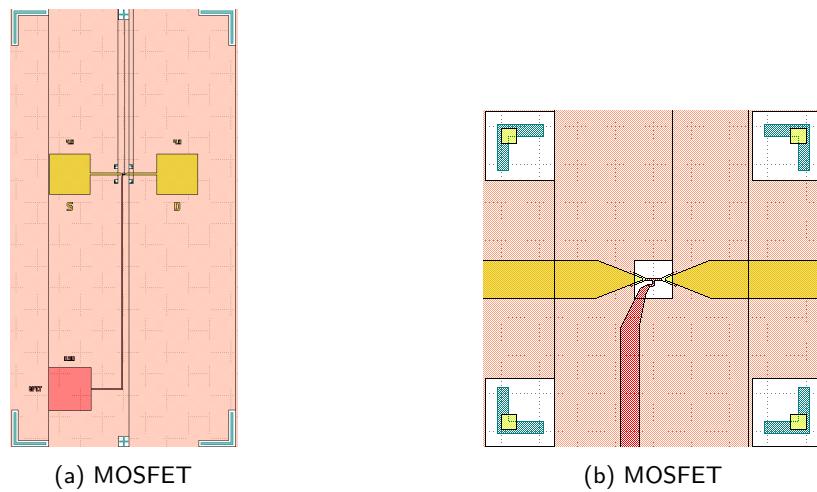


Figure 27: a) Scheme of the typical MOSFET and b) Scheme for the SETs we will characterize

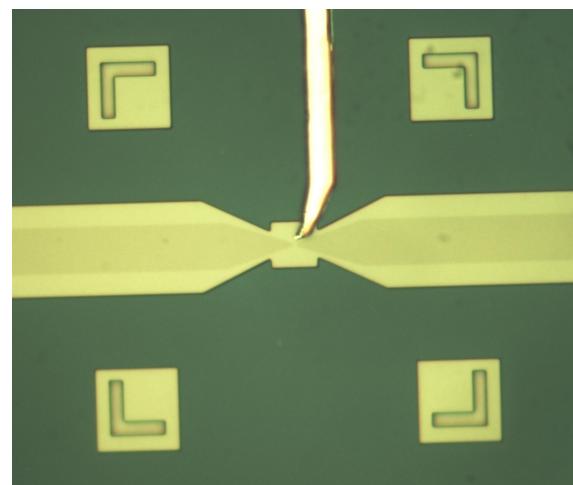


Figure 28: Active area of the MOSFETs imaged with an optical microscope.

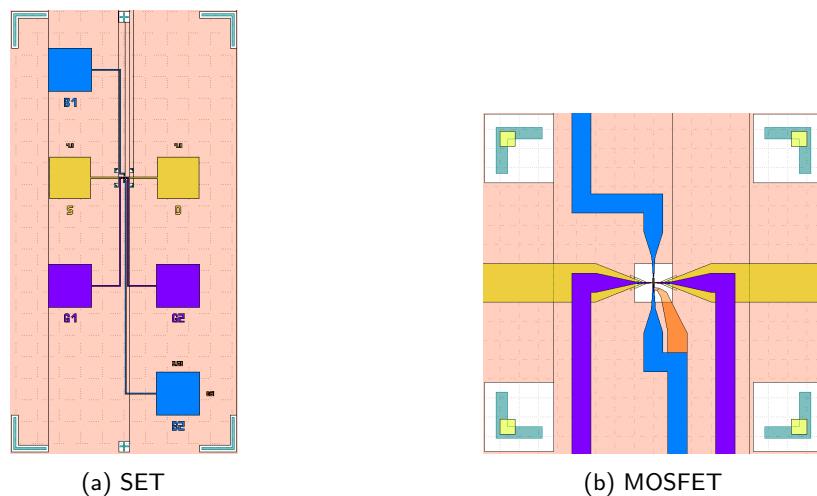


Figure 29: a) Scheme of the typical MOSFET and b) Scheme for the SETs we will characterize

## B Code for the characterization setup

The main code for the characterization can be found on my [GitHub repository](#). The instrumentation is connected to the PC via GPIB connections, except the DAC-ADC, which is done via serial connection as it has a central Arduino Due to operating with the evaluation boards. The drivers for the Arduino have been slightly modified and must be uploaded to the Arduino before starting the measurements at Python scripts unless we are using the same DAC-ADC which already has the drivers uploaded. Qcodes libraries have been implemented to create the stations and datasets. Additionally, it allows us to perform live date measurements with *plottr-inspectr* and very comfortable data management. The GitHub repository contains a README that further explains each file, however, the functions and most of the lines are explained with comments in the files.