RTL IP's
EDA Tools ⟩ — & ⟩ — ASIC
PDKs

EDA Tools
- aflow
- OpenRoad
- OpenLane

→ ASIC ← PDK data

RTL Designs
opencores.org
github.com

AGE of GODS: design of an IC was tightly coupled with in manufacturing process available :)

Ti intel Fairchild

structured design methodology based on λ rules

Lynn Conway and Carver Mead

PDK - Process Design Kit

interface b/w fab & designers :)

FAB

EDA tools

DRC
LVS
PEX

Device models
standard cell Library
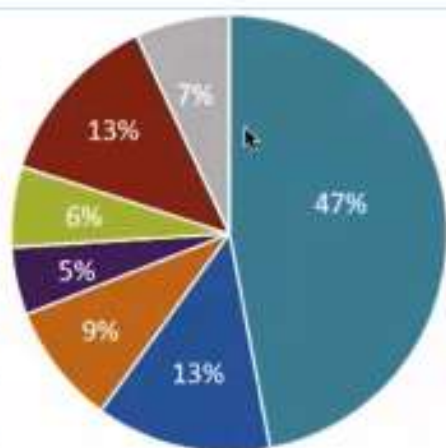
IC
Designers

Process Design Kit

These PDKs are distributed under Non-Disclosure gA reement

Google + SKYWATER Technology

FOSS 130nm Production PDK - Jun30,2020

130nm OLD ?

→ 6% market share (2019)

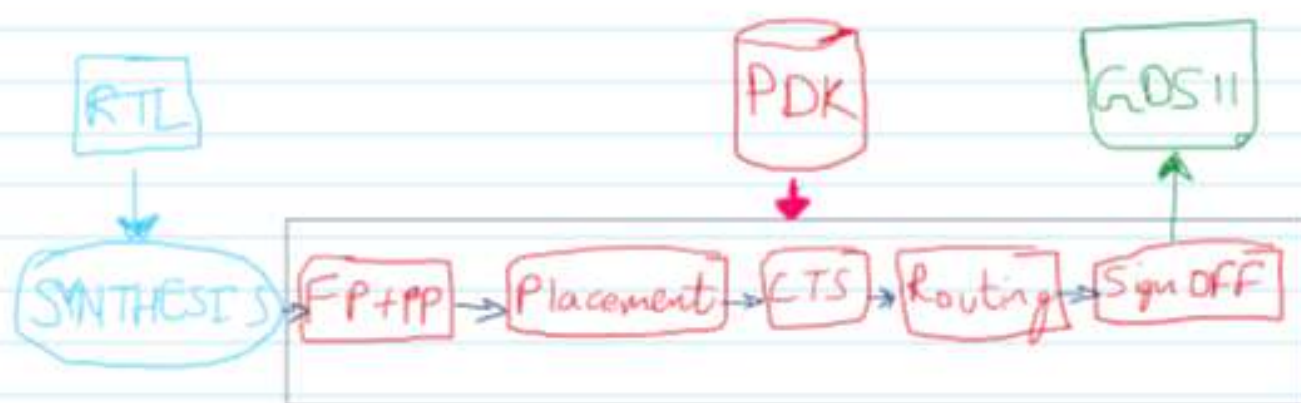→ Don't need much performance for every application

→ Cost cutting as high process nodes requires more sophisticated manufacturing machines.

Intel Pentium @ 3.46GHz
130nm

HURRAY! Lets design an IC ourself 😊
☒ Its really Complicated 😐

RTL to GDSII

Flow to achieve a proper layout that could be sent to Fab :)

RTL → SYNTHESIS
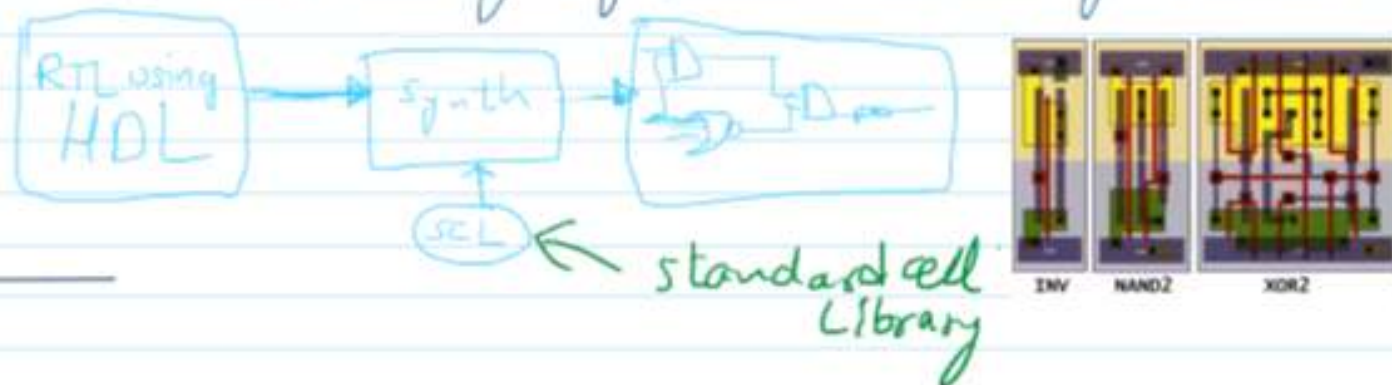
PDK

GDSII

FP+PP → Placement → CTS → Routing → Sign OFF
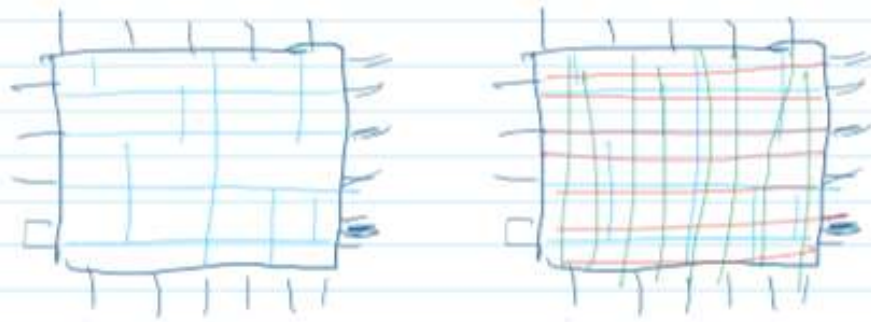
Why end stage in the flow is sign off
Why not Layout

Interpretation: After going through entire RTL-GDSII flow, an IC design is tested for proper timing, power consumption, signal integrity, DRC etc, thus confirming its appropriate functionality acc to specs.
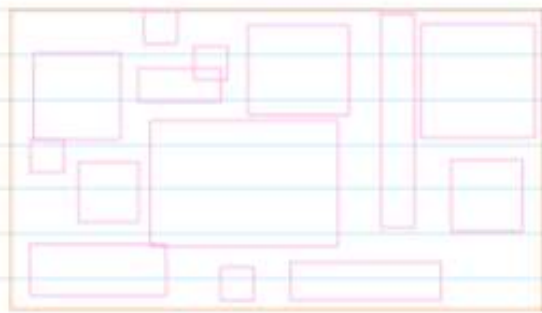
Layout information is sent in Binary file GDSII Graphic Design System II which can be understood by Fab manufacturing equipment interfaced by software
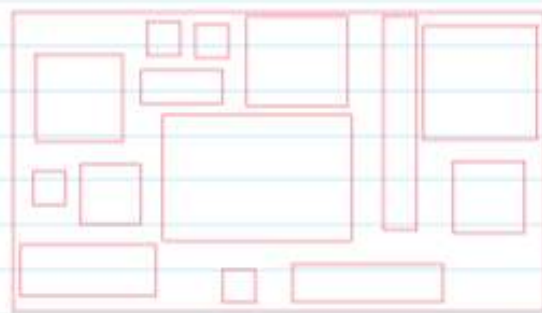
RTL using HDL → synth →

SCL ← standard cell Library

INV   NAND2   XOR2

Floor Planning + Power Planning
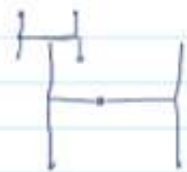

Placement

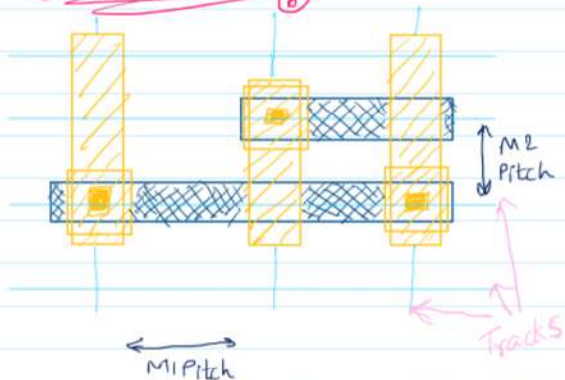Global Placement
(optimal Places for cells)

Detailed Placement
(altered a bit)

Clock Tree Synthesis (CTS):

→ deliver clock to all sequential elmnts (FF)
→ with min. skew (arrival of clock signal @ diff elmnts)
→ good shape (H tree, X tree, Wishbone)

ROUTing:

M2 Pitch

M1 Pitch

Tracks

→ Metal tracks form routing grid
→ Routing grid is Huge
  ↳ Global Route
  ↳ Detailed Route : actual wiring

Sign OFF:-

→ Physical Verification
  i) Design Rule Checking (DRC)
  2) Layout vs Schematic (LVS)

→ STA Analysis (Timing)

Open Lane:

Being everything together in one place where all the necessary open EDA tools like openSTA, magic, netgenetc, are aligned in a flow. Thus, achieving automated RTL to GDS ▯ flow

WORK → tools → openlane_workingdir → open pdk

↳ Skywater 130 is a_pdk; it supports only Commercial tools!

open_pdk makes skywater pDk compatible with openEDA tools by using some scripts

for this
Skywater pdk ──→ sky130A
diff variant

pdks/sky130A   -ls
↓
↳ libs.tech   ←(tools)
↳ libs.ref
   sky130_fd_sc_hd
        foundry ↓   highdensity
             standard
             cell

docker?

Run applications or even "OS" on a host OS

To get openlane interactive features, we use docker!

less config.td

bypasses any older configurations

DAY1

Openlane directory structure:

```
vsduser@vsdsquadron:~/Desktop/work/tools$ clear

vsduser@vsdsquadron:~/Desktop/work/tools$ ls
openlane_working_dir    vsdflow
vsduser@vsdsquadron:~/Desktop/work/tools$ cd openlane_working_dir/
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir$ ls
openlane  openlane_old  pdks
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir$ cd pdks/
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/pdks$ ls
open_pdks  sky130A  skywater-pdk
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/pdks$ cd sky130A/
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/pdks/sky130A$ ls
libs.ref  libs.tech  SOURCES
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/pdks/sky130A$ cd libs.ref/
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.ref$ ls -ltr
total 48
drwxr-xr-x 10 vsduser docker 4096 Jun 28  2021 sky130_osu_sc_t18
drwxr-xr-x 12 vsduser docker 4096 Jun 28  2021 sky130_fd_sc_ms
drwxr-xr-x 12 vsduser docker 4096 Jun 28  2021 sky130_fd_sc_ls
drwxr-xr-x 12 vsduser docker 4096 Jun 28  2021 sky130_fd_sc_hs
drwxr-xr-x 12 vsduser docker 4096 Jun 28  2021 sky130_fd_sc_hdll
drwxr-xr-x  8 vsduser docker 4096 Jun 28  2021 sky130_fd_pr
drwxr-xr-x  9 vsduser docker 4096 Jun 28  2021 sky130_sram_macros
drwxr-xr-x 12 vsduser docker 4096 Jun 28  2021 sky130_fd_sc_hvl
drwxr-xr-x 11 vsduser docker 4096 Jun 28  2021 sky130_fd_io
drwxr-xr-x  4 vsduser docker 4096 Jun 28  2021 sky130_ml_xx_hd
drwxr-xr-x 12 vsduser docker 4096 Jun 28  2021 sky130_fd_sc_lp
drwxr-xr-x 12 vsduser docker 4096 Jun 28  2021 sky130_fd_sc_hd
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.ref$ cd ../
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/pdks/sky130A$ cd libs.tech/
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.tech$ ls -ltr
total 36
drwxr-xr-x  9 vsduser docker 4096 Jun 28  2021 xschem
drwxr-xr-x  2 vsduser docker 4096 Jun 28  2021 xcircuit
drwxr-xr-x  2 vsduser docker 4096 Jun 28  2021 gflow
drwxr-xr-x 10 vsduser docker 4096 Jun 28  2021 openlane
drwxr-xr-x  2 vsduser docker 4096 Jun 28  2021 ngspice
drwxr-xr-x  2 vsduser docker 4096 Jun 28  2021 netgen
```

```
drwxr-xr-x  2 vsduser docker 4096 Jun 28  2021 irsim
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.tech$ cd ../
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/pdks/sky130A$ ls
libs.ref  libs.tech  SOURCES
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/pdks/sky130A$ cd libs.re
bash: cd: libs.re: No such file or directory
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/pdks/sky130A$ cd libs.ref
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.ref$ ls
sky130_fd_io   sky130_fd_sc_hd   sky130_fd_sc_hs   sky130_fd_sc_lp  sky130_fd_sc_ms  sky130_osu_sc_t18
sky130_fd_pr   sky130_fd_sc_hdll  sky130_fd_sc_hvl  sky130_fd_sc_ls  sky130_ml_xx_hd  sky130_sram_macros
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.ref$ cd sky130_fd_sc_hd
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.ref/sky130_fd_sc_hd$ ls
cdl  doc  gds  lef  lib  mag  maglef  spice  techlef  verilog
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.ref/sky130_fd_sc_hd$ cd lib/
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.ref/sky130_fd_sc_hd/lib$ ls
sky130_fd_sc_hd__ff_100C_1v65.lib              sky130_fd_sc_hd__ff_n40C_1v95.lib  sky130_fd_sc_hd__ss_n40C_1v44.lib
sky130_fd_sc_hd__ff_100C_1v95.lib              sky130_fd_sc_hd__ss_100C_1v40.lib  sky130_fd_sc_hd__ss_n40C_1v60_ccsnoise.lib
sky130_fd_sc_hd__ff_n40C_1v56.lib              sky130_fd_sc_hd__ss_100C_1v60.lib  sky130_fd_sc_hd__ss_n40C_1v76.lib
sky130_fd_sc_hd__ff_n40C_1v65.lib              sky130_fd_sc_hd__ss_n40C_1v28.lib  sky130_fd_sc_hd__tt_025C_1v80.lib
sky130_fd_sc_hd__ff_n40C_1v76.lib              sky130_fd_sc_hd__ss_n40C_1v35.lib  sky130_fd_sc_hd__tt_025C_1v80.lib
sky130_fd_sc_hd__ff_n40C_1v95_ccsnoise.lib     sky130_fd_sc_hd__ss_n40C_1v40.lib  sky130_fd_sc_hd__tt_100C_1v80.lib
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.ref/sky130_fd_sc_hd/lib$ cd ../
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.ref/sky130_fd_sc_hd$ ls ltr
ls: cannot access 'ltr': No such file or directory
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.ref/sky130_fd_sc_hd$ ls -ltr
total 88
drwxr-xr-x 2 vsduser docker  4096 Jun 28  2021 verilog
drwxr-xr-x 2 vsduser docker  4096 Jun 28  2021 techlef
drwxr-xr-x 2 vsduser docker  4096 Jun 28  2021 spice
drwxr-xr-x 2 vsduser docker 28672 Jun 28  2021 maglef
drwxr-xr-x 2 vsduser docker 28672 Jun 28  2021 mag
drwxr-xr-x 2 vsduser docker  4096 Jun 28  2021 lib
drwxr-xr-x 2 vsduser docker  4096 Jun 28  2021 lef
drwxr-xr-x 2 vsduser docker  4096 Jun 28  2021 gds
drwxr-xr-x 2 vsduser docker  4096 Jun 28  2021 doc
drwxr-xr-x 2 vsduser docker  4096 Jun 28  2021 cdl
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.ref/sky130_fd_sc_hd$ cd lef/
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.ref/sky130_fd_sc_hd/lef$ ls
```

```
sky130_fd_sc_hd__ff_100C_1v65.lib          sky130_fd_sc_hd__ff_n40C_1v95.lib   sky130_fd_sc_hd__ss_n40C_1v44.lib
sky130_fd_sc_hd__ff_100C_1v95.lib          sky130_fd_sc_hd__ss_100C_1v40.lib   sky130_fd_sc_hd__ss_n40C_1v60_ccsnoise.lib
sky130_fd_sc_hd__ff_n40C_1v56.lib          sky130_fd_sc_hd__ss_100C_1v60.lib   sky130_fd_sc_hd__ss_n40C_1v60.lib
sky130_fd_sc_hd__ff_n40C_1v65.lib          sky130_fd_sc_hd__ss_n40C_1v28.lib   sky130_fd_sc_hd__ss_n40C_1v76.lib
sky130_fd_sc_hd__ff_n40C_1v76.lib          sky130_fd_sc_hd__ss_n40C_1v35.lib   sky130_fd_sc_hd__tt_025C_1v80.lib
sky130_fd_sc_hd__ff_n40C_1v95_ccsnoise.lib  sky130_fd_sc_hd__ss_n40C_1v40.lib   sky130_fd_sc_hd__tt_100C_1v80.lib
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.ref/sky130_fd_sc_hd/lib$ cd ../
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.ref/sky130_fd_sc_hd$ ls ltr
ls: cannot access 'ltr': No such file or directory
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.ref/sky130_fd_sc_hd$ ls -ltr
total 88
drwxr-xr-x 2 vsduser docker  4096 Jun 28  2021 verilog
drwxr-xr-x 2 vsduser docker  4096 Jun 28  2021 techlef
drwxr-xr-x 2 vsduser docker  4096 Jun 28  2021 spice
drwxr-xr-x 2 vsduser docker 28672 Jun 28  2021 maglef
drwxr-xr-x 2 vsduser docker 28672 Jun 28  2021 mag
drwxr-xr-x 2 vsduser docker  4096 Jun 28  2021 lib
drwxr-xr-x 2 vsduser docker  4096 Jun 28  2021 lef
drwxr-xr-x 2 vsduser docker  4096 Jun 28  2021 gds
drwxr-xr-x 2 vsduser docker  4096 Jun 28  2021 doc
drwxr-xr-x 2 vsduser docker  4096 Jun 28  2021 cdl
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.ref/sky130_fd_sc_hd$ cd lef/
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.ref/sky130_fd_sc_hd/lef$ ls
sky130_ef_sc_hd__decap_12.lef  sky130_ef_sc_hd__fakediode_2.lef  sky130_ef_sc_hd__fill_12.lef  sky130_fd_sc_hd.lef
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.ref/sky130_fd_sc_hd/lef$ cd ../
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.ref/sky130_fd_sc_hd$ cd techlef/
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.ref/sky130_fd_sc_hd/techlef$ ls -ltr
total 20
-rwxr-xr-x 1 vsduser docker 18007 Jun 28  2021 sky130_fd_sc_hd.tlef
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.ref/sky130_fd_sc_hd/techlef$ cd ../../../../
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/pdks$ cd ../
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir$ ls -ltr
total 12
drwxr-xr-x  5 vsduser docker 4096 Jun 28  2021 pdks
drwxr-xr-x 10 vsduser docker 4096 Jun 29  2021 openlane_old
drwxr-xr-x 10 vsduser docker 4096 May 20  2023 openlane
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir$ cd openlane
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$
```

```
# Design
set ::env(DESIGN_NAME) "picorv32a"

set ::env(VERILOG_FILES) "./designs/picorv32a/src/picorv32a.v"
set ::env(SDC_FILE) "./designs/picorv32a/src/picorv32a.sdc"

set ::env(CLOCK_PERIOD) "5.000"
set ::env(CLOCK_PORT) "clk"


set ::env(CLOCK_NET) $::env(CLOCK_PORT)



set filename $::env(OPENLANE_ROOT)/designs/$::env(DESIGN_NAME)/$::env(PDK)_$::env(STD_CELL_LIBRARY)_config.tcl
if { [file exists $filename] == 1} {
        source $filename
}
config.tcl (END)
```

File Edit View Search Terminal Tabs Help

vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane ×   vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlan... ×

```
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$ docker
bash-4.2$
bash-4.2$ pwd
/openLANE_flow
bash-4.2$ ls -ltr
total 136
drwxr-xr-x 15 1000   997   4096 Jun 29  2021 scripts
-rw-r--r--  1 1000   997  20787 Jun 29  2021 run_designs.py
-rw-r--r--  1 1000   997   7898 Jun 29  2021 report_generation_wrapper.py
drwxr-xr-x  3 1000   997   4096 Jun 29  2021 regression_results
-rwxr-xr-x  1 1000   997   6519 Jun 29  2021 flow.tcl
drwxr-xr-x  5 1000   997   4096 Jun 29  2021 docs
drwxr-xr-x  5 1000   997   4096 Jun 29  2021 docker_build
drwxr-xr-x 44 1000   997   4096 Jun 29  2021 designs
drwxr-xr-x  2 1000   997   4096 Jun 29  2021 configuration
-rw-r--r--  1 1000   997   5514 Jun 29  2021 conf.py
-rwxr-xr-x  1 1000   997    966 Jun 29  2021 clean_runs.tcl
-rw-r--r--  1 1000   997  25509 Jun 29  2021 README.md
-rw-r--r--  1 1000   997   7273 Jun 29  2021 Makefile
-rw-r--r--  1 1000   997  11350 Jun 29  2021 LICENSE
-rw-r--r--  1 1000   997   1285 Jun 29  2021 CONTRIBUTING.md
-rw-r--r--  1 1000   997    709 Jun 29  2021 AUTHORS.md
-rw-r--r--  1 1000  1000    963 May 19  2023 default.cvcrc
bash-4.2$ ./flow.tcl -interactive
[INFO]:
```

(OPENLANE ASCII art banner)

```
[INFO]: Version: v0.21
[INFO]: Running interactively
% package require openlane 0.9
```

```
% package require openlane 0.9
0.9
% prep -design picorv32a
[INFO]: Using design configuration at /openLANE_flow/designs/picorv32a/config.tcl
[INFO]: Sourcing Configurations from /openLANE_flow/designs/picorv32a/config.tcl
[INFO]: PDKs root directory: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks
[INFO]: PDK: sky130A
[INFO]: Setting PDKPATH to /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A
[INFO]: Standard Cell Library: sky130_fd_sc_hd
[INFO]: Sourcing Configurations from /openLANE_flow/designs/picorv32a/config.tcl
[INFO]: Current run directory is /openLANE_flow/designs/picorv32a/config.tcl
[INFO]: Preparing LEF Files
[INFO]: Extracting the number of available metal layers from /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.
ref/sky130_fd_sc_hd/techlef/sky130_fd_sc_hd.tlef
[INFO]: The number of available metal layers is 6
[INFO]: The available metal layers are li1 met1 met2 met3 met4 met5
[INFO]: Merging LEF Files...
mergeLef.py : Merging LEFs
 sky130_fd_sc_hd.lef: SITEs matched found: 0
 sky130_fd_sc_hd.lef: MACROs matched found: 437
 sky130_ef_sc_hd__fill_12.lef: SITEs matched found: 0
 sky130_ef_sc_hd__fill_12.lef: MACROs matched found: 1
 sky130_ef_sc_hd__decap_12.lef: SITEs matched found: 0
 sky130_ef_sc_hd__decap_12.lef: MACROs matched found: 1
 sky130_ef_sc_hd__fakediode_2.lef: SITEs matched found: 0
 sky130_ef_sc_hd__fakediode_2.lef: MACROs matched found: 1
mergeLef.py : Merging LEFs complete
[INFO]: Trimming Liberty...
[INFO]: Generating Exclude List...
[INFO]: Storing configs into config.tcl ...
[INFO]: Preparation complete
%
```

Q Search

ENG

```
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs$ cd picorv32a/
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a$ ls -ltr
total 28
drwxr-xr-x 2 vsduser docker 4096 Jun 29  2021 src
-rw-r--r-- 1 vsduser docker  209 Jun 29  2021 sky130A_sky130_fd_sc_ms_config.tcl
-rw-r--r-- 1 vsduser docker  209 Jun 29  2021 sky130A_sky130_fd_sc_ls_config.tcl
-rw-r--r-- 1 vsduser docker  209 Jun 29  2021 sky130A_sky130_fd_sc_hs_config.tcl
-rw-r--r-- 1 vsduser docker  209 Jun 29  2021 sky130A_sky130_fd_sc_hdll_config.tcl
-rwxr-xr-x 1 vsduser docker  209 Jun 29  2021 sky130A_sky130_fd_sc_hd_config.tcl
-rwxr-xr-x 1 vsduser docker  444 Jun 29  2021 config.tcl
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a$ less config.tcl
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a$ less  sky130A_sky130_fd_sc_hd_config.tcl
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a$ cd ../../
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$ cd designs/picorv32a/
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a$ clear

vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a$ ls -ltr
total 28
drwxr-xr-x 2 vsduser docker 4096 Jun 29  2021 src
-rw-r--r-- 1 vsduser docker  209 Jun 29  2021 sky130A_sky130_fd_sc_ms_config.tcl
-rw-r--r-- 1 vsduser docker  209 Jun 29  2021 sky130A_sky130_fd_sc_ls_config.tcl
-rw-r--r-- 1 vsduser docker  209 Jun 29  2021 sky130A_sky130_fd_sc_hs_config.tcl
-rw-r--r-- 1 vsduser docker  209 Jun 29  2021 sky130A_sky130_fd_sc_hdll_config.tcl
-rwxr-xr-x 1 vsduser docker  209 Jun 29  2021 sky130A_sky130_fd_sc_hd_config.tcl
-rwxr-xr-x 1 vsduser docker  444 Jun 29  2021 config.tcl
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a$ ls -ltr
total 32
drwxr-xr-x 2 vsduser docker  4096 Jun 29  2021 src
-rw-r--r-- 1 vsduser docker   209 Jun 29  2021 sky130A_sky130_fd_sc_ms_config.tcl
-rw-r--r-- 1 vsduser docker   209 Jun 29  2021 sky130A_sky130_fd_sc_ls_config.tcl
-rw-r--r-- 1 vsduser docker   209 Jun 29  2021 sky130A_sky130_fd_sc_hs_config.tcl
-rw-r--r-- 1 vsduser docker   209 Jun 29  2021 sky130A_sky130_fd_sc_hdll_config.tcl
-rwxr-xr-x 1 vsduser docker   209 Jun 29  2021 sky130A_sky130_fd_sc_hd_config.tcl
-rwxr-xr-x 1 vsduser docker   444 Jun 29  2021 config.tcl
drwxr-xr-x 3 vsduser vsduser 4096 Apr 26 17:05 runs
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a$
```



```
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This is free software, and you are free to change and redistribute it
under certain conditions; type `show_copying' for details.
This program comes with ABSOLUTELY NO WARRANTY; for details type `show_warranty'.
Warning: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.ref/sky130_fd_sc_hd/lib/sky130_fd_sc_hd__ff_n40C_1v9
5.lib line 31, default_operating_condition ff_n40C_1v95 not found.
Warning: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.ref/sky130_fd_sc_hd/lib/sky130_fd_sc_hd__ss_100C_1v6
0.lib line 32, default_operating_condition ss_100C_1v60 not found.
create_clock [get_ports $::env(CLOCK_PORT)]  -name $::env(CLOCK_PORT)  -period $::env(CLOCK_PERIOD)
set input_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
set output_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
puts "\[INFO\]: Setting output delay to: $output_delay_value"
[INFO]: Setting output delay to: 4.946000000000001
puts "\[INFO\]: Setting input delay to: $input_delay_value"
[INFO]: Setting input delay to: 4.946000000000001
set_max_fanout $::env(SYNTH_MAX_FANOUT) [current_design]
set clk_indx [lsearch [all_inputs] [get_port $::env(CLOCK_PORT)]]
#set rst_indx [lsearch [all_inputs] [get_port resetn]]
set all_inputs_wo_clk [lreplace [all_inputs] $clk_indx $clk_indx]
#set all_inputs_wo_clk_rst [lreplace $all_inputs_wo_clk $rst_indx $rst_indx]
set all_inputs_wo_clk_rst $all_inputs_wo_clk
# correct resetn
set_input_delay $input_delay_value  -clock [get_clocks $::env(CLOCK_PORT)] $all_inputs_wo_clk_rst
#set_input_delay 0.0 -clock [get_clocks $::env(CLOCK_PORT)] {resetn}
set_output_delay $output_delay_value  -clock [get_clocks $::env(CLOCK_PORT)] [all_outputs]
# TODO set this as parameter
set_driving_cell -lib_cell $::env(SYNTH_DRIVING_CELL) -pin $::env(SYNTH_DRIVING_CELL_PIN) [all_inputs]
set cap_load [expr $::env(SYNTH_CAP_LOAD) / 1000.0]
puts "\[INFO\]: Setting load to: $cap_load"
[INFO]: Setting load to: 0.01765
set_load  $cap_load [all_outputs]
tns -759.46
wns -24.89
[INFO]: Synthesis was successful
%
```

```
Number of wires:                        14596
Number of wire bits:                    14978
Number of public wires:                  1565
Number of public wire bits:              1947
Number of memories:                         0
Number of memory bits:                      0
Number of processes:                        0
Number of cells:                        14876
  sky130_fd_sc_hd__a2111o_2                 1
  sky130_fd_sc_hd__a211o_2                 35
  sky130_fd_sc_hd__a211oi_2                60
  sky130_fd_sc_hd__a21bo_2                149
  sky130_fd_sc_hd__a21boi_2                 8
  sky130_fd_sc_hd__a21o_2                  57
  sky130_fd_sc_hd__a21oi_2                244
  sky130_fd_sc_hd__a221o_2                 86
  sky130_fd_sc_hd__a22o_2                1013
  sky130_fd_sc_hd__a2bb2o_2              1748
  sky130_fd_sc_hd__a2bb2oi_2              81
  sky130_fd_sc_hd__a311o_2                  2
  sky130_fd_sc_hd__a31o_2                  49
  sky130_fd_sc_hd__a31oi_2                  7
  sky130_fd_sc_hd__a32o_2                  46
  sky130_fd_sc_hd__a41o_2                   1
  sky130_fd_sc_hd__and2_2                 157
  sky130_fd_sc_hd__and3_2                  58
  sky130_fd_sc_hd__and4_2                 345
  sky130_fd_sc_hd__and4b_2                  1
  sky130_fd_sc_hd__buf_1                 1656
  sky130_fd_sc_hd__buf_2                    8
  sky130_fd_sc_hd__conb_1                  42
  sky130_fd_sc_hd__dfxtp_2               1613
  sky130_fd_sc_hd__inv_2                 1615
  sky130_fd_sc_hd__mux2_1               1224
  sky130_fd_sc_hd__mux2_2                   2
  sky130_fd_sc_hd__mux4_1                 221
  sky130_fd_sc_hd__nand2_2                 79
```

Task1: no.of dff cells/total cells=1613/148760=0.108

0.108X100=10.8%