Performance Analysis of a 50 kVA Unified Power Quality Conditioner Model for Low Voltage Distribution Network Application

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***Abstract*—This paper describes the structure and functionalities of a unified power quality conditioner (UPQC) built in Simulink. The UPQC-model consists of a series transformer with a series inverter, connected back to back to a shunt inverter via a dc link capacitor. In the presented model, the UPQC is installed in the middle of a low voltage line, where several loads can be activated to cause power quality disturbances defined by DIN EN 50160, e.g. unbalance, harmonics or rapid voltage changes. The current and voltage control schemes in dq system are explained and the efficacy of the UPQC is shown for several load cases. The complete model is published on Github.com.**

Keywords—Unified Power Quality Conditioner, UPQC, Power Quality, Low Voltage, Unbalance, Harmonics, RVC

I. Introduction

The energy sector faces big changes in the next couple of years due to the European energy transition where mobility and heating will have an increasing impact on electricity supply. This comes on top of the changes in the electricity sector itself. There we can see a trend towards more distributed generation with photovoltaics (PV), wind energy and biomass working now in parallel, but possibly replacing existing centralized power plants in the future. The volatility of renewable energies brings different challenges for all voltage levels [1]. In the research project U-Quality [2], present and future possible power quality (PQ) issues in low voltage (LV) distribution networks are investigated. Further increasing numbers of PV systems, electric vehicles (EV) and heat pumps will likely have an impact on PQ, especially in LV distribution grids. Therefore, it is part of the project U-Quality to develop a prototype of a unified power quality conditioner (UPQC), which could be installed in public distribution grids or used for industry applications to improve PQ.

The principle structure of an UPQC, control schemes and different use cases are known within the research community for many years and have been topic of several publications [3-5]. The UPQC has the potential to mitigate a lot of PQ disturbances at once due to the topology. Therefore, it could, at least technically, be a relevant solution reducing PQ disturbances, if these become more dominant with rising penetration levels of PV, EV and heat pumps.

This paper proposes a control scheme for the UPQC in the dq-domain. The challenging aspect with this approach is the decomposition of the input signals. This is compensated by the advantage, that each PQ criteria can then be treated as an independent control variable. The functionality of the proposed system was proven in various simulations with Simulink respecting each PQ criteria individually first. After that, combinations of PQ disturbances with different magnitudes were investigated.

II. Proposed System

Two voltage source converters (VSC) are connected via a dc link capacitor. The first VSC, being called “series inverter”, is connected in series to the line via a transformer and the second one is connected in parallel, being called “shunt inverter”. In this model the shunt inverter is connected directly to the line, an additional transformer is possible but not necessary for LV applications. The UPQC is placed in the middle of a three-phase four-wire LV line section as shown in Fig. 1. At the end of the line several different loads are connected in parallel, all adjustable and switchable individually. The harmonic load is built as a set of 50 current sources for each phase, so that even high harmonic orders can be set. All other PQ criteria (unbalance, flicker, rapid voltage change (RVC)) are triggered by adjustable constant power loads. A base load adds symmetric active and reactive power consumption. Harmonic and unbalance repercussions from the loads towards the source are getting reduced by the UPQC. But it also improves PQ for connected customers, if the source voltage is distorted. Voltage sags or swells and unbalance can be significantly reduced for customers connected behind the UPQC.

The model has two operation modes which differ in the way the VSCs are modelled. For testing the control structures the VSCs are replaced by ideal voltage sources. In this case the dc link capacitor and the necessary voltage control loop cannot be simulated. The second operation mode respects each VSC as a B6 IGBT bridge, LCL filters and a dc link capacitor.

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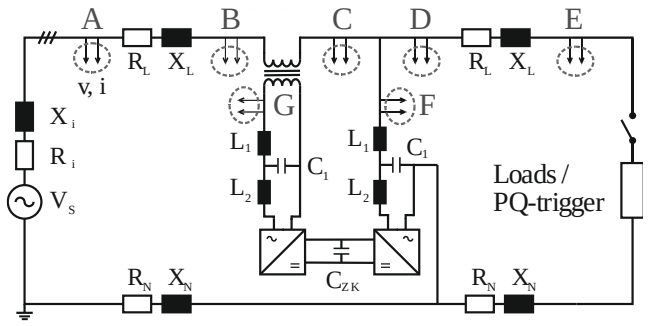

Fig. 1: Schematic circuit diagram of the model and positions of current and voltage measurement points.

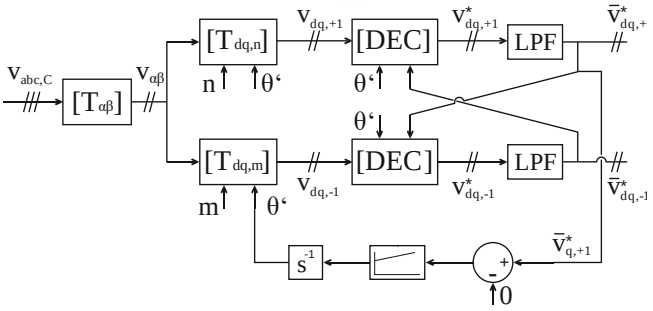

Fig. 2: Block diagram of DDSRF PLL used in the model.

III. Controller Design

As the UPQC is supposed to operate in areas where distortion in the voltage waveform is expected, a suitable phase-locked loop (PLL) is necessary. A stable determination of the phase angle and magnitude of the positive-sequence voltage is fundamental for all control loops used in the system.

A. PLL

As stated in [6], the decoupled double synchronous reference frame (DDSRF) PLL is capable of giving stable outputs under unbalanced and harmonic conditions. Fig. 2 shows the block diagram of the DDSRF PLL used in this UPQC model. The grid voltage at the shunt connection point is used to calculate the phase angle of the positive-sequence system θ' and the decoupled dc terms $\bar{v}^*_{dq,+1}$ and $\bar{v}^*_{dq,-1}$. The two transformation martrices $[T_{\alpha\beta}]$ and $[T_{dq}]$ used for calculation are given by (1) and (2) with θ' = ω*t*, and ω being the fundamental grid frequency.

$$T_{\alpha\beta} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \quad (1)$$

$$T_{dq,n} = \begin{bmatrix} cos(n\,\theta') & sin(n\,\theta') \\ -sin(n\,\theta') & cos(n\,\theta') \end{bmatrix} \quad (2)$$

The decoupled voltage terms $v^*_{dq,n}$ are calculated with the decoupling cell (DEC) (3). In the case of the PLL calculation in Fig. 2, n represents the order of the grid fundamental frequency (+1 = 50 Hz) and m represents the order of the negative-sequence frequency (-1 = -50 Hz).

$$\begin{bmatrix} v^*_{d,n} \\ v^*_{q,n} \end{bmatrix} = \begin{bmatrix} v_{d,n} \\ v_{q,n} \end{bmatrix} - \begin{bmatrix} cos((n-m)\,\theta') & sin((n-m)\,\theta') \\ -sin((n-m)\,\theta') & cos((n-m)\,\theta') \end{bmatrix} \begin{bmatrix} \bar{v}^*_{d,m} \\ \bar{v}^*_{q,m} \end{bmatrix} \quad (3)$$

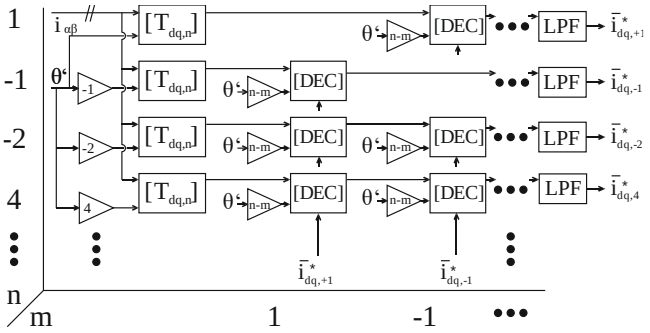

Fig. 3: Scheme of decoupling network for arbitrary orders.

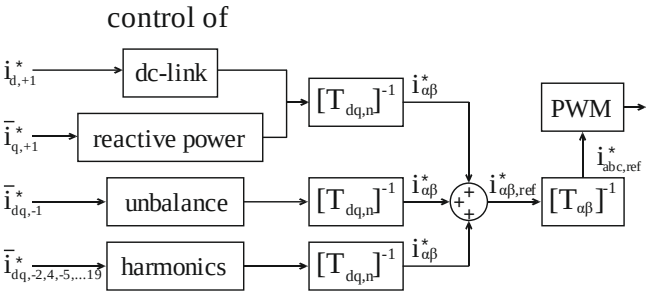

Fig. 4: PWM signal generation.

A low pass filter (LPF) is used to determine the decoupled dq-dc-terms for the positive- and negative-sequence voltage components [6].

B. Shunt Control

The relevant currents for the shunt current control are measured at measurement point (MP) C (currents from and towards the load plus the shunt inverter) and F (currents flowing into and out of the shunt inverter) in Fig. 1. The phase currents are decomposed into all different harmonic orders respected and directly used as control variables. The decoupling used for the PLL is extended for arbitrary harmonic orders according to Fig. 3. n and m represent the orders of frequencies which are decoupled from each other. Orders situated in positive-sequence systems are respected with positive sign and orders situated in the negative-sequence system with a negative sign. Fig. 3 displays the calculation effort, which increases quadratically with the amount of decoupled frequency orders.

The decomposition enables loading the dc link capacitor with active power only, using $i^*_{d,+1,F}$ as input signal for the PI dc link voltage controller. $\bar{i}^*_{q,+1,C}$ is used for compensating any reactive power demand from the load. Other $\bar{i}^*_{dq,n,C}$ currents of higher orders calculated by the DEC are used as inputs for harmonic load current compensation in separate PI controllers. The outputs from all current controllers are retransformed into αβ-domain using $[T_{dq,n}]^{-1}$ with the respective harmonic order. In the αβ-domain, currents of all frequencies are added and subsequently transformed into abc-domain. The abc-signal is used as input for the generation of PWM signals. This process is displayed in Fig. 4.

C. Series Control

The structure of the series and shunt control in the dq domain is very similar. The only differences are the inputs to the control loops which are voltage signals for the series path. The transformations and the decoupling also follow the schemes shown in Fig. 3 and Fig. 4. The time constants of the

LPFs in the PLL and the decoupling calculation have a significant impact on the reaction speed of the UPQC to voltage sags or swells and source voltage unbalance. This is independent from the origin of the voltage change (load or source side). Depending on UPQC user intention, the LPF time constants can be adjusted to improve either steady-state accuracy or reaction speed.

IV. Model Parameters

The general topology of the model is explained in chapter two and illustrated in simplified form in Fig. 1. Further necessary simulation and circuit parameters are shown in Table I.

V. Simulation Results

The proposed system was tested for more than 35 load cases. All scenarios were calculated with and without connected UPQC and the duration of each scenario is 10 s. Dashed lines shown in figures represent scenarios without the UPQC connected and solid lines represent scenarios with the UPQC connected. The UPQC gets connected at 0.5 s, the PQ disturbance starts at 1 s and lasts for 5 s, then the disturbance is switched off again during the last 4 s. The only deviation from this sequence are the simulations of short-term voltage breakdowns to 0.8 p.u. and 0.6 p.u. on the source side, which start at 2 s and have a duration of only 0.5 s. Only results of the operation mode with B6 IGBT-bridges, LCL filters and dc link capacitor are presented. In the following sections specific load cases for individual PQ criteria and one scenario with combined distortion of harmonics, unbalance, RVC and reactive power compensation is displayed. An overview of the scenarios is given with Table II.

A. *Load side unbalance*

Two different unbalance cases with and without UPQC are compared to a no-load scenario. Fig. 5 shows the voltage unbalance factor (VUF) for MP B and MP D over 10 s. An unbalanced load of 25 kW causes a VUF of around 1.5 % measured directly at the load (MP E), which would still be within the limits of 2 % for unbalance according to DIN EN 50160 [7]. At the connection point of the UPQC (MP C, MP D), VUF decreases by about half to 0.8 %, as the UPQC is installed in the middle of the line. An increase of the unbalanced load to 50 kW in the second unbalanced load scenario doubles VUF at all MPs due to linear correlations. With the UPQC connected, VUF at MP D is reduced to 0.1 % and lower, further decreasing in the direction of the transformer. The compensation of the unbalanced load current needs less than 1 s until a steady state is reached. Response times can be easily adjusted within the shunt current control.

Fig. 6 shows the voltages and currents for MP C and MP D for the 25 kW unbalanced load at a steady state moment from 5.9 s to 5.93 s into the simulation. It can be seen that the load current on phase one (MP D) is shifted to all three phases by the UPQC (MP C), but remains asymmetric. The UPQC only minimizes the negative-sequence component of the voltage, but has no impact on the zero system in the model. The results prove that this UPQC model can significantly and quickly improve unbalanced load situations, that would otherwise lead to violation of limits stated in DIN EN 50160 [7].

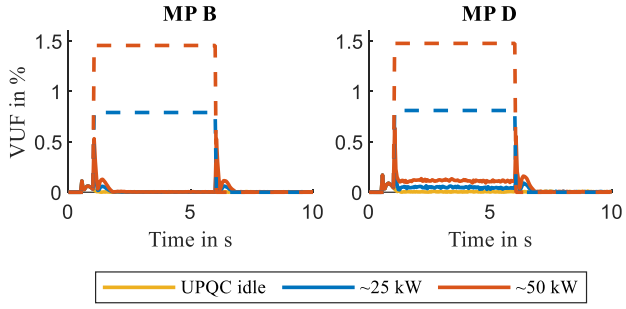

Fig. 5: Unbalance factor VUF at MP B and MP C/D for a ~25 kW and ~50 kW single phase load.

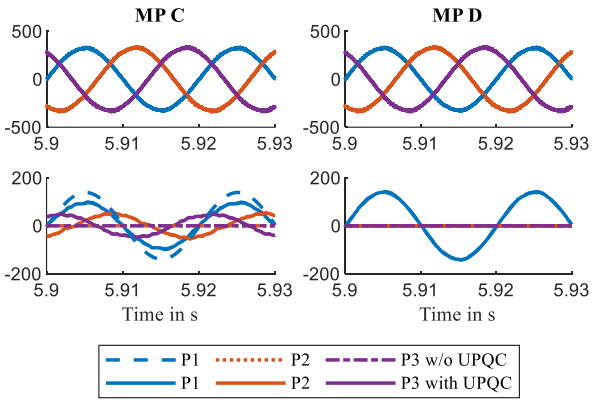

Fig. 6: Improvement of grid current supply displayed for 1.5 cycles in time domain.

TABLE I. Simulation Parameters

Element	Parameter	Value
Source	Voltage	400 V, 50 Hz
	Impedance	R = 0.52 mΩ, L = 0.522 µH
Cable	Impedance	R' = 0.206 Ω/km, L' = 0.256 mH/km
	Length	250 m
VSC	Switching Freq.	20 kHz
Filter	L_{F1}, R_{F1}	930 µH, 100 mΩ
	C_F, R_{FC}	10 µF, 13 Ω
	L_{F2}, R_{F2}	850 µH, 100 mΩ
dc link	Capacitor C_{ZK}	6 mF
	Reference Voltage	700 V
Transformer	Transmission	400:56, 50 kVA

TABLE II. PQ Disturbance Scenarios

Location	Test of	PQ disturbance		
		Unbalance	***RVC***	***Harmonics***
Load side	*Single criteria*	25 kW	20 kW	10 A
		50 kW	40 kW	20 A
		-	80 kW	-
	Combined criteria	25 kW	20 kW	10 A
Source side	*Single criteria*	0.97 p.u.	1.1 p.u. (5 s)	-
		0.94 p.u.	0.9 p.u. (5 s)	-
		0.78 p.u.	0.8 p.u. (0.5 s)	-
		-	0.6 p.u. (0.5 s)	-

B. *Load side harmonics*

Two different harmonic load scenarios are presented here. The values in Table III refer to 10 A and 20 A peak amplitudes of the current sources representing an arbitrary harmonic load. In these two harmonic scenarios, the 2nd, 4th, 5th, 7th, 8th and 19th order is considered. Without a connected UPQC, THD_U values at the load connection point (MP E) reach 5.29 % and 10.67 % respectively. The UPQC in idle mode on the other hand, only increases THD_U at its connection point to around 0.5 %. The effectiveness of the harmonic compensation is displayed for the 10 A scenario.

Fig. 7 shows the relevant orders of i_{dq} values at the UPQC connection point (MP C) for the complete simulation time of 10 s. The simulations of the 10 A harmonic load scenario with and without connection of the UPQC are compared. The connection of the UPQC and charging of the dc link capacitor can be identified at 0.5 s. The effects on the currents flowing into the UPQC subside very quickly again. The dashed lines clearly indicate the time period during which the harmonic load is switched on. With the UPQC connected all harmonic shares get reduced to very low levels after 2 s – 3 s seconds and stay close to zero. After switching off the harmonic load, it takes 2 s – 3 s for the UPQC to reach a steady state again.

The shunt path of the UPQC provides the harmonic power for the load and thus reduces harmonic strain in the cable section and substation. The quality in waveform of the provided current by the UPQC compared to the actual load current is shown in Fig. 8. One and a half cycles of the fundamental frequency are displayed at the end of the harmonic load scenario from 5.90 s – 5.93 s. Only small deviations primarily at minima and maxima can be detected. The improvement in THD_U at different MPs is given by Table III, pointing out the effective harmonic compensation.

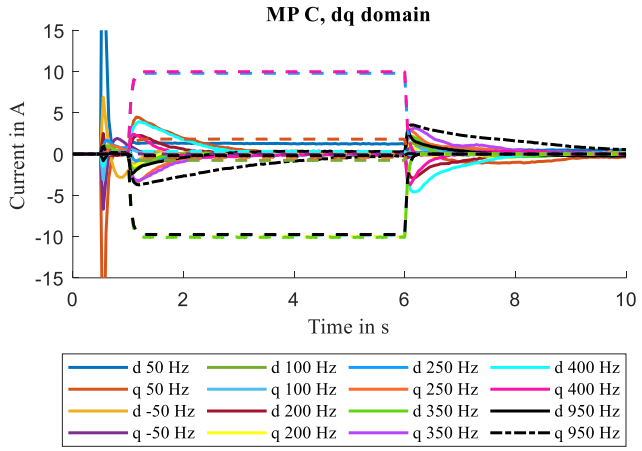

Fig. 7: Reduction of harmonic currents displayed in dq-domain.

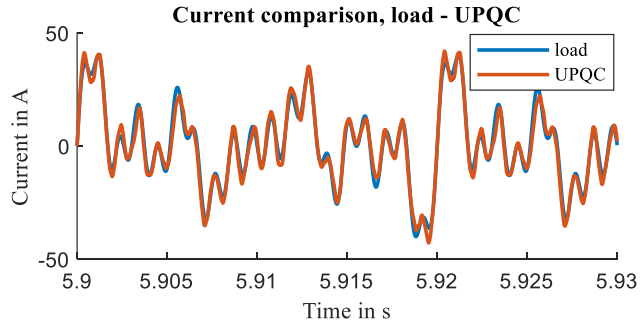

Fig. 8: Harmonic load current and supply current by the UPQC.

C. *Load side RVC*

Fig. 9 displays three different RVC scenarios. A symmetric load, connected at MP E, causes voltage sags of 2 %, 4 % or 7 %. The UPQC reduces the biggest voltage sag in direction of the load from 7 % to 2 % instantly and further declining over time. For the other two scenarios the voltage sag is instantly reduced to 1 % or less, also declining further over time. The graphs also show two disadvantages of the RVC compensation. Firstly, if the cause of the voltage sag disappears, the UPQC produces a voltage swell due to the PI controllers used for the positive-sequence voltage optimization. Secondly, the voltage drop towards the substation increases with compensation, as the power needed by the series VSC, is taken from the grid as a positive-sequence current via the shunt VSC.

D. *Load side combined PQ disturbance*

In this section the results of the simulation with combined PQ disturbances are described. Besides unbalance, harmonics and RVC, there is an additional symmetrical reactive load (3x5 kvar) connected for the complete duration of 10 s. Fig. 10 shows VUF at MP B and MP C. Despite the simultaneous appearance of multiple PQ disturbances, VUF gets reduced from 0.8 %to less than 0.02 % at MP B. The reduction at MP C is not quite as effective as in the case of isolated unbalance compensation shown in Fig. 5, but VUF is still reduced by almost 75 % from 0.8 % to less than 0.25 %.

Fig. 11 shows the relevant currents at MP C in the dq-domain similar to Fig. 3. Four key aspects can be pointed out with this display. The harmonic compensation is not visibly affected by the presence of other PQ disturbances. All harmonics get reduced to levels close to zero after 3 s. Unbalanced currents ($i_{d,-50}$) get reduced close to 0 A from 40 A. The symmetric reactive current $i_{q,50}$ (-30 A) gets effectively compensated to 0 A by the UPQC. The positive-sequence current ($i_{d,50}$) increases from 41.5 A to 57 A, as the UPQC uses only 50 Hz positive-sequence system currents for all compensation processes. The 41.5 A are coming from the RVC triggering load in the first place.

TABLE III. EFFECTIVE THD_U AT DIFFERENT MPS

Scenario	UPQC connected	THD_U in %		
		MP B	***MP C, MP D***	***MP E***
10 A	*No*	1.47	3.84	5.29
	Yes	0.45	1.07	2.18
20 A	*No*	2.98	7.74	10.67
	Yes	1.97	5.00	6.60

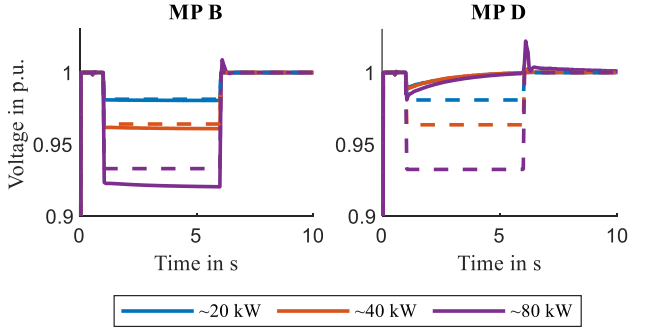

Fig. 9: RVCs caused by symmetric loads, /w and w/o UPQC connected.

Fig. 12 shows the upper segments of three positive voltage half-waves. The first half-wave shows the voltage before the PQ triggering loads are connected. In the second two half-waves the impact of the harmonic loads is visible. Also, the instant improvement in voltage level by the series path gets pointed out with this illustration. In general, it can be stated that this UPQC model is able to improve PQ effectively, even if several PQ disturbances occur in combination and at the same point in time with significant magnitudes.

E. dc link voltage stability

One important criterion for the model of the UPQC being functional, is the stability of the many separate control loops working together. Limits of stability can be reached when current or load values respectively reach unreasonable magnitudes, which are not suitable for average LV grids by any means. Fig. 13 shows the dc link voltage for the combined PQ disturbance presented in the subsection before. After connecting the UPQC at 0.5 s an overshooting of about 5 % of the set value (700 V) can be seen, which subsides within the next seconds. During the presence of PQ disturbances, a ripple in the dc voltage with a magnitude lower than 1 V can be detected, which causes no stability problems for the voltage or current control loops. If harmonics or unbalance with big magnitudes would be investigated, their respected frequencies are also visible in the dc link voltage.

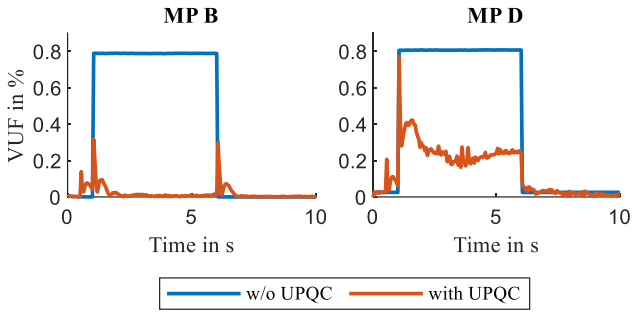

Fig. 10: Unbalance factor VUF in the combined disturbance scenario.

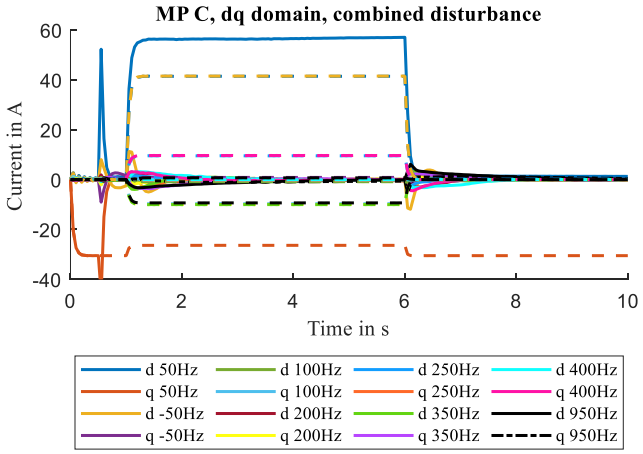

Fig. 11: Reduction of harmonic, unbalanced and reactive currents displayed in dq domain in the combined disturbance scenario.

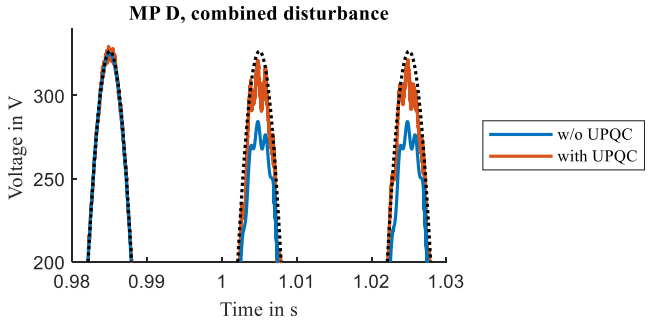

Fig. 12: Changes in voltage waveforms briefly after combined PQ disturbance shown by means of three upper parts of voltage cycles (No load reference as black dotted line).

F. Source side Unbalance

Three scenarios of unbalanced supply voltage at the substation are displayed in Fig. 14. The lower voltage in one phase of 0.97 p.u., 0.94 p.u. and 0.78 p.u. corresponds to an unbalance factor VUF of 1 %, 2 % and 8 % respectively. With active UPQC, voltage unbalance reduces by half for the first two scenarios. 8 % voltage unbalance gets more than quartered not reaching a final steady value within the stress period. These unbalance scenarios show, that the UPQC can improve voltage quality for customers in case of severe voltage unbalance within the grid or coming from medium voltage level.

G. Source side RVC

The lastly investigated PQ distortions are RVCs coming from the substation towards customers. Four such scenarios are displayed in Fig. 15. The first two scenarios are a voltage sag and a voltage swell of 10 % for 5 s each. These very fast changes in supply voltage can be instantly damped by the UPQC by 80 % and by further optimizing the voltage returns towards 1 p.u.. It can be seen in the graph that supporting the voltage level works better than lowering the voltage level. The remaining two scenarios display shorter voltage sags to 0.8 p.u. and 0.6 p.u. for 0.5 s. These major voltage changes get equally damped by the UPQC by 15 - 16 percentage points. In every case shown here, the UPQC model causes a voltage change in the opposite direction of the prior cause, if the voltage returns to its nominal voltage. Fig. 16 shows the upper segments of three positive voltage half waves during the occurrence of the RVCs. The immediate improvement in voltage level can be seen, even in the first half wave after the voltage changes.

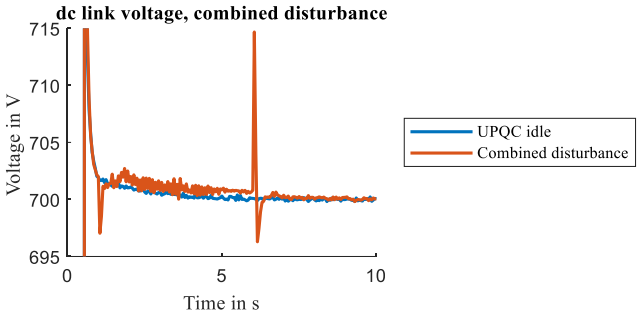

Fig. 13: dc link voltage for idle mode and combined disturbance scenario.

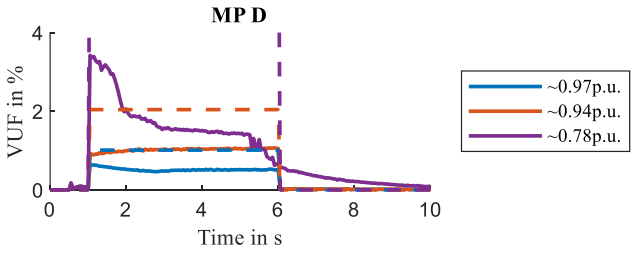

Fig. 14: Unbalance factor VUF during unbalanced grid voltage supply.

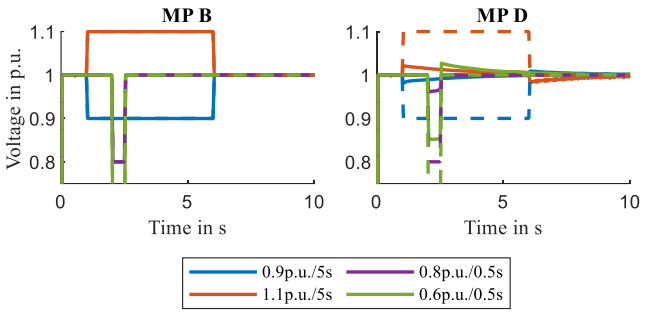

Fig. 15: Improvements on grid voltage level during RVC coming from medium voltage grid level.

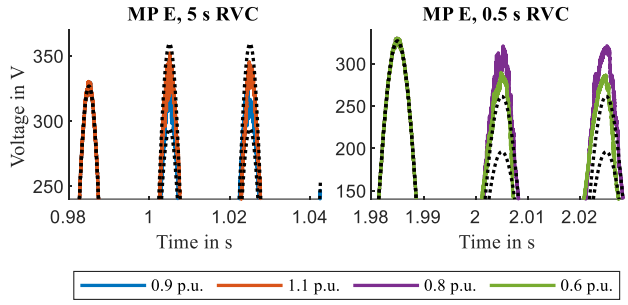

Fig. 16: Changes in voltage waveforms briefly after RVC at medium voltage level shown by means of three upper parts of voltage cycles (No UPQC active as black dotted line).

VI. Conclusion

This paper describes a three-phase four-wire Simulink model of an UPQC for low voltage grid application improving PQ in domestic or industrial grids. The principle control structures in dq-domain for the shunt and the series path are explained. Using the dq domain and decoupling all frequencies that have to be considered, allows the use of individual control variables for each PQ criteria defined by DIN EN 50160 [7]. The current control of the shunt path keeps the dc link capacitor stable at reference voltage. Furthermore, the shunt VSC provides loads, connected behind the UPQC, with unbalanced, harmonic and reactive currents to reduce PQ disturbances within the rest of the grid. The series VSC is able to inject voltages into the line via a series transformer. Unbalance or RVC coming from medium voltage level via the substation can be reduced significantly, improving voltage quality for all customers connected behind the UPQC. Improvements in voltage level are achieved even within the first voltage half wave. The effectiveness of all control loops is displayed at various load scenarios for individually occurring PQ disturbances and combined ones. The simulation results show, that UPQCs have the capability of improving PQ for customers in domestic grids or industrial facilities, especially if voltage quality is an issue and different PQ disturbances appear frequently.

A. *Scopes of future work*

The decoupling described in this paper helps separating control algorithms for different PQ criteria. Nevertheless, there are still many dependencies between LPF time constants, PI control parameters, VSC switching frequency, LCL filter design, which need further investigation. Furthermore, possibilities for influencing and optimizing the zero-sequence system will be considered.

B. *Publication on Github*

The whole Simulink model of the UPQC presented in this paper is published on www.github.com/ (link will follow in paper version to publish).

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