VLSI LAB PROJECT

EE311

Project Title: Ultra Low Power Design of Carry Out Bit of 4-Bit Carry Look-Ahead Adder.

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Objective:

The project "Ultra Low Power Design of Carry Out Bit of 4-Bit Carry Look-Ahead Adder" is intended to lead advances in digital circuitry by designing and implementing a carry-out bit circuit that attains unprecedented levels of energy efficiency and performance. Our foremost objective is to minimize the time delay and substantially cut the amount of power consumption as compared to conventional systems. We seek to push beyond the boundaries of low-power circuit design by using creative design methods and rigorous optimization approaches, creating new standards for energy-efficient computing systems. By harnessing state-of-the-art methodologies such as voltage scaling, power gating, and transistor sizing optimization, we aim to deliver a carry-out bit circuit that not only consumes ultra-low power but also exhibits swift and efficient operation, ensuring minimal latency in the addition process.

This project seeks to contribute to the broader field of digital circuit design by providing practical solutions for energy-conscious computing, fostering sustainability, and environmental awareness in technology development. By successfully implementing an ultra-low power carry-out bit circuit within the context of a 4-bit carry look-ahead adder, we aim to demonstrate the feasibility and scalability of energy-saving technologies, paving the way for their widespread adoption in diverse applications ranging from portable electronics to IoT devices. Our overarching goal is to drive innovation and progress in the realm of low-power digital design, catalyzing a paradigm shift towards more efficient and environmentally friendly computing solutions.

Specifications:

Carry lookahead adders operate by generating two bits called Carry Propagate and Carry Generate which are represented by Cp and Cg. The Cp bit gets propagated to the next stage and the Cg bit is used for generating the output carry bit and this is independent of the input carry bit. The below picture shows the 4-bit **carry lookahead adder architecture**. For the construction of the carry-lookahead adder, we need two Boolean expressions which are for the **carry-lookahead adder formula** for carry to propagate Cp and carry generate Cg.

$Cp_i = Xi \oplus Yi$

$Cg_i = Xi.\ Yi$

With the above expressions, the sum and carry at the output can be given as:

$Sum_i = Cp_i \oplus C_i$

$C_{i+1} = Cg_i + (Cp_i \,.\, C_i)$

With the above fundamental equations, the Boolean expression for carry output at every stage can be known. So

$C1 = Cg_0 + (Cp_0 \,.\, C_0)$

$C2 = Cg_1 + (Cp_1 \,.\, C_1) = Cg_1 + (Cp_1 \,.\, [Cg_0 + (Cp_0 \,.\, C_0)])$

- $Cg_1 + Cp_1 \,.\, Cg_0 + Cp_1 \,.\, Cp_0 \,.\, C_0$

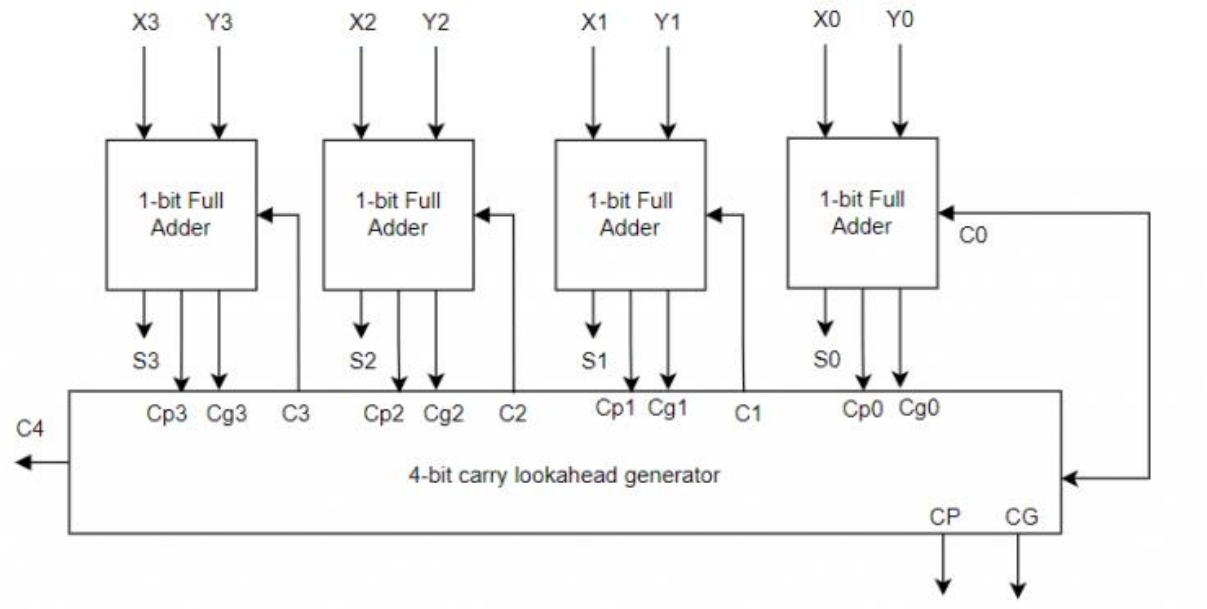
$C3 = Cg_2 + (Cp_2 \,.\, C_2)$

- $Cg_2 + (Cp_2 \,.\, [Cg_1 + Cp_1 \,.\, Cg_0 + Cp_1 \,.\, Cp_0 \,.\, C_0])$

$C4 = Cg_3 + (Cp_3 \,.\, C_3)$

- $Cg_3 + (Cp_3 \,.\, Cg_2 + (Cp_2 .\, [Cg_1 + Cp_1 \,.\, Cg_0 + Cp_1 \,.\, Cp_0 \,.\, C_0])$

As per the above equations, the carry bit of any stage is based on:



A new carry generation scheme for carry out bit of a 4-bit carry look-ahead (CLA) adder is to be presented. To analyze performance, the proposed design for the carry-out bit has to be implemented and verified in the Cadence Virtuoso environment in 180nm technology. Performance parameters should be compared with the conventional design of carry-out bit of 4-bit CLA adder. The proposed

design should achieve a 25% improvement in propagation delay over the conventional CLA design. Due to low transistor count and low dynamic power dissipation, an improvement of 95 % is expected in average power consumption over the conventional carry-out bit of CLA design. As a result, the obtained improvement in PDP must be 94%. Due to enhancements in performance parameters and reduced transistor count, the proposed CLA carry-out bit is expected to have an extensive impact on overall adder performance.

Design:

To design the proposed circuit, at first, we generated the truth table for carry bits C_1, C_2, C_3, and $C_4$by using the input bits in the sequence-
$A_3, B_3, A_2, B_2, A_1, B_1, A_0, B_0, C_0$Here, A_3, B_3 are the MSBs and C_0 is the input carry. By using the truth table, carry bits C_1, C_2, C_3, and C_4 can be expressed as the following simplified sum of products:

$$C_1 = C_0(A_0 + B_0) + (A_0B_0)$$

$$C_2 = C_1(A_1 + B_1) + (A_1B_1)$$

$$C_3 = C_2(A_2 + B_2) + (A_2B_2)$$

$$C_4 = C_3(A_3 + B_3) + (A_3B_3)$$

With careful observation of (1), (2), (3), and (4), we can see that each carry-out equation works as a base for the subsequent carry-out term C_{i+1} . Therefore, to design the n channel Field Effect Transistor (nFET) network for carry C_2 , nFET network for carry bit C_1 needs to be utilized.

Truth Table for C_1, C_2, C_3, and C_4:

C_0	A_0	B_0	C_1
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

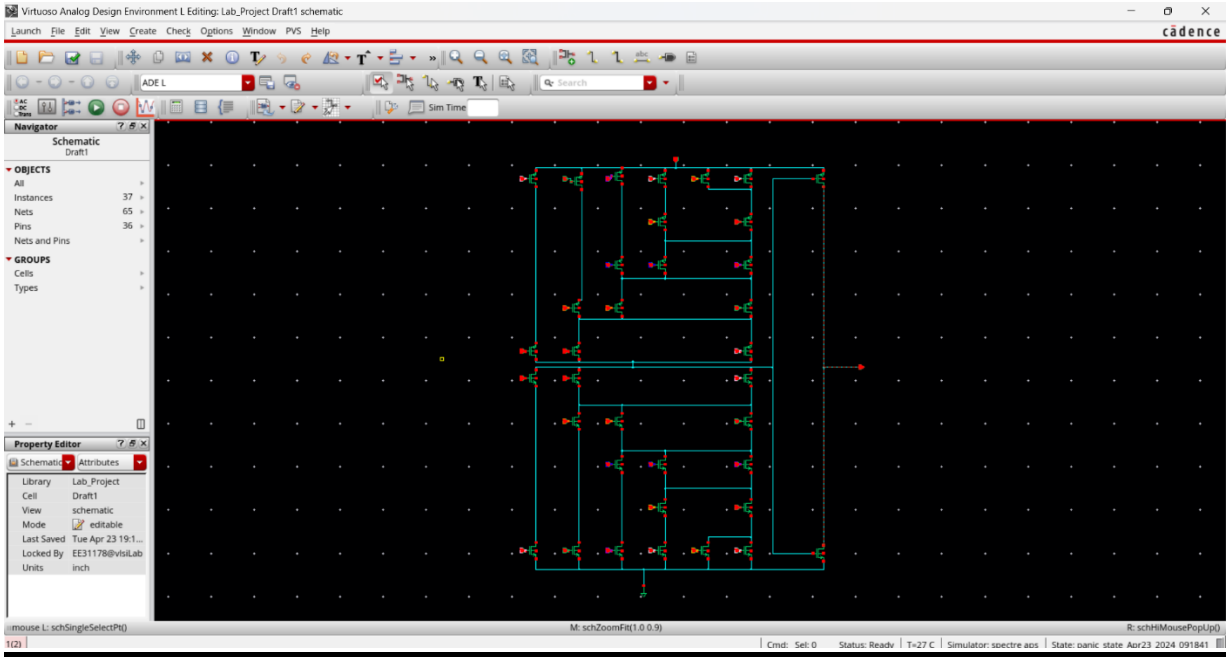
C_1	A_1	B_1	C_2
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

C_2	A_2	B_2	C_3
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

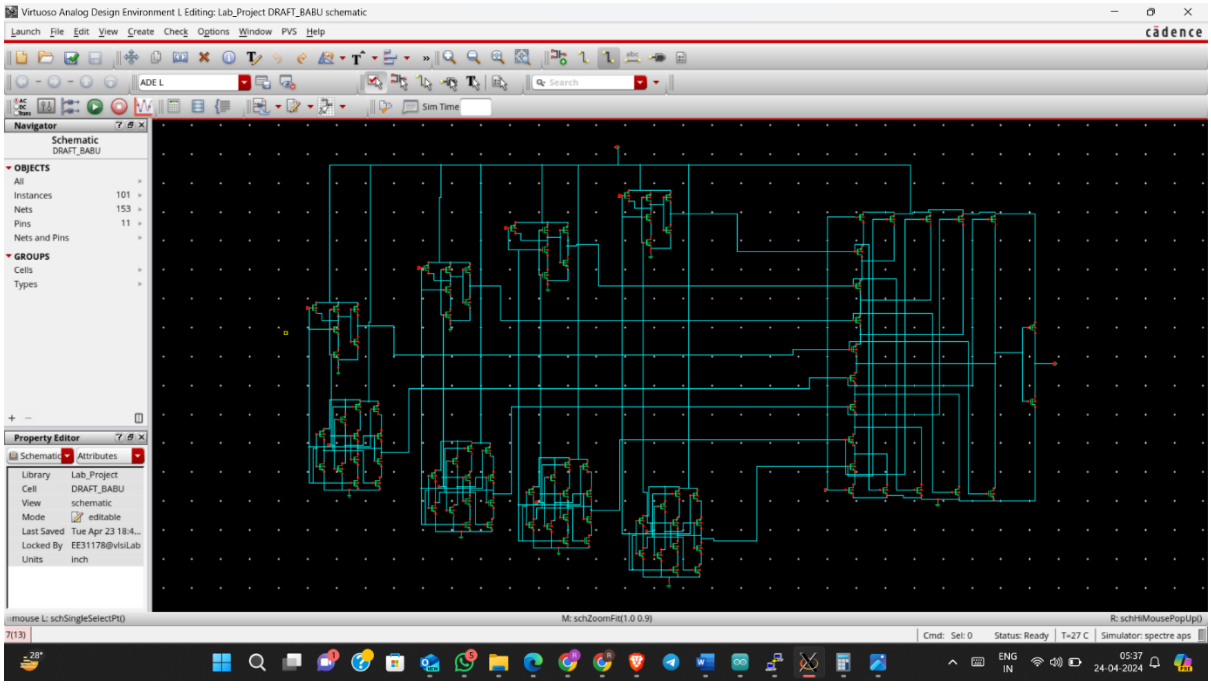
C_3	A_3	B_3	C_4
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

$$C_4 = C_0(A_0 + B_0)(A_1 + B_1)(A_2 + B_2)(A_3 + B_3) + (A_0B_0)(A_1 + B_1)(A_2 + B_2)(A_3 + B_3) + (A_1B_1)(A_2 + B_2)(A_3 + B_3) + (A_2B_2)(A_3 + B_3) + A_3B_3$$

By implementing C_4 with pull up and pull doun networks we get our proposed design of carry out bit



Schematic of proposed design Carry Out bit C_4



Schematic of the Conventional Carry Out bit C_4

Now, to obtain the nFET network for C_2, two series connected nFETs are parallelly connected with the nFET network of C_1. To complete the design, two parallelly connected nFETs are connected in series with this circuit. In the same

way, the nFET network for carry terms C_3 has been generated. Finally, applying the same technique, the nFET network for C_4 has been obtained using nFET network of C_3. In the case of designing the proposed carry-out bit, a mirror equivalent circuit has been used for the pull-up network (pFET network) which provides more symmetrical layout. Structure of the pull-down network (nFET network) and pull-up network (pFET network) in the mirror circuit are exactly the same.

The transistor count for the proposed and conventional carry-out bit design is presented in **Table I**.

Design	Transistor Count
Conventional	92
Proposed	36

Table 1

User Document:

Carry lookahead adders operating with high speed are employed as integrated circuits so that it is simple to integrate adders in many circuits. Also, the increase in the count of transistors is even moderate when implemented for higher bits. When CLA's are used for high-bit calculations, the device offers more speed whereas the circuit complexity also increases. Usually, these are used for 4-bit modules so that they are integrated for high-bit computations. Regularly, carry-lookahead adders are used in Boolean computations.

We can use this design for inputs given.

	Zero Value	One Value	Time Period(ns)
Co	1.8	0	5
Ao	1.8	0	10
Bo	1.8	0	20
A1	1.8	0	40
B1	1.8	0	80
A2	1.8	0	160
B2	1.8	0	320
A3	1.8	0	640
B3	1.8	0	1260

From the above table, we can infer that the frequency of the proposed design is 0.2MHz. So the range of the frequency is in MHz which is considered to be very fast and can be used in many circuits as adders. The average Power is approximately 4uW and Delay is 485ns. Even though the delay is high compared to Conventional design, power is much lower. This makes our circuit very comfortable to use in many other integrated circuits.

In order to get the addition of higher-order bits, it is required to cascade CLA adders. To design either 8-bit, 16-bit or 32-bit parallel adders, then the required number of 4-bit carry lookahead adders can be added using the carry bit.

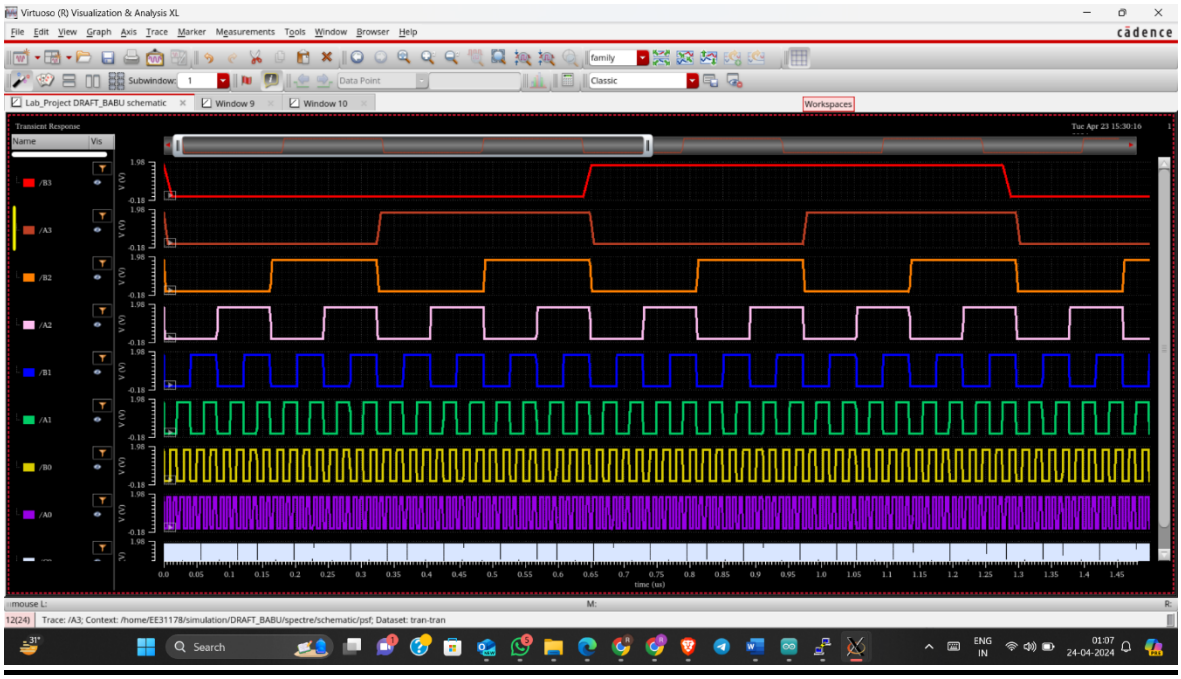
For example, an **8-bit carry lookahead adder circuit diagram** can be drawn and implemented using two 4-bit adders with additional gate delays. In a similar manner, a 32-bit CLA is formed by cascading two 16-bit adders thus forming a single system.

Testing:

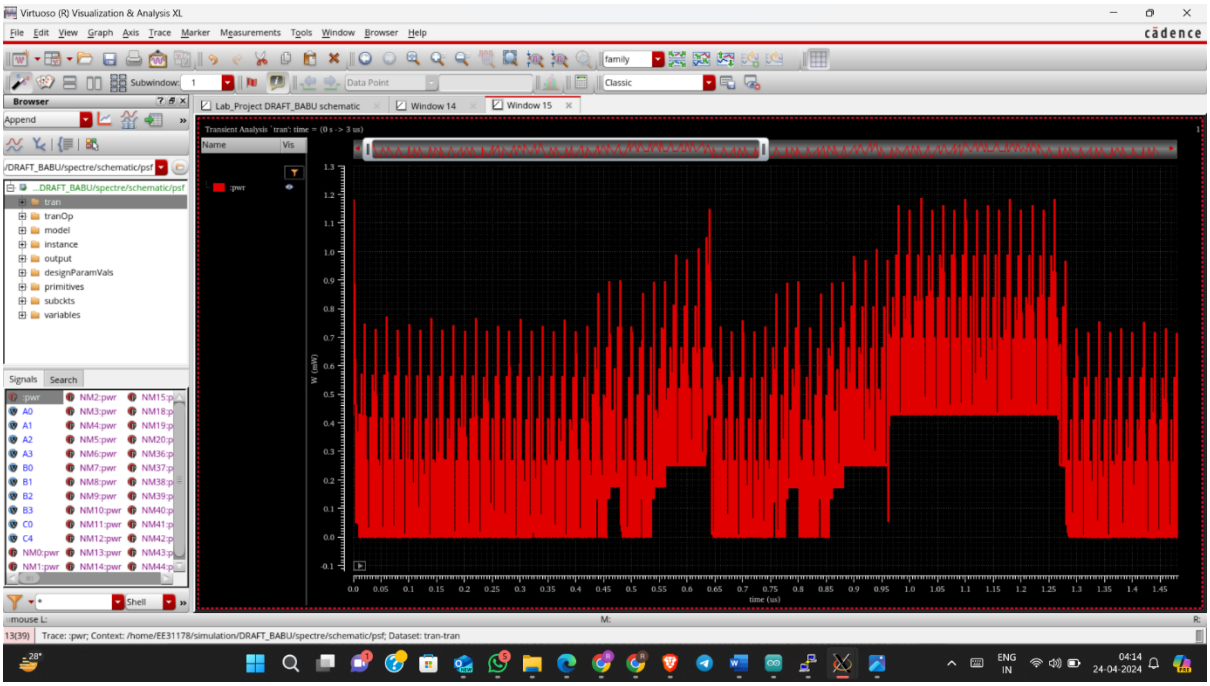
We have done our design with 10u, and 4u sizing of the transistors PMOS and NMOS respectively. But we have seen that the power is too high than expected and the delay is as expected. We have tested them by decreasing the size of the transistors. Here we have a problem with decreasing the size as we know the delay also has risen significantly. We encountered a trade-off between power and delay, in this, we ought to design low-power CLA.

Design	Size	Power(uW)	Delay(ps)	PDP (fJ)
Conventional	1u,0.4u	146.5	331	48.49
Proposed	10u,4u	17.1	213.76	3.655
Proposed	5u,2u	10.61	247.32	2.624
Proposed	1u,0.4u	3.89	485.415	1.888

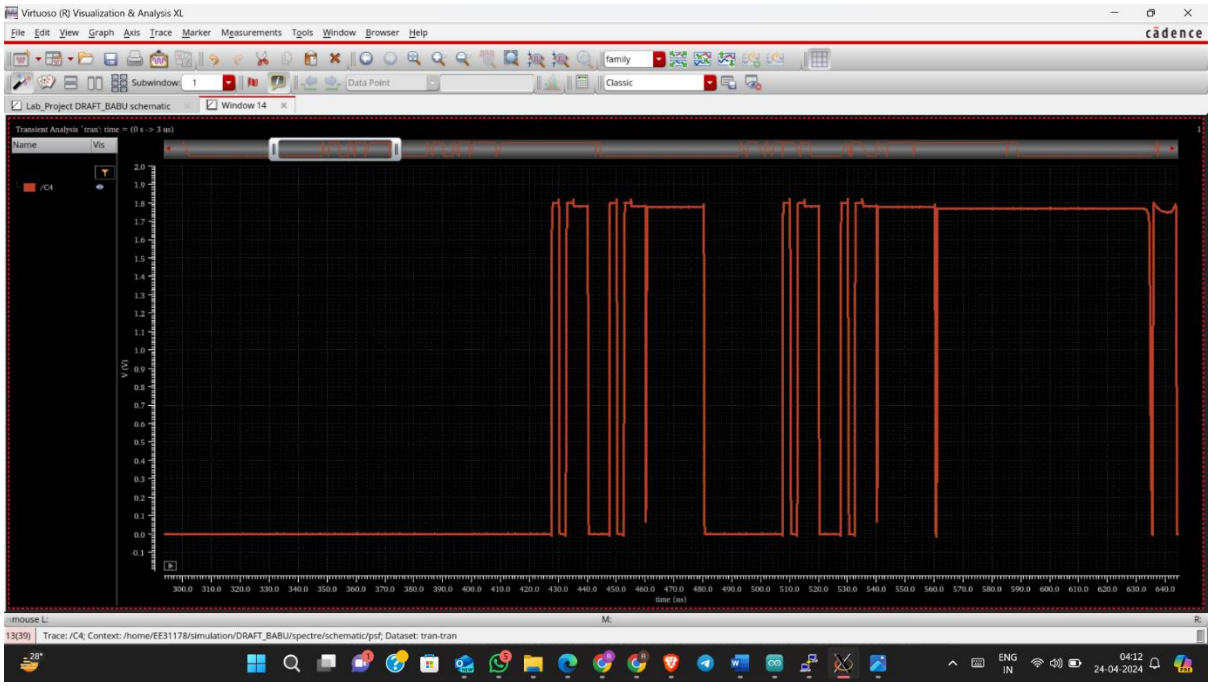
Conventional Design inputs and outputs:



Inputs for conventional Design

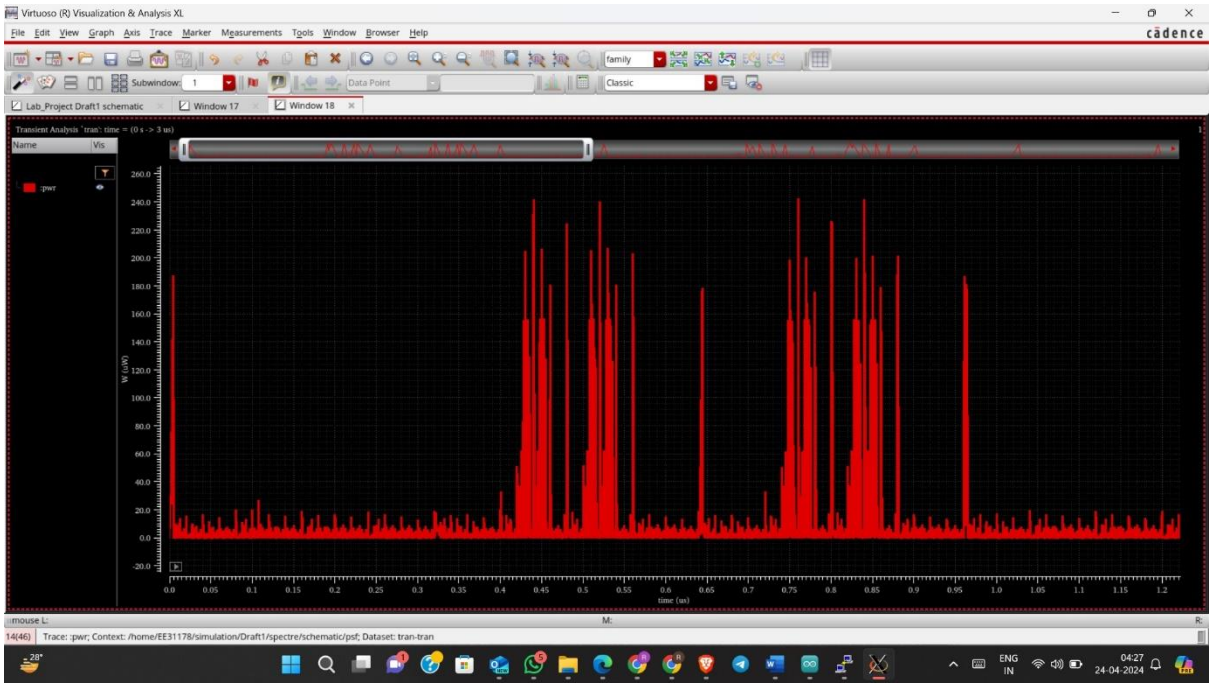


Average Power for conventional Design

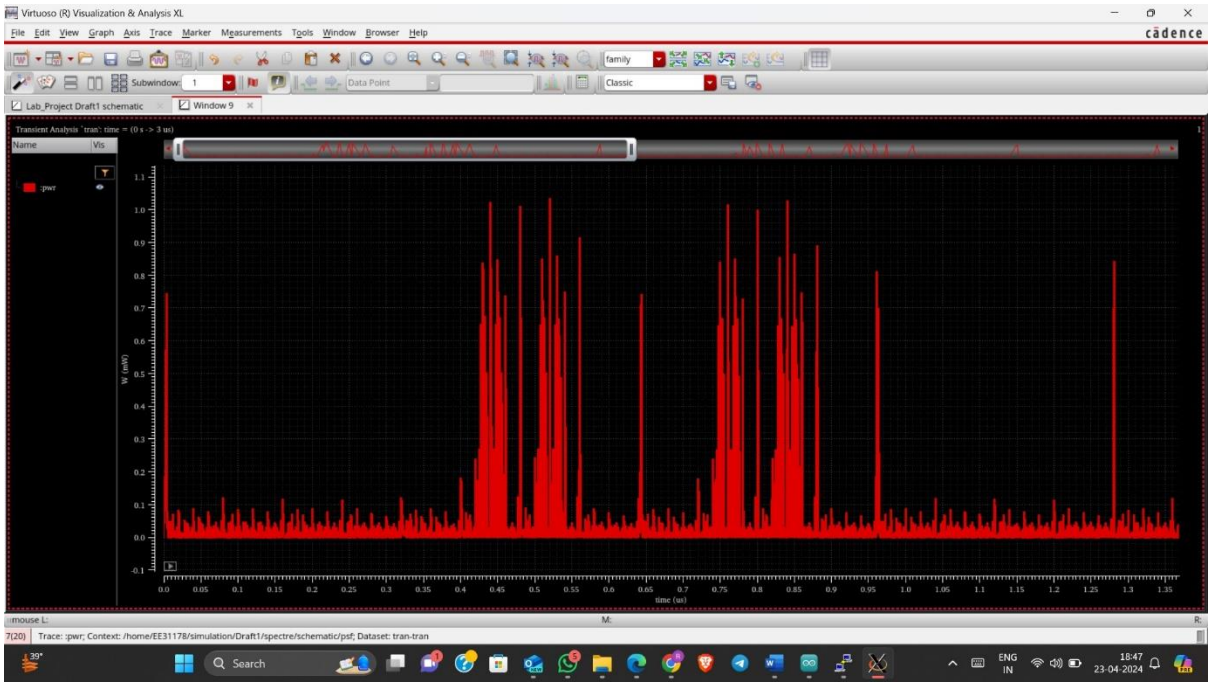


Output graph of conventional Design.

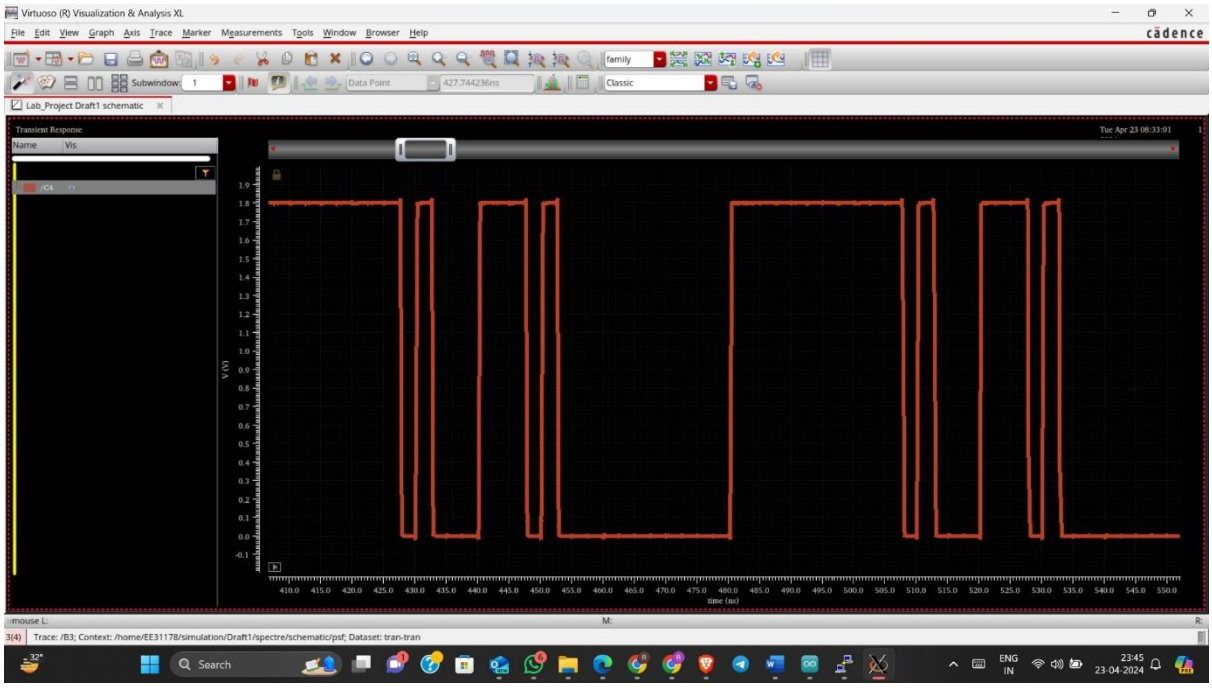
Proposed Design inputs and outputs:



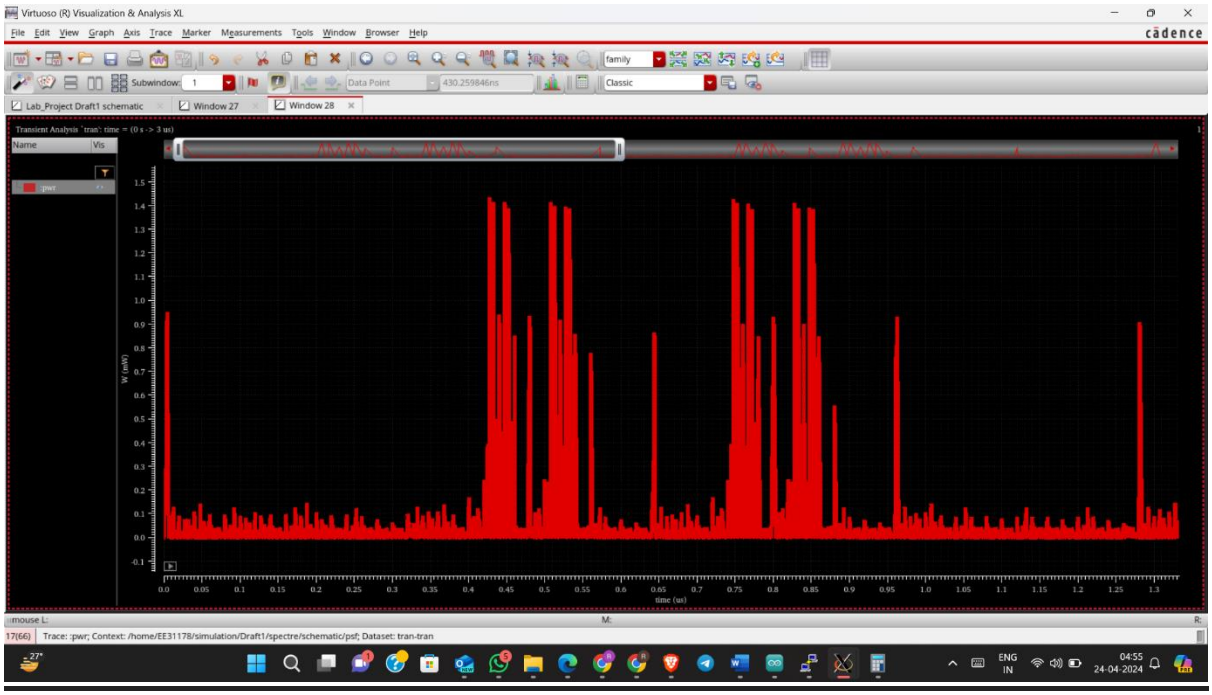
Average Power Graph of Proposed Design at 1uM.



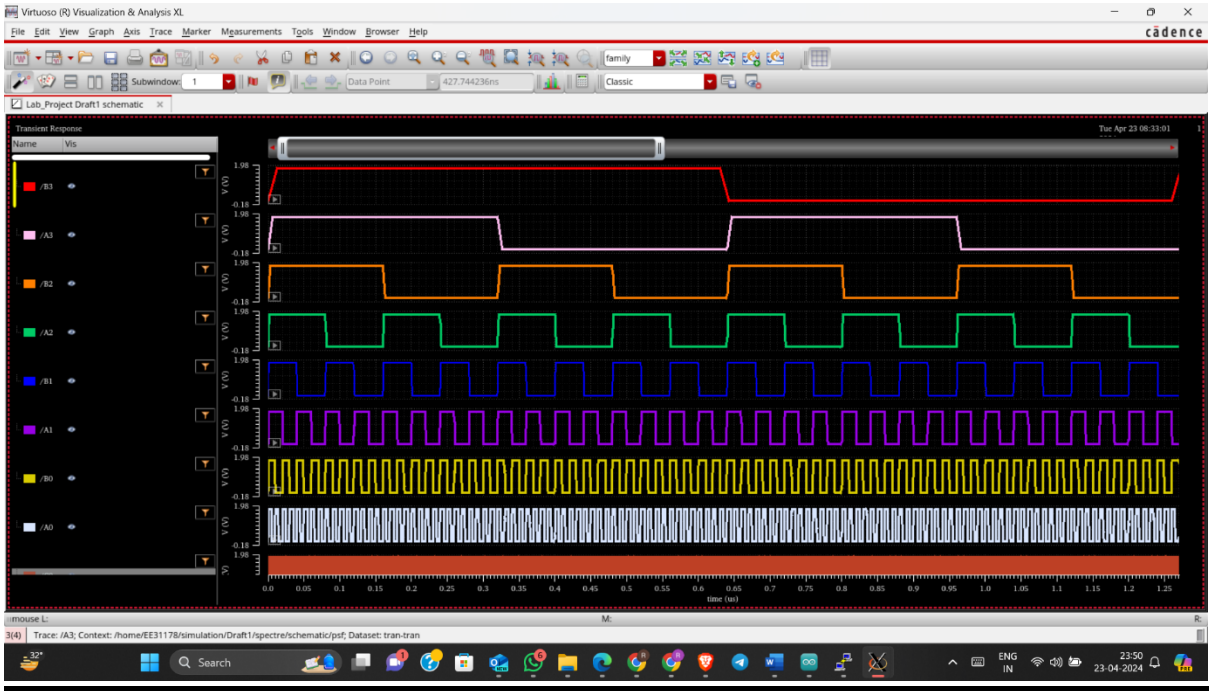
Average Power Graph of Proposed Design at 5uM.



Output Graph of Proposed Design at 1uM



Average Power Graph of Proposed Design at 10uM



Input Graph of Proposed Design

Optimization and Results:

The Power Design of Carry Out Bit for the 4-Bit Carry Look-Ahead Adder utilizes pull-up and pull-down networks to achieve ultra-low power consumption and efficient operation. By employing these networks, we control the flow of current through the circuit, optimizing power usage while maintaining signal integrity. The pull-up network ensures rapid transition to logical high state during carry propagation, while the pull-down network facilitates quick discharge to logical low state, minimizing time delay. This design approach effectively reduces power dissipation by minimizing unnecessary current flow and maximizing the efficiency of signal transitions. Through careful selection of transistor sizes and circuit topology, we aim to achieve a balance between power efficiency and performance, thereby advancing the state-of-the-art in low-power digital circuit design.

Average Power:

Average power for the proposed design and conventional design were calculated using the Calculator option in the waveform window.

	Power(uW)
Conventional	146.5
Proposed	3.89

97.33 % improvement in the power.

Power Delay Product (PDP):

PDP represents the average energy absorbed or consumed by a logic circuit for every switching event. PDP for proposed and conventional design are listed in Table II

	Power(uW)
Conventional	48.49
Proposed	1.888

96.106 % improvement in the PDP.

Conclusion:

In this project, the design of a carry-out bit of 4-bit adder has been proposed and its performance analysis has been done. To compare the proposed circuit with the conventional CLA circuit, Cadence Virtuoso tools were used to carry out simulation in 180nm technology. The proposed design of the carry out bit offered significant improvement in power over the conventional CLA design. The most significant improvement has been achieved in case of average power which is 97.33%. As a result,96.106% improvement in PDP has been obtained.