

$$1. \quad t_H = 20 \text{ ms}$$

$$t_L = 20 \text{ ms}$$

$$T = 40 \text{ ms}$$

$$F = \frac{1}{40 \times 10^{-9}} = \frac{10^9}{40} = \frac{10^3}{40} \times 10^6 = 25 \times 10^6 \text{ Hz} = 25 \text{ MHz}$$

$$\text{duty cycle} = \frac{20}{40} \times 100\% = 50\%$$

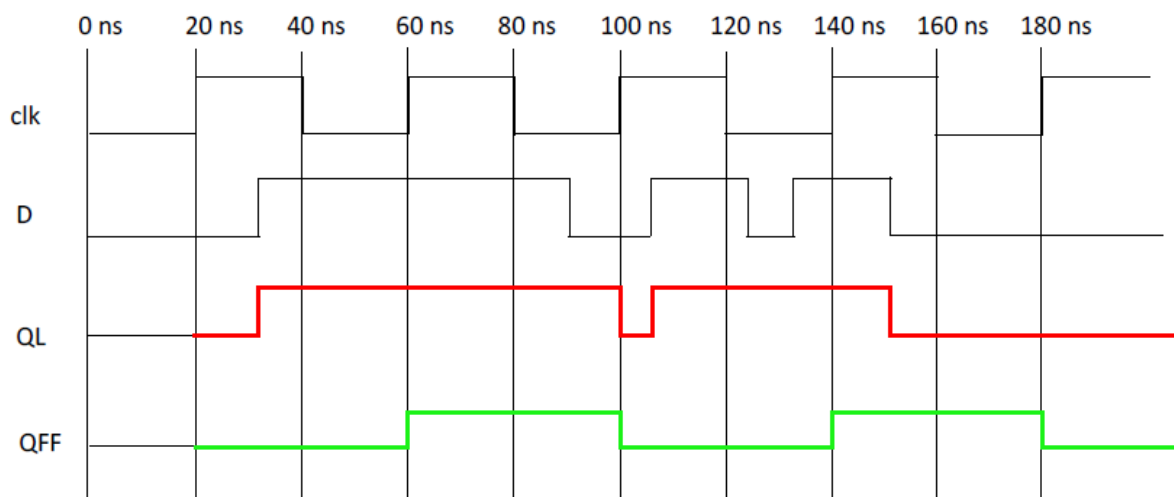


Fig. 1 – Functional behavior of a D latch and a positive-edge-triggered D flip-flop.

2

a) negative-edge-triggered D flip-flop

b) positive-edge-triggered D flip-flop

c) D-Latch

3

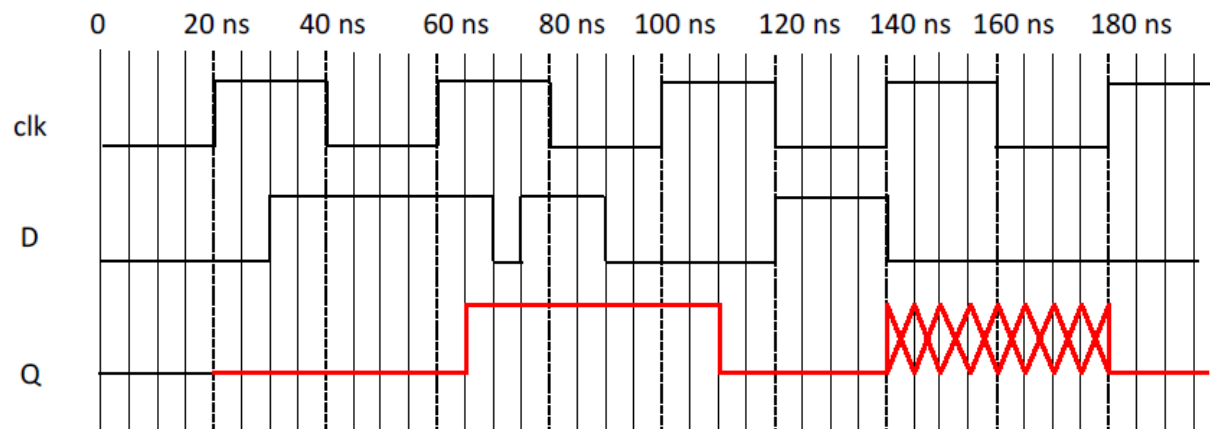


Fig. 3 – A timing diagram of a positive edge-triggered flip-flop to complete.

4

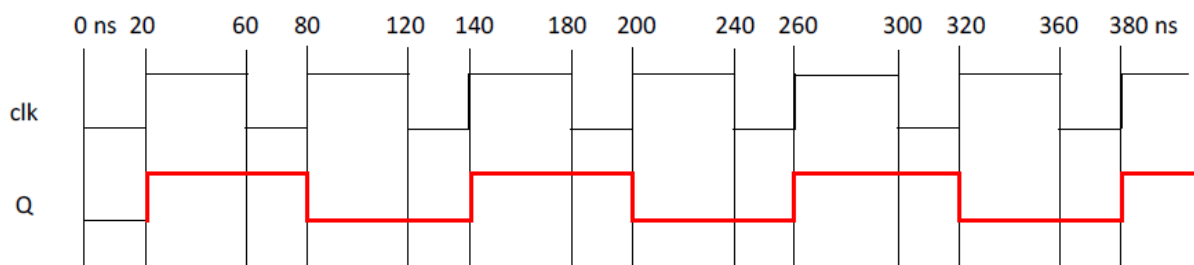


Fig. 4 – A circuit based on a D flip-flop and its timing diagram.

Valores do CLK

$$T = 60 \text{ ms}$$

$$F = \frac{5000}{60} \approx 83,3 \text{ MHz}$$

$$t_H = 40 \text{ ms}$$

$$\text{duty cycle} = \frac{40}{60} \times 100 \approx 66,7\%$$

Valores do sinal Q

$$T = 120 \text{ ms}$$

$$F = \frac{5000}{120} \approx 41,7 \text{ MHz}$$

$$\text{duty cycle} = \frac{60}{120} \times 100\% = 50\%$$

$$T_{\min} = 15 + 5 = 20 \text{ ms}$$

$$F_{\max} = \frac{5000}{20} = 250 \text{ MHz}$$

O circuito duplica o período do clock.

5

a)

inputs $\rightarrow x, clk$

b)

Output $\rightarrow y = x \times Q_1$

c)

$$Q_1^+ = D = Q_0 \times \bar{x}$$

$$Q_0^+ = x$$

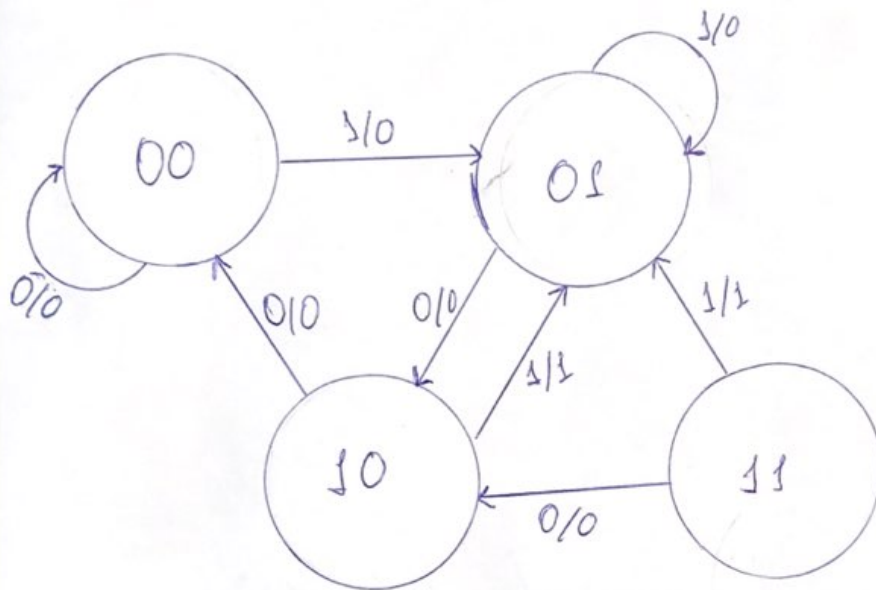
d) Mealy \rightarrow Porque a saída depende da entrada

e)

Tabela de transição saídas

Q_1	Q_0	x	Q_1^+	Q_0^+	y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	1	0	0
0	1	1	0	1	0
1	0	0	0	0	0
1	0	1	0	1	1
1	1	0	1	0	0
1	1	1	0	1	1

f)

legenda: x/y 

g)

O circuito detecta a sequência 101 aceitando sobreposição.

h)

$$20 \text{ MHz} = \frac{1000}{x} \Rightarrow x = \frac{1000}{20} \Rightarrow x = 50 \text{ ms}$$

$$T = t_{\text{setup}} + t_{\text{gate}} + t_{\text{pHL}} \Rightarrow$$

$$50 = 15 + 25 + t_{\text{gate}} \Rightarrow 50 - 40 = t_{\text{gate}} \Rightarrow$$

$$t_{\text{gate}} = 10$$

6

Máquina de Mealy porque a saída depende da entrada

$$T_{max} = 15 + 25 + 0 = 40 \text{ ms}$$

$$F = \frac{1000}{40} = 25 \text{ MHz}$$