1.

$t_H = 20\ ms$

$t_L = 20\ ms$

$T = 40\ ms$

$$F = \frac{1}{40 \times 10^{-3}} = \frac{10^9}{40} = \frac{10^3}{40} \times 10^6 = 25 \times 10^6\ Hz = 25\ MHz$$

$$\text{duty cycle} = \frac{20}{40} \times 100\% = 50\%$$

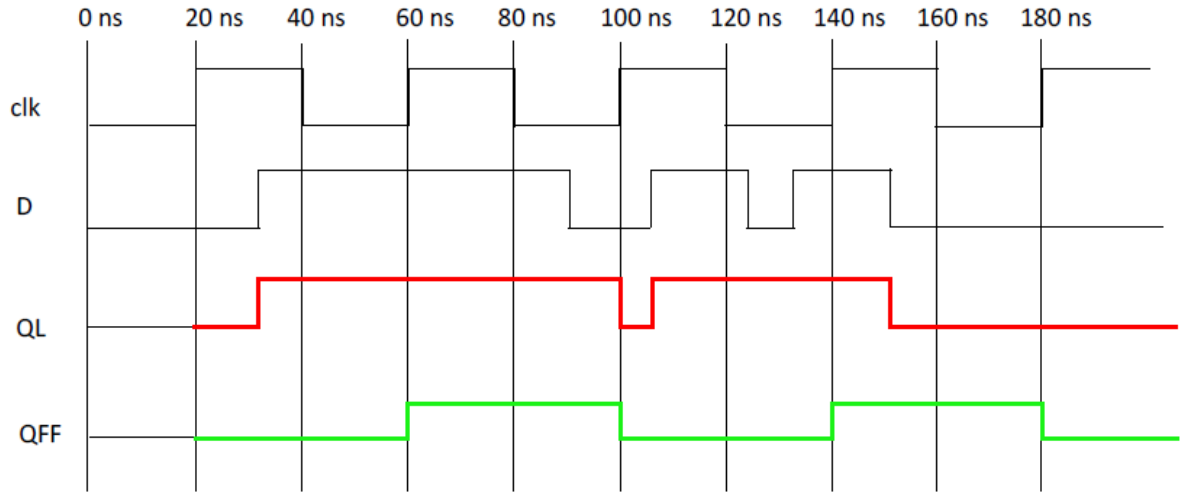

Fig. 1 – Functional behavior of a D latch and a positive-edge-triggered D flip-flop.

2

a) negative-edge-triggered D flip-flop

b) positive-edge-triggered D flip-flop

c) D-Latch

3

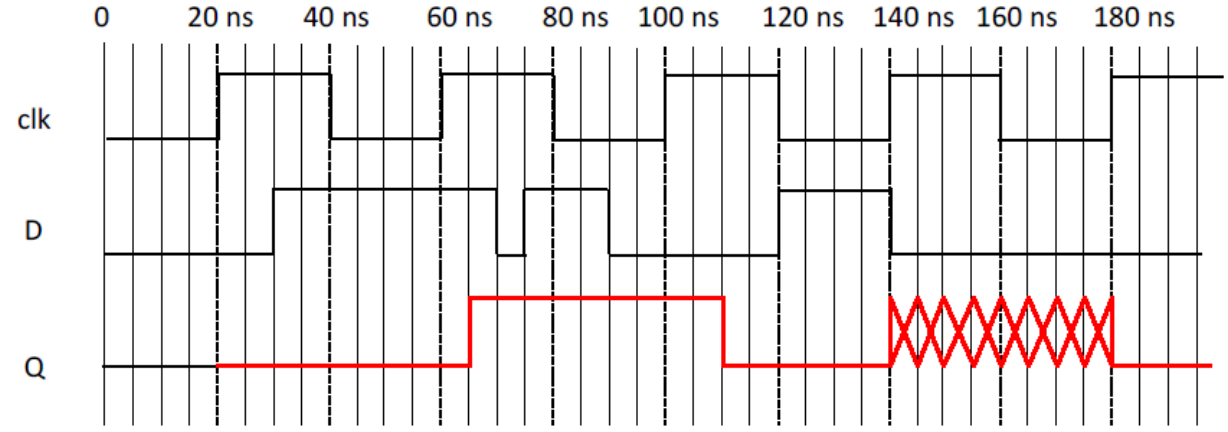

Fig. 3 – A timing diagram of a positive edge-triggered flip-flop to complete.

4

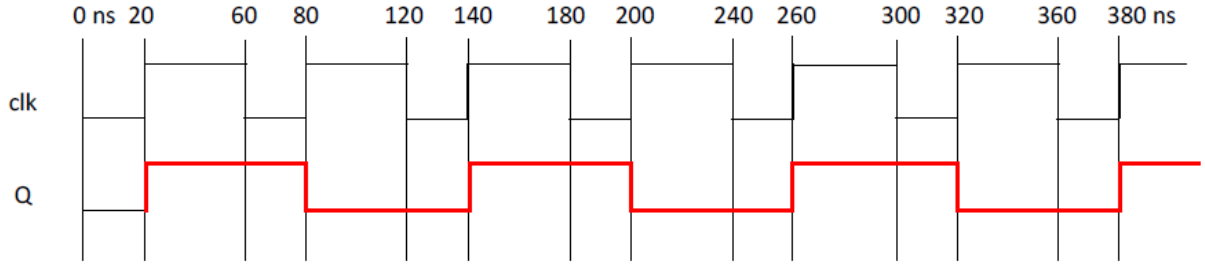

Fig. 4 – A circuit based on a D flip-flop and its timing diagram.

Valores do Clk

$T = 60\,ms$

$F = \frac{1000}{60} \simeq 16{,}7\,MHz$

$t_H = 40\,ms$

$duty\ cycle = \frac{40}{60} \times 100 \simeq 66{,}7\%$

Valores do sinal Q

$T = 120\,ms$

$F = \frac{1000}{120} \simeq 8$

$duty\ cycle = \frac{60}{120} \times 100\% = 50\%$

$T_{min} = 15 + 5 = 20\,ms$

$F_{max} = \frac{1000}{20} = 50\,MHz$

O circuito duplica o período do Clock.