1.

$t_H = 20\ ms$

$t_L = 20\ ms$

$T = 40\ ms$

$F = \frac{1}{40 \times 10^{-3}} = \frac{10^9}{40} = \frac{10^3}{40} \times 10^6 = 25 \times 10^6\ Hz = 25\ MHz$

$duty\ cycle = \frac{20}{40} \times 100\% = 50\%$

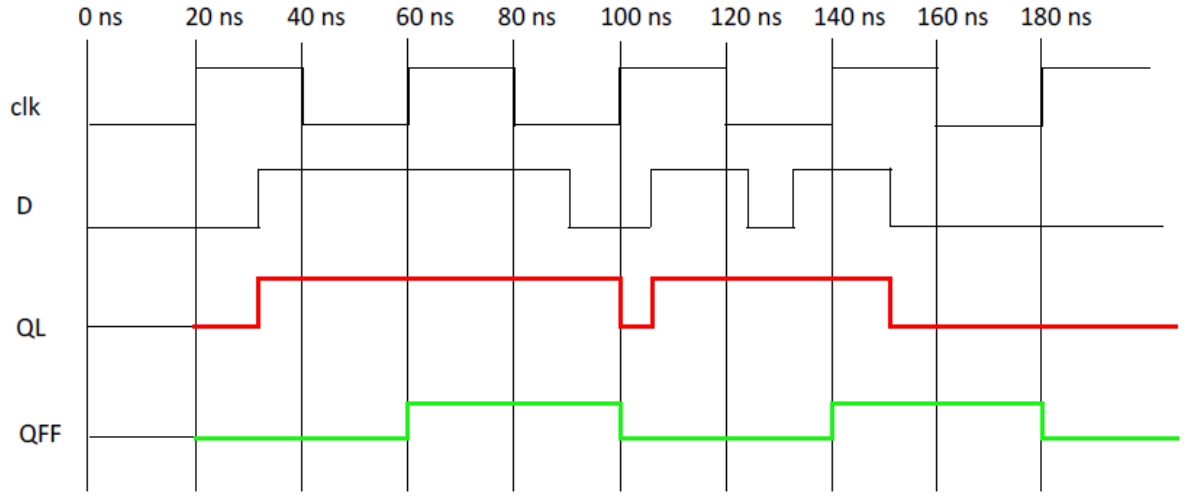


Fig. 1 – Functional behavior of a D latch and a positive-edge-triggered D flip-flop.

2

a) negative-edge-triggered D flip-flop

b) positive-edge-triggered D flip-flop

c) D-Latch

3

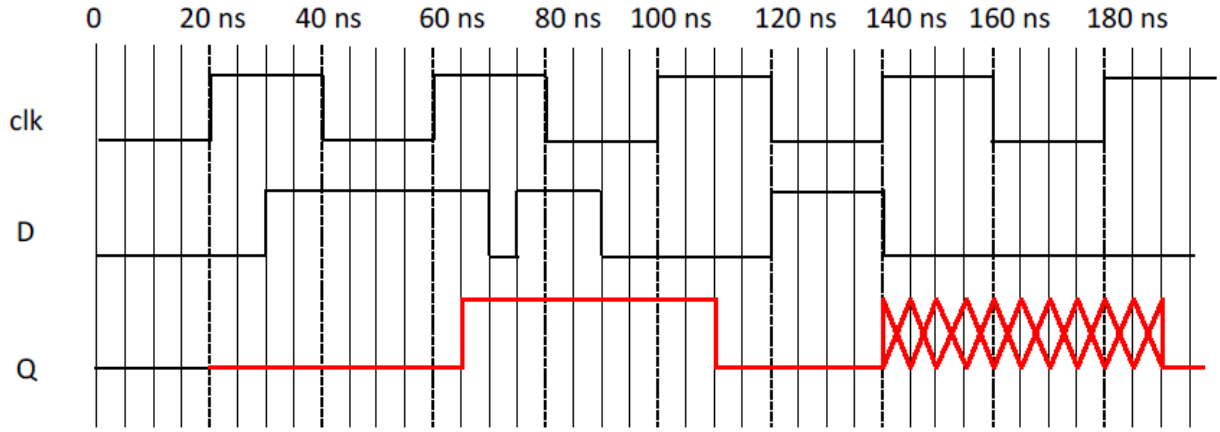


Fig. 3 – A timing diagram of a positive edge-triggered flip-flop to complete.

4

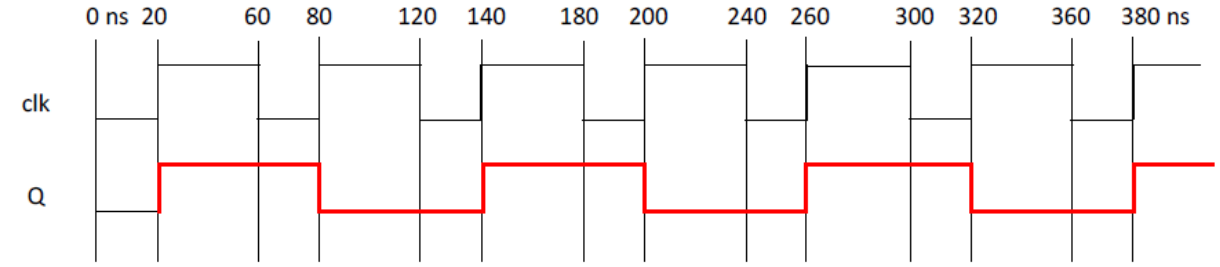


Fig. 4 – A circuit based on a D flip-flop and its timing diagram.

Valores do Clk

$T = 60\,ms$

$F = \frac{1000}{60} \simeq 16{,}7\,MHz$

$t_H = 40\,ms$

$duty\ cycle = \frac{40}{60} \times 100 \simeq 66{,}7\%$

Valores do sinal Q

$T = 120\,ms$

$F = \frac{1000}{120} \simeq 8$

$duty\ cycle = \frac{60}{120} \times 100\% = 50\%$

$T_{min} = 15 + 5 = 20\,ms$

$F_{max} = \frac{1000}{20} = 50\,MHz$

O circuito duplica o período do Clock.

5

a)

inputs -> x, clk

b)

Output -> $y = x \times Q_1$

c)

$Q_1^+ = D = Q0 \times \overline{x}$

$Q_0^+ = x$

d) Mealy -> Porque a saída depende da entrada

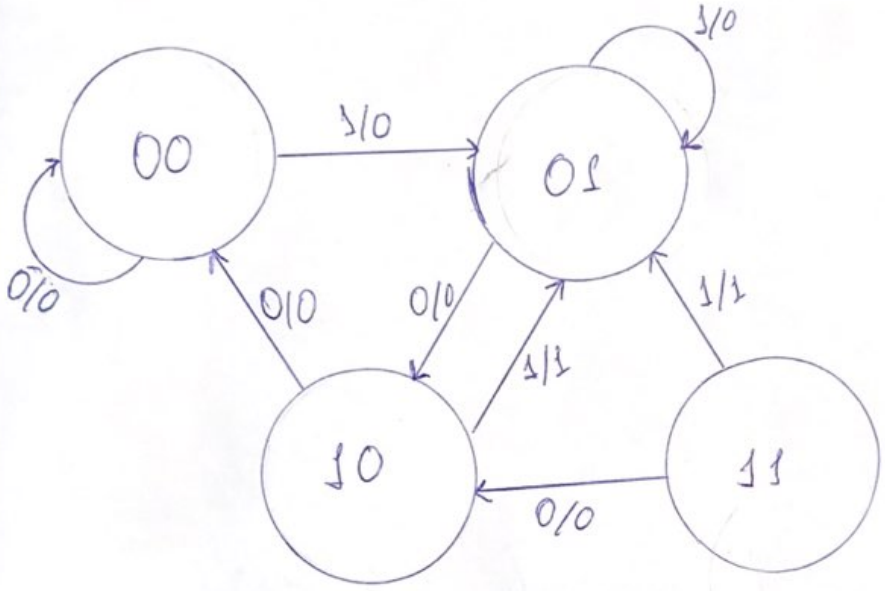
e)

Tabela de transição saídas

Q_1	Q_0	x	Q_1^+	Q_0^+	y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	1	0	0
0	1	1	0	1	0
1	0	0	0	0	0
1	0	1	0	1	1
1	1	0	1	0	0
1	1	1	0	1	1

f)

legenda: x/y



g)

O circuito detota a sequencia 101 aceitando sobreposição.

h)

$20MHz = \frac{1000}{x} <=> x = \frac{1000}{20} <=> x = 50ms$

$T = t_{setup} + t_{gate} + t_pHL <=>$

$50 = 15 + 25 + t_{gate} <=> 50 - 40 = t_{gate} <=>$

$t_{gate} = 10$

6

Máquina de Mealy porque a saída depende da entrada

$$T_{max} = 15 + 25 + 0 = 40\,ms$$

$$F = \frac{1000}{40} = 25\,MHz$$

Este diagrama pode estar errado.