TPS2660x 60-V, 2-A Industrial eFuse with Integrated Reverse Input Polarity Protection

1 Features

- 4.2 V to 55 V Operating Voltage, 60-V ABSmax
- Integrated Reverse Input Polarity Protection down to –60 V
  – Zero Additional Components Required
- Integrated Back to Back MOSFETs with 150-mΩ total RON
- 0.1 A to 2.23 A Adjustable current limit (±5% accuracy at 1 A)
- Load protection during Surge (IEC 61000-4-5) with minimum external components
- IMON Current Indicator Output (±8.5% accuracy)
- Low Quiescent Current, 300 µA in Operating, 20 µA in Shutdown
- Adjustable UVLO, OVP Cut Off, Output Slew Rate Control
- Reverse Current Blocking
- Fixed 38-V Over Voltage Clamp (TPS26602 only)
- Available in Easy-to-Use 16-Pin HTSSOP and 24-Pin VQFN Packages
- Selectable Current-Limiting Fault Response Options (Auto-Retry, Latch Off, Circuit Breaker Modes)
- UL 2367 Recognition Pending

2 Applications

- Programmable Logic Controller
- Distributed Control System (DCS)
- Control and Automation
- Redundant Supply ORing
- Industrial Surge Protection

3 Description

The TPS2660x devices are compact, feature rich high voltage eFuses with a full suite of protection features. The wide supply input range of 4.2 to 55 V allows control of many popular DC bus voltages. The device can withstand and protect the loads from positive and negative supply voltages up to ± 60 V. Integrated back to back FETs provide reverse current blocking feature making the device suitable for systems with output voltage holdup requirements during power fail and brownout conditions. Load, source and device protection are provided with many adjustable features including overcurrent, output slew rate and overvoltage, undervoltage thresholds. The internal robust protection control blocks along with the high voltage rating of the TPS2660x helps to simplify the system designs for Surge protection.

A shutdown pin provides external control for enabling and disabling the internal FETs as well as placing the device in a low current shutdown mode. For system status monitoring and downstream load control, the device provides fault and precise current monitor output. The MODE pin allows flexibility to configure the device between the three current-limiting fault responses (circuit breaker, latch off, and Auto-retry modes).

The devices are available in a 5-mm × 4.4-mm 16-pin HTSSOP as well as 5-mm x 4-mm 24-pin VQFN package and are specified over a –40°C to +125°C temperature range.

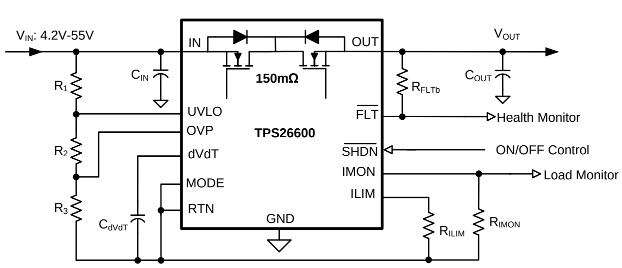
Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS26600 TPS26602	HTSSOP (16)	5.00 mm × 4.40 mm
TPS26600 TPS26601 TPS26602	VQFN (24)(2)	5.00 mm × 4.00 mm

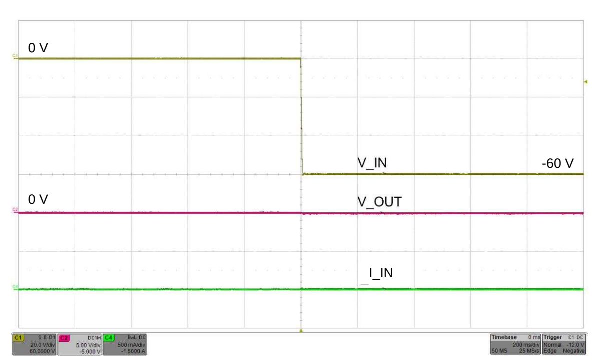
(1) For all available packages, see the orderable addendum at the end of the data sheet.

(2) Preview

Simplified Schematic



Reverse Input Polarity Protection at –60-V Supply



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4 Revision History

Changes from Original (July 2016) to Revision A — **Page**

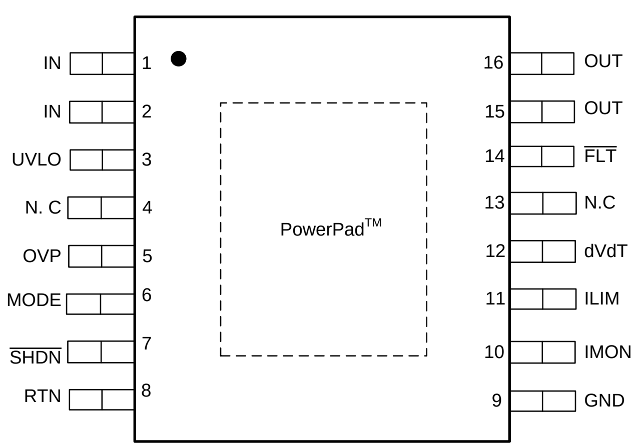
- Changed device status from *Product Preview* to *Production Data* ... 1

5 Device Comparison Table

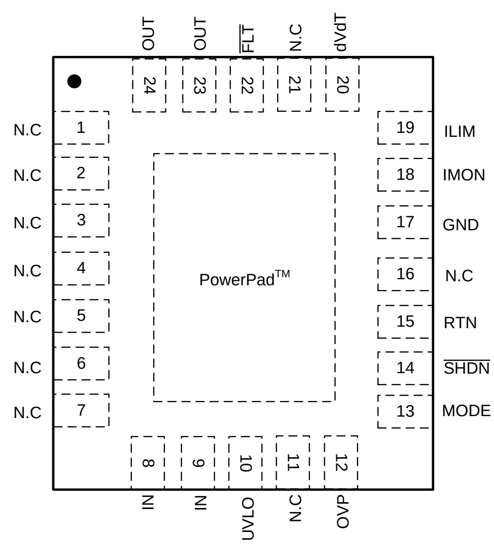
Part Number	Over Voltage Protection	Over Load Fault Response with MODE = Open
TPS26600	Over voltage cut-off, adjustable	Circuit breaker with auto-retry
TPS26601	Over voltage cut-off, adjustable	Circuit breaker with latch
TPS26602	Over voltage clamp, fixed (38 V)	Circuit breaker with auto-retry

6 Pin Configuration and Functions

PWP Package
16-Pin HTSSOP
Top View



RHF Package
24-Pin VQFN
Top View



Pin Functions

PIN			TYPE	DESCRIPTION
NAME	TPS26600/1/2			
	HTSSOP	VQFN		
dVdT	12	20	I/O	A capacitor from this pin to RTN sets output voltage slew rate See the *Hot Plug-In and In-Rush Current Control* section
$\overline{FLT}$	14	22	O	Fault event indicator. It is an open drain output. If unused, leave floating
GND	9	17	—	Connect GND to system ground
ILIM	11	19	I/O	A resistor from this pin to RTN sets the overload and short-circuit current limit. See the *Overload and Short Circuit Protection* section
IMON	10	18	O	Analog current monitor output. This pin sources a scaled down ratio of current through the internal FET. A resistor from this pin to RTN converts current to proportional voltage. If unused, leave it floating
IN	1-2	8-9	Power	Power input and supply voltage of the device
MODE	6	13	I	Mode selection pin for over load fault response. See the *Device Functional Modes* section
N.C.	4 , 13	1-7, 11, 21	—	No Connect
OUT	15-16	23-24	Power	Power output of the device
OVP	5	12	I	Input for setting the programmable overvoltage protection threshold (For TPS26600/1 Only). An overvoltage event turns-off the internal FET and asserts $\overline{FLT}$ to indicate the overvoltage fault. Connect OVP pin to RTN pin externally to select the internal default threshold. For Over voltage clamp response (TPS26602 Only) connect OVP to RTN externally

Pin Functions (continued)

PIN			TYPE	DESCRIPTION
NAME	TPS26600/1/2			
	HTSSOP	VQFN		
PowerPad™	—	—	—	PowerPad must be connected to RTN plane on PCB using multiple vias for enhanced thermal performance. Do not use PowerPad as the only electrical connection to RTN
RTN	8	15	—	Reference for device internal control circuits
$\overline{\text{SHDN}}$	7	14	I	Shutdown Pin. Pulling $\overline{\text{SHDN}}$ low makes the device to enter into low power shutdown mode. Cycling $\overline{\text{SHDN}}$ pin voltage resets the device that has latched off due to a fault condition
UVLO	3	10	I	Input for setting the programmable undervoltage lockout threshold. An undervoltage event turns-off the internal FET and asserts $\overline{\text{FLT}}$ to indicate the power-failure. Connect UVLO pin to RTN pin to select the internal default threshold

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (all voltages referred to GND (unless otherwise noted))(1)

		MIN	MAX	UNIT
IN , IN-OUT	Input voltage	–60	60	V
IN , IN-OUT (10 msec transient), T_A = 25 °C	Input voltage	–70	70	V
[IN, OUT, $\overline{FLT}$, UVLO, $\overline{SHDN}$] to RTN	Input voltage	–0.3	60	V
[OVP, dVdT, ILIM, IMON, MODE] to RTN	Input voltage	–0.3	5	V
RTN	Input voltage	–60	0.3	V
$I_{\overline{FLT}}$, I_{dVdT}, $I_{\overline{SHDN}}$	Sink current		10	mA
I_{dVdT}, I_{ILIM}, I_{IMON}	Source current	Internally limited		
T_J	Operating junction temperature	–40	150	°C
T_J	Transient junction temperature	–65	$T_{(TSD)}$	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (all voltages referred to GND (unless otherwise noted))

		MIN	NOM	MAX	UNIT
IN	Input voltage	–55		55	V
UVLO, OUT, $\overline{FLT}$	Input voltage	0		55	V
OVP, dVdT, ILIM, IMON, $\overline{SHDN}$	Input voltage	0		4	V
ILIM	Resistance	5.36		120	kΩ
IMON	Resistance	1			kΩ
IN, OUT	External capacitance	0.1			µF
dVdT	External capacitance	10			nF
– $dV_{(IN)}/dt$	$V_{(IN)}$ falling slew rate			20	V/µs
T_J	Operating junction temperature	–40	25	125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TPS2660 PWP (HTSSOP) 16 PINS	TPS2660 RHF (VQFN) 24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	38.6	30.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	22.7	20.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	18.2	7.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.5	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	18	7.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.5	1.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

–40°C ≤ T_A = T_J ≤ +125°C, $V_{(IN)}$ = 24 V, $V_{(\overline{SHDN})}$ = 2 V, $R_{(ILIM)}$ = 120 kΩ, IMON = $\overline{FLT}$ = OPEN, $C_{(OUT)}$ = 1 µF, $C_{(dVdT)}$ = OPEN. (All voltages referenced to GND, (unless otherwise noted))

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
$V_{(IN)}$	Operating input voltage		4.2		55	V
$V_{(PORR)}$	Internal POR threshold, rising		3.9	4	4.1	V
$V_{(PORHys)}$	Internal POR hysteresis		250	275	300	mV
$IQ_{(ON)}$	Supply current	Enabled: $V_{(\overline{SHDN})}$ = 2 V	190	300	390	µA
$IQ_{(OFF)}$		$V_{(\overline{SHDN})}$ = 0 V	11	20	33	µA
$I_{(VINR)}$	Reverse input supply current	$V_{(IN)}$ = –60 V, $V_{(OUT)}$ = 0 V			52	µA
$V_{(OVC)}$	Over voltage clamp	$V_{(IN)}$ > 42 V, TPS26602 only	36	37.5	40	V
UNDERVOLTAGE LOCKOUT (UVLO) INPUT						
$V_{(IN\_UVLO)}$	Factory set $V_{(IN)}$ undervoltage trip level	$V_{(IN)}$ rising, $V_{(UVLO)}$ = 0 V	14.25	14.9	15.75	V
		$V_{(IN)}$ falling, $V_{(UVLO)}$ = 0 V	13.25	13.8	14.75	
$V_{(SEL\_UVLO)}$	Internal UVLO select threshold		180	200	240	mV
$V_{(UVLOR)}$	UVLO threshold voltage, rising		1.175	1.19	1.225	V
$V_{(UVLOF)}$	UVLO threshold voltage, falling		1.095	1.1	1.125	V
$I_{(UVLO)}$	UVLO Input leakage current	0 V ≤ $V_{(UVLO)}$ ≤ 60 V	–100	0	100	nA
LOW IQ SHUTDOWN ($\overline{SHDN}$) INPUT						
$V_{(\overline{SHDN})}$	Output voltage	$I_{(\overline{SHDN})}$ = 0.1 µA	2	2.7	3.4	V
$V_{(SHUTF)}$	$\overline{SHDN}$ threshold voltage for low IQ shutdown, falling		0.55	0.76	0.94	V
$I_{(\overline{SHDN})}$	Leakage current	$V_{(\overline{SHDN})}$ = 0.4 V	–10			µA
OVER VOLTAGE PROTECTION (OVP) INPUT						
$V_{(IN\_OVP)}$	Factory set $V_{(IN)}$ over voltage trip level	$V_{(IN)}$ rising, $V_{(OVP)}$ = 0 V	31	32.6	34	V
		$V_{(IN)}$ falling, $V_{(OVP)}$ = 0 V	28.5	30.3	31.5	
$V_{(SEL\_OVP)}$	Internal OVP select threshold		180	200	240	mV
$V_{(OVPR)}$	Over-voltage threshold voltage, rising		1.175	1.19	1.225	V
$V_{(OVPF)}$	Over-voltage threshold, falling		1.095	1.1	1.125	V
$I_{(OVP)}$	OVP input leakage current	0 V ≤ $V_{(OVP)}$ ≤ 4 V	–100	0	100	nA
OUTPUT RAMP CONTROL (dVdT)						
$I_{(dVdT)}$	dVdT charging current	$V_{(dVdT)}$ = 0 V	4	4.7	5.5	µA
$R_{(dVdT)}$	dVdT discharging resistance	$V_{(\overline{SHDN})}$ = 0 V, with $I_{(dVdT)}$ = 10 mA sinking		14		Ω
$GAIN_{(dVdT)}$	dVdT to OUT gain	$V_{(OUT)}$ /$V_{(dVdT)}$	23.75	24.6	25.5	V/V
CURRENT LIMIT PROGRAMMING (ILIM)						
$V_{(ILIM)}$	ILIM bias voltage			1		V
$I_{(OL)}$	Overload current limit	$R_{(ILIM)}$ = 120 kΩ, $V_{(IN)}$ – $V_{(OUT)}$ = 1 V	0.085	0.1	0.115	A
		$R_{(ILIM)}$ = 12 kΩ, $V_{(IN)}$ – $V_{(OUT)}$ = 1 V	0.95	1	1.05	
		$R_{(ILIM)}$ = 8 kΩ, $V_{(IN)}$ – $V_{(OUT)}$ = 1 V	1.425	1.5	1.575	
		$R_{(ILIM)}$ = 5.36 kΩ, $V_{(IN)}$ – $V_{(OUT)}$ = 1 V	2.11	2.23	2.35	
$I_{(OL\_R-OPEN)}$		$R_{(ILIM)}$ = OPEN, Open resistor current limit (single point failure test: UL60950)		0.055		
$I_{(OL\_R-SHORT)}$		$R_{(ILIM)}$ = SHORT, Shorted resistor current limit (single point failure test: UL60950)		0.095		
$I_{(CB)}$	Circuit breaker detection threshold	$R_{(ILIM)}$ = 120 kΩ, MODE = open	0.045	0.073	0.11	A
		$R_{(ILIM)}$ = 5.36 kΩ, MODE = open	2	2.21	2.4	

Electrical Characteristics (continued)

–40°C ≤ T_A = T_J ≤ +125°C, $V_{(IN)}$ = 24 V, $V_{(\overline{SHDN})}$ = 2 V, $R_{(ILIM)}$ = 120 kΩ, IMON = $\overline{FLT}$ = OPEN, $C_{(OUT)}$ = 1 µF, $C_{(dVdT)}$ = OPEN. (All voltages referenced to GND, (unless otherwise noted))

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(SCL)}$	Short-circuit current limit	$R_{(ILIM)}$ = 120 kΩ, $V_{(IN)}$ – $V_{(OUT)}$ = 5 V	0.08	0.1	0.12	A
		$R_{(ILIM)}$ = 8 kΩ, $V_{(IN)}$ – $V_{(OUT)}$ = 5 V	1.425	1.5	1.575	
		$R_{(ILIM)}$ = 5.36 kΩ, $V_{(IN)}$ – $V_{(OUT)}$ = 5 V	2.11	2.23	2.35	
$I_{(FASTRIP)}$	Fast-trip comparator threshold			1.87 × $I_{(OL)}$ + 0.015		A
CURRENT MONITOR OUTPUT (IMON)						
$GAIN_{(IMON)}$	Gain factor $I_{(IMON)}$:$I_{(OUT)}$	0.1 A ≤ $I_{(OUT)}$ ≤ 2 A	72	78.28	85	µA/A
PASS FET OUTPUT (OUT)						
R_{ON}	IN to OUT total ON resistance	0.1 A ≤ $I_{(OUT)}$ ≤ 2 A, T_J = 25°C	140	150	160	mΩ
		0.1 A ≤ $I_{(OUT)}$ ≤ 2 A, T_J = 85°C			210	
		0.1 A ≤ $I_{(OUT)}$ ≤ 2 A, –40°C ≤ T_J ≤ +125°C	80	150	250	
$I_{lkg(OUT)}$	OUT leakage current in Off state	$V_{(IN)}$ = 60 V, $V_{(\overline{SHDN})}$= 0 V, $V_{(OUT)}$ = 0 V, sourcing			12	µA
		$V_{(IN)}$ = 0 V, $V_{(\overline{SHDN})}$= 0 V, $V_{(OUT)}$ = 24 V, sinking			11	
		$V_{(IN)}$ = –60 V, $V_{(\overline{SHDN})}$= 0 V, $V_{(OUT)}$ = 0 V, sinking			35	
$V_{(REVTH)}$	$V_{(IN)}$ – $V_{(OUT)}$ threshold for reverse protection comparator, falling		–15	–10	–5	mV
$V_{(FWDTH)}$	$V_{(IN)}$ – $V_{(OUT)}$ threshold for reverse protection comparator, rising		85	96	110	mV
FAULT FLAG ($\overline{FLT}$): ACTIVE LOW						
$R_{(\overline{FLT})}$	$\overline{FLT}$ Pull-down resistance	$V_{(OVP)}$ = 2 V, $I_{(\overline{FLT})}$ = 5 mA sinking	40	85	160	Ω
$I_{(\overline{FLT})}$	$\overline{FLT}$ Input leakage current	0 V ≤ $V_{(\overline{FLT})}$ ≤ 60 V	–100		100	nA
THERMAL SHUT DOWN (TSD)						
$T_{(TSD)}$	TSD threshold, rising			157		ºC
$T_{(TSDhyst)}$	TSD hysteresis			10		ºC
MODE						
MODE_SEL	Thermal fault mode selection	MODE = 402 kΩ to RTN	Current limiting with Latch			
		MODE = Open	Circuit breaker mode with auto-retry			
		MODE = Open (TPS26601 only)	Circuit breaker mode with latch			
		MODE = Short to RTN	Current limiting with Auto-retry			

7.6 Timing Requirements

–40°C ≤ T_A = T_J ≤ +125°C, $V_{(IN)}$ = 24 V, $V_{(\overline{SHDN})}$ = 2 V, $R_{(ILIM)}$ = 120 kΩ, IMON = $\overline{FLT}$ = OPEN, $C_{(OUT)}$ = 1 µF, $C_{(dVdT)}$ = OPEN. (All voltages referenced to GND, (unless otherwise noted))

			MIN	NOM	MAX	UNIT
IN and UVLO INPUT						
$UVLO\_t_{ON(dly)}$	UVLO turnon delay	UVLO↑ (100 mV above $V_{(UVLOR)}$) to $V_{(OUT)}$ = 100 mV, $C_{(dvdt)}$ = open		250		µs
		UVLO↑ (100 mV above $V_{(UVLOR)}$) to $V_{(OUT)}$ = 100 mV, $C_{(dvdt)}$ ≥ 10 nF, [$C_{(dvdt)}$ in nF]		250 + 14.5 × $C_{(dvdt)}$		µs
$UVLO\_t_{off(dly)}$	UVLO turnoff delay	UVLO↓ (100 mV below $V_{(UVLOF)}$) to $\overline{FLT}$↓		10		µs
SHUTDOWN CONTROL INPUT ($\overline{SHDN}$)						
$t_{SD(dly)}$	SHUTDOWN exit delay	$\overline{SHDN}$↑ to $V_{(OUT)}$ = 100 mV, $C_{(dvdt)}$ ≥ 10 nF, [$C_{(dvdt)}$ in nF]		250 + 14.5 × $C_{(dvdt)}$		µs
		$\overline{SHDN}$↑ to $V_{(OUT)}$ = 100 mV, $C_{(dvdt)}$ = open		250		µs
	SHUTDOWN entry delay	$\overline{SHDN}$↓ (below $V_{(SHUTF)}$) to $\overline{FLT}$↓		10		µs
OVER VOLTAGE PROTECTION INPUT (OVP)						
$t_{OVP(dly)}$	OVP exit delay	OVP↓ (20 mV below $V_{(OVPF)}$) to $V_{(OUT)}$ = 100 mV, TPS26600 & TPS26601 only		200		µs
	OVP disable delay	OVP↑ (20 mV above $V_{(OVPR)}$) to $\overline{FLT}$↓, TPS26600 and TPS26601 only		6		µs
CURRENT LIMIT						
$t_{FASTTRIP(dly)}$	Fast-trip comparator delay	$I_{(OUT)}$ > $I_{(FASTRIP)}$		250		ns
REVERSE PROTECTION COMPARATOR						
$t_{REV(dly)}$	Reverse protection comparator delay	($V_{(IN)}$ – $V_{(OUT)}$)↓ (100 mV overdrive below $V_{(REVTH)}$) to internal FET turn OFF		1.5		µs
		($V_{(IN)}$ – $V_{(OUT)}$)↓ (10 mV overdrive below $V_{(REVTH)}$) to $\overline{FLT}$↓		45		µs
$t_{FWD(dly)}$		($V_{(IN)}$ – $V_{(OUT)}$)↑ (10 mV overdrive above $V_{(FWDTH)}$) to $\overline{FLT}$↑		70		µs
THERMAL SHUTDOWN						
t_{retry}	Retry delay in TSD			512		ms
OUTPUT RAMP CONTROL (dVdT)						
t_{dVdT}	Output ramp time	$\overline{SHDN}$↑ to $V_{(OUT)}$ = 23.9 V, with $C_{(dVdT)}$ = 47 nF		10		ms
		$\overline{SHDN}$↑ to $V_{(OUT)}$ = 23.9 V, with $C_{(dVdT)}$ = open		1.6		ms
FAULT FLAG ($\overline{FLT}$)						
$t_{CB(dly)}$	$\overline{FLT}$ assertion delay in circuit breaker mode	MODE = OPEN, delay from $I_{(OUT)}$ > $I_{(OL)}$ to $\overline{FLT}$↓		4		ms
$t_{CBretry(dly)}$)	Retry delay in circuit breaker mode	MODE = OPEN		540		ms
t_{PGOODF}	PGOOD delay (de-glitch) time	Falling edge		875		µs
t_{PGOODR}		Rising edge, $C_{(dVdT)}$ = open		1400		µs
		Rising egde, $C_{(dVdT)}$ ≥ 10 nF, [$C_{(dvdt)}$ in nF]		875 + 20 × $C_{(dVdT)}$		µs

7.7 Typical Characteristics

–40°C ≤ T_A = T_J ≤ +125°C, $V_{(IN)}$ = 24 V, $V_{(\overline{SHDN})}$ = 2 V, $R_{(ILIM)}$ = 120 kΩ, IMON = $\overline{FLT}$ = OPEN, $C_{(OUT)}$ = 1 µF, $C_{(dVdT)}$ = OPEN. (Unless stated otherwise)

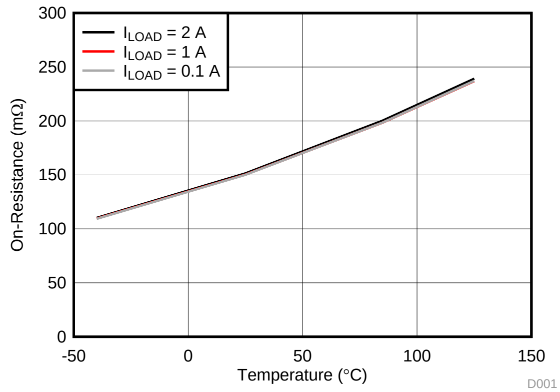


Figure 1. On-Resistance vs Temperature Across Load Current

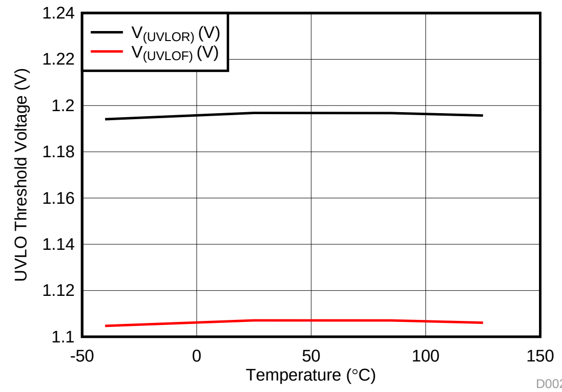


Figure 2. UVLO Threshold Voltage vs Temperature

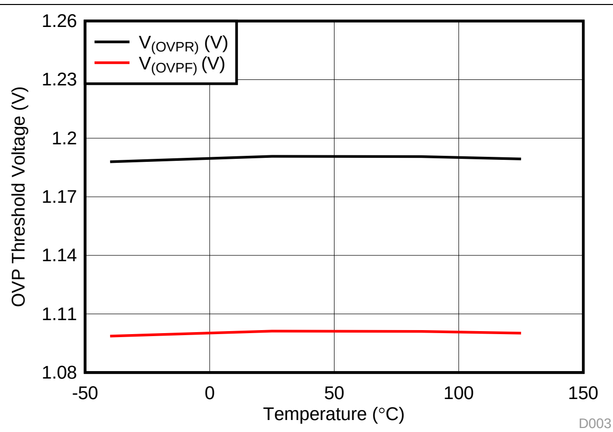


Figure 3. OVP Threshold Voltage vs Temperature

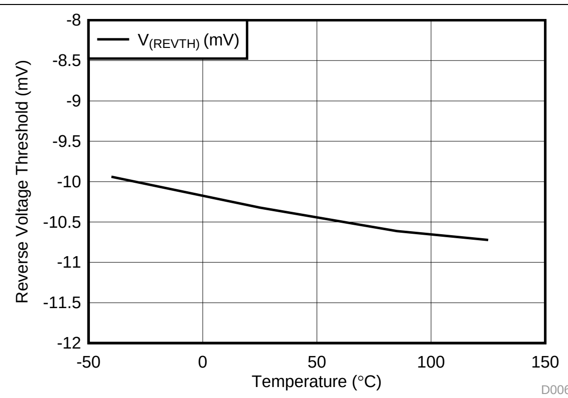


Figure 4. Reverse Voltage Threshold vs Temperature

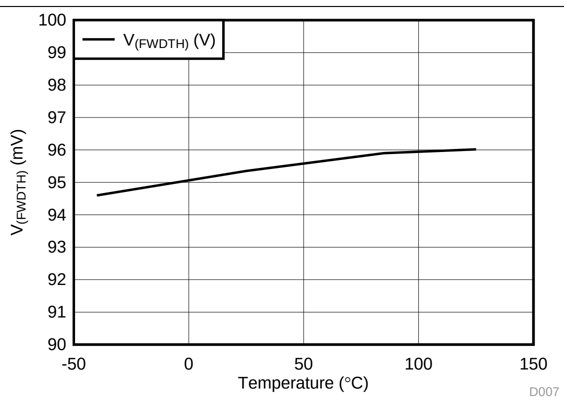


Figure 5. $V_{(FWDTH)}$ vs Temperature

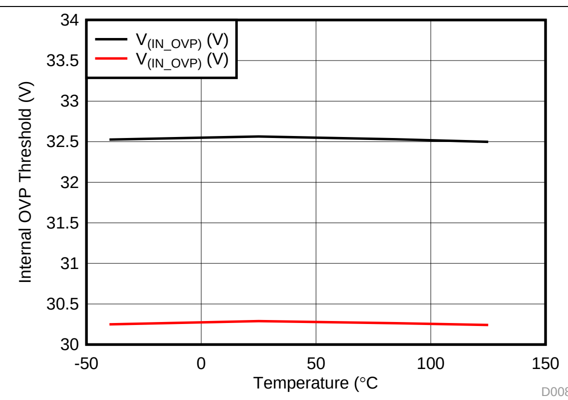


Figure 6. Internal OVP Threshold vs Temperature

Typical Characteristics (continued)

–40°C ≤ T_A = T_J ≤ +125°C, $V_{(IN)}$ = 24 V, $V_{(\overline{SHDN})}$ = 2 V, $R_{(ILIM)}$ = 120 kΩ, IMON = $\overline{FLT}$ = OPEN, $C_{(OUT)}$ = 1 µF, $C_{(dVdT)}$ = OPEN. (Unless stated otherwise)

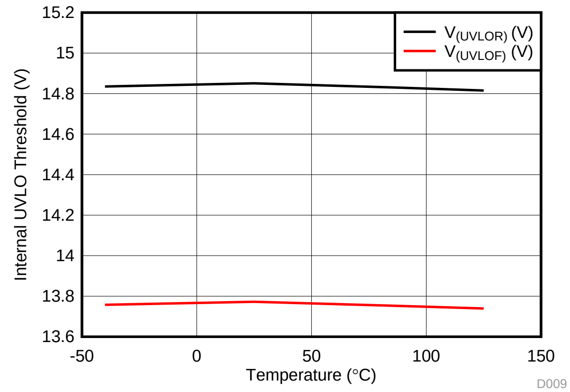


Figure 7. Internal UVLO Threshold vs Temperature

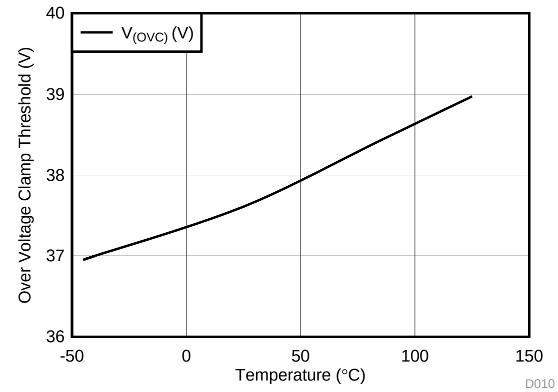


Figure 8. Overvoltage Clamp Threshold vs Temperature

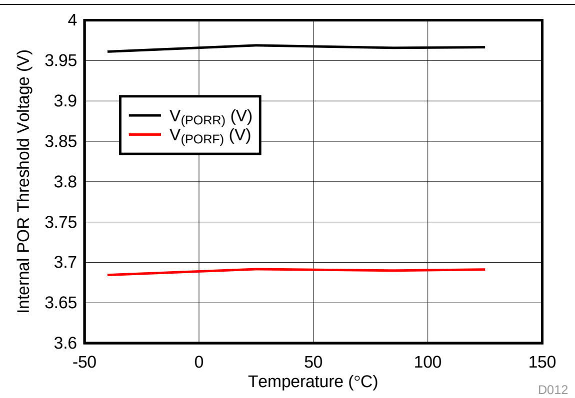


Figure 9. Internal POR Threshold Voltage vs Temperature

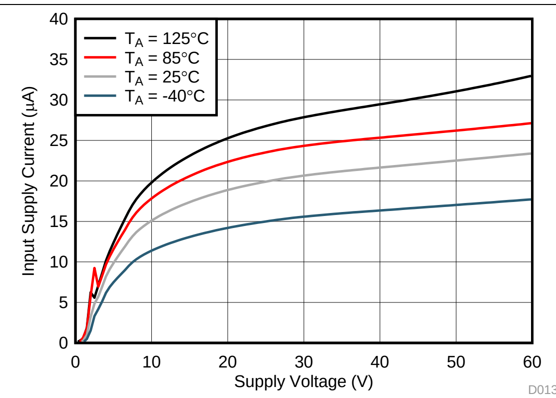


Figure 10. Input Supply Current vs Supply Voltage in Shutdown

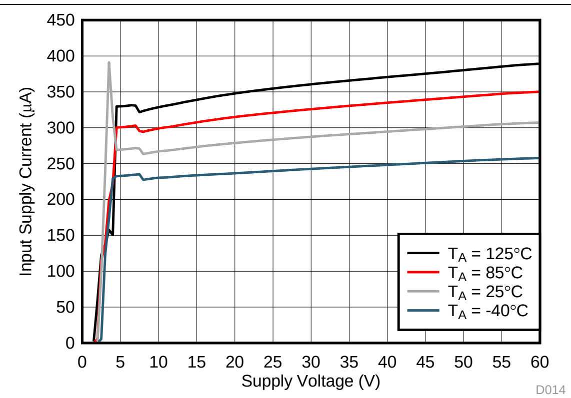
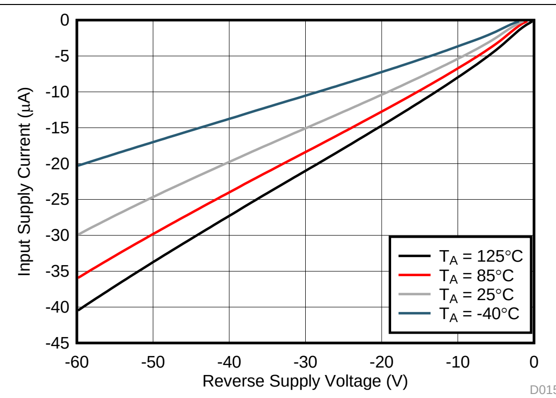


Figure 11. Input Supply Current vs Supply Voltage During Normal Operation



$V_{(OUT)}$ = 0 V

Figure 12. Input Supply Current vs Reverse Supply Voltage, – $V_{(IN)}$

Typical Characteristics (continued)

–40°C ≤ T_A = T_J ≤ +125°C, $V_{(IN)}$ = 24 V, $V_{(\overline{SHDN})}$= 2 V, $R_{(ILIM)}$ = 120 kΩ, IMON = $\overline{FLT}$ = OPEN, $C_{(OUT)}$ = 1 µF, $C_{(dVdT)}$ = OPEN. (Unless stated otherwise)

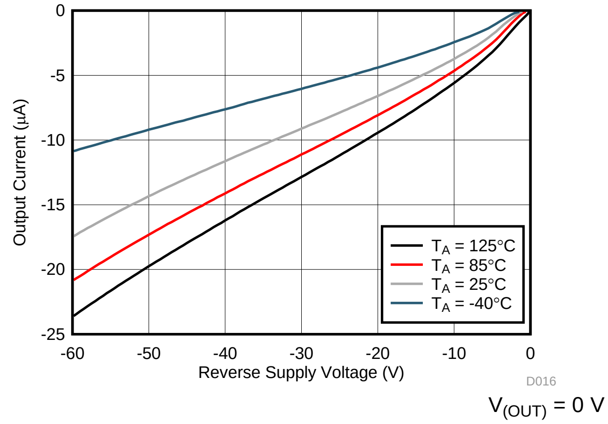


Figure 13. Output Current vs Reverse Supply Voltage, – $V_{(IN)}$

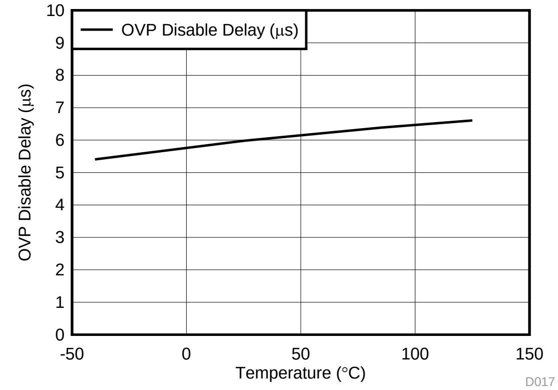


Figure 14. OVP Disable Delay vs Temperature

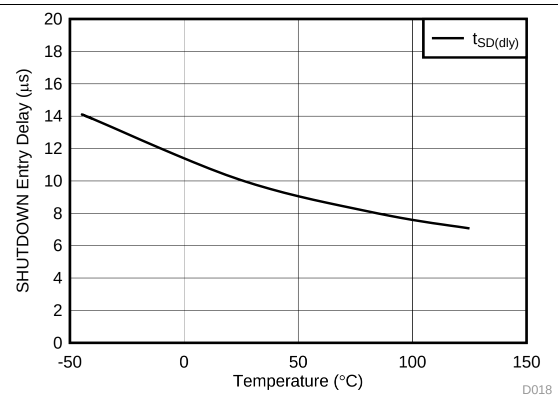


Figure 15. SHUTDOWN Entry Delay vs Temperature

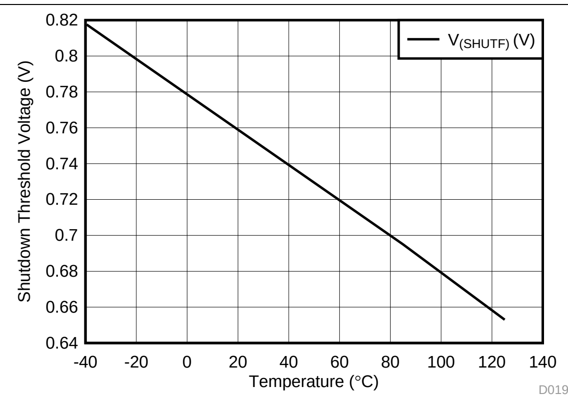


Figure 16. Shutdown Threshold Voltage Shutdown vs Temperature

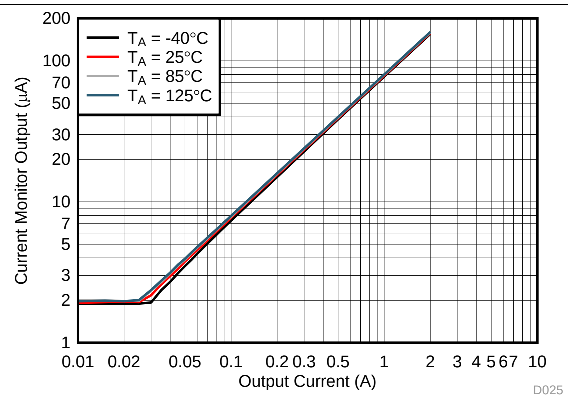


Figure 17. Current Monitor Output vs Output Current

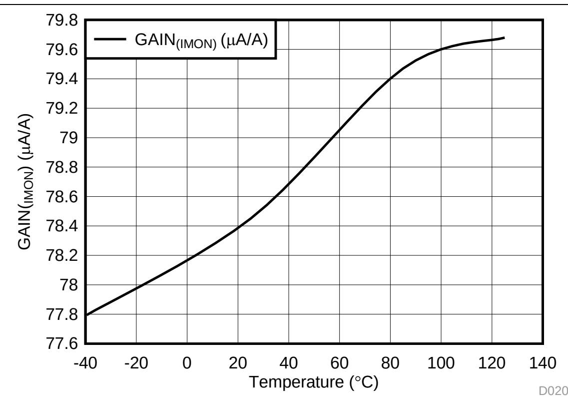


Figure 18. $GAIN_{(IMON)}$ vs Temperature

Typical Characteristics (continued)

–40°C ≤ T_A = T_J ≤ +125°C, $V_{(IN)}$ = 24 V, $V_{(\overline{SHDN})}$= 2 V, $R_{(ILIM)}$ = 120 kΩ, IMON = $\overline{FLT}$ = OPEN, $C_{(OUT)}$ = 1 µF, $C_{(dVdT)}$ = OPEN. (Unless stated otherwise)

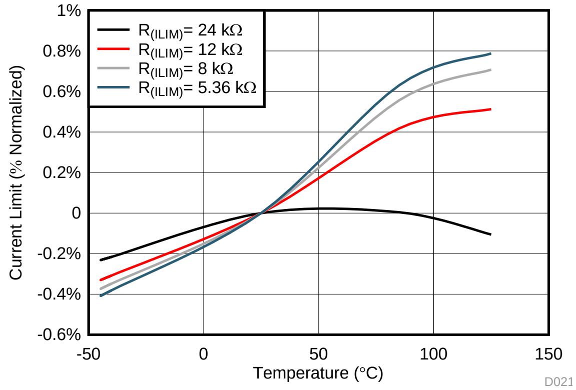


Figure 19. Current Limit (% Normalized) vs Temperature

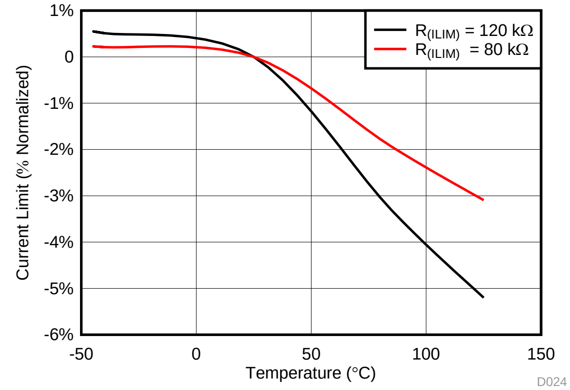


Figure 20. Current Limit (% Normalized) vs Temperature

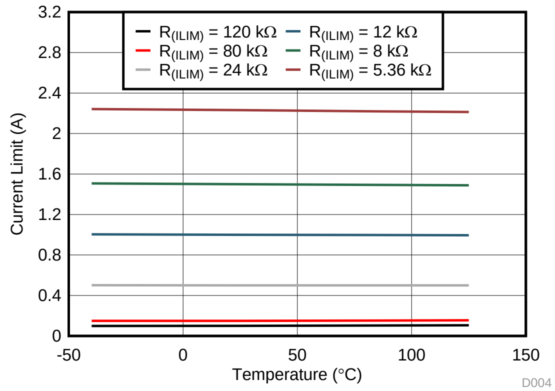


Figure 21. Over Load Current Limit vs Temperature

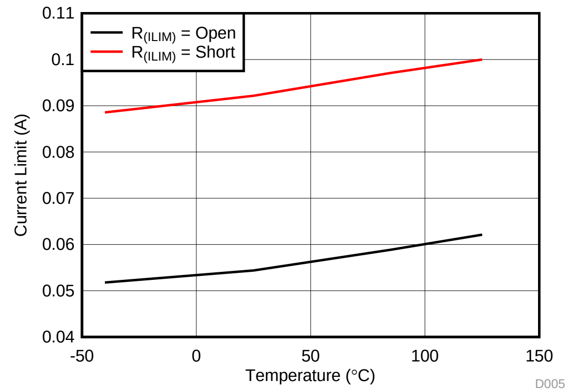


Figure 22. Current Limit for $R_{(ILIM)}$ = Open and Short vs Temperature

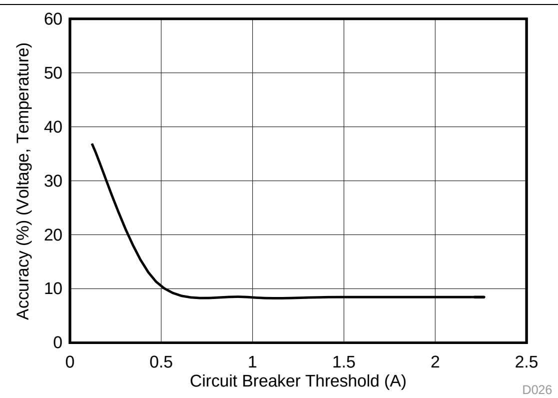


Figure 23. Circuit Breaker Threshold Accuracy vs Circuit Breaker Threshold $I_{(CB)}$

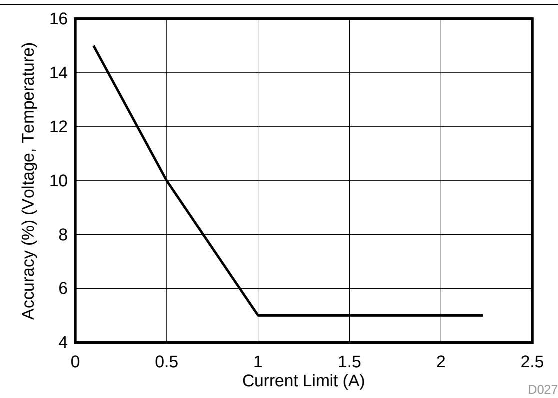


Figure 24. Current Limit Accuracy vs Current Limit, $I_{(OL)}$

Typical Characteristics (continued)

–40°C ≤ T_A = T_J ≤ +125°C, $V_{(IN)}$ = 24 V, $V_{(\overline{SHDN})}$= 2 V, $R_{(ILIM)}$ = 120 kΩ, IMON = $\overline{FLT}$ = OPEN, $C_{(OUT)}$ = 1 µF, $C_{(dVdT)}$ = OPEN. (Unless stated otherwise)

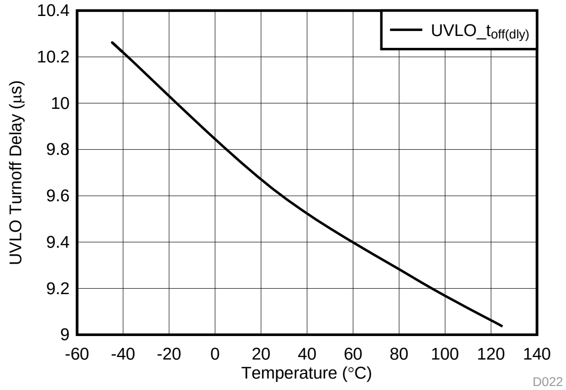
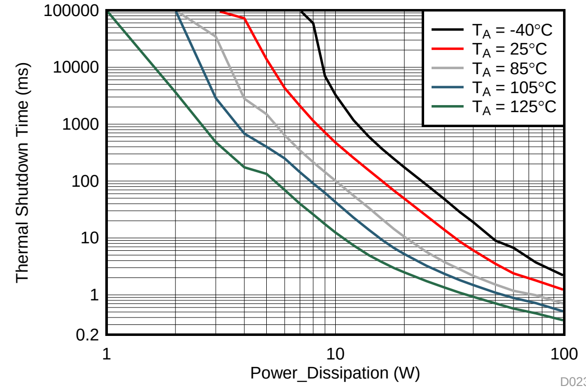
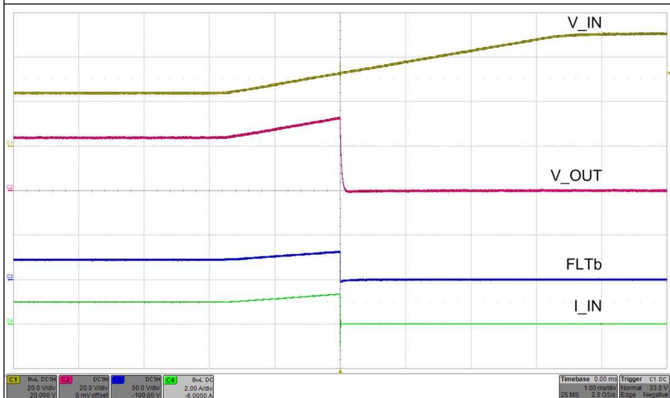


Figure 25. UVLO Turnoff delay vs Temperature



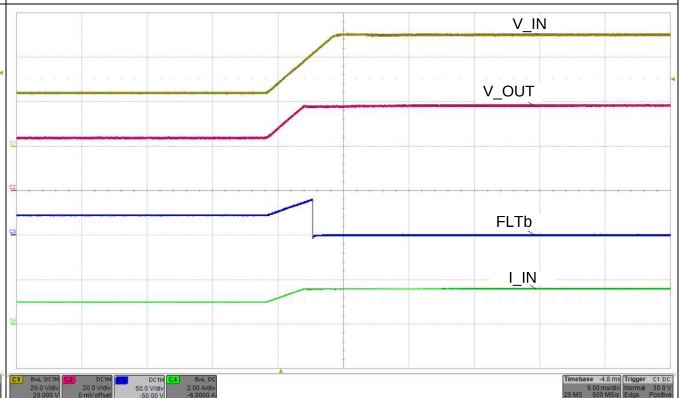
Taken on 2-Layer board, 2 oz.(0.08-mm thick) with HTSSOP device with RTN plane area: 1 cm^2 (Top) and 4.6 cm^2 (Bottom)

Figure 26. Thermal Shutdown Time vs Power Dissipation



R_{ILIM} = 5.36 kΩ OVP connected to RTN R_{FLTb} = 100 kΩ R_{LOAD} = 24 Ω

Figure 27. OVP Over Voltage Cut-Off Response

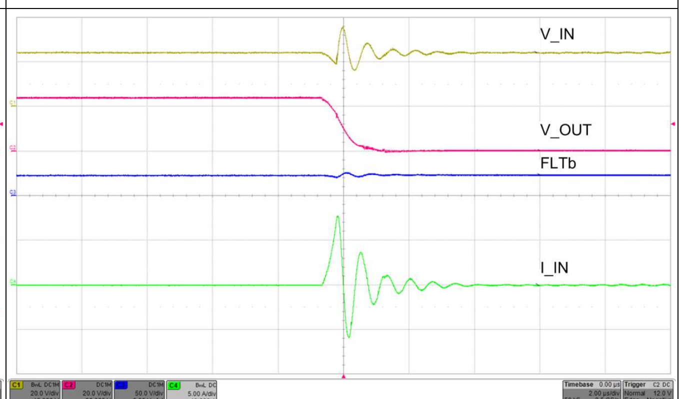


R_{ILIM} = 5.36 kΩ R_{FLTb} = 100 kΩ R_{LOAD} = 24 Ω

Figure 28. OV Clamp Response (TPS26602 Only)

R_{ILIM} = 5.36 kΩ R_{FLTb} = 100 kΩ

Figure 29. Hot-Short: Fast Trip Response and Current Regulation

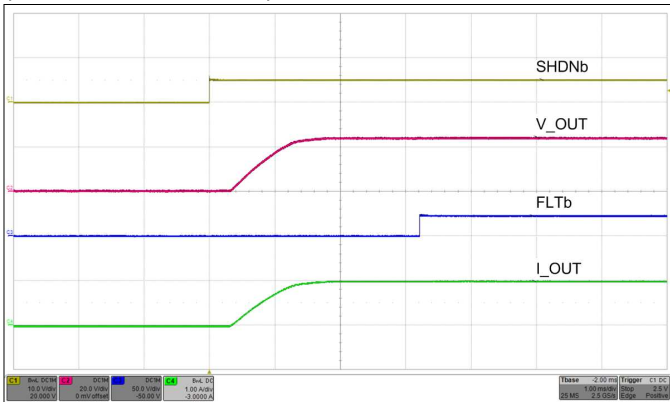


R_{ILIM} = 5.36 kΩ

Figure 30. Hot-Short: Fast Trip Response (Zoomed)

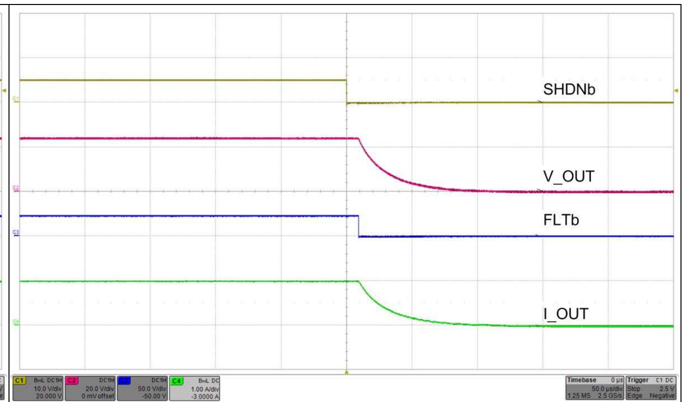
Typical Characteristics (continued)

–40°C ≤ T_A = T_J ≤ +125°C, $V_{(IN)}$ = 24 V, $V_{(\overline{SHDN})}$= 2 V, $R_{(ILIM)}$ = 120 kΩ, IMON = $\overline{FLT}$ = OPEN, $C_{(OUT)}$ = 1 µF, $C_{(dVdT)}$ = OPEN. (Unless stated otherwise)



R_{ILIM} = 5.36 kΩ R_{FLTb} = 100 kΩ R_{LOAD} = 24 Ω

Figure 31. Turnon Control with $\overline{SHDN}$



R_{ILIM} = 5.36 kΩ R_{FLTb} = 100 kΩ R_{LOAD} = 24 Ω

Figure 32. Turnoff Control with $\overline{SHDN}$

8 Parameter Measurement Information

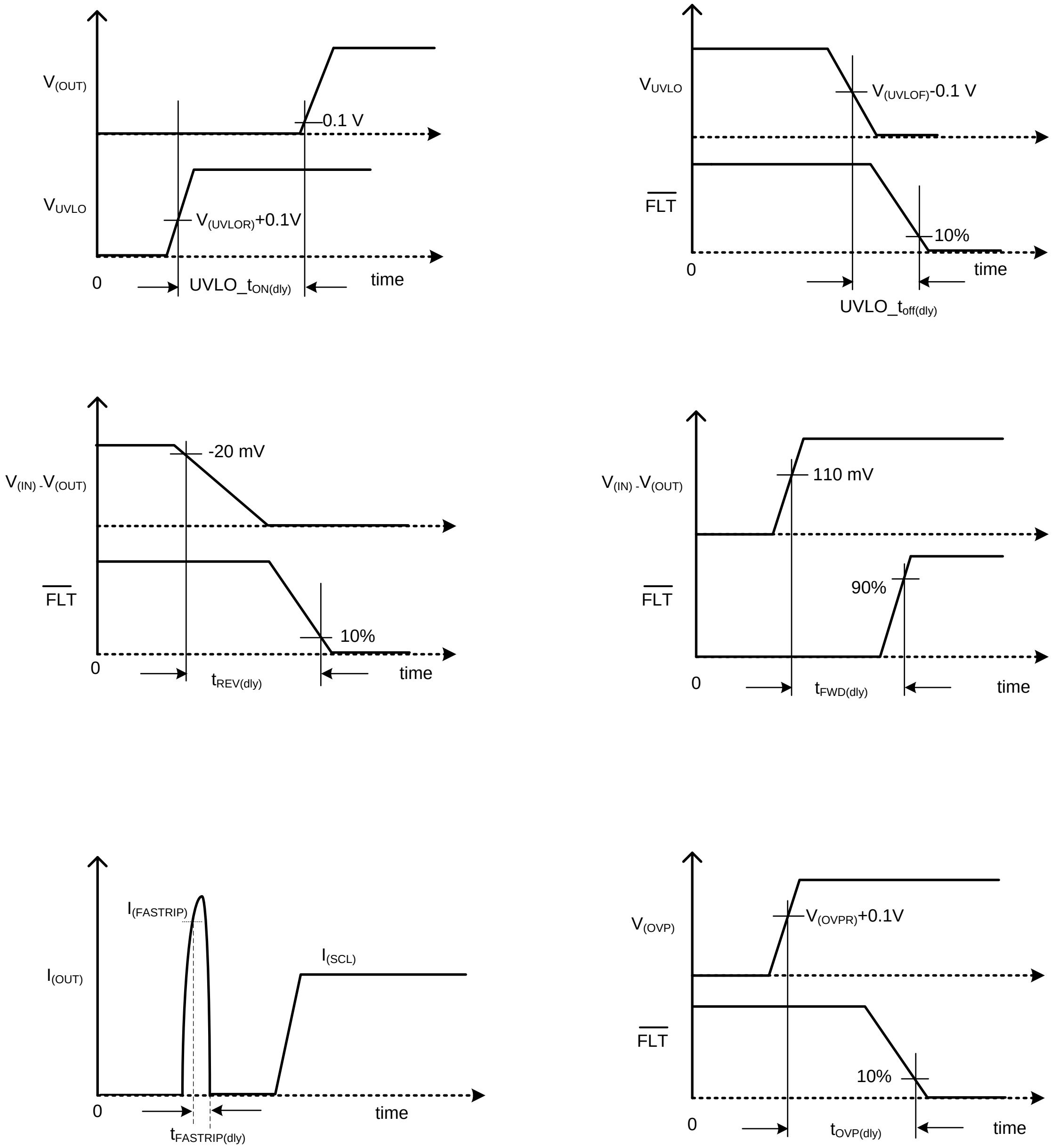


Figure 33. Timing Waveforms

9 Detailed Description

9.1 Overview

The TPS2660x is a family of high voltage industrial eFuses with integrated back-to-back MOSFETs and enhanced built-in protection circuitry. It provides robust protection for all systems and applications powered from 4.2 V to 55 V. The device can withstand ±60 V positive and negative supply voltages without damage. For hot-pluggable boards, the device provides hot-swap power management with in-rush current control and programmable output voltage slew rate features. Load, source and device protections are provided with many programmable features including overcurrent, overvoltage, undervoltage. The precision overcurrent limit (±5% at 1 A) helps to minimize over design of the input power supply, while the fast response short circuit protection 250 ns (typical) immediately isolates the faulty load from the input supply when a short circuit is detected.

The internal robust protection control blocks of the TPS2660x along with its ± 60 V rating helps to simplify the system designs for the surge compliance ensuring complete protection of the load and the device.

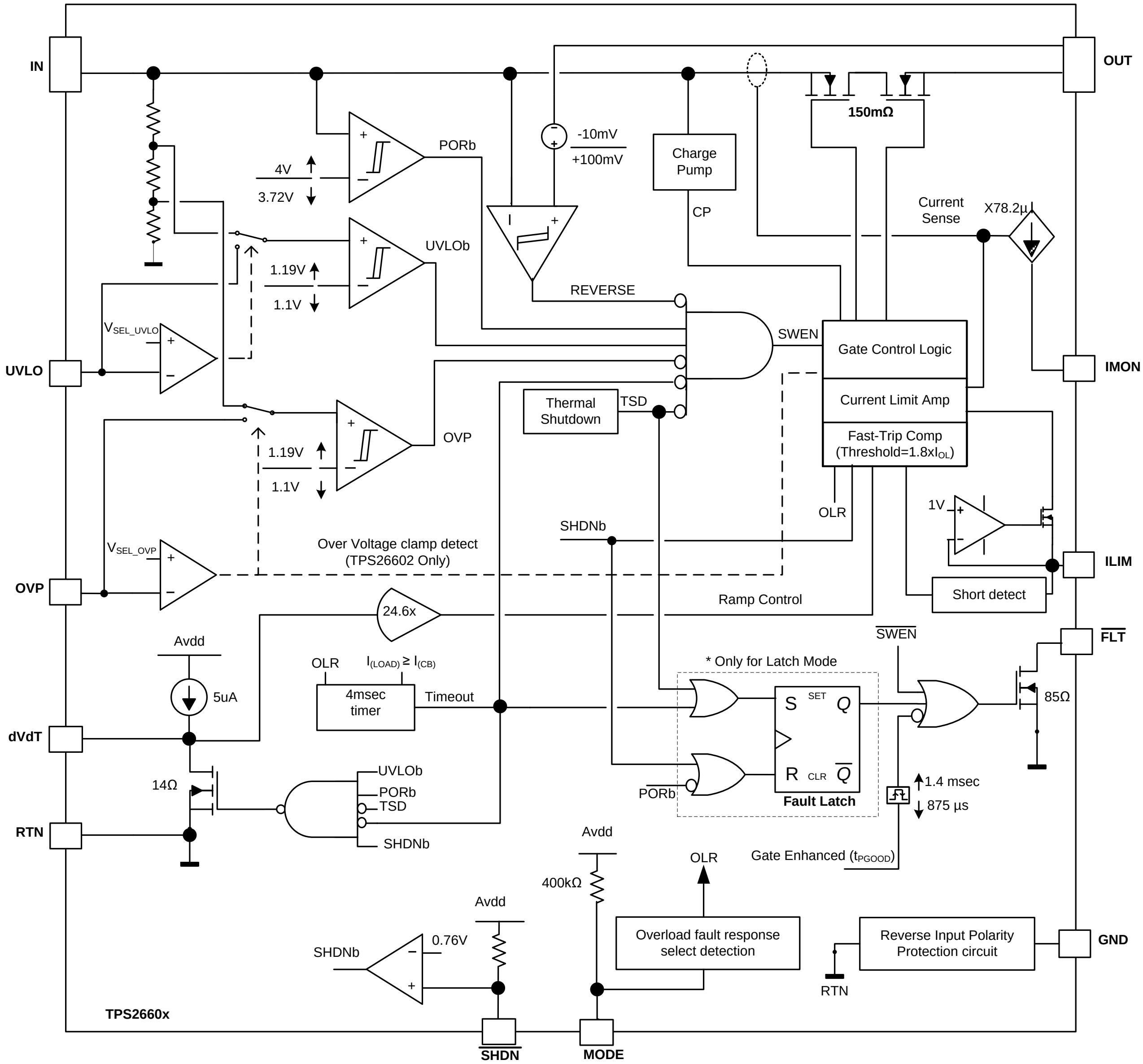
The device provides precise monitoring of voltage bus for brown-out and overvoltage conditions and asserts fault signal for the downstream system. The TPS2660x monitor functions threshold accuracy of ±3% ensures tight supervision of the supply bus, eliminating the need for a separate supply voltage supervisor chip.

The device monitors $V_{(IN)}$ and $V_{(OUT)}$ to provide true reverse current blocking when a reverse condition or input power failure condition is detected. The TPS2660x is also designed to control redundant power supply systems. A pair of TPS2660x devices can be configured for Active ORing between the main power supply and the auxiliary power supply, (see the *System Examples* section).

Additional features of the TPS2660x include:

- Current monitor output for health monitoring of the system
- Electronic circuit breaker operation with overload timeout using MODE pin
- A choice of latch off or automatic restart mode response during current limit fault using MODE pin
- Over temperature protection to safely shutdown in the event of an overcurrent event
- De-glitched fault reporting for brown-out and overvoltage faults
- Look ahead overload current fault indication (see the *Look Ahead Overload Current Fault Indicator* section)

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Undervoltage Lockout (UVLO)

Undervoltage comparator input. When the voltage at UVLO pin falls below $V_{(UVLOF)}$ during input power fail or input undervoltage fault, the internal FET quickly turns off and $\overline{FLT}$ is asserted. The UVLO comparator has a hysteresis of 90 mV. To set the input UVLO threshold, connect a resistor devider network from IN supply to UVLO terminal to RTN as shown in Figure 34.

Feature Description (continued)

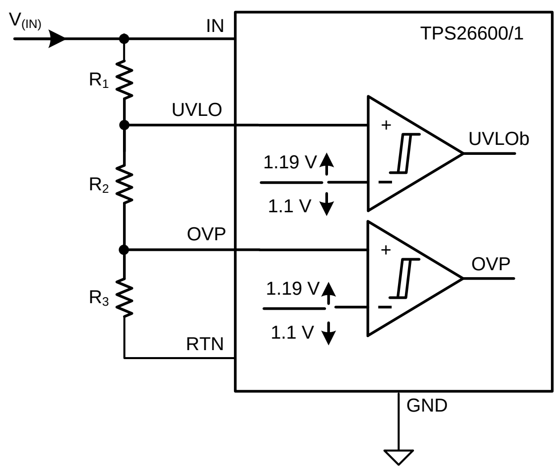


Figure 34. UVLO and OVP Thresholds Set by R_1, R_2 and R_3

The TPS2660x also features a factory set 15-V input supply undervoltage lockout $V_{(IN\_UVLO)}$ threshold with 1 V hysteresis. This feature can be enabled by connecting the UVLO terminal directly to the RTN terminal. If the Under-Voltage Lock-Out function is not needed, the UVLO terminal must be connected to the IN terminal. UVLO terminal must not be left floating.

The device also implements an internal power ON reset (POR) function on the IN terminal. The device disables the internal circuitry when the IN terminal voltage falls below internal POR threshold $V_{(PORF)}$. The internal POR threshold has a hysteresis of 275 mV.

9.3.2 Overvoltage Protection (OVP)

The TPS2660x incorporate circuitry to protect the system during overvoltage conditions. The TPS26600 and TPS26601 feature over voltage cut off functionality. A voltage more than $V_{(OVPR)}$ on OVP pin turns off the internal FET and protects the downstream load. To program the OVP threshold externally, connect a resistor divider from IN supply to OVP terminal to RTN as shown in Figure 34. The TPS26600 and TPS26601 also feature a factory set 33-V Input overvoltage cut off $V_{(IN\_OVP)}$ threshold with a 2-V hysteresis. This feature can be enabled by connecting the OVP terminal directly to the RTN terminal. Figure 27 illustrates the over voltage cut-off functionality.

The TPS26602 features an internally fixed 38 V overvoltage clamp (V_{OVC}) functionality. The OVP terminal of the TPS26602 must be connected to the RTN terminal directly. The TPS26602 clamps the output voltage to V_{OVC}, when the input voltage exceeds 38 V. During the output voltage clamp operation, the power dissipation in the internal MOSFET is $P_D = (V_{IN} – V_{OVC}) \times I_{OUT}$. Excess power dissipation for prolonged period can make the device to enter into thermal shutdown. Figure 28 illustrates the over voltage clamp functionality.

9.3.3 Reverse Input Supply Protection

To protect the electronic systems from reverse input supply due to mis-wiring, often a power component like a schottky diode is added in series with the supply line as shown in Figure 35. These additional discretes result in a lossy and bulky protection solution. The TPS2660x devices feature fully integrated reverse input supply protection and does not need an additional diode. These devices can withstand –60 V reverse voltage without damage. Figure 36 illustrates the reverse input polarity protection functionality.

Feature Description (continued)

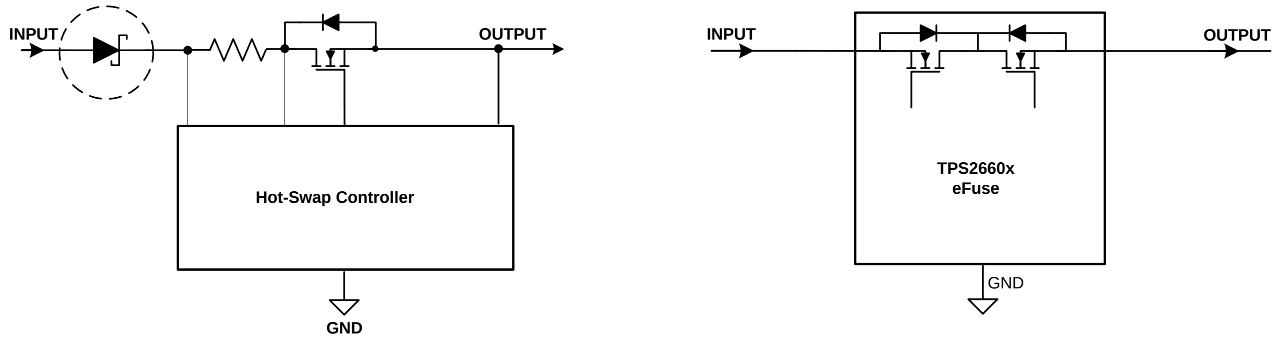


Figure 35. Reverse Input Supply Protection Circuits - Discrete vs TPS2660x

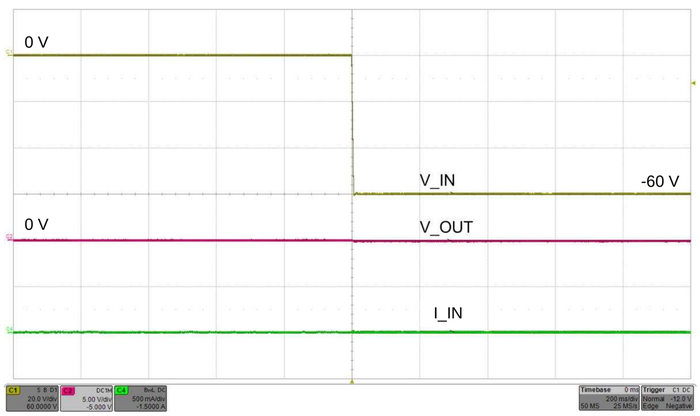


Figure 36. Reverse Input Supply Protection at –60 V

9.3.4 Hot Plug-In and In-Rush Current Control

The devices are designed to control the in-rush current upon insertion of a card into a live backplane or other "hot" power source. This limits the voltage sag on the backplane's supply voltage and prevents unintended resets of the system power. The controlled start up also helps to eliminate conductive and radiative interferences. An external capacitor connected from the dVdT pin to RTN defines the slew rate of the output voltage at power-on as shown in Figure 37 and Figure 38.

Feature Description (continued)

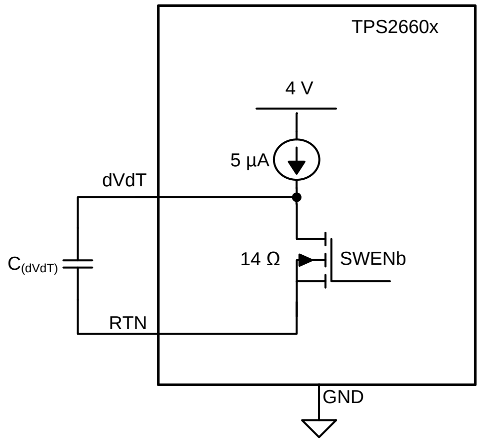


Figure 37. Output Ramp Up Time t_{dVdT} is Set by $C_{(dVdT)}$

The dVdT pin can be left floating to obtain a predetermined slew rate (t_{dVdT}) on the output. When the terminal is left floating, the devices set an internal output voltage ramp rate of 23.9 V/1.6 ms. A capacitor can be connected from dVdT pin to RTN to program the output voltage slew rate slower than 23.9 V/1.6 ms. Use Equation 1 and Equation 2 to calculate the external $C_{(dVdT)}$ capacitance.

Equation 1 governs slew rate at start-up.

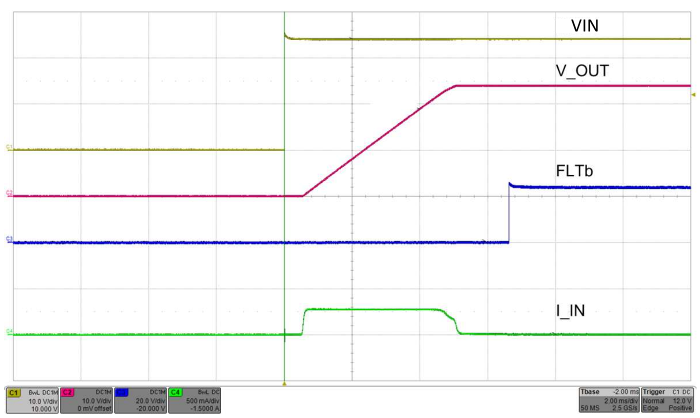
$$I_{(dVdT)} = \left(\frac{C_{(dVdT)}}{Gain_{(dVdT)}}\right) \times \left(\frac{dV_{(OUT)}}{dt}\right)$$

where

- $I_{(dVdT)}$ = 4.7 µA (typical)
- $\frac{dV_{(OUT)}}{dt}$
- $Gain_{(dVdT)}$ = dVdT to V_{OUT} gain = 24.6 (1)

The total ramp time (t_{dVdT}) of $V_{(OUT)}$ for 0 to $V_{(IN)}$ can be calculated using Equation 2.

$$t_{dVdT} = 8 \times 10^3 \times V_{(IN)} \times C_{(dVdT)} \quad (2)$$



C_{dVdT}= 22 nF C_{OUT} = 47 µF R_{ILIM} = 5.36 kΩ

Figure 38. Hot Plug-In and In-Rush Current Control at 24-V Input

Feature Description (continued)

9.3.5 Overload and Short Circuit Protection

The device monitors the load current by sensing the voltage across the internal sense resistor. The FET current is monitored during start-up and normal operation.

9.3.5.1 Overload Protection

The device offers following choices for the overload protection fault response:

- Active current limiting (Auto-retry/Latch-off modes)
- Electronic Circuit Breaker with overload timeout (Auto-retry/Latch-off modes)

See the configurations in Table 1 to select a specific overload fault response.

Table 1. Overload Fault Response Configuration Table

MODE Pin Configuration	Overload Protection Type	Device
Open	Electronic circuit breaker with auto-retry	TPS26600, TPS26602
	Electronic circuit breaker with latch-off	TPS26601
Shorted to RTN	Active current limiting with auto-retry	TPS26600, TPS26601, TPS26602
A 402-kΩ resistor across MODE pin to RTN pin	Active current limiting with latch-off	TPS26600, TPS26601, TPS26602

9.3.5.1.1 Active Current Limiting

When the active current limiting mode is selected, during overload events, the device continuously regulates the load current to the overcurrent limit $I_{(OL)}$ programmed by the $R_{(ILIM)}$ resistor as shown in Equation 3.

$$I_{OL} = \frac{12}{R_{(ILIM)}}$$

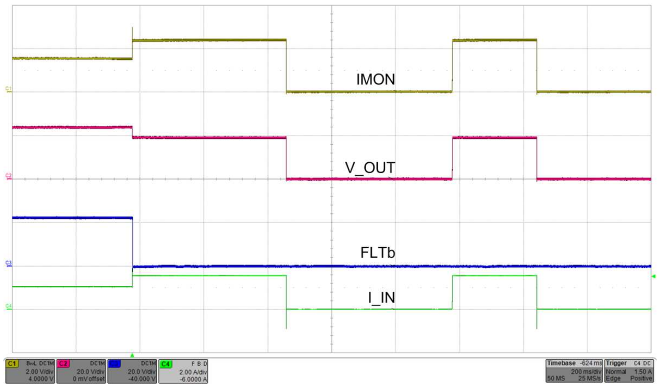
where

- $I_{(OL)}$ is the overload current limit in Ampere
- $R_{(ILIM)}$ is the current limit resistor in kΩ (3)

During an overload condition, the internal current-limit amplifier regulates the output current to $I_{(LIM)}$. The $\overline{FLT}$ signal assert after a delay of 875 µs.The output voltage droops during the current regulation, resulting in increased power dissipation in the device. If the device junction temperature reaches the thermal shutdown threshold ($T_{(TSD)}$), the internal FET is turn off. The device configured in latch-off mode stays latched off until it is reset by either of the following conditions:

- Cycling $V_{(IN)}$ below $V_{(PORF)}$
- Toggling $\overline{SHDN}$

Whereas the device configured in auto-retry mode, commences an auto-retry cycle 512 ms after $T_J < [T_{(TSD)} – 10°C]$. The $\overline{FLT}$ signal remains asserted until the fault condition is removed and the device resumes normal operation. Figure 39 and Figure 40 illustrates behavior of the system during current limiting with auto-retry functionality.

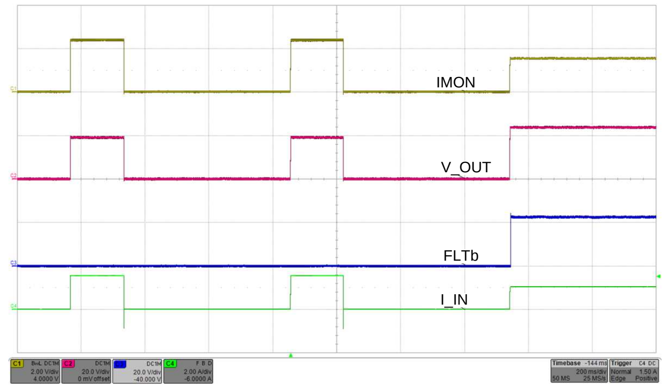


Load transition from 22 Ω to 12 Ω

MODE pin connected to RTN

R_{ILIM} = 8 kΩ

Figure 39. Auto-Retry MODE Fault Behavior



R_{ILIM} = 5.36 kΩ

Figure 40. Response During Coming Out of Overload Fault

9.3.5.1.2 Electronic Circuit Breaker with Overload Timeout, MODE = OPEN

In this mode, during overload events, the device allows the overload current to flow through the device until $I_{(LOAD)} < I_{(FASTRIP)}$. The circuit breaker threshold $I_{(CB)}$ can be programmed using the $R_{(ILIM)}$ resistor as shown in Equation 4.

$$I_{(CB)} = \frac{12}{R_{(ILIM)}} + 0.03A$$

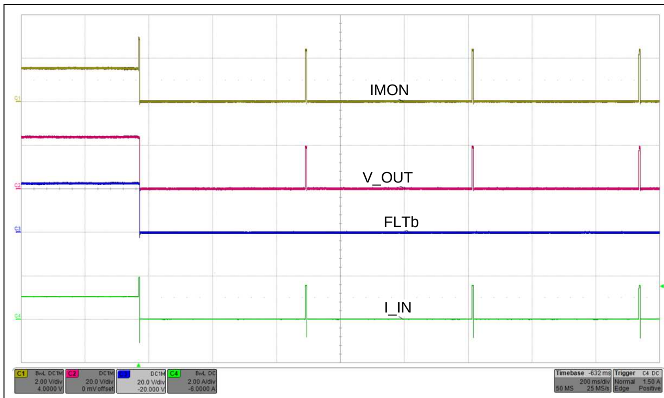
where

- $I_{(CB)}$ is circuit breaker current threshold in Ampere
- $R_{(ILIM)}$ is the current limit resistor in kΩ (4)

An internal timer starts when $I_{(CB)} < I_{LOAD} < I_{FASTRIP}$, and when the timer exceeds $t_{CB(dly)}$, the device turns OFF the internal FET and $\overline{FLT}$ is asserted. Once the internal FET is turned off, the device configured in latch-off mode stays latched off, until it is reset by either of the following conditions:

- Cycling $V_{(IN)}$ falling below $V_{(PORF)}$
- Toggling $\overline{SHDN}$

whereas the device configured in auto-retry mode, commences an auto-retry cycle after 540 ms. The $\overline{FLT}$ signal remains asserted until the fault condition is removed and the device resumes normal operation. Figure 41 and Figure 42 illustrate behavior of the system during electronic circuit breaker with auto-retry functionality.

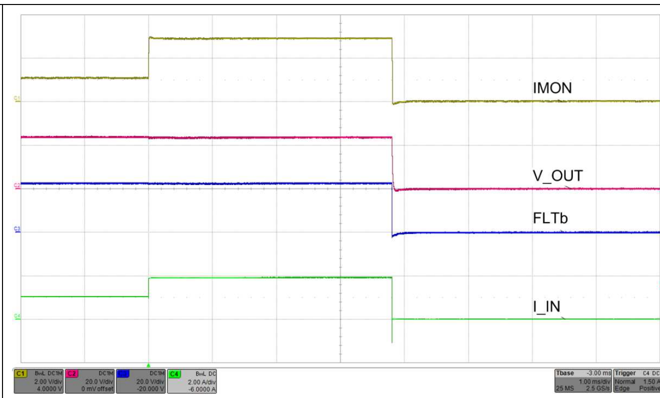


MODE left floating

Load Transition from 22 Ω to 12 Ω

R_{ILIM} = 8 kΩ

Figure 41. Circuit Breaker Functionality

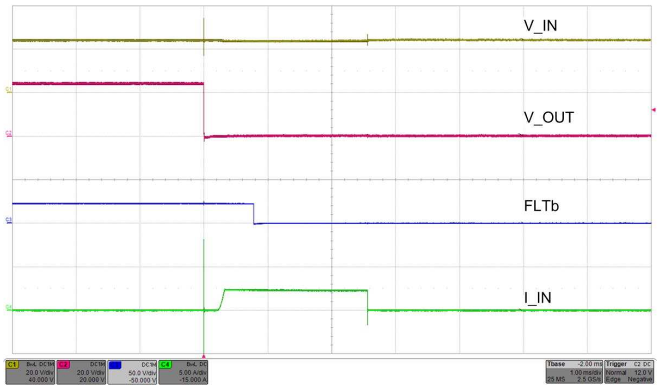


Load Transition from 22 Ω to 12 Ω , R_{ILIM} = 8 kΩ

Figure 42. Zoomed at the Instance of Load Step

9.3.5.2 *Short Circuit Protection*

During a transient output short circuit event, the current through the device increases very rapidly. As the current-limit amplifier cannot respond quickly to this event due to its limited bandwidth, the device incorporates a fast-trip comparator, with a threshold $I_{(FASTRIP)}$. The fast-trip comparator turns off the internal FET within 250 ns (typical), when the current through the FET exceeds $I_{(FASTRIP)}$ ($I_{(OUT)} > I_{(FASTRIP)}$), and terminates the rapid short-circuit peak current. The fast-trip threshold is internally set to 87% higher than the programmed overload current limit ($I_{(FASTRIP)} = 1.87 \times I_{(OL)} + 0.015$). The fast-trip circuit holds the internal FET off for only a few microseconds, after which the device turns back on slowly, allowing the current-limit loop to regulate the output current to $I_{(OL)}$. Then, device behaves similar to overload condition. Figure 43 and Figure 44 illustrate the behavior of the system when the current exceeds the fast-trip threshold.



VIN = 24 V, R_{ILIM} = 5.36 kΩ

Figure 43. Output Hot Short Functionality at 24-V Input

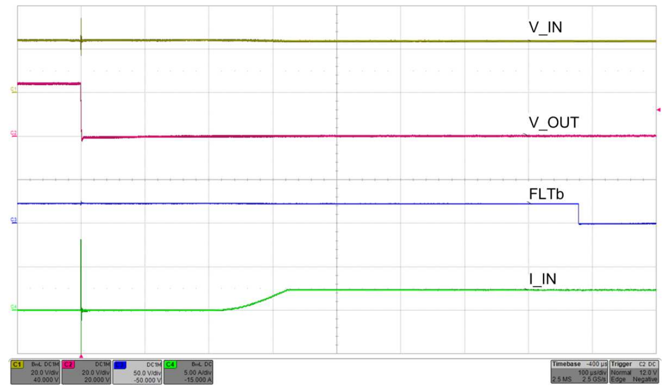
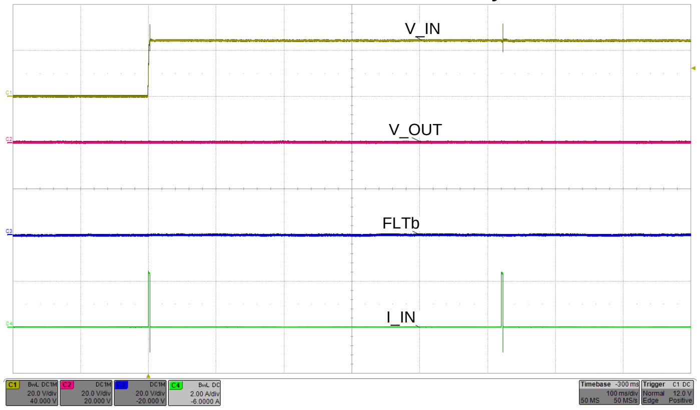


Figure 44. Zoomed at the Instance of Output Short

9.3.5.2.1 Start-Up with Short-Circuit On Output

When the device is started with short-circuit on the output, it limits the load current to the current limit $I_{(OL)}$ and behaves similar to the overload condition. Figure 45 illustrates the behavior of the device in this condition. This feature helps in quick isolation of the fault and hence ensures stability of the DC bus.



MODE pin connected to RTN

VIN = 24 V R_{ILIM} = 5.36 kΩ

Figure 45. Start-Up with Short on Output

9.3.5.3 *FAULT Response*

The $\overline{FLT}$ open-drain output asserts (active low) under following conditions:

- Fault events such as undervoltage, overvoltage, over load, reverse current and thermal shutdown conditions

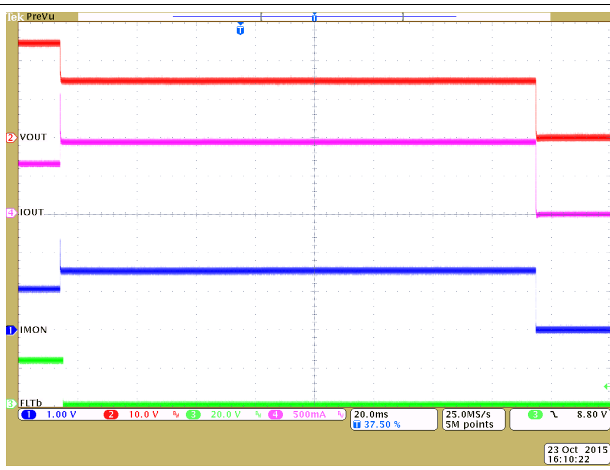
- When the device enters low current shutdown mode when $\overline{\text{SHDN}}$ is pulled low
- During start-up when the internal FET GATE is not fully enhanced

The device is designed to eliminate false reporting by using an internal "de-glitch" circuit for fault conditions without the need for an external circuitry.

The $\overline{\text{FLT}}$ signal can also be used as Power Good indicator to the downstream loads like DC-DC converters. An internal Power Good (PGOOD) singal is OR'd with the fault logic. During start up, when the device is operating in dVdT mode, PGOOD and $\overline{\text{FLT}}$ remains low and is de-asserted after the dVdT mode is completed and the internal FET is fully enhanced. The PGOOD signal has deglitch time incorporated to ensure that internal FET is fully enhanced before heavy load is applied by the downstream converters. Rising deglitch delay is determined by $t_{PGOOD(degl)}$ = Maximum {(875 + 20 × $C_{(dVdT)}$), t_{PGOODR}}, where $C_{(dVdT)}$ is in nF and $t_{PGOOD(degl)}$ is in µs. $\overline{\text{FLT}}$ can be left open or connected to RTN when not used. $V_{(IN)}$ falling below $V_{(PORF)}$ = 3.72 V resets $\overline{\text{FLT}}$.

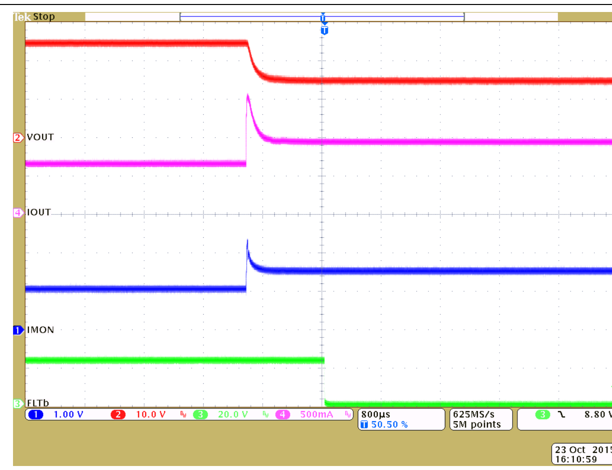
9.3.5.3.1 *Look Ahead* Overload Current Fault Indicator

With the device configured in current limit operation and when the overload condition exists for more than t_{PGOODF}, 875 µs (typical), the $\overline{\text{FLT}}$ asserts to warn of impending turn-off of the internal FETs due to the subsequent thermal shutdown event. Figure 46 and Figure 47 depict this behavior. The $\overline{\text{FLT}}$ signal remains asserted until the fault condition is removed and the device resumes normal operation.



R_{ILIM} = 12 kΩ MODE pin connected to RTN Load transient event from 37 Ω to 15 Ω

Figure 46. Look Ahead Overload Current Fault Indication



R_{ILIM} = 12 kΩ MODE pin connected to RTN Load transient event from 37 Ω to 15 Ω

Figure 47. Output Turn OFF Due to Thermal Shutdown with $\overline{\text{FLT}}$asserted in advance

9.3.5.4 Current Monitoring

The current source at IMON terminal is internally configured to be proportional to the current flowing from IN to OUT. This current can be converted into a voltage using a resistor $R_{(IMON)}$ from IMON terminal to RTN terminal. The IMON voltage can be used as a means of monitoring current flow through the system. The maximum voltage range ($V_{(IMONmax)}$) for monitoring the current is limited to minimum of ([$V_{(IN)}$ – 1.5 V, 4 V]) to ensure linear output. This puts a limitation on maximum value of $R_{(IMON)}$ resistor and is determined by Equation 5.

$$R_{(IMONmax)} = \frac{\text{Min}\left[(V_{(IN)} - 1.5),\ 4\ \text{V}\right]}{1.8 \times I_{(LIM)} \times GAIN_{(IMON)}} \tag{5}$$

The output voltage at IMON terminal is calculated using Equation 6 and Equation 7.

For I_{OUT} > 50 mA,

$$V_{(IMON)} = \left[I_{(OUT)} \times GAIN_{(IMON)}\right] \times R_{(IMON)}$$

Where,

- $GAIN_{(IMON)}$ is the gain factor $I_{(IMON)}:I_{(OUT)}$ = 78.4 µA/A (Typical)
- $I_{(OUT)}$ is the load current
- $I_{(MON\_OS)}$ = 2 µA (Typical) (6)

For I_{OUT} < 50 mA (typical), use Equation 7.

$$V_{(IMON)} = (I_{(IMON\_OS)}) \times R_{(IMON)} \tag{7}$$

This pin must not have a bypass capacitor to avoid delay in the current monitoring information.

In case of reverse input polarity fault, an external 100-kΩ resistor is recommended between IMON pin and ADC input to limit the current through the ESD protection structures of the ADC .

9.3.5.5 IN, OUT, RTN, and GND Pins

The device has two pins for input (IN) and output (OUT). All IN pins must be connected together and to the power source. A ceramic bypass capacitor close to the device from IN to GND is recommended to alleviate bus transients. The recommended input operating voltage range is 4.2 to 55 V. Similarly all OUT pins must be connected together and to the load. $V_{(OUT)}$, in the ON condition, is calculated using Equation 8.

$$V_{(OUT)} = V_{(IN)} - \left(RON \times I_{(OUT)}\right)$$

Where,

- RON is the total ON resistance of the internal FETs. (8)

GND pin must be connected to the system ground. RTN is the device ground reference for all the internal control blocks. Connect the TPS2660x support components: $R_{(ILIM)}$, $C_{(dVdT)}$, $R_{(IMON)}$, $R_{(MODE)}$ and resistors for UVLO and OVP with respect to the RTN pin. Internally, the device has reverse input polarity protection block between RTN and the GND terminal. Connecting RTN pin to GND pin disables the reverse input polarity protection feature and the TPS2660x gets permanently damaged when operated under this fault event.

9.3.5.6 Thermal Shutdown

The device has a built-in over temperature shutdown circuitry designed to protect the internal FETs, if the junction temperature exceeds $T_{(TSD)}$. After the thermal shutdown event, depending upon the mode of fault response, the device either latches-off or commences an auto-retry cycle 512 ms after T_J < [$T_{(TSD)}$ – 10°C]. During the thermal shutdown, the fault pin $\overline{FLT}$ pulls low to indicate a fault condition.

9.3.5.7 Low Current Shutdown Control ($\overline{SHDN}$)

The internal FETs and hence the load current can be switched off by pulling the $\overline{SHDN}$ pin below 0.76 V threshold with a micro-controller GPIO pin or can be controlled remotely with an opto-isolator device as shown in Figure 48 and Figure 49. The device quiescent current reduces to 20 µA (typical) in shutdown state. To assert $\overline{SHDN}$ low, the pull down must sink at least 10 µA at 400 mV. To enable the device, $\overline{SHDN}$ must be pulled up to atleast 1 V. Once the device is enabled, the internal FETs turn on with dVdT mode.

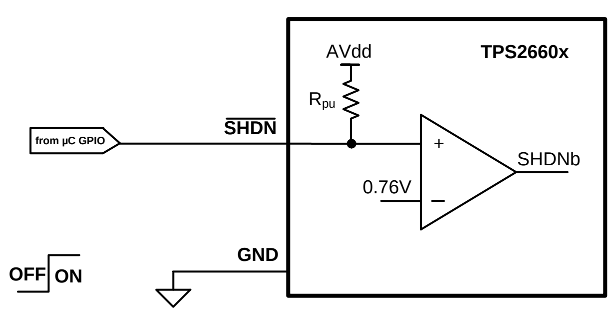


Figure 48. Shutdown Control

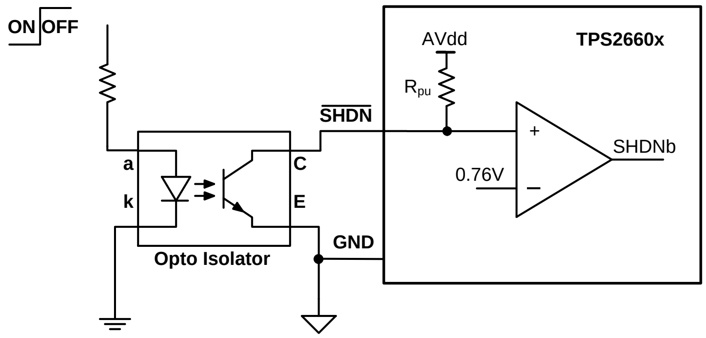


Figure 49. Opto-Isolator Shutdown Control

9.4 Device Functional Modes

The TPS26600, TPS26601 and TPS26602 respond differently to overload and short circuit conditions. The operational differences are explained in Table 2.

Table 2. Device Operational Differences Under Different MODE Configurations

MODE Pin Configuration	MODE Connected to RTN (Current Limit with Auto-Retry)	A 402-kΩ Resistor Connected between MODE and RTN Pins (Current Limit with Latchoff)	MODE Pin = Open (Circuit Breaker with Auto-Retry - TPS26600 and TPS26602), (Circuit Breaker with Latch - TPS26601 Only)
Start up	Inrush current controlled by dVdT		
	Inrush limited to $I_{(OL)}$ level as set by $R_{(ILIM)}$	Inrush limited to $I_{(OL)}$ level as set by $R_{(ILIM)}$	Inrush limited to $I_{(OL)}$ level as set by $R_{(ILIM)}$
			Fault Timer runs when current is limited to $I_{(OL)}$
			Fault timer expires after $t_{CB(dly)}$ causing the FETs to turn off
	If $T_J > T_{(TSD)}$, device turns off	If $T_J > T_{(TSD)}$, device turns off	Device turns off if $T_J > T_{(TSD)}$ before timer expires
Over current response	Current is limited to $I_{(OL)}$ level as set by $R_{(ILIM)}$	Current is limited to $I_{(OL)}$ level as set by $R_{(ILIM)}$	Current is allowed through the device if $I_{(LOAD)} < I_{(FASTTRIP)}$
	Power dissipation increases as $V_{(IN)} – V_{(OUT)}$ increases	Power dissipation increases as $V_{(IN)} – V_{(OUT)}$ increases	Fault timer runs when the current increases above $I_{(OL)}$
			Fault timer expires after $t_{CB(dly)}$ causing the FETs to turn off
	Device turns off when $T_J > T_{(TSD)}$	Device turns off when $T_J > T_{(TSD)}$	Device turns off if $T_J > T_{(TSD)}$ before timer expires
	Device attempts restart 540 ms after $T_J < [T_{(TSD)} – 10°C]$	Device remains off	TPS26600 and TPS26602 attempt restart 540 ms after $T_J < [T_{(TSD)} – 10°C]$. TPS26601 remains off
Short-circuit response	Fast turn off when $I_{(LOAD)} > I_{(FASTRIP)}$		
	Quick restart and current limited to $I_{(OL)}$, follows standard startup		

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The TPS2660x is an industrial eFuse, typically used for Hot-Swap and Power rail protection applications. It operates from 4.2 V to 55 V with programmable current limit, overvoltage, undervoltage and reverse polarity protections. The device aids in controlling in-rush current and provides robust protection against reverse current and filed miss-wiring conditions for systems such as PLCs, Industrial PCs, Control and Automation and Sensors. The device also provides robust protection for multiple faults on the system rail.

The *Detailed Design Procedure* section can be used to select component values for the device.

Alternatively, the WEBENCH® software may be used to generate a complete design. The WEBENCH® software uses an iterative design procedure and accesses a comprehensive database of components when generating a design. Additionally, a spreadsheet design tool TPS2660x Design Calculator is available in the web product folder.

10.2 Typical Application

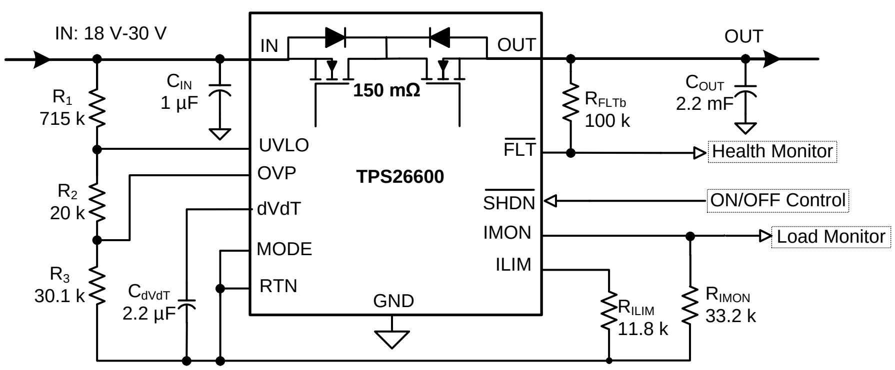


Figure 50. 24-V, 1-A eFuse Input Protection Circuit for Industrial PLC CPU

10.2.1 Design Requirements

Table 3 shows the Design Requirements for TPS2660x.

Table 3. Design Requirements

DESIGN PARAMETER		EXAMPLE VALUE
$V_{(IN)}$	Typical input voltage	24 V
$V_{(UV)}$	Undervoltage lockout set point	18 V
$V_{(OV)}$	Overvoltage cutoff set point	30 V
$RL_{(SU)}$	Load during start-up	48 Ω
$I_{(LIM)}$	Current limit	1 A
$C_{(OUT)}$	Load capacitance	2200 µF
T_A	Maximum ambient temperature	85°C

10.2.2 Detailed Design Procedure

10.2.2.1 Step by Step Design Procedure

To begin the design process, the designer needs to know the following parameters:

- Input operating voltage range
- Maximum output capacitance
- Maximum current limit
- Load during start-up
- Maximum ambient temperature

  This design procedure below seeks to control junction temperature of the device in both steady state and start-up conditions by proper selection of the output ramp-up time and associated support components. The designer can adjust this procedure to fit the application and design criteria.

10.2.2.2 Programming the Current-Limit Threshold—$R_{(ILIM)}$ Selection

The $R_{(ILIM)}$ resistor at the ILIM pin sets the over load current limit, this can be set using Equation 9.

$$R_{(ILIM)} = \frac{12}{I_{LIM}} = 12k\Omega$$

where

- I_{LIM} = 1A (9)

Choose the closest standard 1% resistor value : $R_{(ILIM)}$ = 11.8 kΩ

10.2.2.3 Undervoltage Lockout and Overvoltage Set Point

The undervoltage lockout (UVLO) and overvoltage trip point are adjusted using an external voltage divider network of R1, R2 and R3 connected between IN, UVLO, OVP and RTN pins of the device. The values required for setting the undervoltage and overvoltage are calculated by solving Equation 10 and Equation 11.

$$V_{(OVPR)} = \frac{R_3}{R_1 + R_2 + R_3} \times V_{(OV)} \tag{10}$$

$$V_{(UVLOR)} = \frac{R_2 + R_3}{R_1 + R_2 + R_3} \times V_{(UV)} \tag{11}$$

For minimizing the input current drawn from the power supply $\{I_{(R123)} = V_{(IN)}/(R_1+R_2+R_3)\}$, it is recommended to use higher value resistance for R_1,R_2 and R_3.

However, the leakage current due to external active components connected at resistor string can add error to these calculations. So, the resistor string current, I(R123) must be chosen to be 20x greater than the leakage current of UVLO and OVP pins.

From the device electrical specifications, $V_{(OVPR)}$ = 1.19 V and $V_{(UVLOR)}$ = 1.19 V. From the design requirements, $V_{(OV)}$ is 30 V and $V_{(UV)}$ is 18 V. To solve the equation, first choose the value of R3 = 30.1 kΩ and use Equation 10 to solve for (R_1 + R_2) = 728.7 kΩ. Use Equation 11 and value of (R_1 + R_2) to solve for R_2 = 20.05 kΩ and finally R1= 708.6 kΩ.

Choose the closest standard 1% resistor values: R_1 = 715 kΩ, R_2 = 20 kΩ, and R_3 = 30.1 kΩ.

The UVLO and the OVP pins can also be connected to the RTN pin to enable the internal default $V_{(OV)}$ = 33 V and $V_{(UV)}$ = 15 V.

The power failure is detected on falling edge of the supply. This threshold voltage is 7.5% lower than the rising threshold, V(UV). The voltage at which the device detects power fail can be calculated using Equation 12.

$$V_{(PFAIL)} = 0.925 \times V_{(UV)} \tag{12}$$

10.2.2.4 Programming Current Monitoring Resistor—R_{IMON}

The voltage at IMON pin $V_{(IMON)}$ represents the voltage proportional to the load current. This can be connected to an ADC of the downstream system for health monitoring of the system. The $R_{(IMON)}$ must be configured based on the maximum input voltage range of the ADC used. $R_{(IMON)}$ is set using Equation 13.

$$R_{(IMON)} = \frac{V_{(IMON\,max)}}{I_{(LIM)} \times 75 \times 10^{-6}} \tag{13}$$

For $I_{(LIM)}$ = 1 A, and considering the operating voltage range of ADC from 0 V to 2.5 V, $V_{(IMONmax)}$ is 2.5 V and $R_{(IMON)}$ is determined by Equation 14.

$$R_{(IMON)} = \frac{2.5}{1 \times 75 \times 10^{-6}} = 33.3\mathrm{k}\Omega \tag{14}$$

Selecting the $R_{(IMON)}$ value less than determined ensures that ADC limits are not exceeded for maximum value of the load current. Choose the closest standard 1% resistor value : $R_{(IMON)}$ = 33.2 kΩ.

If current monitoring up to $I_{(FASTRIP)}$ is desired, $R_{(IMON)}$ can be reduced by a factor of 1.8 as shown Equation 5.

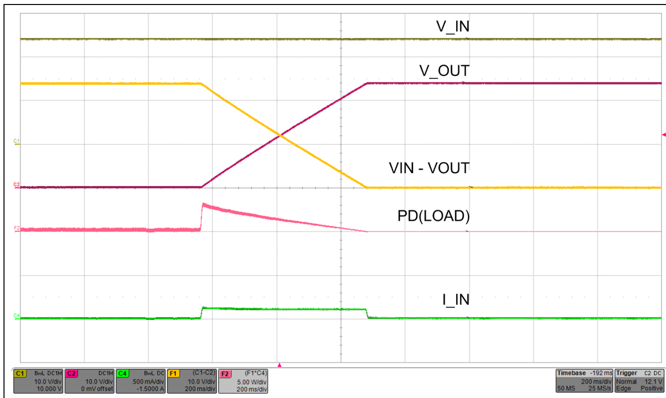
10.2.2.5 Setting Output Voltage Ramp Time—(t_{dVdT})

For a successful design, the junction temperature of the device must be kept below the absolute-maximum rating during dynamic (start-up) and steady state conditions. The dynamic power dissipation is often an order magnitude greater than the steady state power dissipation. It is important to determine the right start-up time and the in-rush current limit for the system to avoid thermal shutdown during start-up with and without load.

The ramp-up capacitor $C_{(dVdT)}$ is calculated considering the two possible cases:

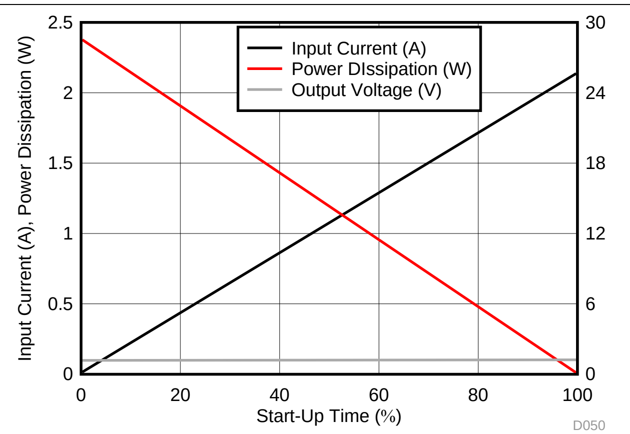
10.2.2.5.1 Case1: Start-Up Without Load—Only Output Capacitance C(OUT) Draws Current During Start-Up

During start-up, as the output capacitor charges, the voltage difference across the internal FET decreases, and the power dissipation decreases. Typical ramp-up of the output voltage, inrush current and instantaneous power dissipated in the device during start-up are shown in Figure 51. The average power dissipated in the device during start-up is equal to the area of triangular plot (red curve in Figure 52) averaged over t_{dVdT} .



V_{IN} = 24 V C_{dVdT} = 2.2 µF C_{OUT} = 2.2 mF

Figure 51. Start-Up without Load



V_{IN} = 24 V C_{dVdT} = 2.2 µF C_{OUT} = 2.2 mF

Figure 52. $P_{D(INRUSH)}$ Due to Inrush Current

The inrush current is determined as shown in Equation 15.

$$I = C \times \frac{dV}{dT} \geq I_{(INRUSH)} = C_{(OUT)} \times \frac{V_{(IN)}}{t_{dVdT}} \tag{15}$$

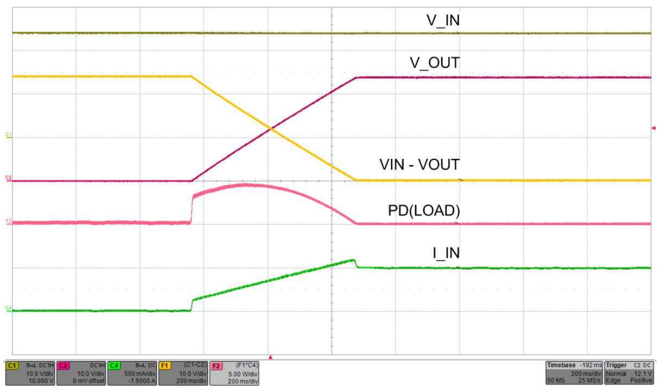
Average power dissipated during start-up is given by Equation 16.

$$P_{D(INRUSH)} = 0.5 \times V_{(IN)} \times I_{(INRUSH)} \quad (16)$$

Equation 16 assumes that the load does not draw any current until the output voltage reaches its final value.

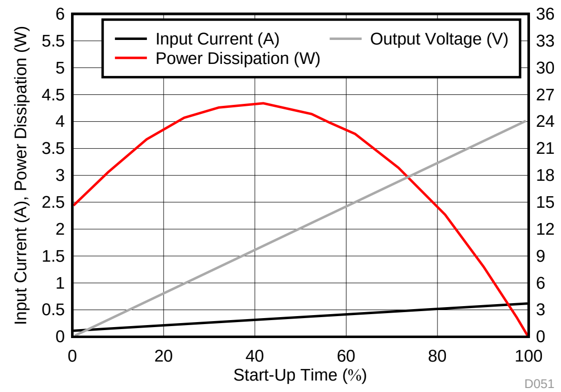
10.2.2.5.2 Case2: Start-Up With Load—Output Capacitance $C_{(OUT)}$ and Load Draws Current During Start-Up

When the load draws current during the turn-on sequence, additional power is dissipated in the device. Considering a resistive load $R_{L(SU)}$ during start-up, typical ramp-up of output voltage, load current and the instantaneous power dissipation in the device are shown in Figure 53. Instantaneous power dissipation with respect to time is plotted in Figure 54. The additional power dissipation during start-up is calculated using Equation 17.



V_{IN} = 24 V $R_{L(SU)}$ = 48 Ω
C_{dVdT} = 2.2 µF C_{OUT} = 2.2 mF

Figure 53. Start-Up with Load



V_{IN} = 24 V $R_{L(SU)}$ = 48 Ω
C_{dVdT} = 2.2 µF C_{OUT} = 2.2 mF

Figure 54. $P_{D(INRUSH)}$ Due to Inrush and Load Current

$$P_{D(LOAD)} = \frac{1}{6} \times \frac{V_{(IN)}^2}{R_{L(SU)}} \quad (17)$$

Total power dissipated in the device during startup is given by Equation 18.

$$P_{D(STARTUP)} = P_{D(INRUSH)} + P_{D(LOAD)} \quad (18)$$

Total current during startup is given by Equation 19.

$$I_{(STARTUP)} = I_{(INRUSH)} + I_{L(t)} \quad (19)$$

For the design example under discussion,

Select the inrush current $I_{(INRUSH)}$ = 0.1 A and calculate t_{dVdT} using Equation 20.

$$t_{(dVdT)} = 2.2m \times \frac{24}{0.1} = 0.528s \quad (20)$$

For a given start-up time, C_{dVdT} capacitance value is calculated using Equation 21.

$$C_{(dVdT)} = \frac{t_{(dVdT)}}{8 \times 10^3 \times V_{(IN)}} = 2.7\mu F$$

where

- $t_{(dVdT)}$ = 0.528 s
- $V_{(IN)}$ = 24 V (21)

Choose the closest standard value: 2.2µF/16V capacitor.

The inrush power dissipation is calculated, using Equation 22.

$$P_{D(INRUSH)} = 0.5 \times V_{(IN)} \times I_{(INRUSH)} = 1.2W$$

where

- $V_{(IN)}$ = 24 V
- $I_{(INRUSH)}$ = 0.1 A (22)

Considering the start-up with 48-Ω load, the additional power dissipation, is calculated using Equation 23.

$$P_{D(LOAD)} = \left(\frac{1}{6}\right) \times \frac{V_{(IN)}^2}{R_{L(SU)}} = 2W$$

where

- $V_{(IN)}$ = 24 V
- $R_{L(SU)}$ = 48 Ω (23)

The total device power dissipation during start up is given by Equation 24.

$$P_{D(STARTUP)} = P_{D(INRUSH)} + P_{D(LOAD)} = 3.2W$$

where

- $P_{D(INRUSH)}$ = 1.2 W
- $P_{D(LOAD)}$ = 2 W (24)

The power dissipation with or without load, for a selected start-up time must not exceed the thermal shutdown limits as shown in Figure 55.

From the thermal shutdown limit graph, at T_A = 85°C, thermal shutdown time for 3.2 W is close to 28000 ms. It is safe to have a minimum 30% margin to allow for variation of the system parameters such as load, component tolerance, input voltage and layout. Selected 2.2 µF C_{dVdT} capacitor and 528 ms start-up time (t_{dVdT}) are within limit for successful startup with 48 Ω load.

Higher value $C_{(dVdT)}$ capacitor can be selected to further reduce the power dissipation during startup.

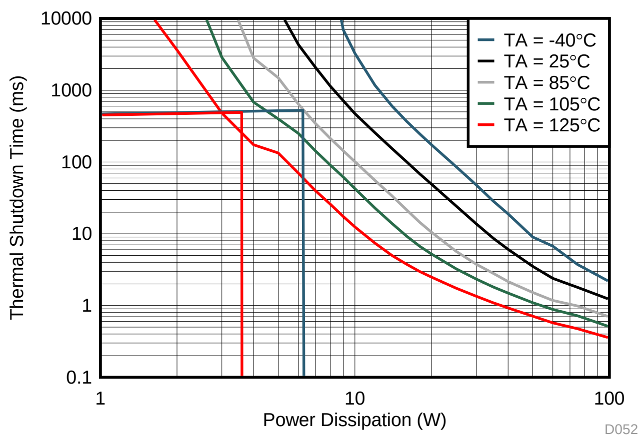


Figure 55. Thermal Shutdown Time vs Power Dissipation

10.2.2.5.3 Support Component Selections—R_{FLTb} and $C_{(IN)}$

The R_{FLTb} serves as pull-up for the open-drain fault output. The current sink by this pin must not exceed 10 mA (see the *Absolute Maximum Ratings* table). Typical resistance value in the range of 10 kΩ to 100 kΩ is recommended for R_{FLTb}. The C_{IN} is a local bypass capacitor to suppress noise at the input. Typical capacitance value in the range of 0.1 µF to 1 µF is recommended for $C_{(IN)}$.

10.2.3 Application Curves

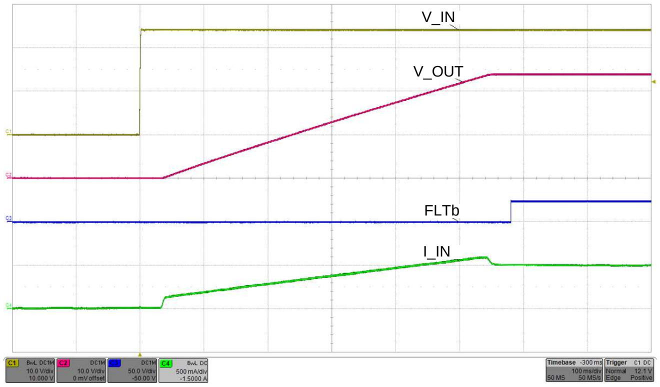


Figure 56. Start-Up with VIN—48-Ω Load

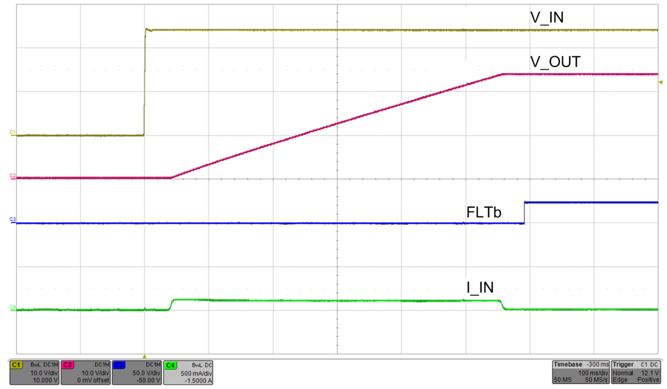


Figure 57. Start-Up with VIN—No Load

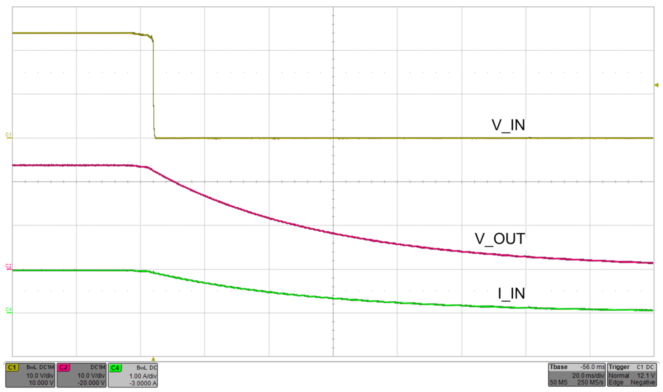


Figure 58. Power Fail with 24-Ω Load—Supports 1-A Load for 10-ms Power Fail

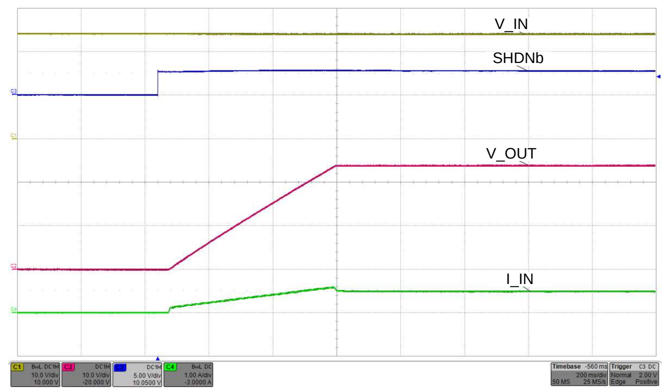


Figure 59. Start-Up with Shutdown Pin—48-Ω Load

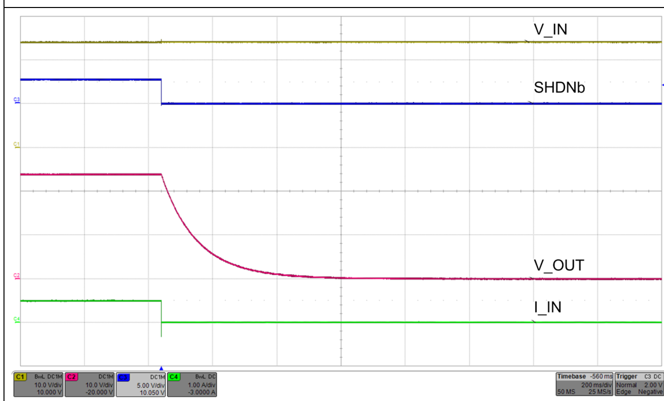


Figure 60. Power Down with Shutdown Pin—48-Ω Load

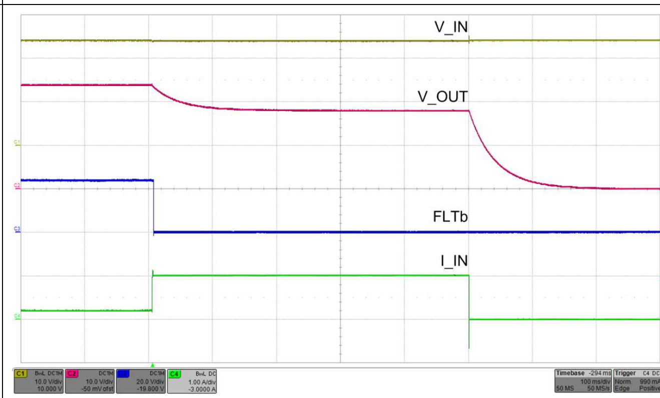


Figure 61. Over Load Response—Load Stepped from 100-Ω to 1 8-Ω Load

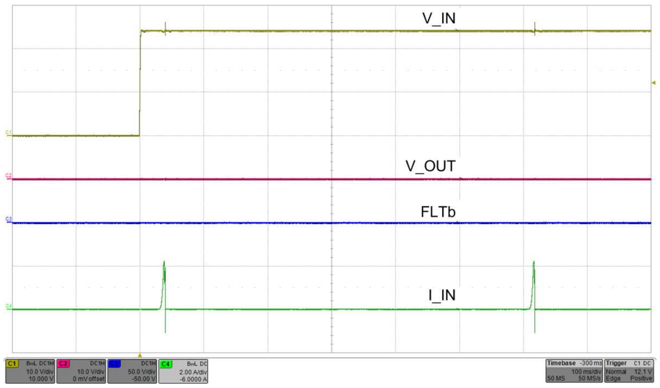


Figure 62. Turnon with Short Circuit on Output

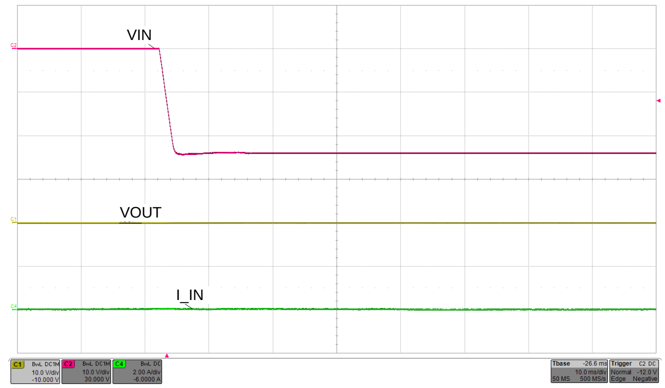


Figure 63. Reverse Polarity Protection

10.3 System Examples

10.3.1 Acive ORing Operation

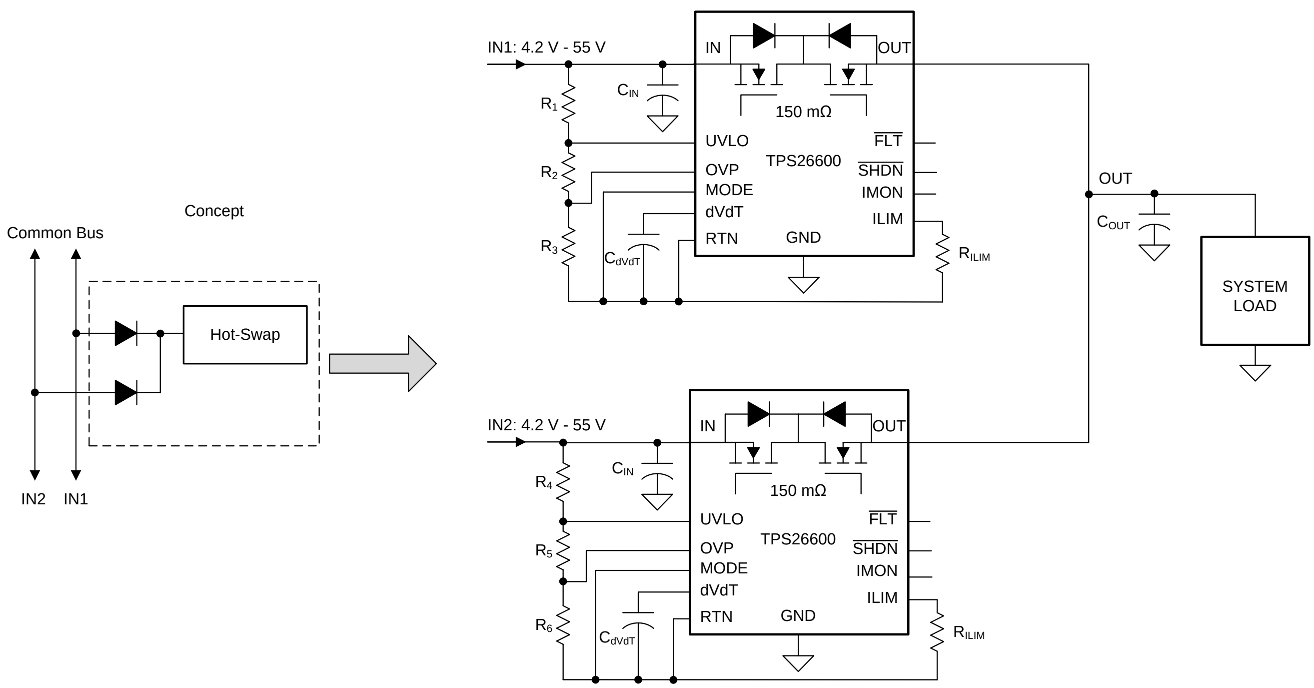


Figure 64. Active ORing Application Schematic

Figure 64 shows a typical redundant power supply configuration of the system. Schottky ORing diodes have been popular for connecting parallel power supplies, such as parallel operation of wall adapter with a battery or a hold-up storage capacitor. The disadvantage of using ORing diodes is high voltage drop and associated power loss. The TPS2660x with integrated, N-channel back to back FETs provide a simple and efficient solution.

A fast reverse comparator controls the internal FET and it is turned ON or OFF with hysteresis as shown in Figure 65. The internal FET is turned off within 1.5 µs (typical) as soon as $V_{(IN)} – V_{(OUT)}$ falls below –110 mV. It turns on within 40 µs (typical) once the differential forward voltage $V_{(IN)} – V_{(OUT)}$ exceeds 100 mV. Figure 66 and Figure 67 show typical switch-over waveforms of Active ORing implementation using the TPS26600.

System Examples (continued)

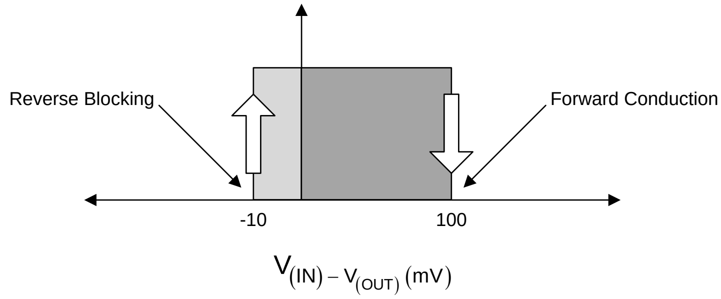
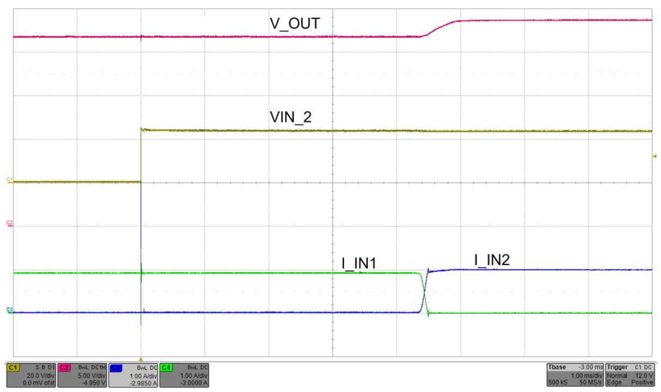
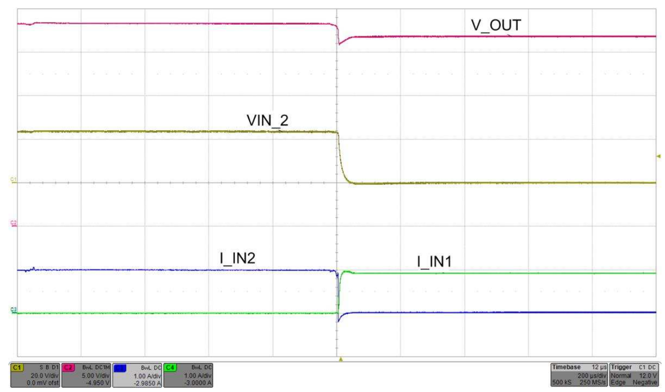


Figure 65. Active ORing Thresholds



VIN1 = 22 V Cout = 47 µF Rload = 24 Ω
VIN2: Plugged In at 24 V $C_{(dVdT)}$ = 22 nF

Figure 66. Active ORing Between Two Supplies VOUT Change Over to VIN2



VIN1 = 22 V Cout = 47 µF Rload = 24 Ω
VIN2: Plugged Out $C_{(dVdT)}$ = 22 nF

Figure 67. Active ORing Between Two Supplies VOUT Change Over to VIN1

NOTE

All control pins of the un-powered TPS2660x device in the Active ORing configuration will measure approximately 0.7 V drop with respect to GND. The system micro-controller should ignore IMON and $\overline{FLT}$ pin voltage measurements of this device when these signals are being monitored.

System Examples (continued)

10.3.2 Field Supply Protection in PLC, DCS I/O Modules

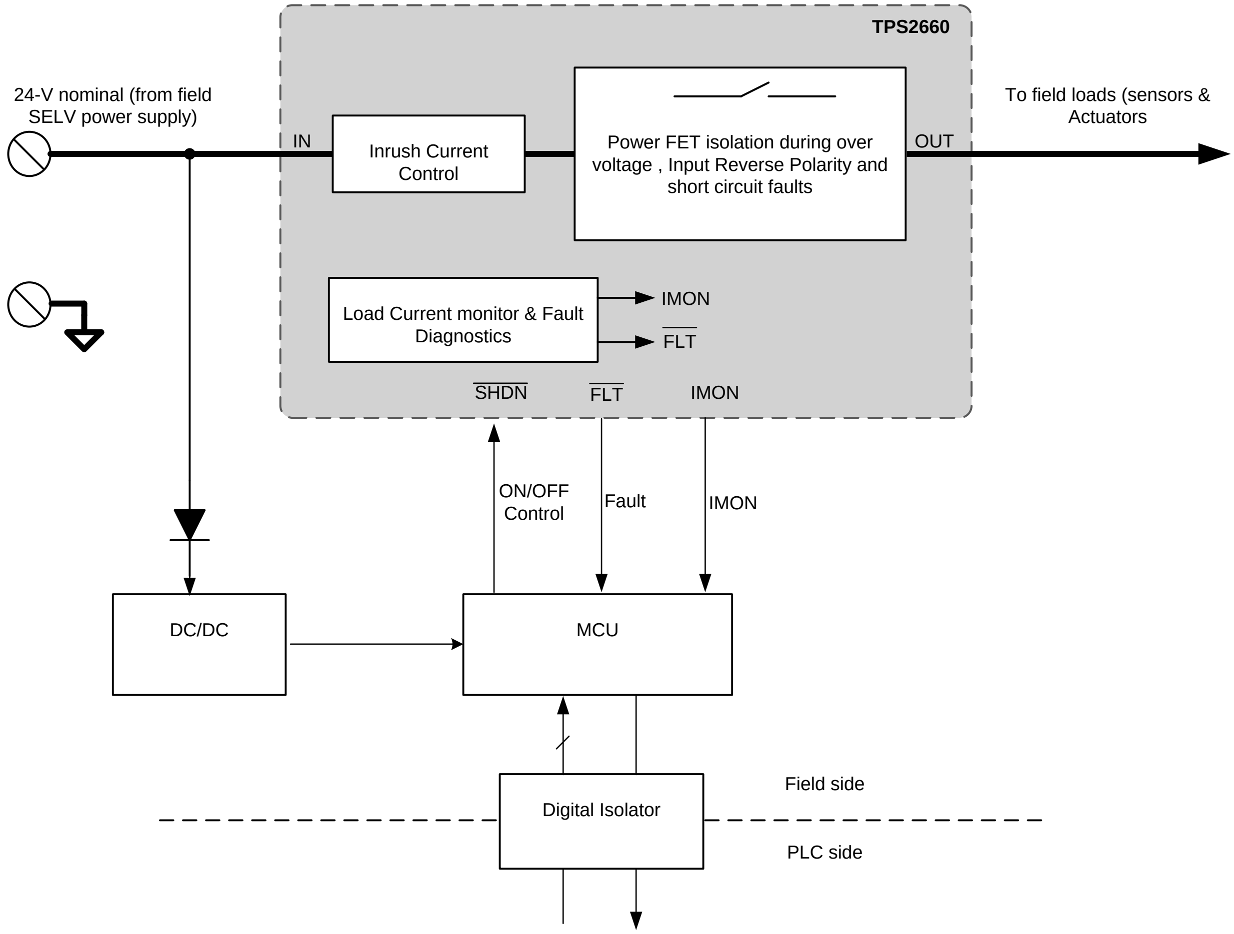


Figure 68. Power Delivery Circuit Block Diagram in I/O Modules

The PLC or Distributed Control System (DCS) I/O modules are often connected to an external field power supply to support higher power requirements of the field loads like sensors and actuators. Power-supply faults or miswiring can damage the loads or cause the loads not to operate correctly. The TPS2660x can be used as a front end protection circuit to protect and provide stable supply to the field loads. Under voltage, Over voltage and reverse polarity protection features of the TPS2660x prevent the loads to experience voltages outside the operating range, which can permanently damage the loads.

Field power supply is often connected to multiple I/O modules and is capable of delivering more current than a single I/O module can handle. Over current protection scheme of the TPS2660x limits the current from the power supply to the module so that the maximum current does not rise above what the board is designed for. Fast short circuit protection scheme isolates the faulty load from the field supply quickly and prevents the field supply to dip and cause interrupts in the other I/O modules connected to the same field supply. High accurate (±5% at 1 A) current limit facilitates more I/O modules to be connected to field supply. Load current monitor (IMON) and fault indication ($\overline{\text{FLT}}$) features facilitate continuous load monitoring.

The TPS2660x also acts as a smart diode with protection against reverse current during output side mis-wiring. Reverse current can potentially damage the field power supply and cause the I/O modules to run hot or may cause permanent damage.

If the field power supply is connected in reverse polarity (which is not unlikely as field power supplies are usually connected with screw terminals), field loads can permanently get damaged due to the reverse voltage. The reverse polarity protection feature of the TPS2660x prevents the reverse voltage to appear at the load side.

System Examples (continued)

10.3.3 Simple 24-V Power Supply Path Protection

With the TPS2660x, a simple 24-V power supply path protection can be realized using a minimum of three external components as shown in the schematic diagram in Figure 69. The external components required are: a $R_{(ILIM)}$ resistor to program the current limit, $C_{(IN)}$ and $C_{(OUT)}$ capacitors.

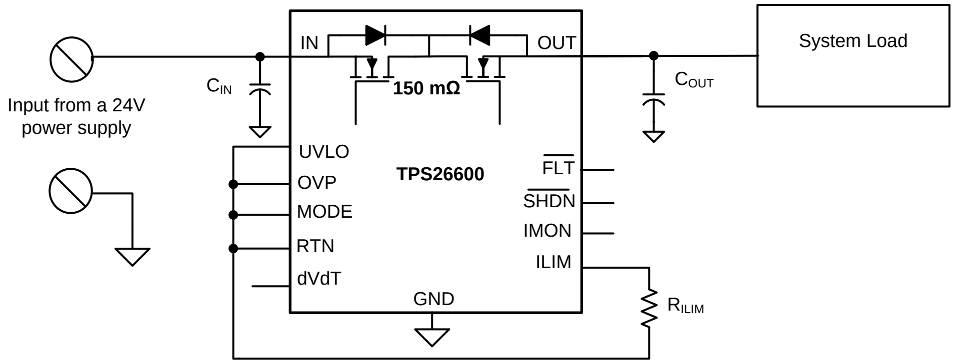


Figure 69. TPS26600 Configured for a Simple 24-V Supply Path Protection

Protection features with this configuration include:

- Load and device protection from reverse input polarity fault down to –60V
- 15 V (typical) rising under voltage lock-out threshold
- 33 V (typical) rising over voltage cut-off threshold
- Protection from 60 V from the external SELV supply
- Inrush current control with 24V/1.6 ms output voltage slew rate
- Reverse Current Blocking
- Accurate current limiting with Auto-Retry

10.4 Do's and Don'ts

- Do not connect RTN to GND. Connecting RTN to GND disables the Reverse Polarity protection feature
- Do connect the TPS2660x support components $R_{(ILIM)}$, $C_{(dVdT)}$, $R_{(IMON)}$, $R_{(MODE)}$ and UVLO, OVP resistors with respect to RTN pin
- Do connect device PowerPAD to the RTN plane for an enhanced thermal performance

11 Power Supply Recommendations

The TPS2660x eFuse is designed for the supply voltage range of 4.2 V ≤ V_{IN} ≤ 55 V. If the input supply is located more than a few inches from the device, an input ceramic bypass capacitor higher than 0.1 µF is recommended. Power supply must be rated higher than the current limit set to avoid voltage droops during over current and short circuit conditions.

11.1 Transient Protection

In case of short circuit and over load current limit, when the device interrupts current flow, input inductance generates a positive voltage spike on the input and output inductance generates a negative voltage spike on the output. The peak amplitude of voltage spikes (transients) is dependent on value of inductance in series to the input or output of the device. Such transients can exceed the *Absolute Maximum Ratings* of the device if steps are not taken to address the issue.

Typical methods for addressing transients include

- Minimizing lead length and inductance into and out of the device
- Using large PCB GND plane
- Schottky diode across the output to absorb negative spikes
- A low value ceramic capacitor ($C_{(IN)}$ to approximately 0.1 µF) to absorb the energy and dampen the transients.

The approximate value of input capacitance can be estimated with Equation 25.

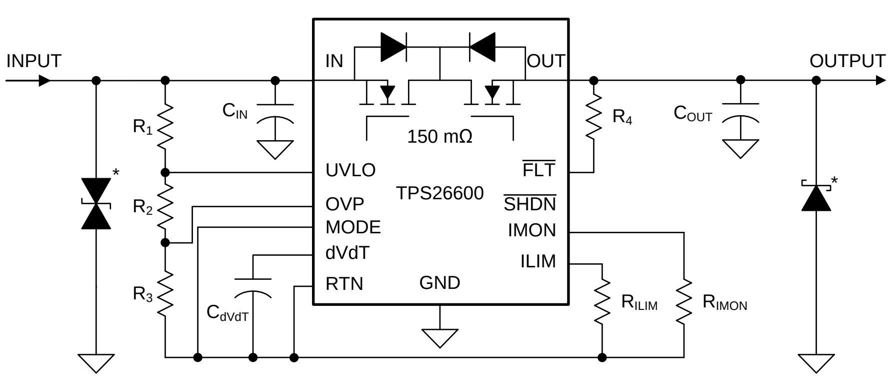
$$V_{spike(Absolute)} = V_{(IN)} + I_{(Load)} \times \sqrt{\frac{L_{(IN)}}{C_{(IN)}}} \qquad (25)$$

where

- $V_{(IN)}$ is the nominal supply voltage
- $I_{(LOAD)}$ is the load current,
- $L_{(IN)}$ equals the effective inductance seen looking into the source
- $C_{(IN)}$ is the capacitance present at the input

Some applications may require additional Transient Voltage Suppressor (TVS) to prevent transients from exceeding the *Absolute Maximum Ratings* of the device. These transients can occur during positive and negative surge tests on the supply lines. In such applications it is recommended to place atleast 1 µF of input capacitor to limit the falling slew rate of the input voltage within a maximum of 20 V/µs

The circuit implementation with optional protection components (a ceramic capacitor, TVS and schottky diode) is shown in Figure 70.



* Optional components needed for suppression of transients

Figure 70. Circuit Implementation with Optional Protection Components

12 Layout

12.1 Layout Guidelines

- For all the applications, a 0.1 µF or higher value ceramic decoupling capacitor is recommended between IN terminal and GND.
- The optimum placement of decoupling capacitor is closest to the IN and GND terminals of the device. Care must be taken to minimize the loop area formed by the bypass-capacitor connection, the IN terminal, and the GND terminal of the IC. See Figure 71 and Figure 72 for PCB layout examples with HTSSOP and VQFN packages respectively.
- High current carrying power path connections must be as short as possible and must be sized to carry atleast twice the full-load current.
- RTN, which is the reference ground for the device must be a copper plane or island.
- Locate all the TPS2660x support components $R_{(ILIM)}$, $C_{(dVdT)}$, $R_{(IMON)}$, and MODE, UVLO, OVP resistors close to their connection pin. Connect the other end of the component to the RTN with shortest trace length.
- The trace routing for the R_{ILIM} and $R_{(IMON)}$ components to the device must be as short as possible to reduce parasitic effects on the current limit and current monitoring accuracy. These traces must not have any coupling to switching signals on the board.
- Protection devices such as TVS, snubbers, capacitors, or diodes must be placed physically close to the device they are intended to protect, and routed with short traces to reduce inductance. For example, a protection Schottky diode is recommended to address negative transients due to switching of inductive loads, and it must be physically close to the OUT and GND pins.
- Thermal Considerations: When properly mounted, the PowerPAD package provides significantly greater cooling ability. To operate at rated power, the PowerPAD must be soldered directly to the board RTN plane directly under the device. Other planes, such as the bottom side of the circuit board can be used to increase heat sinking in higher current applications. Designs that do not need reverse input polarity protection can have RTN, GND and PowerPAD connected together. PowerPAD in these designs can be connected to the PCB ground plane.

12.2 Layout Example

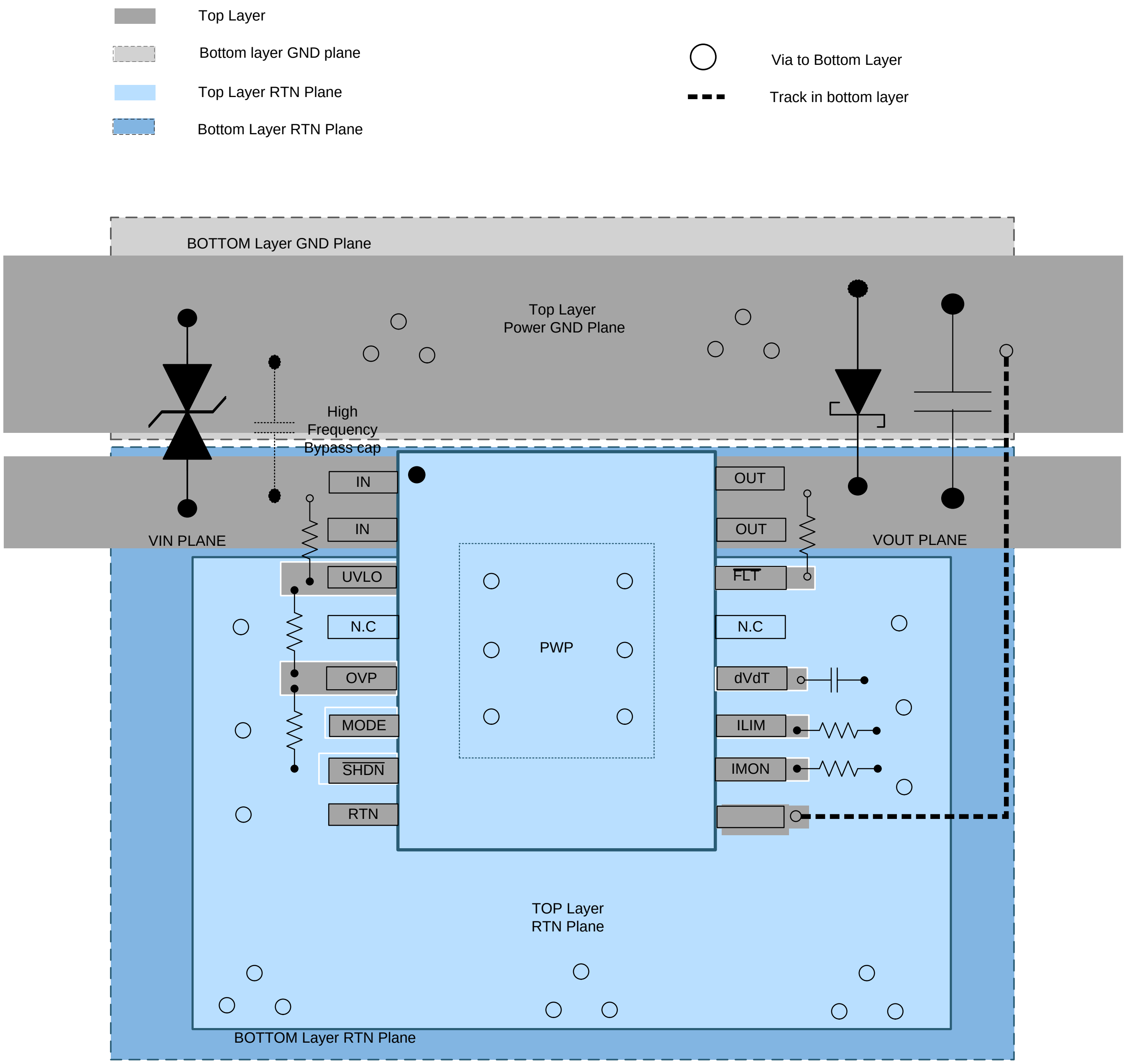


Figure 71. Typical PCB Layout Example with HTSSOP Package with a 2 Layer PCB

Layout Example (continued)

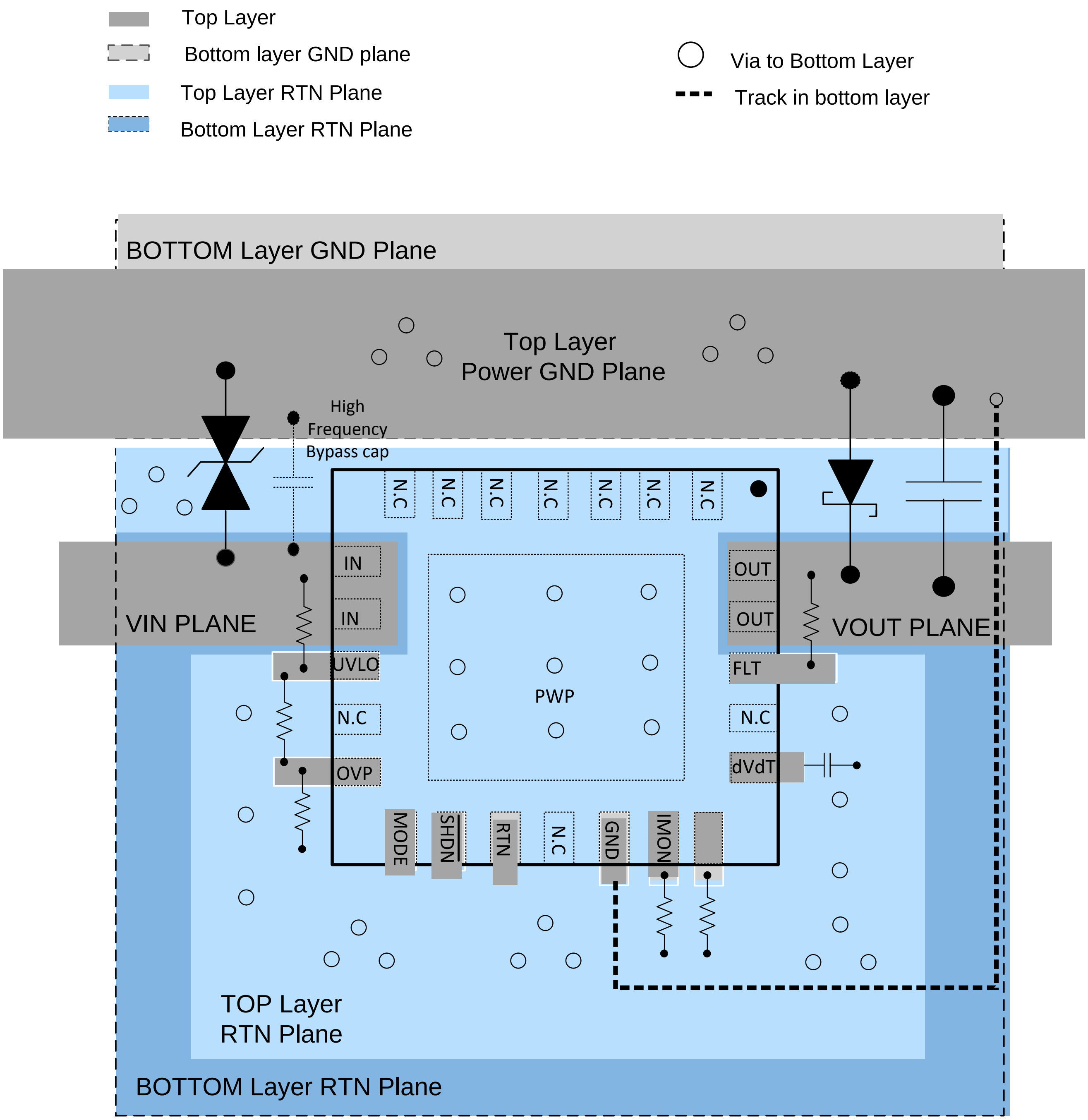


Figure 72. Typical PCB Layout Example with VQFN Package with a 2 Layer PCB

13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

For related documentation see the following:

TPS26600-02EVM: Evaluation Module for TPS2660x User's Guide, SLVUAV3

13.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS26600PWPR	ACTIVE	HTSSOP	PWP	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	26600	Samples
TPS26600PWPT	ACTIVE	HTSSOP	PWP	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	26600	Samples
TPS26600RHFR	PREVIEW	VQFN	RHF	24	3000	TBD	Call TI	Call TI	-40 to 125		
TPS26600RHFT	PREVIEW	VQFN	RHF	24	250	TBD	Call TI	Call TI	-40 to 125		
TPS26601RHFR	PREVIEW	VQFN	RHF	24	3000	TBD	Call TI	Call TI	-40 to 125		
TPS26601RHFT	PREVIEW	VQFN	RHF	24	3000	TBD	Call TI	Call TI	-40 to 125		
TPS26602PWPR	ACTIVE	HTSSOP	PWP	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	26602	Samples
TPS26602PWPT	ACTIVE	HTSSOP	PWP	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	26602	Samples
TPS26602RHFR	PREVIEW	VQFN	RHF	24	3000	TBD	Call TI	Call TI	-40 to 125		
TPS26602RHFT	PREVIEW	VQFN	RHF	24	3000	TBD	Call TI	Call TI	-40 to 125		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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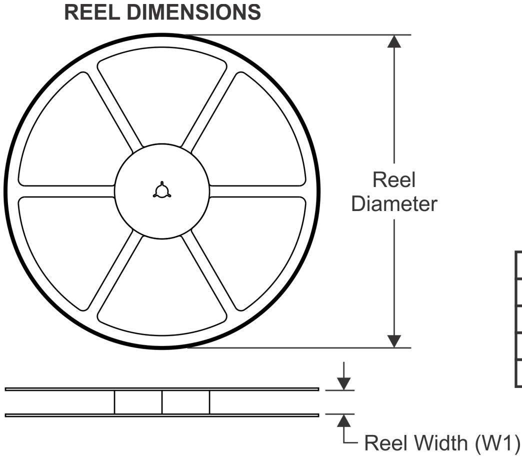
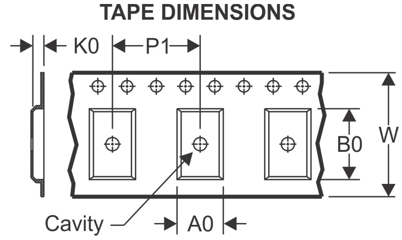
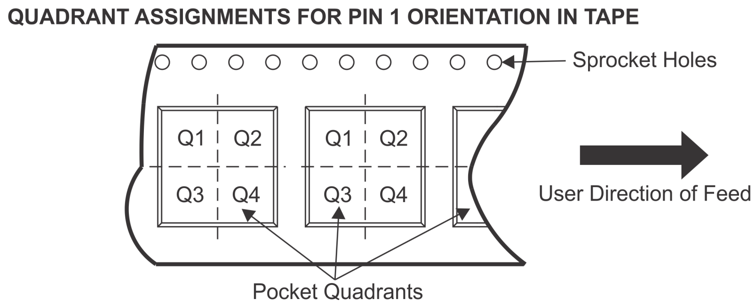
TAPE AND REEL INFORMATION





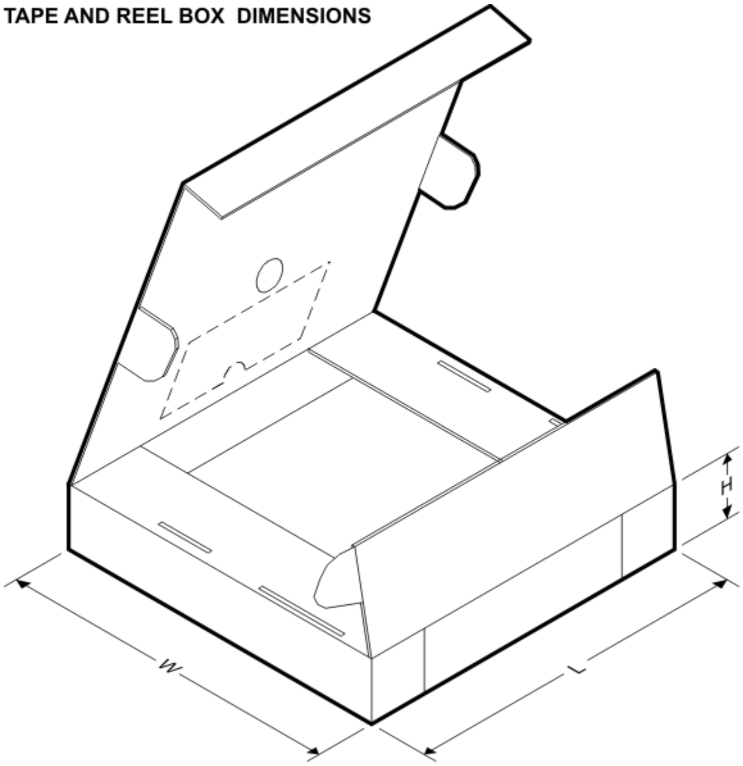
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS26600PWPR	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS26600PWPT	HTSSOP	PWP	16	250	180.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS26602PWPR	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS26602PWPT	HTSSOP	PWP	16	250	180.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

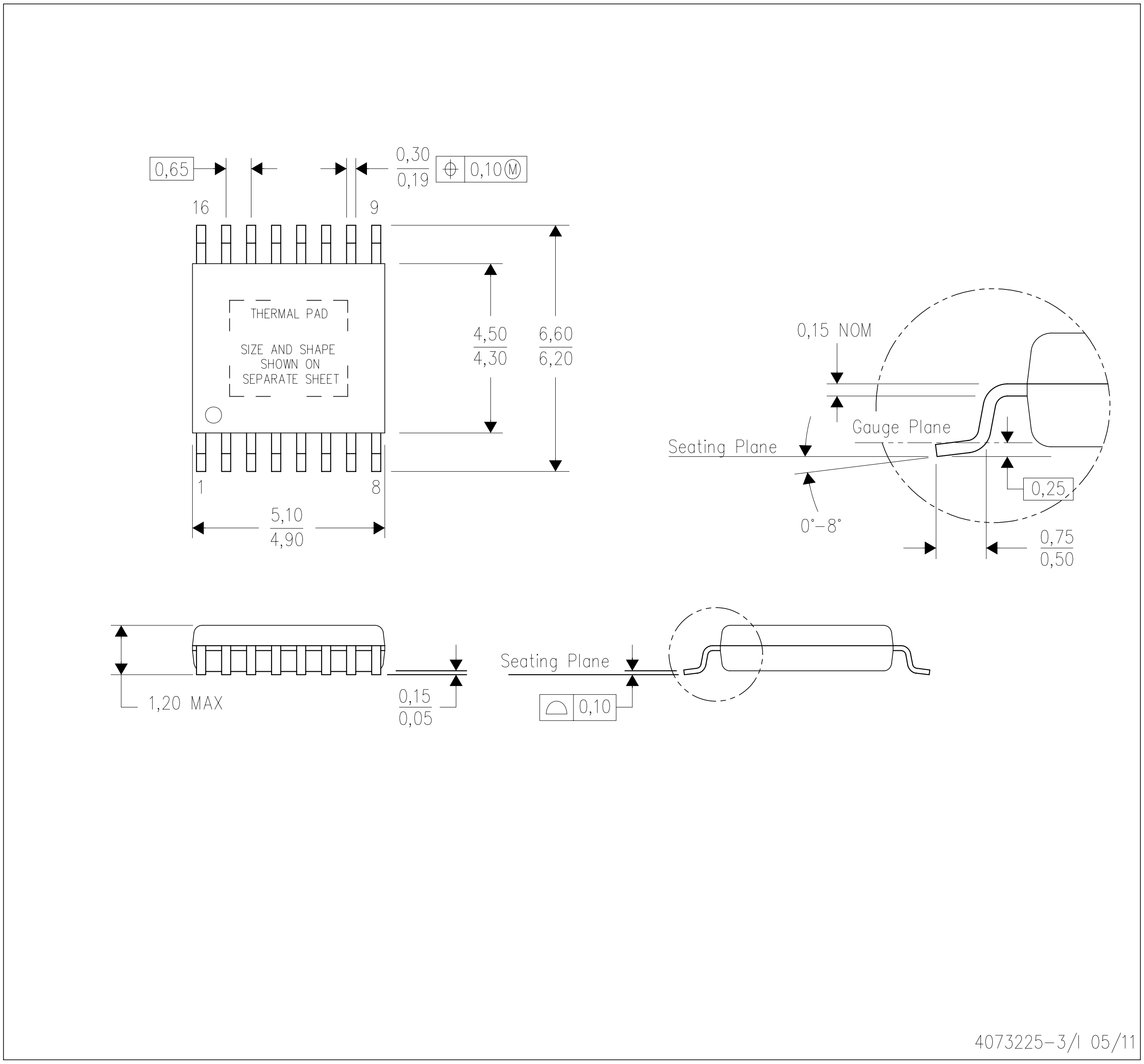
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS26600PWPR	HTSSOP	PWP	16	2000	367.0	367.0	38.0
TPS26600PWPT	HTSSOP	PWP	16	250	210.0	185.0	35.0
TPS26602PWPR	HTSSOP	PWP	16	2000	367.0	367.0	38.0
TPS26602PWPT	HTSSOP	PWP	16	250	210.0	185.0	35.0

PWP (R-PDSO-G16) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO-153

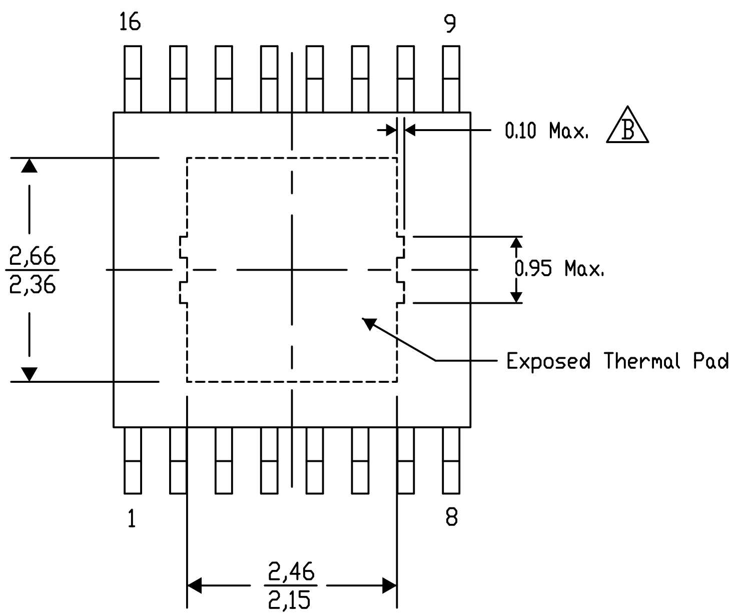
PWP (R-PDSO-G16) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



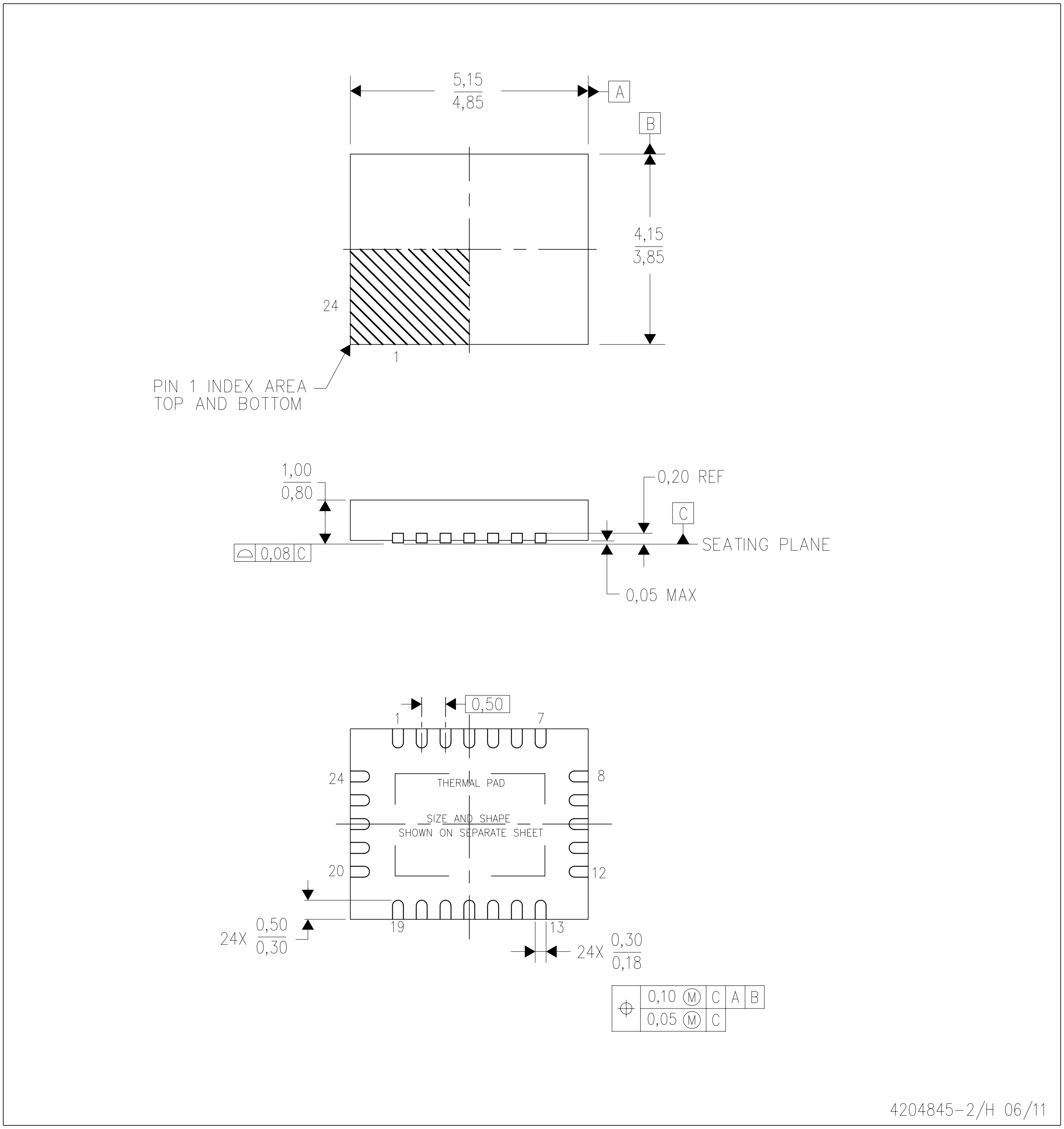
Top View

Exposed Thermal Pad Dimensions

4206332-58/A0 01/16

NOTE: A. All linear dimensions are in millimeters

RHF (R–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265