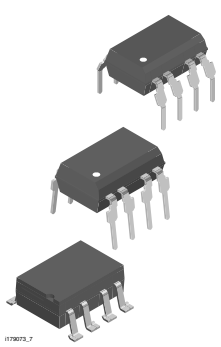
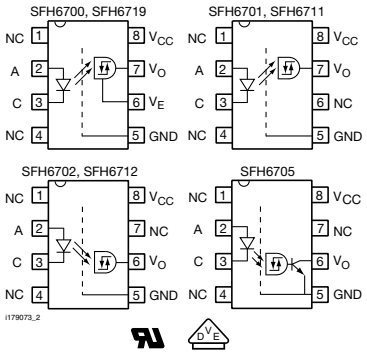
High Speed Optocoupler, 5 MBd, 1 kV/µs dV/dt





FEATURES

- Data rate 5 MBits/s (2.5 MBit/s over temperature)
- Buffer
- Isolation test voltage, 5300 V_{RMS} for 1 s
- TTL, LSTTL and CMOS compatible
- Internal shield for very high common mode transient immunity
- Wide supply voltage range (4.5 V to 15 V)
- Low input current (1.6 mA to 5 mA)
- Three state output (SFH6700, SFH6719)
- Totem pole output (SFH6701, SFH6702, SFH6711, SFH6712)
- Open collector output (SFH6705)
- Compliant to RoHS Directive to 2002/95/EC and in accordance WEEE 2002/96/EC

Pb-free

e3

RoHS COMPLIANT

DESCRIPTION

The SFH67xx high speed optocoupler series consists of a GaAlAs infrared emitting diode, optically coupled with an integrated photo detector. The detector incorporates a Schmitt-Trigger stage for improved noise immunity. Using the enable input, the output can switched to the high ohmic state, which is necessary for data bus applications. A Faraday shield provides a common mode transient immunity of 1000 V/µ at V_{CM} = 50 V for SFH6700, SFH6701, SFH6702, SFH6705 and 2500 V/µ at V_{CM} = 400 V for SFH6711, SFH6712, SFH6719.

The SFH67xx uses an industry standard DIP-8 package. With standard lead bending, creepage distance and clearance of ≥ 7 mm with lead bending options 6, 7, and 9 ≥ 8 mm are achieved.

APPLICATIONS

- Industrial control
- Replace pulse transformers
- Routine logic interfacing
- Motion/power control
- High speed line receiver
- Microprocessor system interfaces
- Computer peripheral interfaces

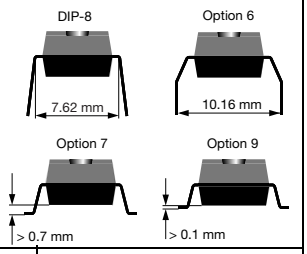
AGENCY APPROVALS

- UL1577, file no. E52744 system code H or J, double protection
- DIN EN 60747-5-5 (VDE 0884) available with option 1

ORDERING INFORMATION

S	F	H	6	7	#	#	-	X	0	0	#	T

PART NUMBER — PACKAGE OPTION — TAPE AND REEL



AGENCYCERTIFIED/ PACKAGE	THREE STATE	TOTEM POLE		OPEN COLLECTOR
UL				
DIP-8	SFH6700	SFH6701	SFH6711	SFH6705
	SFH6719	SFH6702	SFH6712	-
DIP-8, 400 mil, option 6	-	SFH6702-X006	-	SFH6705-X006
SMD-8, option 7	-	SFH6701-X007	SFH6711-X007	SFH6705-X007
	-	SFH6702-X007	SFH6712-X007	-
SMD-8, option 9	SFH6700-X009	SFH6702-X009T (1)	SFH6701-X009T (1)	-

Note

- Also available in tubes. To order, do not add T on end

TRUTH TABLE (positive logic)			
PARTS	**IR DIODE**	**ENABLE**	**OUTPUT**
SFH6700	on	H	Z
	off	H	Z
SFH6719	on	L	H
	off	L	L
SFH6701	on		H
	off		L
SFH6702	on		H
	off		L
SFH6705	on		H
	off		L
SFH6711	on		H
	off		L
SFH6712	on		H
	off		L

ABSOLUTE MAXIMUM RATINGS (T_{amb} = 25 °C, unless otherwise specified)				
PARAMETER	**TEST CONDITION**	**SYMBOL**	**VALUE**	**UNIT**
INPUT				
Reverse voltage		V_R	3	V
DC forward current		I_F	10	mA
Surge forward current	t ≤ 1 µs	I_{FSM}	1	A
Power dissipation		P_{diss}	20	mW
OUTPUT				
Supply voltage		V_{CC}	- 0.5 to + 15	V
Three state enable voltage (SFH6700, SFH6719 only)		V_{EN}	- 0.5 to + 15	V
Output voltage		V_O	- 0.5 to + 15	V
Average output current		I_O	25	mA
Power dissipation		P_{diss}	100	mW
COUPLER				
Storage temperature range		T_{stg}	- 55 to + 125	°C
Ambient temperature range		T_{amb}	+ 85	°C
Lead soldering temperature	t = 10 s	T_{sld}	260	°C
Isolation test voltage		V_{ISO}	5300	V_{RMS}
Pollution degree			2	
Creepage distance and clearance	Standard lead bending		7	mm
	Options 6, 7, 9		8	mm
Comparative tracking index per DIN IEC 112/VDE 0303, part 1			175	
Isolation resistance	V_{IO} = 500 V, T_{amb} = 25 °C	R_{IO}	10^{12}	Ω
	V_{IO} = 500 V, T_{amb} = 100 °C	R_{IO}	10^{11}	Ω

Note

- Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of this document. Exposure to absolute maximum ratings for extended periods of the time can adversely affect reliability.

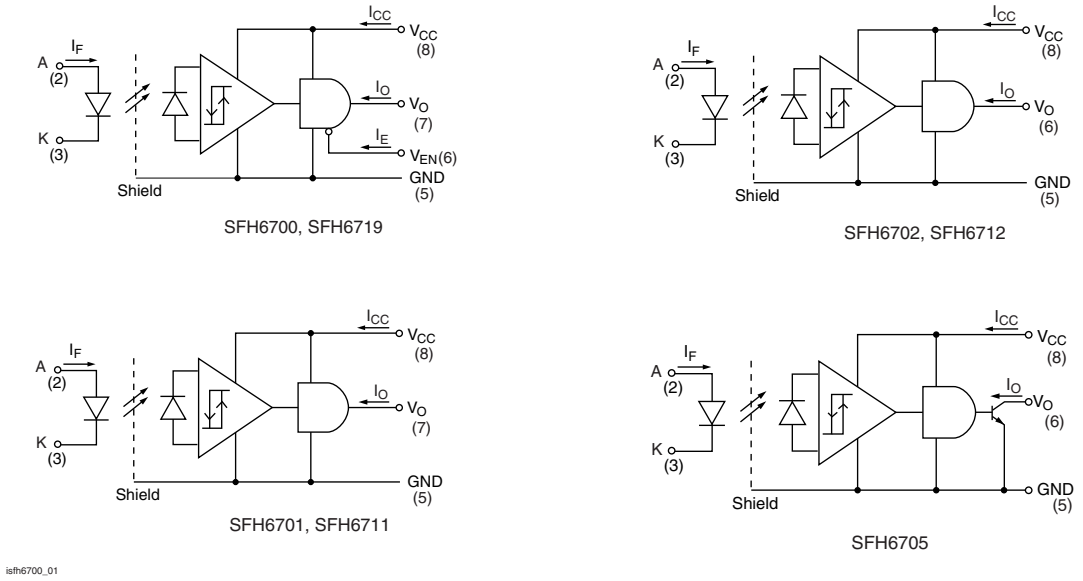


Fig. 1 - Schematics

RECOMMENDED OPERATING CONDITIONS (1)							
PARAMETER	**TEST CONDITION**	**PART**	**SYMBOL**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Supply voltage			V_{CC}	4.5		15	V
Enable voltage high		SFH6700	V_{EH}	2		15	V
		SFH6719	V_{EH}	2		15	V
Enable voltage low		SFH6700	V_{EL}	0		0.8	V
		SFH6719	V_{EL}	0		0.8	V
Forward input current			I_{Fon}	1.6 (2)		5	mA
			I_{Foff}			0.1	mA
Operating temperature			T_{amb}	- 40		85	°C
Output pull-up resistor		SFH6705	R_L	350		4	kΩ
Fan output	R_L = 1 kΩ	SFH6705	N			16	LS TTL loads

Notes

(1) A 0.1 µF bypass capacitor connected between pins 5 and 8 must be used.

(2) We recommended using a 2.2 mA to permit at least 20 % CTR degradation guard band.

ELECTRICAL CHARACTERISTICS (1)						
PARAMETER	**TEST CONDITION**	**SYMBOL**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
INPUT						
Forward voltage	I_F = 5 mA	V_F		1.6	1.75	V
	I_F = 5 mA	V_F			1.8	V
Input current hysteresis	V_{CC} = 5 V, I_{HYS} = I_{Fon} - I_{Fon}	I_{HYS}		0.1		mA
Reverse current	V_R = 3 V	I_R		0.5	10	µA
Capacitance	V_R = 0 V, f = 1 MHz	C_O		60		pF
Thermal resistance		R_{thJA}		700		K/W
OUTPUT						
Logic low output voltage	I_{OL} = 6.4 mA	V_{OL}			0.5	V
Logic high output voltage (except SFH6705)	I_{OH} = 2.6 mA, V_{OH} = V_{CC} - 1.8 V		2.4			V
Output leakage current (V_{OUT} > V_{CC}) (except SFH6705)	V_O = 5.5 V, V_{CC} = 4.5 V, I_F = 5 mA	I_{OHH}		0.5	100	µA
	V_O = 15 V, V_{CC} = 4.5 V, I_F = 5 mA	I_{OHH}		1	500	µA

ELECTRICAL CHARACTERISTICS (1)

PARAMETER	TEST CONDITION	SYMBOL	MIN.	TYP.	MAX.	UNIT
OUTPUT						
Output leakage current (SFH6705 only)	V_O = 5.5 V, V_{CC} = 5.5 V, I_F = 5 mA	I_{OHH}		0.5	100	µA
	V_O = 15 V, V_{CC} = 15 V, I_F = 5 mA	I_{OHH}		1	500	µA
Logic high enable voltage (SFH6700/19 only)		V_{EH}	2			V
Logic low enable voltage (SFH6700/19 only)		V_{EL}			0.8	V
Logic high enable current (SFH6700/19 only)	V_{EN} = 2.7 V	I_{EH}			20	µA
	V_{EN} = 5.5 V	I_{EH}			100	µA
	V_{EN} = 15 V	I_{EH}		0.001	250	µA
Logic low enable current (SFH6700/19 only)	V_{EN} = 0.4 V	I_{EL}	- 320	- 50		µA
High impedance state output current (SFH6700/19 only)	V_O = 0.4 V, V_{EN} = 2 V, I_F = 5 mA	I_{OZL}	- 20			µA
	V_O = 2.4 V, V_{EN} = 2 V, I_F = 0 mA	I_{OZH}			20	µA
	V_O = 5.5 V, V_{EN} = 2 V, I_F = 0 mA	I_{OZH}			100	µA
		I_{OZH}		0.001	500	µA
Logic low supply current	V_{CC} = 5.5 V, I_F = 0	I_{CCL}		3.7	6	mA
	V_{CC} = 15 V, I_F = 0	I_{CCL}		4.1	6.5	mA
Logic high supply current	V_{CC} = 5.5 V, I_F = 5 mA	I_{CCH}		3.4	4	mA
	V_{CC} = 15 V, I_F = 5 mA	I_{CCH}		3.7	5	mA
Logic low short circuit output current (2)	V_O = V_{CC} = 5.5 V, I_F = 0	I_{OSL}	25			mA
	V_O = V_{CC} = 15 V, I_F = 0	I_{OSL}	40			mA
Logic high short circuit output current (2)	V_{CC} = 5.5 V, V_O = 0 V, I_F = 5	I_{OSL}			- 10	mA
	V_{CC} = 15 V, V_O = 0 V, I_F = 5	I_{OSL}			- 25	mA
Thermal resistance		R_{thJA}		300		K/W
COUPLER						
Capacitance (input to output)	f = 1 MHz, pins 1 to 4 and 5 to 8 shorted together	C_{IO}		0.6		pF
Isolation resistance	V_{IO} = 500 V, T_{amb} = 25 °C	R_{IO}	10^{12}			Ω
	V_{IO} = 500 V, T_{amb} = 100 °C	R_{IO}	10^{11}			Ω

Notes

(1) - 40 °C ≤ T_{amb} ≤ 85 °C; 4.5 V ≤ V_{CC} ≤ 15 V; 1.6 mA ≤ I_{Fon} ≤ 5 mA; 2 ≤ V_{EH} ≤ 15 V; 0 ≤ V_{EL} ≤ 0.8 V; 0 mA ≤ I_{Foff} ≤ 0.1 mA.
Typical values: T_{amb} = 25 °C; V_{CC} = 5 V; I_{Fon} = 3 mA unless otherwise specified. Minimum and maximum values are testing requirements. Typical values are characteristics of the device and are the result of engineering evaluation. Typical values are for information only and are not part of the testing requirements.

(2) Output short circuit time ≤ 10 ms.

SWITCHING CHARACTERISTICS (1)

PARAMETER	TEST CONDITION	PART	SYMBOL	MIN.	TYP.	MAX.	UNIT
Propagation delay time to logic low output level, SFH6700, SFH6701, SFH6702, SFH6711, SFH6712, SFH6719 (2)	Without peaking capacitor		t_{PHL}		120		ns
	With peaking capacitor		t_{PHL}		115	300	ns
			t_{PLH}		125		ns
			t_{PLH}		90	300	ns
Output enable time to logic high (SFH6700, SFH6719) (2)			t_{PZH}		20		ns
Output enable time to logic low (SFH6700, SFH6719) (2)			t_{PZL}		25		ns
Output disable time from logic low (SFH6700, SFH6719) (2)			t_{PLZ}		50		ns
Output rise time (2)	10 % to 90 %		t_r		40		ns
Output fall time (2)	90 % to 10 %		t_f		10		ns

SWITCHING CHARACTERISTICS (1)

PARAMETER	TEST CONDITION	PART	SYMBOL	MIN.	TYP.	MAX.	UNIT
Propagation delay time to logic low output level (3)	Without peaking capacitor	SFH6705	t_{PHL}		115		ns
	With peaking capacitor	SFH6705	t_{PHL}		105	300	ns
	Without peaking capacitor	SFH6705	t_{PLH}		125		ns
	With peaking capacitor	SFH6705	t_{PLH}		90	300	ns
Output rise time (3)	10 % to 90 %		t_r		25		ns
	90 % to 10 %		t_r		4		ns

Notes

(1) 0 °C ≤ T_{amb} ≤ 85 °C; 4.5 V ≤ V_{CC} ≤ 15 V; 1.6 mA ≤ I_{Fon} ≤ 5 mA; 2 ≤ V_{EH} ≤ 15 V (SFH6700/19); 0 ≤ V_{EL} ≤ 0.8 V (SFH6700, SFH6719); 0 mA ≤ I_{Foff} ≤ 0.1 mA

(2) Typical values: T_{amb} = 25 °C; V_{CC} = 5 V; I_{Fon} = 3 mA unless otherwise specified (4)

(3) Typical values: T_{amb} = 25 °C, V_{CC} = 5 V; I_{Fon} = 3 mA; R_L = 390 Ω unless otherwise specified (4)

(4) A 0.1 µF bypass capacitor connected between pins 5 and 8 must be used

COMMON MODE TRANSIENT IMMUNITY (1)

PARAMETER	TEST CONDITION	PART	SYMBOL	MIN.	TYP.	MAX.	UNIT
Logic high common mode transient immunity	$\|V_{CM}\|$ = 50 V, I_F = 1.6 mA	SFH6700	$\|CM_H\|$ (2)	1000			V/µs
		SFH6701	$\|CM_H\|$ (2)	1000			V/µs
		SFH6702	$\|CM_H\|$ (2)	1000			V/µs
		SFH6705	$\|CM_H\|$ (2)	1000			V/µs
	$\|V_{CM}\|$ = 400 V, I_F = 1.6 mA	SFH6711	$\|CM_H\|$ (2)	2500			V/µs
		SFH6712	$\|CM_H\|$ (2)	2500			V/µs
		SFH6719	$\|CM_H\|$ (2)	2500			V/µs
Logic Low common mode transient immunity	$\|V_{CM}\|$ = 50 V, I_F = 0 mA	SFH6700	$\|CM_L\|$ (3)	1000			V/µs
	$\|V_{CM}\|$ = 50 V, I_F = 0 mA	SFH6701	$\|CM_L\|$ (3)	1000			V/µs
		SFH6702	$\|CM_L\|$ (3)	1000			V/µs
		SFH6705	$\|CM_L\|$ (3)	1000			V/µs
	$\|V_{CM}\|$ = 400 V, I_F = 0 mA	SFH6711	$\|CM_L\|$ (3)	2500			V/µs
		SFH6712	$\|CM_L\|$ (3)	2500			V/µs
		SFH6719	$\|CM_L\|$ (3)	2500			V/µs

Notes

(1) T_{amb} = 25 °C, V_{CC} = 5 V

(2) CM_H is the maximum slew rate of a common mode voltage V_{CM} at which the output voltage remains at logic high level (V_O > 2 V)

(3) CM_L is the maximum slew rate of a common mode voltage V_{CM} at which the output voltage remains at logic high level (V_O < 0.8 V)

TYPICAL CHARACTERISTICS (T_{amb} = 25 °C, unless otherwise specified)

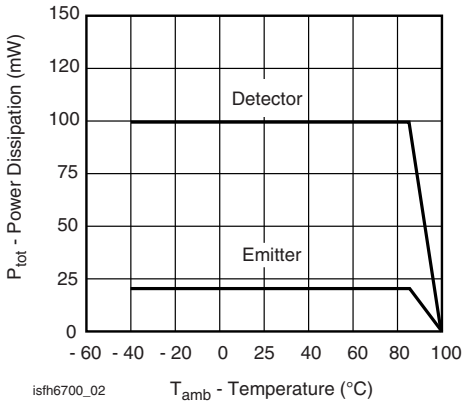


Fig. 2 - Permissible Total Power Dissipation vs. Temperature

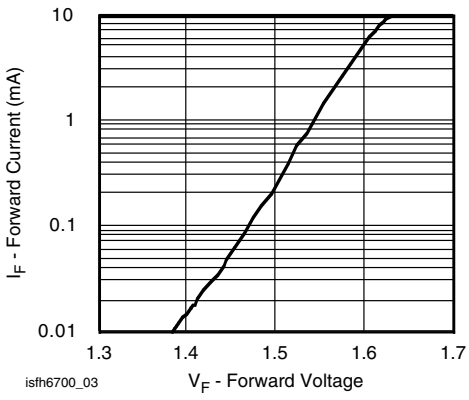


Fig. 3 - Typical Input Diode Forward Current vs. Forward Voltage

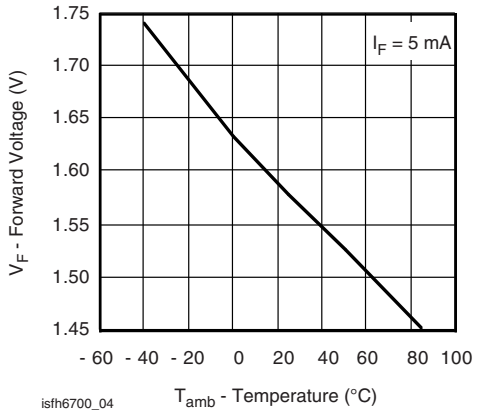


Fig. 4 - Typical Forward Input Voltage vs. Temperature

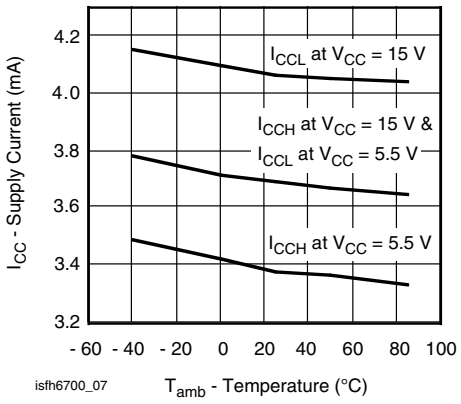


Fig. 7 - Typical Supply Current vs. Temperature

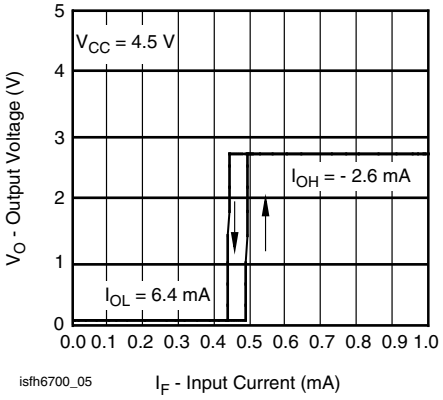


Fig. 5 - Typical Output Voltage vs. Forward Input Current (except SFH6705)

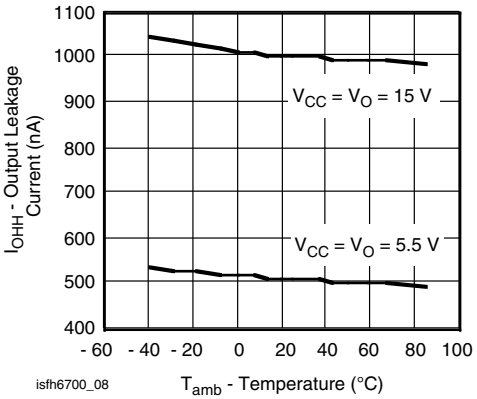


Fig. 8 - Typical Output Leakage Current vs. Temperature

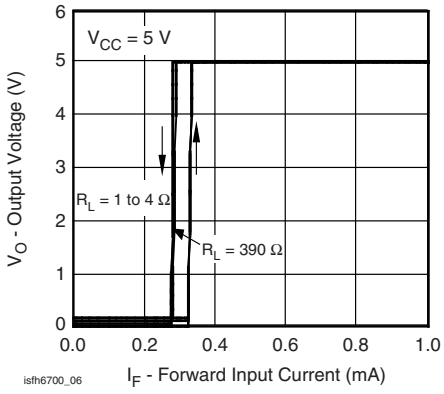


Fig. 6 - Typical Output Forward Voltage vs. Forward Input Current (only SFH6705)

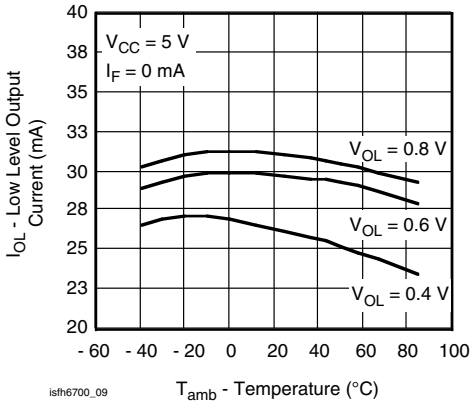


Fig. 9 - Typical Low Level Output Current vs. Temperature

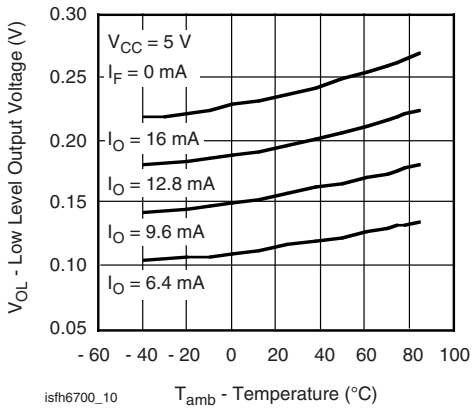


Fig. 10 - Typical Low Level Output Voltage vs. Temperature

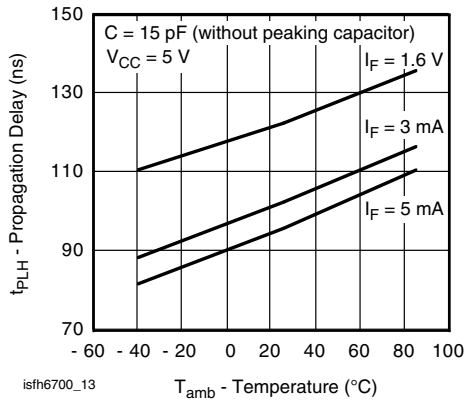


Fig. 13 - Typical Propagation Delay to Logic High vs. Temperature (except SFH6705)

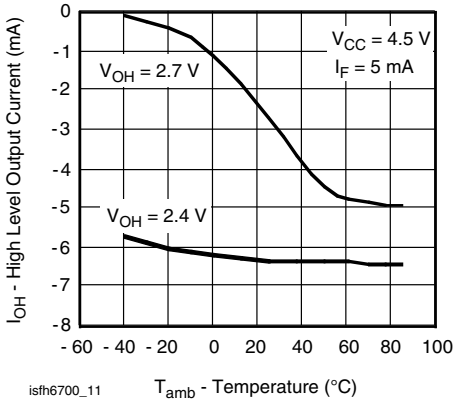


Fig. 11 - Typical High Level Output Current vs. Temperature (except SFH6705)

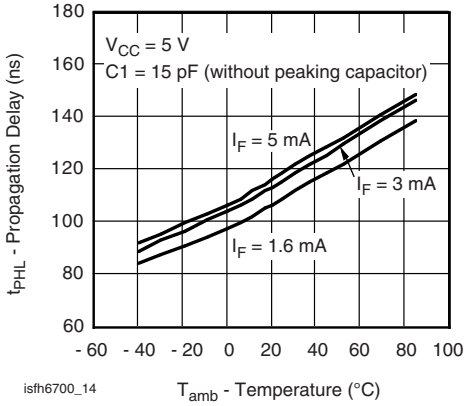


Fig. 14 - Typical Propagation Delay to Logic Low vs. Temperature (except SFH6705)

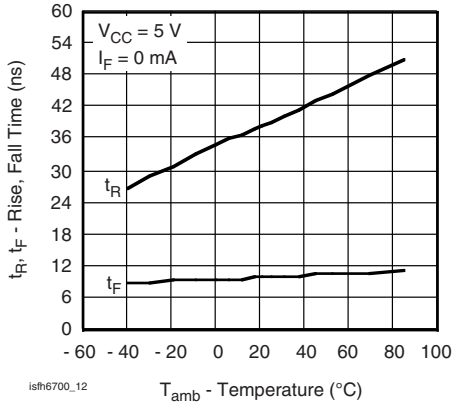


Fig. 12 - Typical Rise, Fall Time vs. Temperature (except SFH6705)

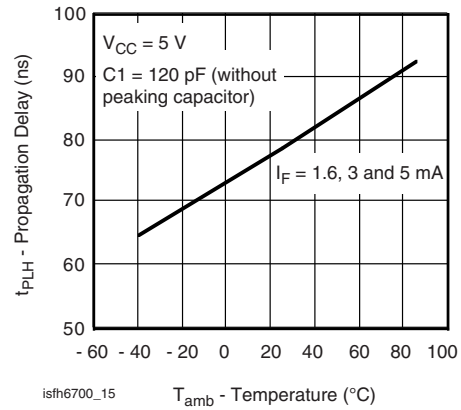


Fig. 15 - Typical Propagation Delays to Logic High vs. Temperature (except SFH6705)

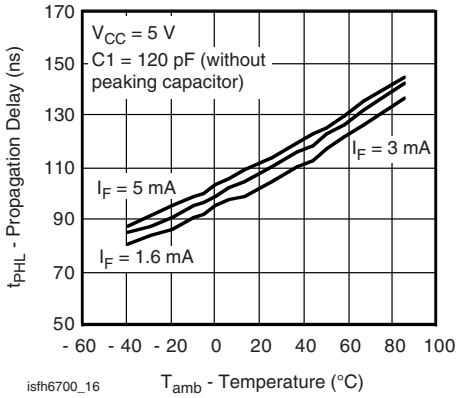


Fig. 16 - Typical Propagation Delay to Logic Low vs. Temperature

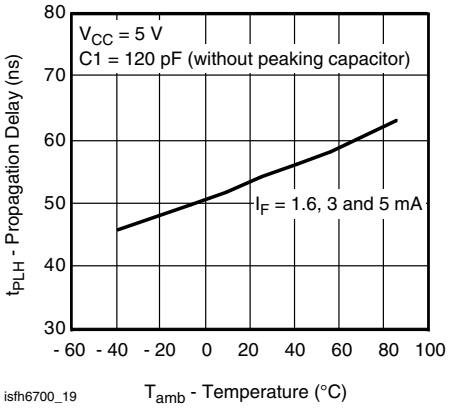


Fig. 19 - Typical Propagation Delays to Logic High vs. Temperature

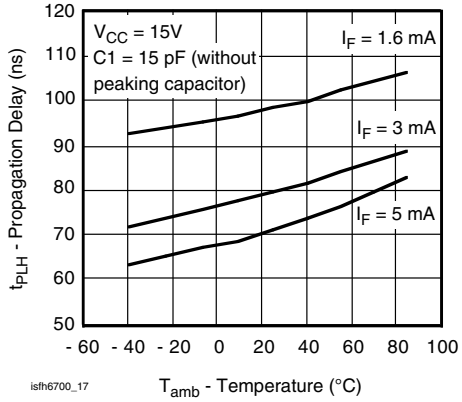


Fig. 17 - Typical Propagation Delays to Logic High vs. Temperature

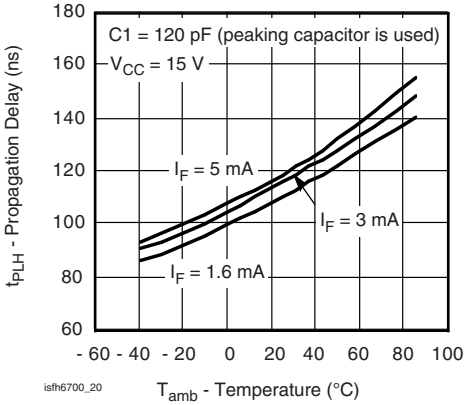


Fig. 20 - Typical Propagation Delays to Logic Low vs. Temperature (except SFH6705)

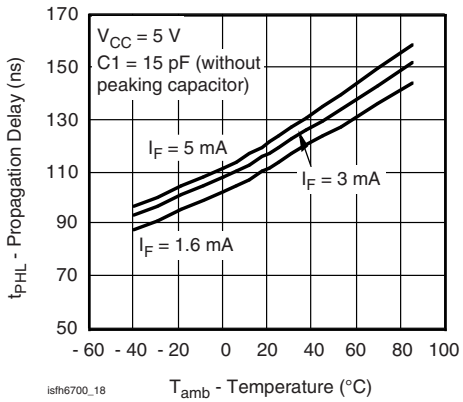


Fig. 18 - Typical Propagation Delays to Logic Low vs.Temperature

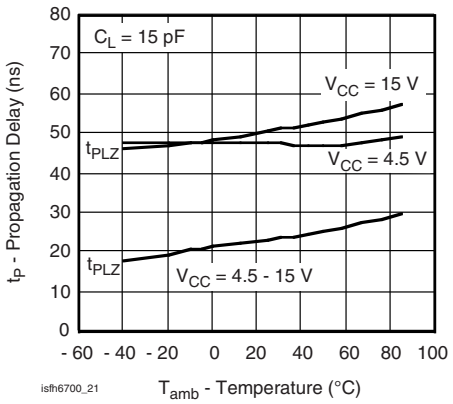


Fig. 21 - Typical Logic Low Enable Propagation Delays vs. Temperature (only SFH6700/11)

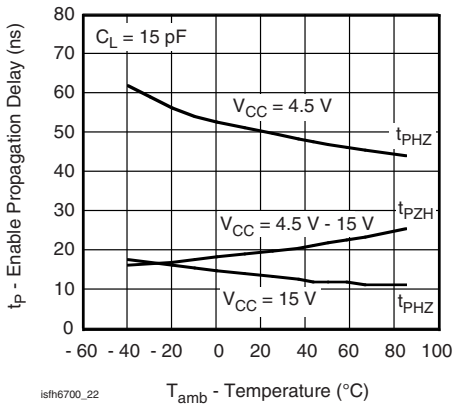


Fig. 22 - Typical Logic High Enable Propagation Delays vs. Temperature (only SFH6700/11)

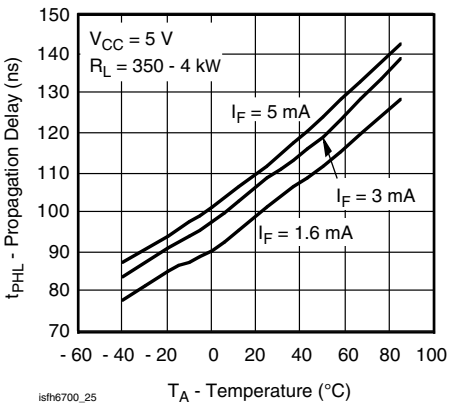


Fig. 25 - Typical Propagation Delays to Low Level vs. Temperature (only SFH6705)

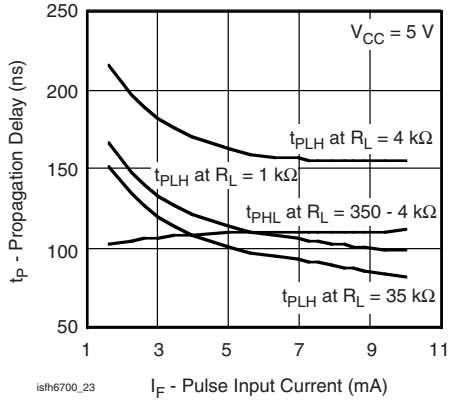


Fig. 23 - Typical Propagation Delays vs. Pulse Input Current (only SFH6705)

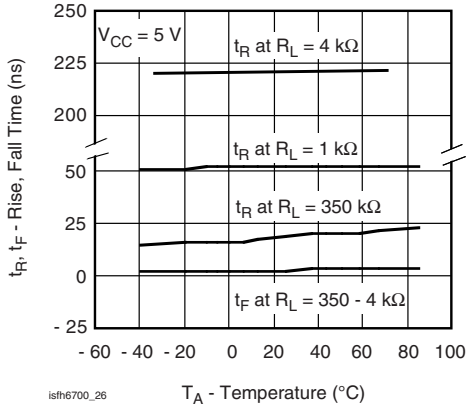


Fig. 26 - Typical Rise, Fall Time vs. Temperature (only SFH6705)

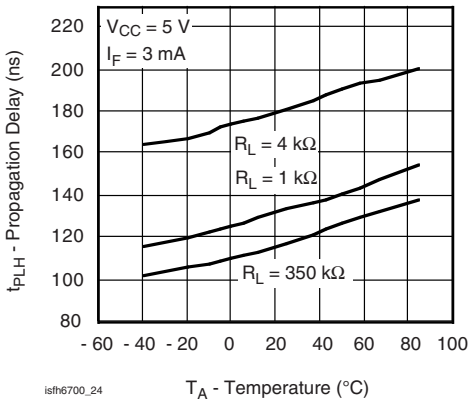
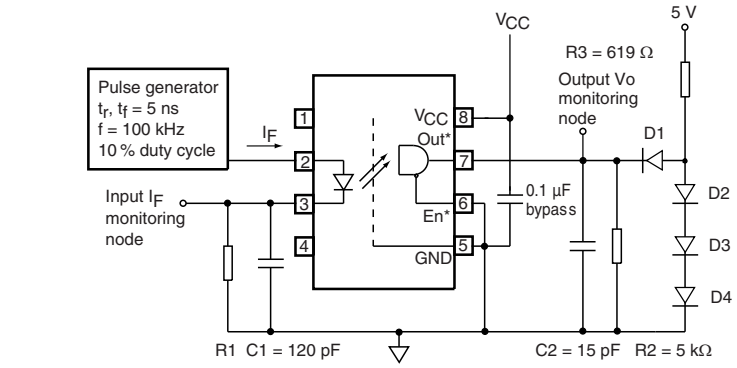


Fig. 24 - Typical Propagation Delays to High Level vs. Temperature (only SFH6705)



The probe and jig capacitances are included in C1 and C2 All diodes are 1N916 or 1N3064

R1	2.15 kΩ	1.1 kΩ	681 Ω
I_{Fon}	1.6 mA	3 mA	5 mA

* SFH6701, SFH6702, SFH6711, SFH6712 without V_{EN}
* SFH6702, SFH6712 pin 6 V_{OUT} and pin 7 NC

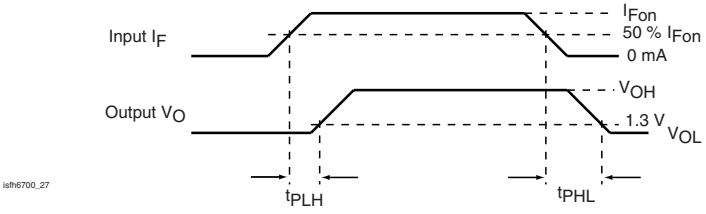
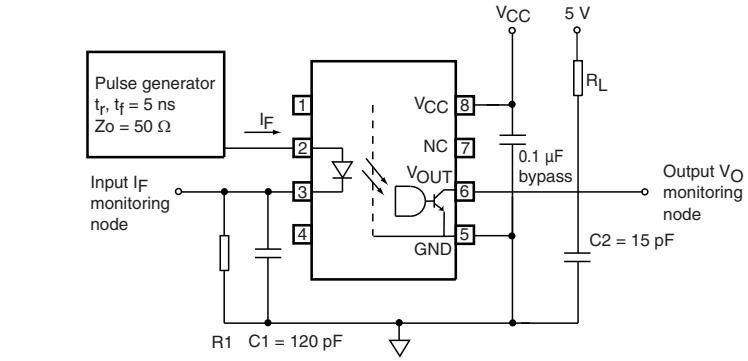


Fig. 27 - Test Circuit for t_{PLH}, t_{PHL}, t_r and t_f



The probe and jig capacitances are included in C1 and C2

R1	2.15 kΩ	1.1 kΩ	681 Ω
I_{Fon}	1.6 mA	3 mA	5 mA

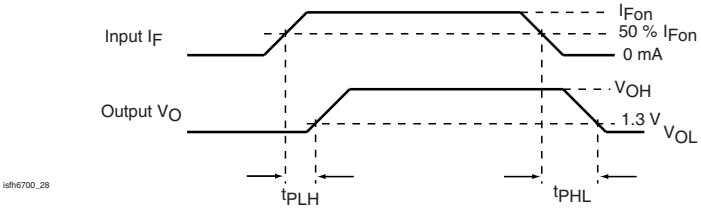


Fig. 28 - Test Circuit for t_{PLH}, t_{PHL}, t_r and - SFH6705

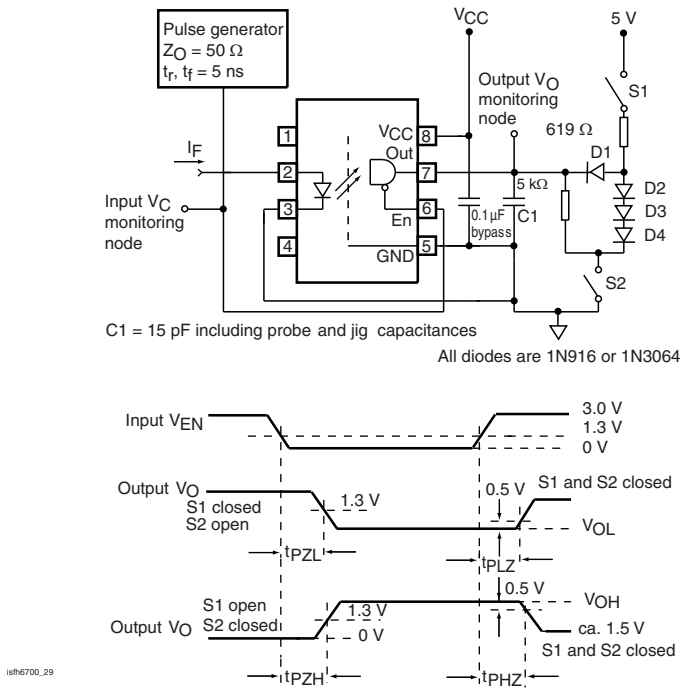


Fig. 29 - Test Circuit for t_{PHZ}, t_{PZH}, t_{PLZ} and t_{PZL} - SFH6700/19

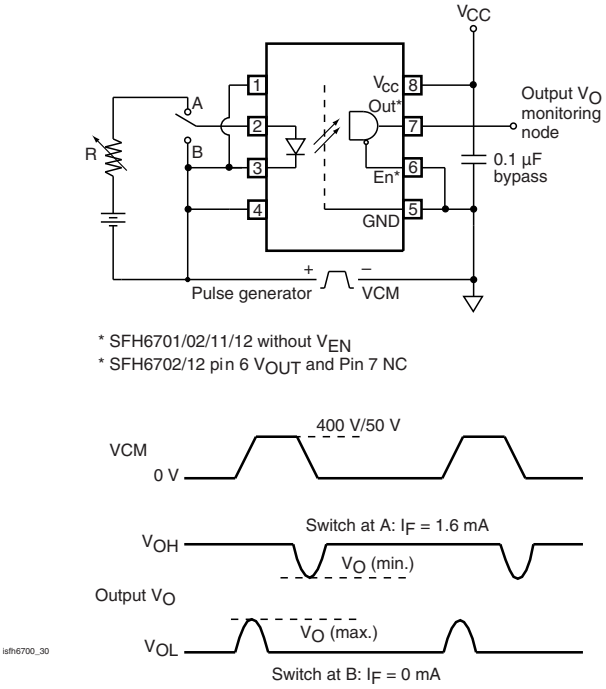


Fig. 30 - Test Circuit for Common Mode Transient Immunity and Typical Waveforms - SFH6700/01/02/11/12/19

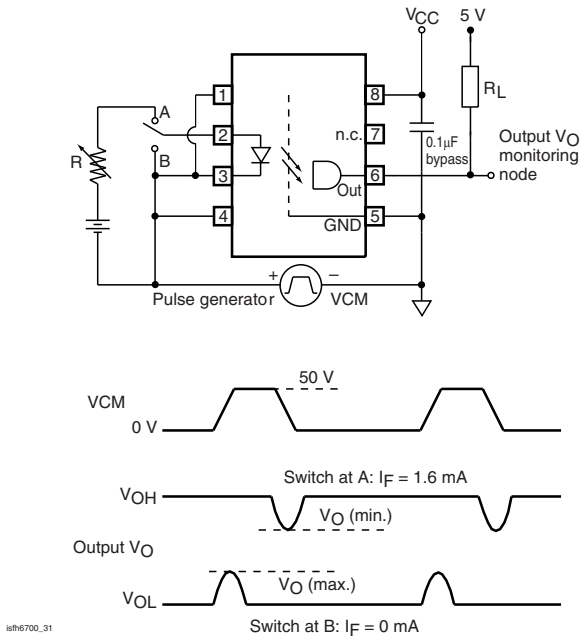
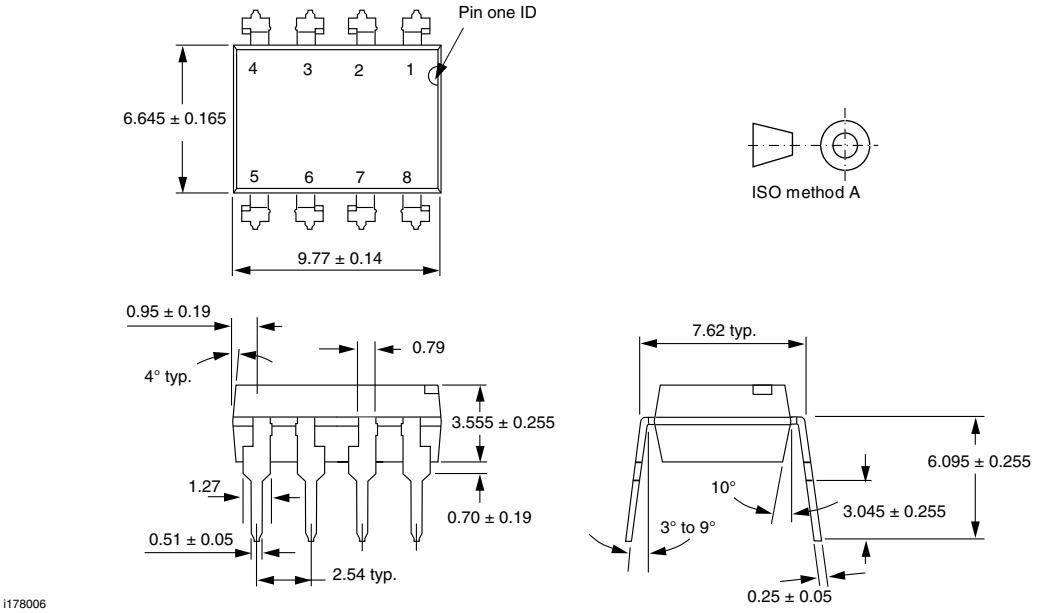
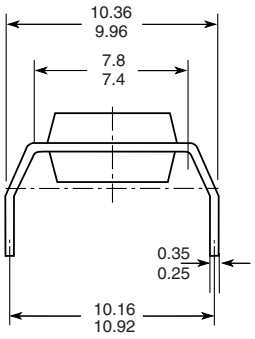


Fig. 31 - Test Circuit for Common Mode Transient Immunity and Typical Waveforms - SFH6705

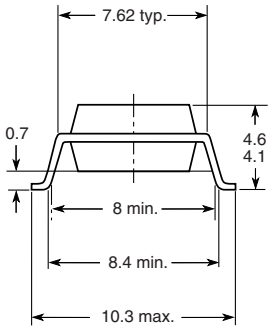
PACKAGE DIMENSIONS in millimeters



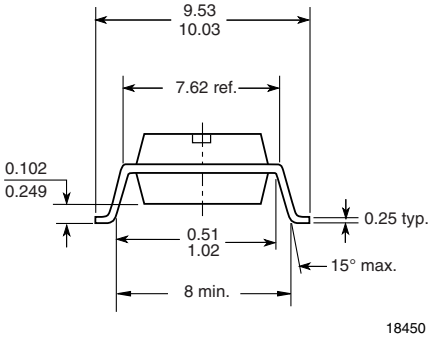
Option 6



Option 7



Option 9



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