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DESIGN SIMULATION AND IMPLEMENTATION OF CASCADED BUCK SQUARE CONVERTER FOR HIGH VOLTAGE STEP-DOWN APPLICATIONS

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Abstract

DC-DC converter has several applications, including power supplies to the electronic circuits, integrated circuits, and microprocessors; moreover, they can be used as an auxiliary power supply for the modular inverter systems, thus feeding the drivers, controller IC's and its protection circuit. Applications where we need to step down DC voltages and a high conversion ratio are required; a cascaded buck converter can efficiently perform the task. Cascaded buck has been extensively reported in the power electronics literature. The main features of cascaded buck are a large regulation range high voltage step-down ratio. Single-stage buck converter has issues related to the size of parameters and a high conversion ratio. As the duty ratio comes closer to 0 or 1, degradation occurs in inductor current and output voltages. Buck square converter provides us higher conversion ratio and a large range of load regulation. The proposed design bucks a high voltage DC (315V) to a very low voltage DC (5V). This paper illustrates the buck square idea and provides information about how to design this converter. Hardware design is implemented having a high conversion ratio, i.e., high voltage input and low voltage output (315V DC to 5V DC), and desired results were observed.

Keywords: Buck square converter, Cascaded buck converter, Power electronics.

1. Introduction

The control of DC-DC converter is very important in many applications in engineering, as machine drives, input sage regulation in renewable energy systems, supplying of electronic equipment, etc. [1, 2]. Due to the environmental problems and energy shortage, the world is paying attention to renewable energy sources like solar cells (PV arrays) and wind turbine generators [3]. The output from renewable energy sources is unregulated and needs power converters for regulation such as DC-DC converters [4-10].

The power generated from these sources can be connected to grids through power converters. Moreover, the power system based on renewable energy sources and storage devices like batteries is another solution to provide electricity to remote areas. Typically, batteries are required for that stand-alone system so that in the absence of renewable energy sources, batteries are used to supply the load power [11]. Buck converters are used for the charging purpose of batteries because of their low control complexity and simplicity of structure.

For a high step-down voltage conversion ratio, i.e., high input and low output voltage systems, a voltage divider can easily obtain a lower voltage level (reference). Still, it dissipates much power and for power delivery purposes it offers very bad and poor efficiency, and also load regulation is very poor, it cannot be used. Buck converter is an efficient way to step down the high-level DC voltages to a low-level DC voltage. The limitation of the single-stage buck converter is that it is not desirable to use it for a high voltage step down-ratio. The conventional buck is not desirable because an extreme duty cycle is required to achieve this high conversion ratio. The conduction losses of diode increase because switching time is extremely low [12].

Moreover, to operate the converter at high frequency, ultra-fast switching devices are required. The power loss increases in buck converter due to the voltage and current stress in active power devices. As the duty ratio comes closer to 0 or 1, degradation occurs in inductor current and output voltages [13]. As a result, the output voltages and efficiency of the converter gets deteriorated.

Several stage buck converters (cascaded buck) have been proposed to overcome the limitations of the single-stage buck converter for a high voltage step-down ratio [14]. The buck square is a two-cascaded buck converter used in those applications where higher conversion ratios and non-isolation are required. Cascaded buck converter has been extensively used and has many applications in power electronics literature. The converter can be operated in continuous conduction mode (CCM) and discontinuous conduction mode (DCM). However, for n-stage buck converter, more including power switches and gate driver circuits, due to which cost and power losses in converter increases, and its efficiency get effected, i.e., decreases [15].

This paper proposed methodology, design, and calculations for 50W load with the input of 315V DC. The input of the first converter is 315V DC and will use a duty cycle (D) of 0.13. The output of the first converter is the input to the second converter that converts the voltage to 5V, as shown in Fig. 1.

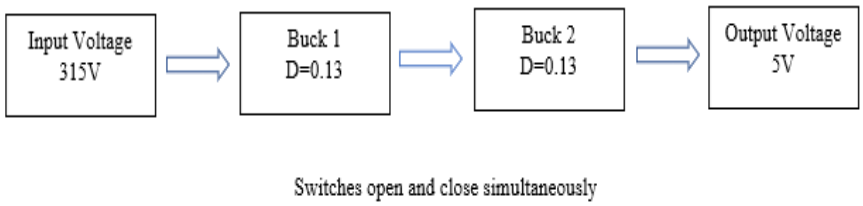


Fig. 1. Cascaded Buck block diagram.

2. Converter Analysis

A buck square circuit (two-stage cascaded buck) is shown in Fig. 2. The circuit consists of two inductors, two power switches, two capacitors, diodes, and a load. The pulse width modulation (PWM) of frequency f is provided to both power switches (MOSFETs) simultaneously so that the switch opens and closes simultaneously. The ON and OFF time of switches is controlled by the duty cycle (D) of PWM. The duty cycle of PWM is adjusted according to the step-down voltage conversion ratio required. Only one gate driver is required to open and close both switches simultaneously.

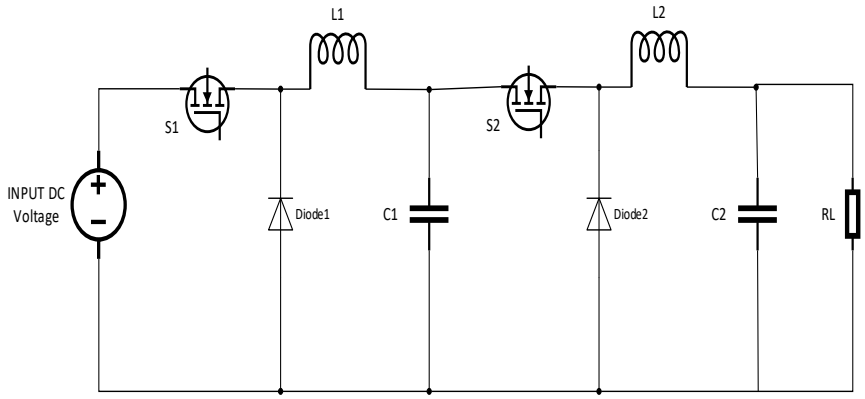


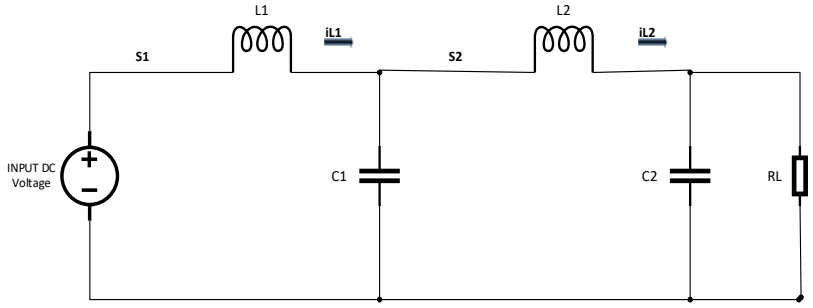
Fig. 2. Buck square circuit.

3. Mathematical Derivations

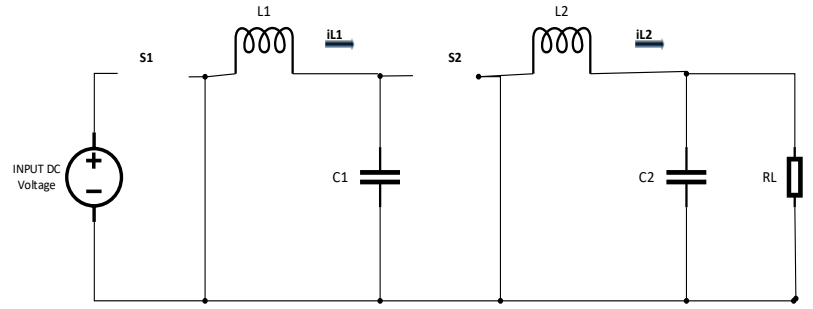
Switching action is shown in Table 1, and four different circuit configurations are obtained, as shown in Fig. 3. By using these switching actions, system equations are obtained, and by using these equations, formulas are derived that are then used to obtain the values of inductor and capacitors.

Table 1. Switching modes.

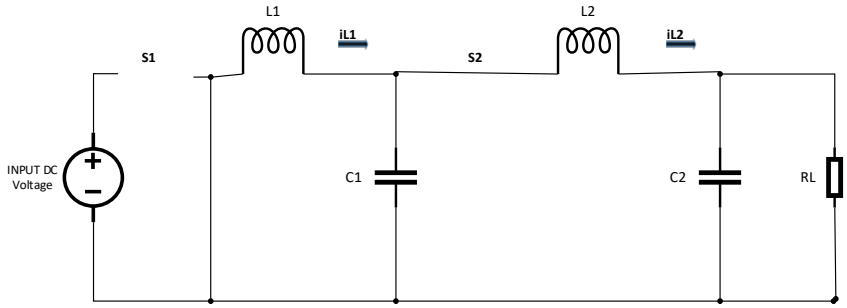
S_1	S_2	Circuit Fig. 2
1	1	a
0	0	b
0	1	c
1	0	d



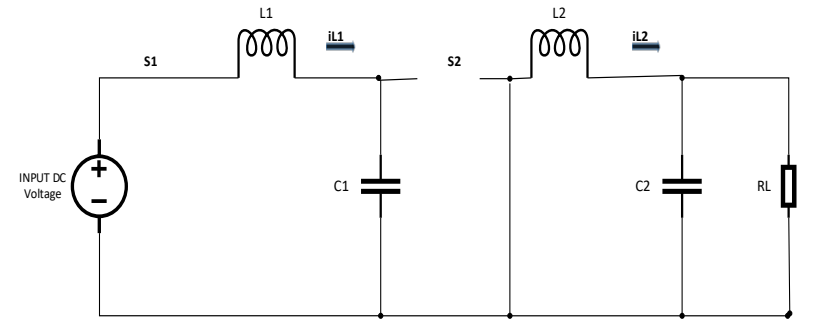
(a) Both Switches closes simultaneously



(b) Both Switches opens simultaneously



(c) S_1 open, S_2 close



(d) S_1 close, S_2 open

Fig. 3. Different switching modes

3.1. Case 1

Let's consider the switches (S_1, S_2) are closed simultaneously. In this state, the capacitor C_1 works as a voltage source for the second stage. The diodes (D_1, D_2) in both stages are reversed biased. The circuit in that case, is shown in Fig. 3(a). The system equations from this circuit are given by the Eqs. (1)-(4).

During this period, when the switches are closed, the voltages the inductors (L_1, L_2) are given by

$$\frac{di_{L1}}{dt} = \frac{V_s - V_{C1}}{L_1} \tag{1}$$

$$\frac{di_{L2}}{dt} = \frac{V_{C1} - V_{C2}}{L_2} \tag{2}$$

and the current across the capacitors C_1 and C_2 are given by

$$\frac{dV_{C1}}{dt} = \frac{i_{L1} - i_{L2}}{C_1} \tag{3}$$

$$\frac{dV_{C2}}{dt} = \frac{R_L i_{L2} - V_{C2}}{RC_2} \tag{4}$$

3.2. Case 2

Now consider the switches (S_1, S_2) are opened simultaneously. The circuit obtained in that case is shown in Fig. 3(b). Both the inductors in this state system are discharging and creates two independent loops through diodes of each stage. The system equations in this state are given by Eqs. (5)-(8).

In this switching action, the voltages across inductors L_1 and L_2 are given by

$$\frac{di_{L1}}{dt} = \frac{-V_{C1}}{L_1} \tag{5}$$

$$\frac{di_{L2}}{dt} = \frac{-V_{C2}}{L_2} \tag{6}$$

and the capacitors currents are given by

$$\frac{dV_{C1}}{dt} = \frac{i_{L1}}{C_1} \tag{7}$$

$$\frac{dV_{C2}}{dt} = \frac{R_L i_{L2} - V_{C2}}{RC_2} \tag{8}$$

In that case, the formula for capacitor C_1 after solving equations is as below

3.3. Case 3

Now, if the switch S_1 is closed and S_2 is open, it means Duty cycle $D_1 < D_2$. As a result, the second stage of the cascaded buck has a conversion ratio greater than the first stage of the cascaded buck. In this case, the equations are given as Eqs. (9)-(12).

$$\frac{di_{L1}}{dt} = \frac{-V_{C1}}{L_1} \tag{9}$$

$$\frac{di_{L2}}{dt} = \frac{V_{C1} - V_{C2}}{L_2} \tag{10}$$

and the capacitors currents are given by

$$\frac{dV_{C1}}{dt} = \frac{i_{L1} - i_{L2}}{C_1} \tag{11}$$

$$\frac{dV_{C2}}{dt} = \frac{R_L i_{L2} - V_{C2}}{RC_2} \tag{12}$$

In this case, there are two changed OFF and ON states for each switch. When both switches are ON, Fig. 3(a), then both inductor currents i_{L1} and i_{L2} rise linearly, and capacitor current i_{C1} decreases at a rate of i_{L1}-i_{L2}. Output voltages V_O discharges through the load resistance R_L. As D_1<D_2, the switch S_1 gets OFF, and S_2 remains ON, Fig. 3(c). In this state, i_{L1} decreases linearly, and i_{L2} increases linearly. The capacitor current i_{C1} decreases at the rate - i_{L1}-i_{L2}, and output voltages V_O get decreased. A state comes when both S_1 and S_2 are OFF, Fig. 3(b). At this state, i_{L1} decreases continuously, while iL2 reduces linearly, iC1 lessons at the rate of -iL1 and VO are linearly increased. In that case, the formula for capacitor C_1 after solving equations is as below

$$C_1 = \left[i_{L1} + \frac{\Delta i_{L1}(D_1 - D_2)}{2(1-D_1)}\right](1 - D_2)T\left(\frac{1}{\Delta V_O}\right) \tag{13}$$

3.4. Case 4

Now, if the switch S_1 is closed and S_2 is open, it means Duty cycle D_1> D_2. As a result, the first stage of the cascaded buck has a lower conversion ratio than the second stage. In this case, the equations are given as Eqs. (14)-(17).

$$\frac{di_{L1}}{dt} = \frac{V_S - V_{C1}}{L_1} \tag{14}$$

$$\frac{di_{L2}}{dt} = \frac{-V_{C2}}{L_2} \tag{15}$$

and the capacitors currents are given by

$$\frac{dV_{C1}}{dt} = \frac{i_{L1}}{C_1} \tag{16}$$

$$\frac{dV_{C2}}{dt} = \frac{R_L i_{L2} - V_{C2}}{RC_2} \tag{17}$$

In this case, there are two changed OFF and ON states for each switch. When both switches are ON, Fig. 3(a), then i_{L1} and i_{L2} rise linearly, and capacitor current i_{C1} decreases at a rate of i_{L1}-i_{L2}. Output voltages V_O discharges through the load resistance R_L. As D_1>D_2, the switch S_2 gets OFF, and S_1 remains ON, Fig. 3(d). In this state, i_{L2} decreases linearly, and i_{L1} increases linearly. The capacitor current i_{C1} decreases at the rate i_{L1}, and output voltages V_O increases. A state comes when both S_1 and S_2 are OFF, Fig. 3(b). At this state, i_{L2} decreases continuously, while i_{L1} reduces linearly, i_{C1} lessons at the rate of -i_{L1}-$i_{L2}$and V_O is linearly increased. In that case, the formula for capacitor C_1 after solving equations is as below

$$C_1 = \left[i_{L1} + \frac{\Delta i_{L1}(D_1 - D_2)}{2(D_1)}\right](1 - D_2)T\left(\frac{1}{\Delta V_O}\right) \tag{18}$$

4. Design Parameters/Formulas

In equilibrium, the voltages across the inductor $L_1$are zero, and by Using the approximation for small-ripple, then solving Eqs. (1) and (5), we obtain

$$V_{C1} = V_s D \tag{19}$$

Similarly, from Eqs. (2) and (6), taking voltages across L_2 at equilibrium gives

$$V_{C2} = V_{C1} D \tag{20}$$

From Eqs. (19) and (20), the static gain (duty ratio) is obtained for the convertor that is given by

$$D = \sqrt{(V_o}/V_s)$$

or

$$D^2 = \frac{V_o}{V_s} \tag{21}$$

The Eqs. (1)-(8) are obtained from cases 1 and 2 are used to derive formulas for inductors and capacitors. The formulas for inductor and capacitor values are given by Eqs. (22)-(25)

$$L1 = \frac{(Vs - Vc_1)D_1 T}{\Delta i_{L_1}} \tag{22}$$

$$L2 = \frac{(Vc_1 - V_0)D_2 T}{\Delta i_{L_2}} \tag{23}$$

$$C_1 = \frac{i_{L_1}(1 - D_2)T}{\Delta V_{C1}} \tag{24}$$

$$C_2 = \frac{T\Delta i_{L_2}}{8\Delta V_{C_2}} \tag{25}$$

Here C_1 is for the state when D_1=D_2 and both switches operate simultaneously. For non-similar duty ratios, C_1 will be equal to equations given in case 3 and case 4 according to conditions.

Where V_S are input voltages to the first stage of the cascaded buck convertor, V_{C1} is the voltage across capacitor C_1, D_1 and D_2 are the duty cycles for both switches, Δi_{L_1}, Δi_{L_2}, ΔV_{C1} and ΔV_{C2} are inductor current ripples and capacitor voltage ripples, respectively. For the same duty cycle, D_1=D_2=D.

5. Calculations

To calculate the values of inductors and capacitors for a 50W converter with a high conversion ratio having high input DC voltages (315V) to low DC voltages (5V), the duty ratio is first calculated using Eq. (21).

Both switches operate simultaneously, i.e., D_1=D_2

$$D = \sqrt{(V_o}/V_s)$$

V_O = 5V, V_S = 315V

$D = \sqrt{(5/315)}$

$D = 0.13\ or\ 13\%$

This percentage of the gate pulse has a high reference value due to which MOSFET's gets in conducting mode. The rest of the gate pulse has zero references, and MOSFET remains OFF for that duration.

Also, for 50 W power with output voltage 5V, the values of load current and load resistances can be calculated, i.e., I_L = 10A and R_L = 0.5ohm.

Using the value of D, calculate the values of capacitors and inductors using the capacitance and inductance formulas with 10% ripple, V_s = 315V, V_{C1} obtained from Eq. (9), V_{C2}=5V, and frequency f=20 kHz. The values obtained after solving are given in Table 2.

Table 2. Values.

Capacitor's	Inductor's
C_1 = 64.798uF	L_1 = 14.6mH
C_2 = 625uF	L_2 = 0.231595mF

6. Results and Discussions

The proposed converter shown in Fig. 4 is simulated in PSIM software, and hardware is also performed. The results and waveforms of the converter were observed.

6.1. Simulation circuit

The figure shows the simulation circuit of the buck square converter. Two buck converters are connected in series. The output of the first stage is the input of the second stage. The circuit includes two inductors, two capacitors, Power MOSFET for switching, and diodes. Input voltages are set at 315V, and the desired output is obtained. Switching frequency is set at 20 k, and considering case 1 & case 2, duty ratio D is adjusted to 0.13 or 13% for both gate drivers.

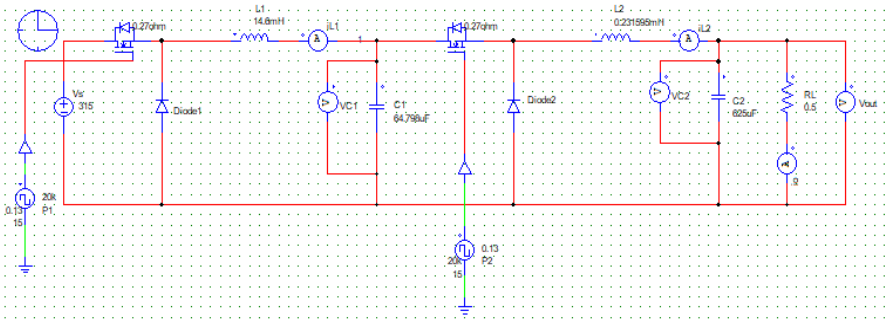
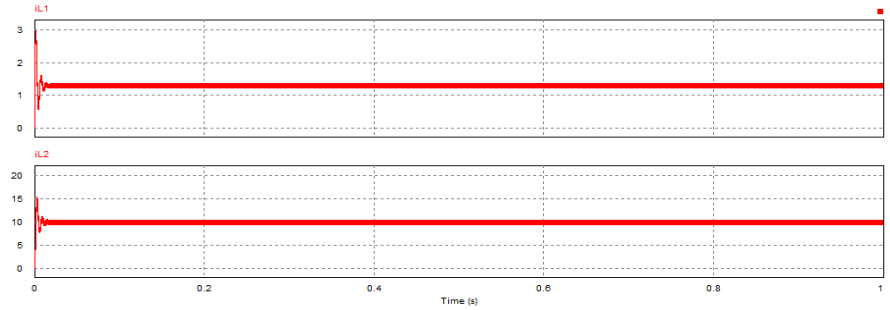


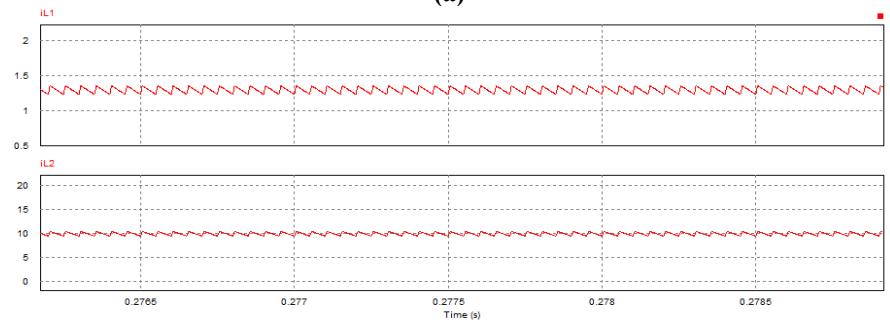
Fig. 4. Buck square simulation circuit.

(i) Current waveforms

The current I flows through inductors, and the waveform obtained is shown in Fig. 5(a). The magnified waveform is shown in Fig. 5(b). The inductor current rises and decays as it charges and discharges.



(a)

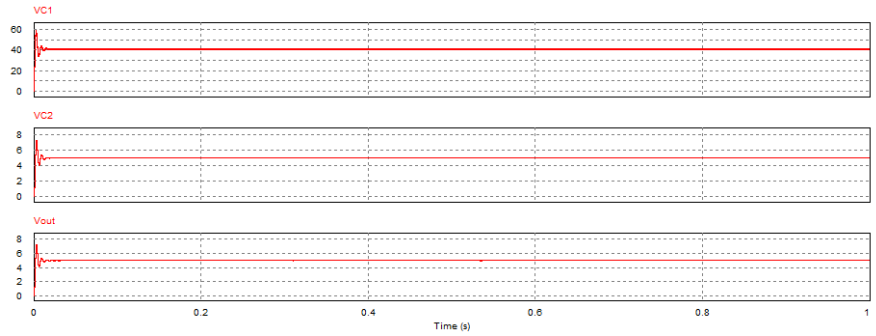


(b)

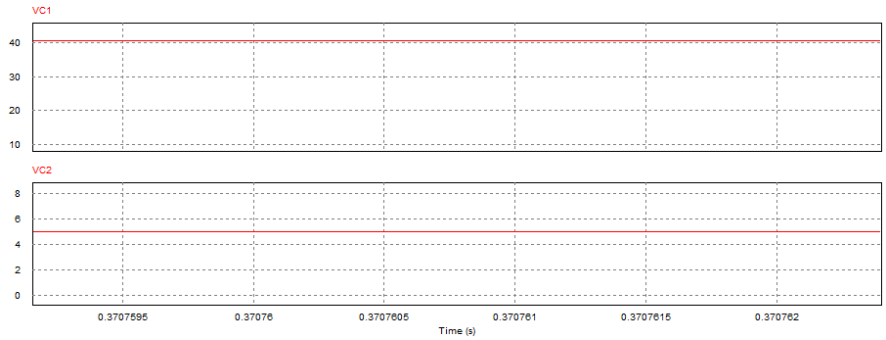
Fig. 5. Inductor current waveform.

(ii) Voltage waveforms

Figure 6(a) shows the voltages across the capacitors, and its magnified view is shown in Fig. 6(b). From the figure, it can be observed that the output voltage of the first stage is 41V. The output of the first stage is made the input of the second stage. The final output of the converter is bucked up to 5V, as shown in the graph.



(a)



(b)

Fig. 6. Capacitor voltage waveform.

The results observed for capacitor voltages, output voltages, inductor current, and output current from simulations are according to the desired values as calculated. Output voltages, inductor current, and output currents were observed for the proposed converter at V_S=315V by varying duty ratio D from 0.08 to 0.17. Here $V_{O1}=V_{C1}$ and $V_{O2}=V_{C2}$. Results obtained from these are shown in Table 3.

Table 3. Average output voltages and inductor currents of the proposed converter at Vs=315 V with D varied from 0.08 to 0.17.

D	Vo1 (V)	Vo2 (V)	iL1 (A)	iL2 (A)	io (A)
0.08	25.299	1.928	0.2704	3.6675	3.856
0.09	28.489	2.428	0.3948	4.6199	4.855
0.1	31.687	2.98	0.5499	5.6787	5.984
0.11	34.894	3.589	0.7395	6.8381	7.178
0.12	38.109	4.249	0.9659	8.1006	8.499
0.13	41.335	4.963	1.2323	9.4629	9.92
0.14	44.568	5.724	1.542	10.923	11.45
0.15	47.81	6.54	1.896	12.4823	13.074
0.16	51.06	7.397	2.299	14.133	14.175
0.17	51.758	8.049	2.88	16.655	16.61

Output voltages, inductor current and, output currents were observed for the proposed converter at V_S=250V by varying duty ratio D from 0.08 to 0.17. Results obtained from these are shown in Table 4.

Table 4. Average output voltages and inductor currents of the proposed converter at Vs=250 V with D varied from 0.08 to 0.17.

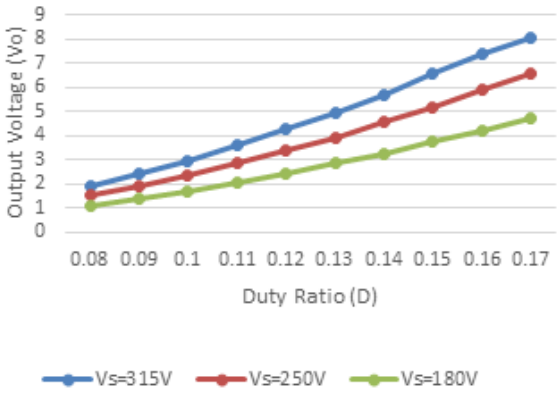
D	Vo1 (V)	Vo2 (V)	iL1 (A)	iL2 (A)	io (A)
0.08	20.079	1.53	0.2146	2.911	3.061
0.09	22.612	1.927	0.313	3.67	3.853
0.1	25.149	2.367	0.436	4.507	4.733
0.11	27.694	2.848	0.587	5.43	5.697
0.12	30.256	3.373	0.767	6.429	6.745
0.13	32.805	3.94	0.978	7.51	7.875
0.14	35.37	4.543	1.22	8.67	9.085
0.15	37.94	5.19	1.55	9.91	10.38
0.16	40.525	5.87	1.825	11.217	11.47
0.17	43.112	6.594	2.186	12.603	13.19

Output voltages, inductor current, and output currents were observed for the proposed converter at V_S=180 V by varying duty ratio D from 0.08 to 0.17. Results obtained from these are shown in Table 5.

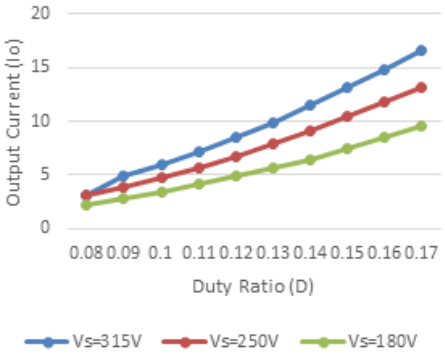
Table. 5 Average output voltages and inductor currents of the proposed converter at Vs=180 V with D varied from 0.08 to 0.17.

D	Vo1 (V)	Vo2 (V)	iL1 (A)	iL2 (A)	io (A)
0.08	14.457	1.10	0.1545	2.0957	2.204
0.09	16.28	1.39	0.2256	2.6399	2.774
0.1	18.11	1.7	0.3142	3.245	3.41
0.11	19.94	2.05	0.4226	3.9075	4.1
0.12	21.78	2.43	0.552	4.6289	4.856
0.13	23.62	2.84	0.7042	5.4074	5.67
0.14	25.47	3.27	0.881	6.242	6.54
0.15	27.32	3.74	1.084	7.133	7.47
0.16	29.18	4.23	1.3142	8.076	8.455
0.17	31.04	4.75	1.5737	9.0743	9.495

From the observed values, the relation between duty ratio vs output voltage and output current was observed. Results are plotted and compared for different input voltages, as shown in Fig. 7.



(a) output voltages vs. duty ratio.



(b) output current vs. duty ratio.

Fig. 7. Graphs for the proposed converter on different input voltages.

Different input voltages were applied, and the output voltages were observed for the proposed converter with duty ratio D (13%) constant. The results obtained were plotted, and it was observed that input voltages are related to output by linear relation, as shown in Fig. 8. Output voltages increase according to the input voltages.

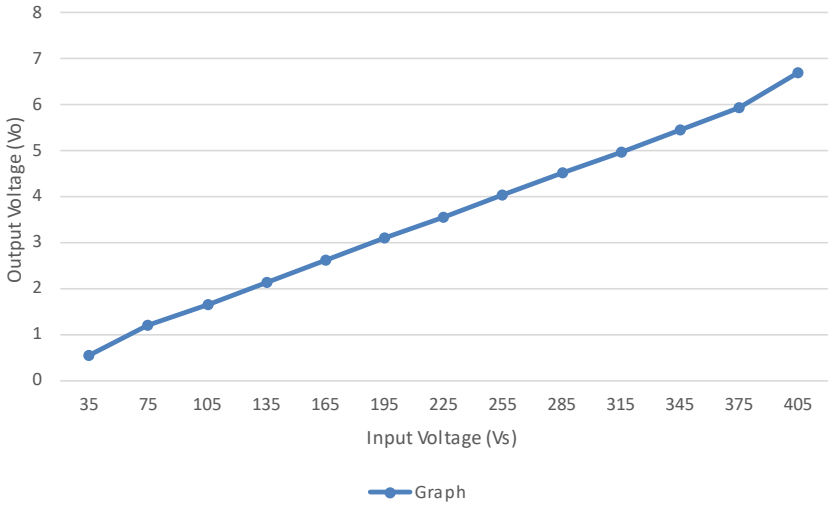


Fig. 8. Plot for V_O against Vs.

Table 6 represents the design parameters of the proposed converter. Specifications of converter such as power, voltages are given in Table 6.

Table 6. Design parameters.

Parameter	Value
Input Voltages	315 V
Switching Frequency	20 kHz
Duty ratio	13%
Current ripple (δI_L)	10%
Voltage ripple (δV_C)	2%
Output Voltages (V_{out})	5 V
Power (W)	50 W

6.2. Simulations for non-similar duty ratios

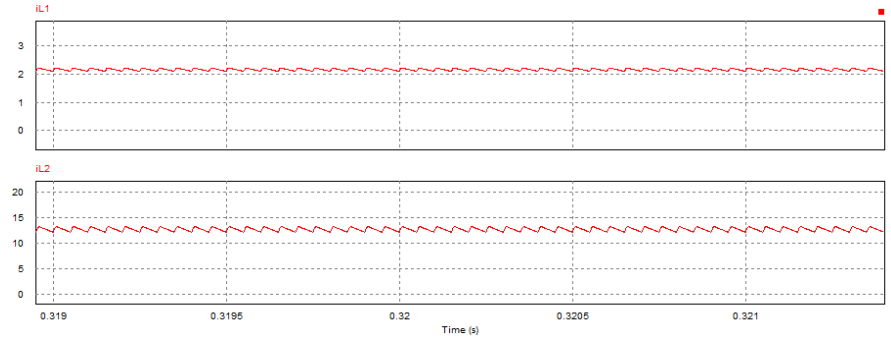
Now let us consider the other two cases, i.e., $D_1>D_2$ and $D_1<D_2$, and observe the effect of different duty ratios on the output voltages and current. Both the switches have different duty ratios. Figures 9 and 10 show results for both cases.

(1) First consider case 3, $D_1<D_2$ (D_1=0.13, D_2=0.17). Figs. 9(a) and (b) show the inductor current and capacitor voltage. From the graph, it can be observed that the inductor current is increased due to the duty ratio.

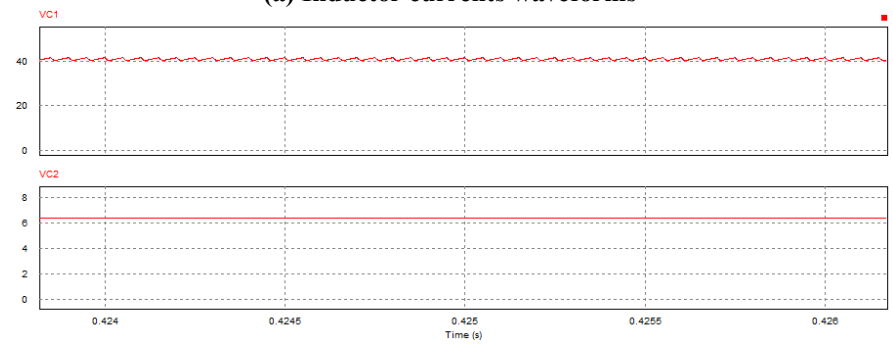
In this case, there are two changed OFF and ON states for each switch. When both switches are ON, both inductor currents iL1 and iL2 rise linearly, and capacitor current iC1 decreases at i_{L1}-i_{L2}. Output voltages V_O discharges through

load resistance. As $D_1<D_2$, the switch S_1 gets OFF, and S_2 remains ON. In this state, i_{L1} decreases linearly, and i_{L2} increases linearly. The capacitor current i_{C1} decreases at the rate - i_{L1}-i_{L2}, and output voltages V_O get reduced. A state comes when both S_1 and S_2 are OFF. At this state, i_{L1} decreases continuously, while iL2 reduces linearly, iC1 lessons at the rate of -iL1 and VO are linearly increased.

Duty cycle $D_1< D_2$ means the second stage of the cascaded buck has a conversion ratio greater than the first stage of the cascaded buck.



(a) Inductor currents waveforms



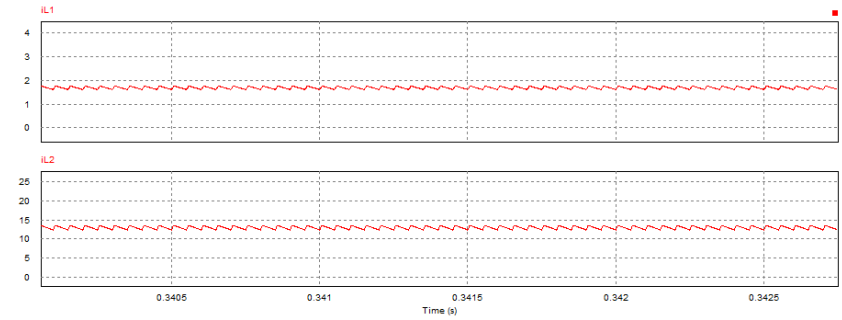
(b) Capacitor voltages waveforms

Fig. 9. Inductor current and capacitor voltage waveforms.

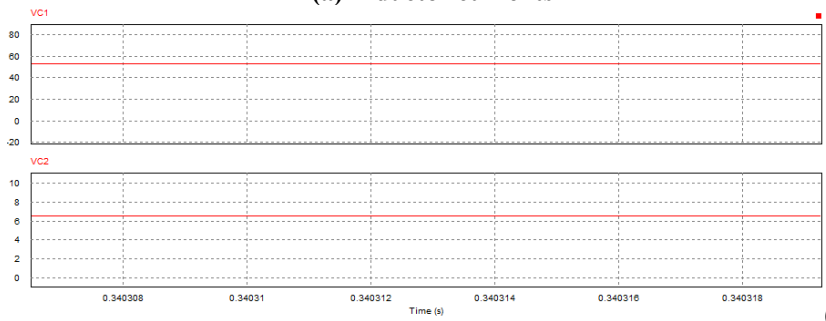
(2) Now consider case 4, $D_1>D_2$ (D_1=0.17, D_2=0.13). Figures 10(a) and (b) show the inductor current and capacitor voltage. From the graph, it can be observed that the inductor current is increased due to the duty ratio.

The case discussed below represents that there are two changed OFF and ON states for each switch. When both switches are ON, then i_{L1} and i_{L2} rise linearly, and capacitor current i_{C1} decreases at a rate of i_{L1}-i_{L2}. Output voltages V_O discharges through the load resistance R_L. As $D_1>D_2$, the switch S_2 gets OFF, and S_1 remains ON. In this state, i_{L2} decreases linearly, and i_{L1} increases linearly. The capacitor current i_{C1} decreases at the rate i_{L1}, and output voltages V_O increases. A state comes when both S_1 and S_2 are OFF. At this state, i_{L2} decreases continuously, while iL1 reduces linearly, iC1 lessons at the rate of -iL1-iL2 and VO are linearly increased.

Duty cycle $D_1> D_2$ means the first stage of the cascaded buck has a conversion ratio greater than the second stage of the cascaded buck.



(a) Inductor currents



(b) Capacitor voltages

Fig. 10. Inductor current and capacitor voltage waveforms.

6.3. Hardware design and results

For hardware design, some design parameters are changed. In hardware, the switching losses, diode conduction losses get involved, due to which some parameters were adjusted according to the hardware. Inductors are designed for the given values. Its design procedure is as below.

(i) Inductor design:

AWG gauge used: 22

Conductor diameter: 0.645 mm

L_1 current up to 4 A

L_2current up to 12 A

Diameter of core: 63 mm

Radius out: 0.0315 m

Radius inner: 0.0175 m

Area out: 3117.25 mm^2

Area inner: 962.11 mm^2

Area of core: 2155.14 rea of core

$L_C = \pi * (R_{OUT} + R_{in}) = 153.93$ mm

$R_C = L_C/u*Ac = 0.4433\times10^6$

Number of turns for $L_1 = 21$

Number of turns for $L_2 = 12$

(ii) Hardware circuits and results

Figure 11 shows the hardware circuit of the buck square converter. PCB was designed for circuits, and connectors were used for connections. Heat sinks were used on MOSFET for cooling purposes. MOSFET's and diodes are selected according to the parameters of the first and second stage cascaded buck converter. The function generator was used to generate a pulse having a frequency of 20 k, and the required duty cycle was adjusted to put MOSFET's in ON condition. MOSFET and Diode used for the first stage are IRFP460 and BY329F, respectively and for the second stage, MOSFET and Diode used are IRFP260N and BY359 respectively.

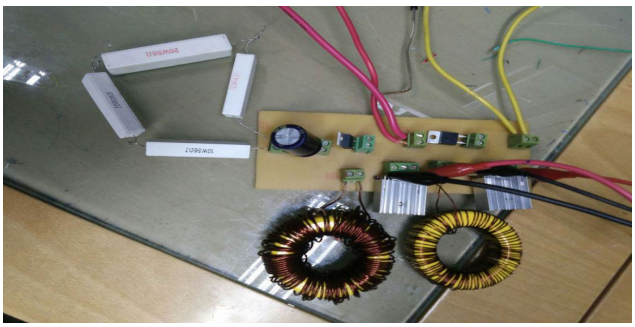


Fig. 11. Buck square converter.

Results

The input voltages were supplied using a trainer. And the voltages were increased steadily, and according to that, output voltages were observed. Input voltages were raised up to 310 V, and output voltages respective to the input voltages were 6.79V. The converter decreases the voltages in two steps. The first stage of cascaded buck steps down the input voltages from the source, and the output of the first stage becomes an input to the second stage of cascaded buck. The final output was obtained after the second stage of the converter. The input and output results are shown in Fig. 12.

The losses in the hardware circuit were because of different parameters like diode conduction losses, switching losses, inductor type, etc.

The main achievement of the research was that the hardware design was practically implemented for a high voltage steep down ratio, and high DC voltages were converted to a low level of DC voltages. The results obtained were near to the calculated and simulations values.

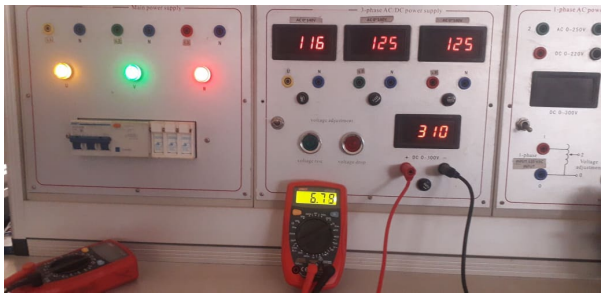


Fig. 12. Input and output voltages.

7. Environmental Aspect

The buck square converter is used in DC-DC distribution systems, where isolation is a problem. The efficiency of DC distribution systems is higher than AC distribution systems. Now a day, research is going towards the DC system. So, this buck square converter will be used in the DC system due to its high efficiency and an extensive range of load regulation. Buck square converter has higher efficiency.

8. Application

Buck square converter provides us higher conversion ratio with a large range of load regulation. So,

- This project can be utilized in those applications where we need a higher conversion ratio.
- The proposed system may be used in the power supply or may also be used in different projects as a subproject.
- Due to its high conversion ratio, the buck square converter can be utilized in DC-DC low and high voltage distribution systems.
- High voltages can be converted to low voltages using this converter without the isolation process.

9. Conclusion

The paper has presented a dc-dc converter with a high step-down conversion ratio. The operating principle of the converter has been discussed, and the conversion ratio of the converter has been examined. The goal was to achieve an efficient buck square converter that converts a very high voltage DC to a very low DC value. The attempt to portray the idea was very successful. The hardware prototype of the proposed circuit bucks 310V DC to 6.79V DC without the use of inverters and transformers, just as discussed in this paper. The simulation results and experimental hardware results indicate that the proposed converter is suitable for high-input voltage to low-output voltage conversion and also suitable for their applications.

10. Future Scope

Refer to this paper, small variations in the input voltage vary the output voltages, i.e., the output voltages are directly affected by changing the input voltages. This limitation causes changing voltages at the output which is undesirable for applications.

In the future, the following improvements are required:

- To overcome the limitation, variations in the input voltages do not affect the output voltages, i.e., output voltages remain constant.
- To generate pulse using microcontroller
- To design a converter without using an auxiliary power supply (external or extra supply used to power the MOSFET gate driver circuit).
- The range of input voltages and converter power can be increased

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