# UBC Department of Electrical and Computer Engineering

# CPEN 412 Syllabus

# Microcomputer Systems Design

* Description: Microprocessor and system buses; advanced I/O methods; priority interrupts; event/exception handling; serial I/O; computer networking; memory system design; interaction of hardware and software, microprocessor comparison, testability issues, safety critical systems.
* Pre-reqs: One of [EECE 353](https://courses.students.ubc.ca/cs/courseschedule?pname=subjarea&tname=subj-course&dept=EECE&course=353), [CPEN 311](https://courses.students.ubc.ca/cs/courseschedule?pname=subjarea&tname=subj-course&dept=CPEN&course=311) and one of [EECE 259](https://courses.students.ubc.ca/cs/courseschedule?pname=subjarea&tname=subj-course&dept=EECE&course=259), [CPEN 211](https://courses.students.ubc.ca/cs/courseschedule?pname=subjarea&tname=subj-course&dept=CPEN&course=211), [EECE 355](https://courses.students.ubc.ca/cs/courseschedule?pname=subjarea&tname=subj-course&dept=EECE&course=355), [CPEN 312](https://courses.students.ubc.ca/cs/courseschedule?pname=subjarea&tname=subj-course&dept=CPEN&course=312).

# Rationale

Microcomputers are now at the heart of all modern electronic and computer based systems, particularly for real-time and Internet of Things (IoT) devices. The design of these systems requires a detailed understanding of the particular processor, its operation, interfacing, timing and protocols with respect to memory and IO devices as well as an appreciation of the sophistication of modern microcomputers that now include multiple cores, caches and embedded operating systems.

# Resources

* All material is posted on Canvas

### Copyright Notice

* All materials of this course (handouts, lecture slides, assessments, course readings, etc.) are the intellectual property of Dr. Paul Davies or licensed to be used in this course by the copyright owner. Redistribution or uploading of this material to other sites without permission of the copyright holder(s) constitutes a breach of copyright and may lead to academic discipline.

# Course Structure

* Description: 3 Hours Lecture + 2 Hours Lab per week. Details here <https://courses.students.ubc.ca/cs/courseschedule?pname=subjarea&tname=subj-course&dept=CPEN&course=412>
* Your instructor will provide very detailed animated power point slides that you will be asked to read ahead of the lectures as well as sample code you are asked to experiment with.
* Piazza will be used and I encourage all students to discuss their issues and perhaps have them resolved by other students, but do not post code or solutions on Piazza as this could open you up to academic misconduct.

# Course Content

**Part A – Processor to Memory Interfacing**

* Memory Address Decoding: Full, Partial and Block decoding techniques, data bus width and byte/word alignment issues.
* Timing Analysis: Designing for Worst Case.
* Static Memory. Cell design, chip architecture, interfacing, access time calculations, synchronous vs Asynchronous operation, pipelining, dual port etc.
* Dynamic Memory (Dram): Cell and device architecture, asynchronous vs modern synchronous devices. Interfacing, protocol, timing, dram controllers, refreshing etc.
* Non-Volatile Memory Technologies: Rom, UV-Eproms, EEProm, Flash (NOR/NAND). Timing, cell and device architecture, interfacing, protocols (H/W and S/W).
* Error Correcting Memory systems (ECC): SED/SEC and DED/SEC designs.
* Direct Memory Access Controllers (DMAC) for high speed data transfers.
* Cache Design for High Speed CPU operation with Synchronous Dram. Direct vs set associative.
* Multi-core CPUs utilizing caches and shared main memory. Bus Arbitration, Hardware Mutual Exclusion, Cache Coherency, Bus “Snooping”

**Part B**

* Exception and Interrupt handling: Vectored vs non-vectored interrupts
* Buses as Transmission Lines: Issues surrounding reflections, propagation delays and termination.
* High Speed Microcomputer Buses: Electrical Interfacing, Protocol, Timing
  + Backplane buses: VME, PCi,
  + FPGA buses: Avalon, AMBA,
  + Network Buses: PCIe, Network on Chips.
* Slow speed Serial Chip and Network Buses: SPi, I2C and Canbus.
* Analog Interfacing: ADCs, DACs, Sample and Hold chips, analog switches, DAQs
* WiFi and Bluetooth, Graphics and Touchscreen interfaces, GPS and Timers, Opto-isolation + PWM, DC and Stepper Motor control: Incremental and Absolute position.
* Embedded OS’s: uC/OS II – Multithreading, Synchronisation etc.

# Course Learning Outcomes

Students shall be able to

1. Appreciate the differences between different manufacturer’s CPUs e.g. effect of data width, address range, timing and protocol and design memory and IO interfaces accordingly.
2. Appreciate the need for and role played by different kinds of volatile and non-volatile memory (Sram, Dram, EEProm, and Flash etc.) and design S/W drivers and memory controllers to interface the CPU to that technology.
3. Appreciate the role for ECC memory in high reliability memory systems and be able to design DED/SEC circuitry to perform that task.
4. Understand the importance, role and impact of standardized CPU, Backplane and other bus standards play in selecting a system’s architecture.
5. Apply simulation of circuit in the verification and testing of a circuit.
6. Understand the role played by Caches in building high performance single and multiple CPU systems and be able to design and quantify the performance of different types of cache design.
7. Appreciate the role played by an operating system in providing support for multi-tasking, abstraction of hardware via device drivers and support for open source software
8. Design and synthesize circuits to enable networking of multiple microcontrollers in a distributed system.
9. Design circuits to utilize non-volatile memory and bootloader code to boot applications at power on such as IIC and Flash technologies
10. Demonstrate an understanding of interfacing a wide variety of common peripheral devices to a microcomputer system, including “hostile” high voltage devices.

# Course Activities and Assessment

**Assignment component:**

**Practical Hands-on Labs and Assignments : 50%**

**Exam Component:**

**Quizzes: 15%**

**Final Project: 35%**

* **Lab and assignment submission dates are published on the Canvas Calendar. Please be aware of these as they are hard deadlines.**

# Required Materials

**Altera DE1SoC Board**



**Zoom.**

**Other software outlined on Canvas**

# Course Policies

* Labs that are late will be subject to a 20% penalty per hour.
* Students are expected to attend lectures and labs
* There will be one mid-term and one final end of term exam. Both will be closed book exams (any relevant material required will be distributed with the exam), and will cover material from lectures and homework/labs/assignments.
* Students must obtain at least 50% overall in each of the Assignment component and the Exam component in order to pass the course
* Please note the following policies on grading and missed in-class assessments, in accordance with the [Academic Calendar language on Grading Practices](http://calendar.ubc.ca/vancouver/index.cfm?tree=3,42,96,0)
* Please use this link for online reporting of in term concessions<https://academicservices.engineering.ubc.ca/form-request-for-academic-concession-in-term-work/>

Use of Integrity Statements

* You may be asked to agree to an academic integrity statement as part of testing or other assessment activities.  As a student in a professional program, doing your part to adhere to course rules and upholding the academic integrity of your educational experience is in your best interest.  Every effort will be made to ensure that assessment is fair for all students in the course.  You can do your part by following the rules set out by your course instructors, and seeking assistance or clarification if you have any questions.

# University Policies

UBC provides resources to support student learning and to maintain healthy lifestyles but recognizes that sometimes crises arise and so there are additional resources to access including those for survivors of sexual violence. UBC values respect for the person and ideas of all members of the academic community. Harassment and discrimination are not tolerated nor is suppression of academic freedom. UBC provides appropriate accommodation for students with disabilities and for religious, spiritual and cultural observances. UBC values academic honesty and students ae expected to acknowledge the ideas generated by others and to uphold the highest academic standards in all of their actions. Details of the policies and how to access support are available [here](http://senate.ubc.ca/policies-resources-support-student-success).