

Altium I

(Circuit Design + Layout)

ELEC391
Summer T1 2018

Contents

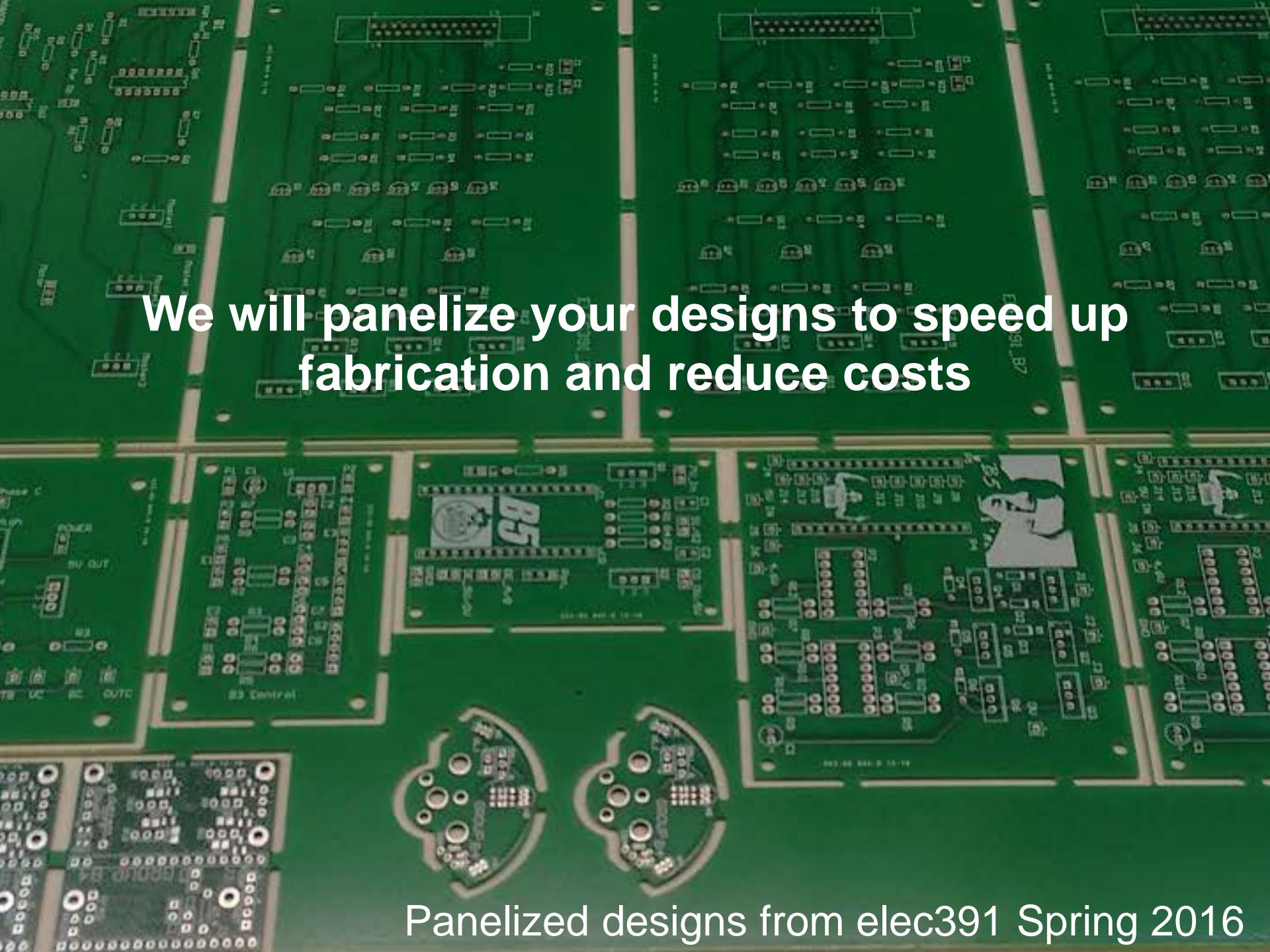
- PCB Design support for ELEC391
- PCB design flow
- How to install Altium Designer 2016
- Understanding Altium Designer
- Walk-through example
- PCB design best practices
- Anatomy of a PCB

Credits: Unless explicitly stated all source material is from the Altium website and Altium training documents.

PCB Design support for ELEC391:

Altium 2016, 150 licenses

- Jun 4 Altium I (Circuit Design + Layout)
- PCB Submissions Jun 10



We will panelize your designs to speed up
fabrication and reduce costs

Panelized designs from elec391 Spring 2016

Submission Instructions

- FR4 62mils, 7mils/7mils, 2-layers, top overlay only.
- Designs must pass DRC
- You can send several different boards per submission.
- You can request several copies of each but that increases your area.
- Email pcb@ece.ubc.ca
Subject: [PCB] ELEC391, Group #, submission#
- Attach: *PcbDoc files only
Body:
Total number of designs (not copies) to fabricate
Name of designs to fabricate and number of copies for each

Rules and Checks

The screenshot illustrates the Altium Designer interface for managing design rules and constraints. A red circle labeled '1' highlights the 'Design' menu, which is currently selected. Below it, a red box encloses the 'Rules...' button and the 'Rule Wizard...' button. Another red box encloses the 'Board Shape' button. A red arrow points from the 'Board Shape' button towards the 'Design Rule Check...' button in the bottom right corner.

Design Rule Check...

Reset Error Markers

Browse Violations Shift+V

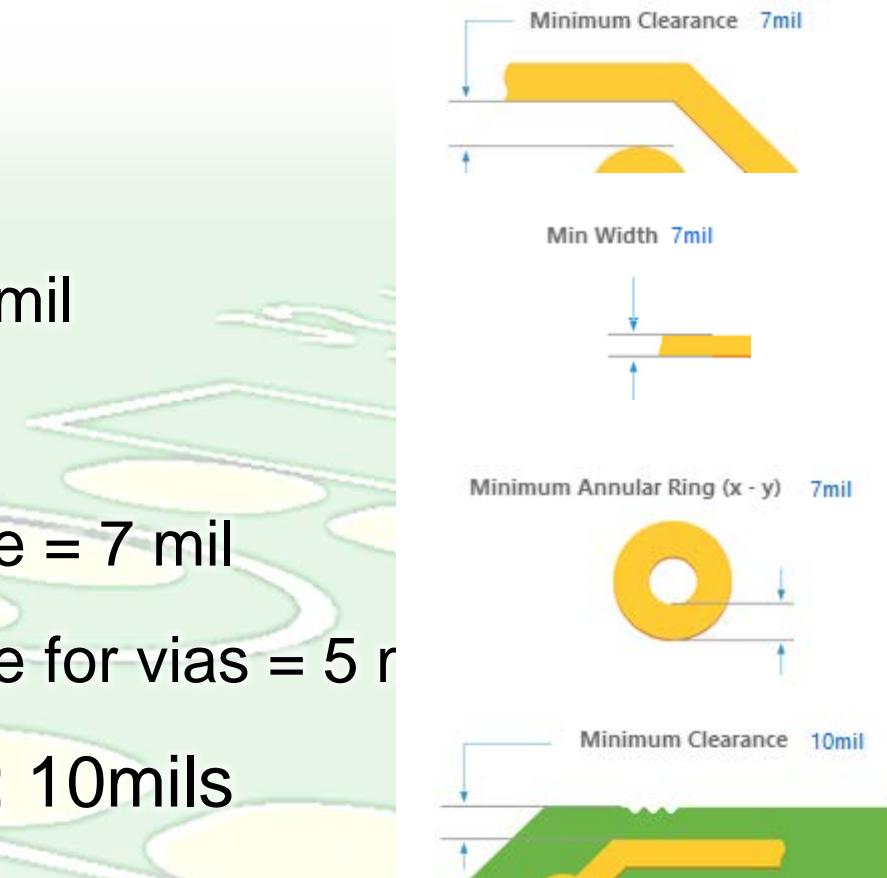
Browse Objects Shift+X

Design Rules

Name	Priority	Enabled	Type	Category	Scope	Attributes
All_components_test	1	<input checked="" type="checkbox"/>	Room Definition	Placement	InComponentClass/P Region [RQ = {5480mil, 2310mil, 31515mil, 21540mil} Style Under Comp - All Sides - Top, Bottom - Pref Size = 60mil]	
AssemblyTestpoint	1	<input checked="" type="checkbox"/>	Assembly Testpoint Style	Testpoint	All	
AssemblyTestpointUsage	1	<input checked="" type="checkbox"/>	Assembly Testpoint Usage	Testpoint	All	Under Comp - All Sides - Top, Bottom - Pref Size = 60mil
ComponentClearance	1	<input checked="" type="checkbox"/>	Component Clearance	Placement	All - All	Clearance = 10mil
ComponentRouting	1	<input checked="" type="checkbox"/>	Component Routing	Routing	All	Horizontal Clearance = 10mil Vertical Clearance = 10mil Pref Gap = 10mil Min Gap = 10mil Max Gap = 10mil Ref
FabricationTestpoint	1	<input checked="" type="checkbox"/>	Fabrication Testpoint Style	Testpoint	All	Under Comp - All Sides - Top, Bottom - Pref Size = 60mil
FabricationTestpointUsage	1	<input checked="" type="checkbox"/>	Fabrication Testpoint Usage	Testpoint	All	Testpoint - One Required - Multiple - Not Allowed
Fanout_RGA	1	<input checked="" type="checkbox"/>	Fanout Control	Routing	3DGA	Style - Auto - Direction - Alternating In and Out Via Grid = 1
Fanout_Default	5	<input checked="" type="checkbox"/>	Fanout Control	Routing	All	Style - Auto - Direction - Alternating In and Out Via Grid = 1
Fanout_LCC	2	<input checked="" type="checkbox"/>	Fanout Control	Routing	3DCC	Style - Auto - Direction - Alternating In and Out Via Grid = 1
Fanout_Small	4	<input checked="" type="checkbox"/>	Fanout Control	Routing	[CompPinCount > 5] 3DQC	Style - Auto - Direction - Out Then In Via Grid = 1
Fanout_SOIC	3	<input checked="" type="checkbox"/>	Fanout Control	Routing	3DQC	Style - Auto - Direction - Alternating In and Out Via Grid = 1
HoleSize_1	1	<input checked="" type="checkbox"/>	Hole Size	Placement	All	Min = 4mil Max = 4mil
HoleSize_2	2	<input checked="" type="checkbox"/>	Hole Size	Placement	All	Min = 20mil Max = 30mil
HoleToHoleClearance	1	<input checked="" type="checkbox"/>	Hole To Hole Clearance	Manufacturing	All - All	Hole To Hole Clearance = 10mil
LayerPins	1	<input checked="" type="checkbox"/>	Layer Pins	Manufacturing	All	Layer Pins - Enforce
MinimumAnnularRing	1	<input checked="" type="checkbox"/>	Minimum Annular Ring	Manufacturing	All	Min = 2mil
MinimumSolderMaskSilver	1	<input checked="" type="checkbox"/>	Minimum Solder Mask Silver	Manufacturing	All - All	Minimum Solder Mask Silver = 10mil
NetAntennae	1	<input checked="" type="checkbox"/>	Net Antennae	Manufacturing	All	Net Antennae Tolerance = 0mil
PasteMarkExpansion	1	<input checked="" type="checkbox"/>	PasteMark Expansion	Mask	All	Expansions = 0mil
PlaneConnect	1	<input checked="" type="checkbox"/>	Plane Connect	Plane	All	Connect = 10mil
PolygonConnect	1	<input checked="" type="checkbox"/>	Polygon Connect Style	Plane	All	Style - Relief Connect - Expansion = 20mil Width = 10mil
RoutingCorners	1	<input checked="" type="checkbox"/>	Routing Corners	Routing	All - All	Style - Relief Connect - Width = 10mil Angle = 90° - Extra
RoutingLayers	1	<input checked="" type="checkbox"/>	Routing Layers	Routing	All	Style - 45 Degree - Min Setback = 10mil Max Setback = 10mil Layer - Enforce
RoutingPriority	1	<input checked="" type="checkbox"/>	Routing Priority	Routing	All	
RoutingTopology	1	<input checked="" type="checkbox"/>	Routing Topology	Routing	All	
RoutingVia	1	<input checked="" type="checkbox"/>	Routing Via	Routing	All	

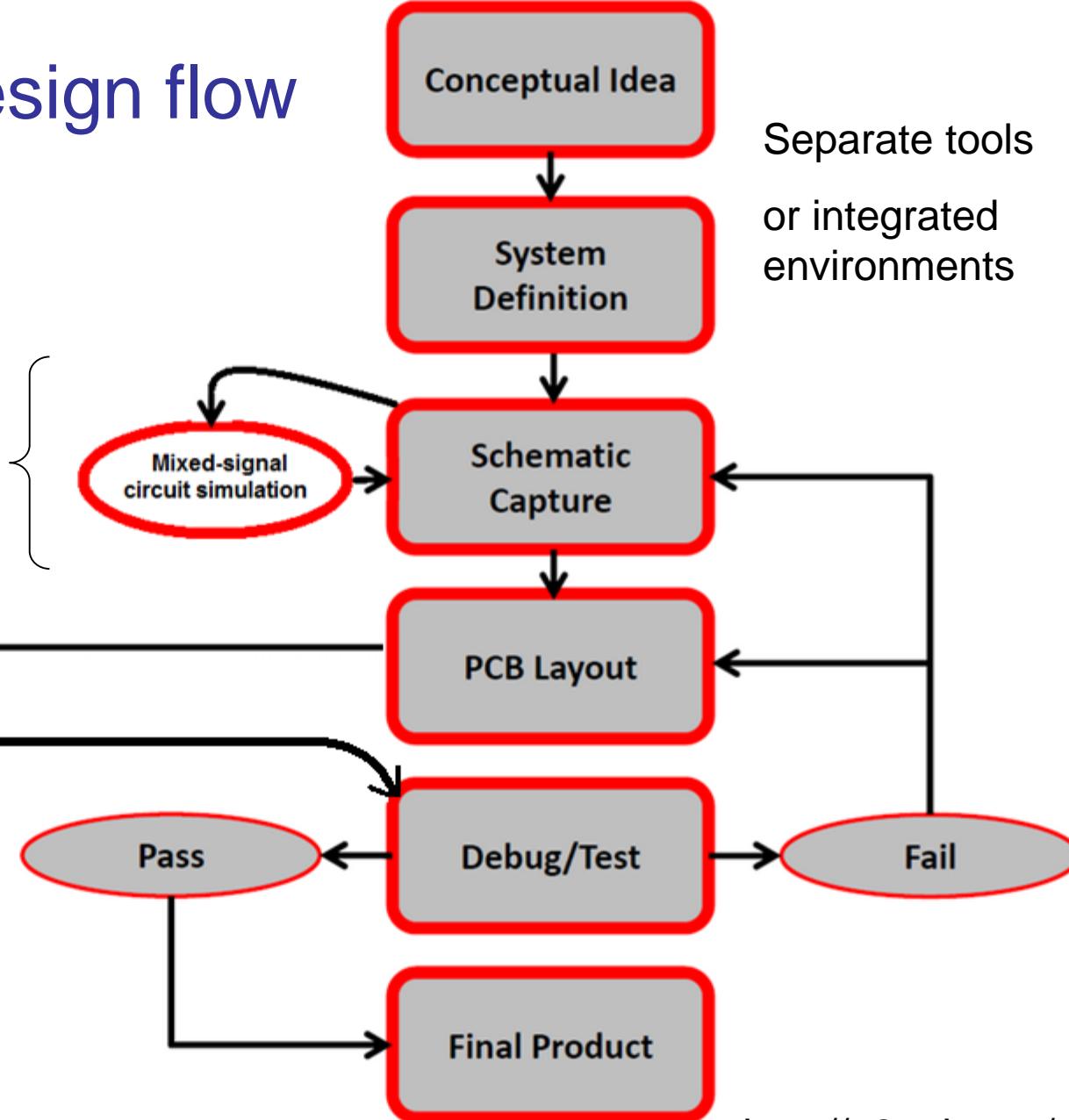
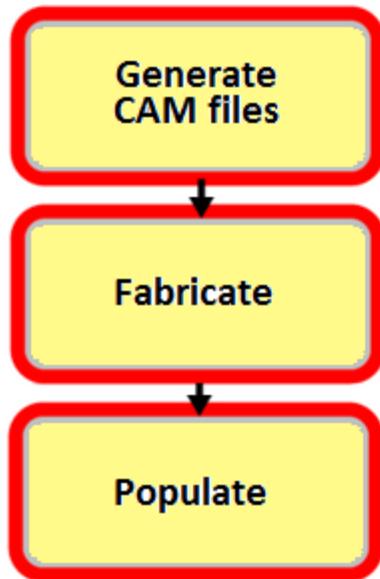
Rules – design rules

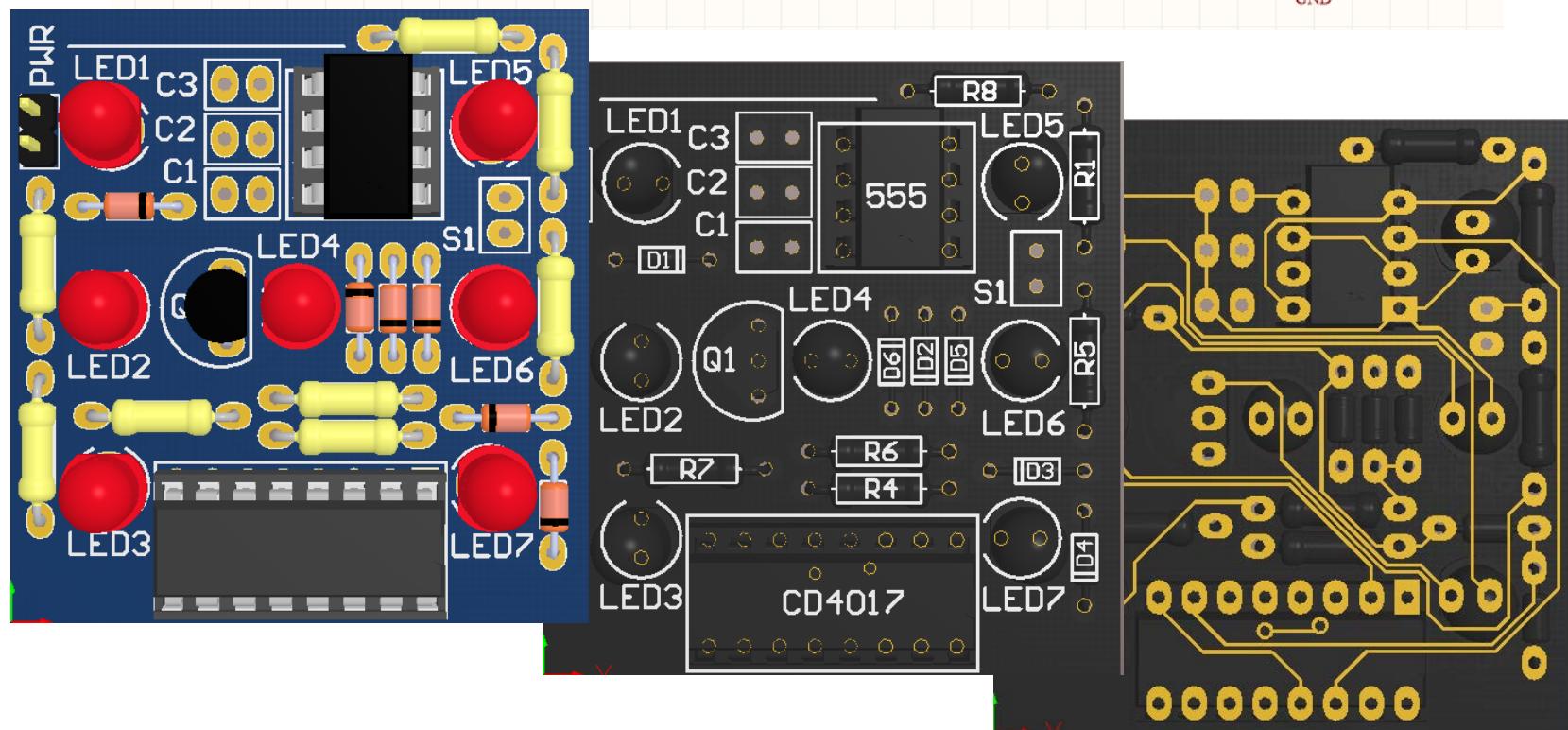
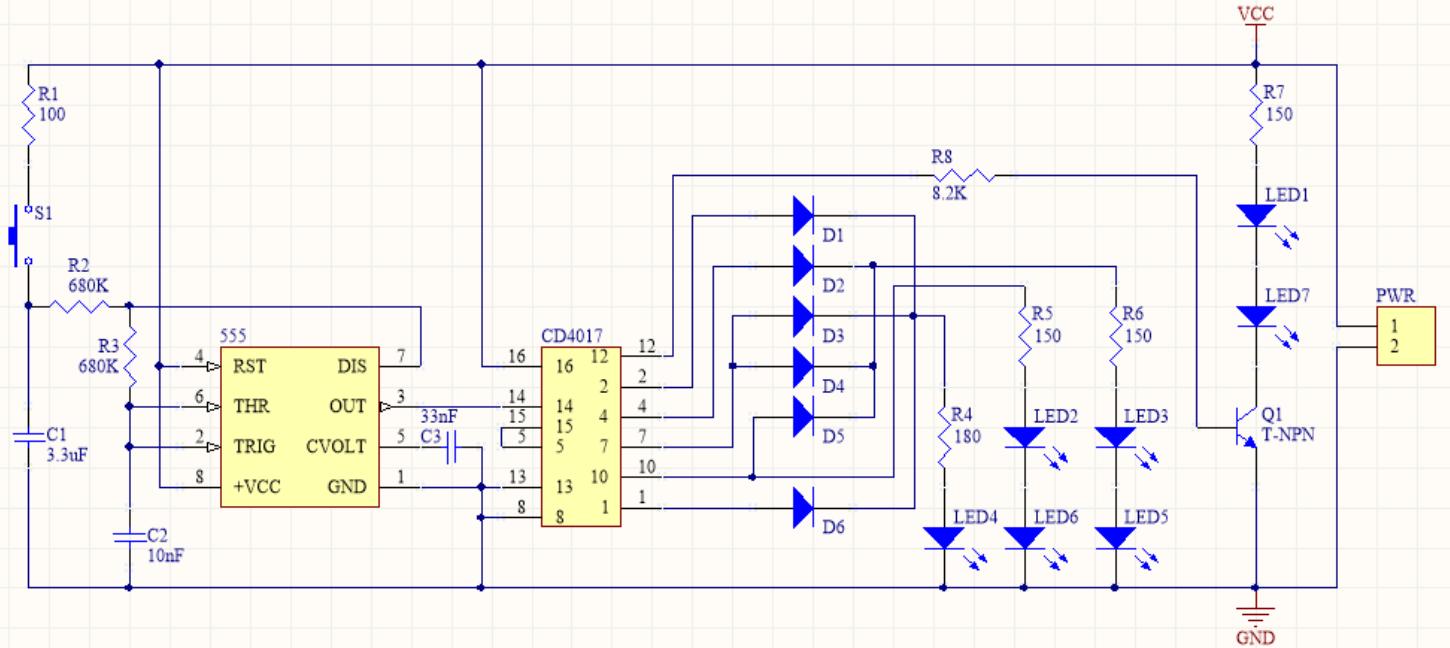
- Component clearance and (electrical) clearance:
 - Minimum distance = 7 mil
- (Routing) width:
 - Minimum trace width = 7 mil
- Annular ring size:
 - Minimum annular ring size = 7 mil
 - Minimum annular ring size for vias = 5 mil
- Board outline clearance: 10mils



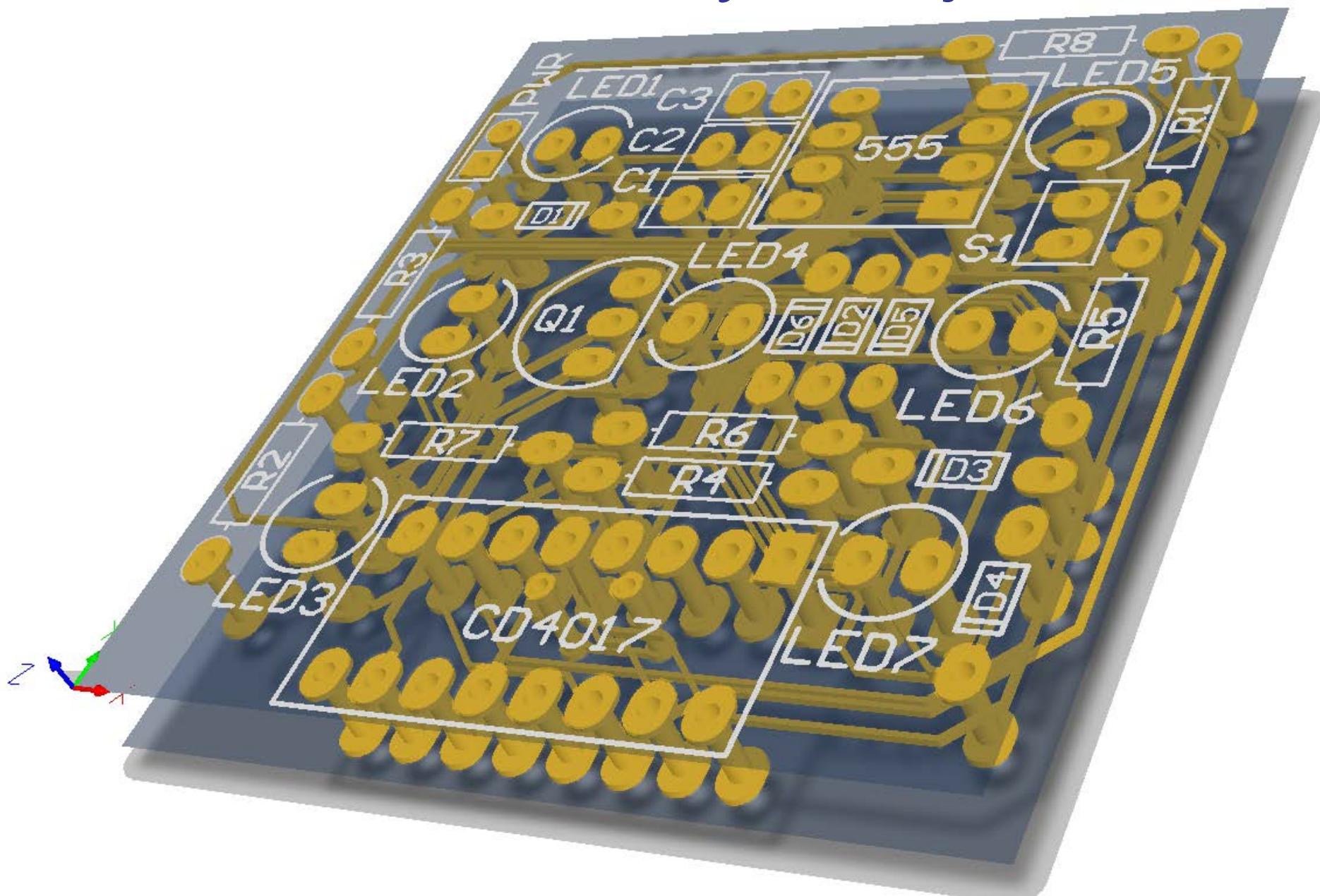
Typical PCB Design flow

Front-end design
and capture





PCBs are multi-layer objects



Altium Designer 2016

A complete product development system

System requirements (MS W7, W8, W10)



- Front-end design and capture
- Physical PCB design
- FPGA hardware design
- FPGA system implementation and debugging
- Embedded software development
- Mixed-signal circuit simulation
- Signal integrity analysis
- PCB manufacturing

How to install Altium 2016

- Link to our download site:
<https://download.ece.ubc.ca>
- Create an Altium Live account:
<http://live.altium.com/#signin> (slow)
email: engservices@ece.ubc.ca (fast)



Electronic Software Distribution

Search

 Enter search term

Admin

Groups

Software

Eligibility

History

Previous Downloads

Accepted Licenses

Help

Login

Eligibility

ISO Files

ALTIUM DESIGNER

Circuit Design Software

External Links

- [Altium](#)
- [Altium Designer](#)

[Summer 09 Release](#)[10](#)[2014](#)[16](#)

ALTIUM DESIGNER 16

File	Size	
README.html		README
AltiumDesigner16Setup.exe	10.4 MB	Windows installer (requires .NET Framework 4.5)
EULA.pdf	56.2 KB	End-User License Agreement
OfflineSetupAD16_1_9.zip	3 GB	Windows installer

1

3

2

USING THE ECE LICENSE SERVER

The ECE license server for Altium is accessible only from the UBC network. Before starting Altium, you should be connected by one of the following means:

- A wired connection on the ECE network
- A wired connection on UBC ResNet
- A wireless connection at the UBC Vancouver campus on the ubcprivate, ubcsecure, or ubc network (ubcvisitor and eduroam are not sufficient)
- A [myVPN](#) connection to the UBC Vancouver network
- A [myVPN](#) connection to the ece.prof pool

Start Altium, and from your "My Account" page, click on "Setup private license server". Enter:

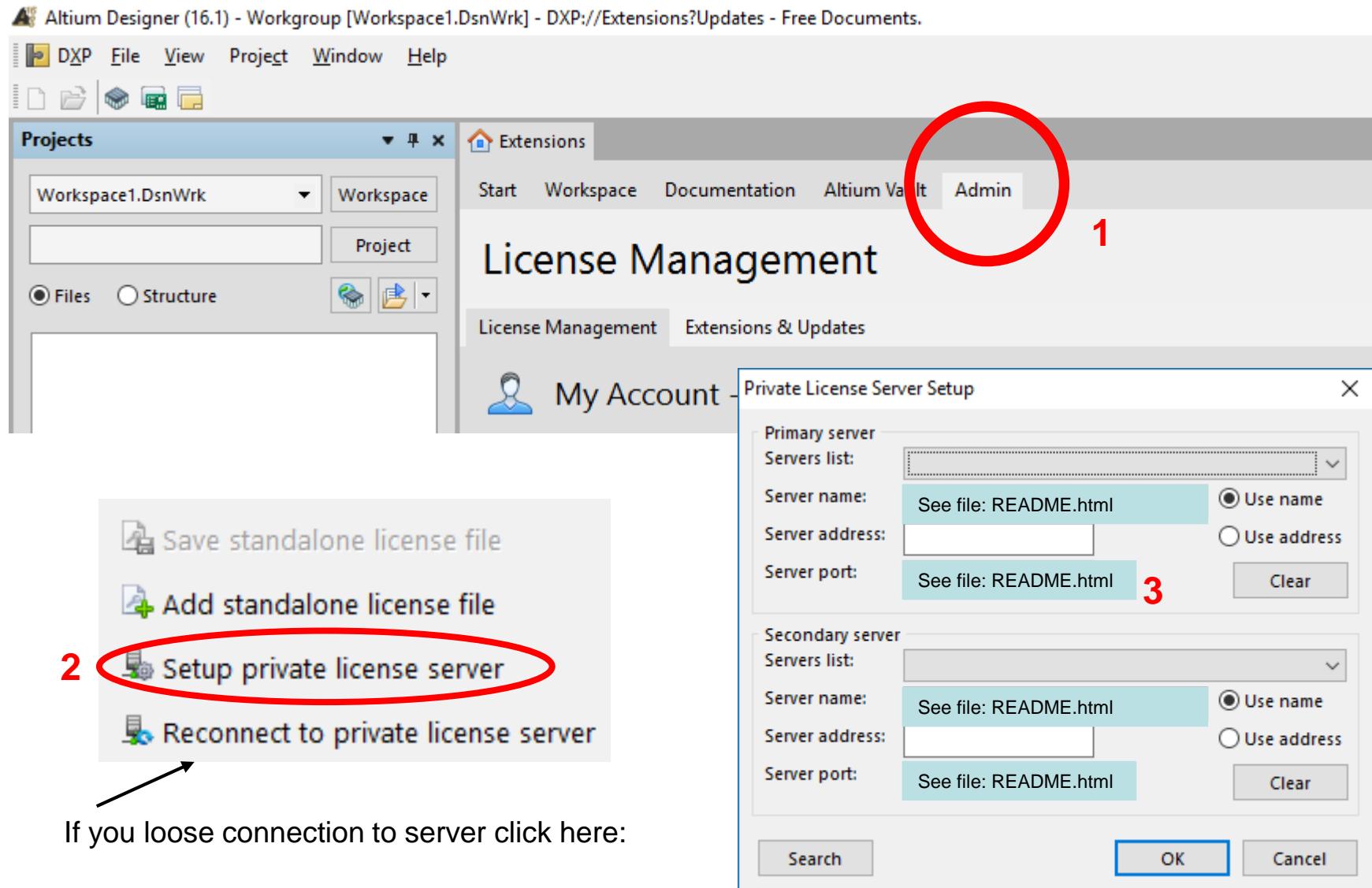
Server name:**Server port:****Secondary server name:****Server port:**

See file: README.html

Select the new license that appears and click on "Use". You may as well also delete any old, expired licenses that are also showing.

Install .zip file

To set license server



As per README.html file

Connecting to the Altium Vault

Stream

Start Workspace Documentation Altium Vault Admin

Vault

Stream Users Roles Vault

 You are not connected to any Vault Server.

To connect to a Vault, go to DXP Preferences - Data Management - Vaults settings.

To learn more about design data management, please visit <http://live.altium.com/#vaults>

Preferences

Cloud Preferences

Your settings can now be stored in the cloud. Once you are signed in simply enable your cloud preferences.

[Disable cloud preferences ➔](#)

 **System**

- System
- Data Management
 - Version Control
 - Design Repositories
 - Vaults**
 - Publishing Destinations
 - Backup
 - File Locking
 - Local History
 - Templates
 - Installed Libraries

 **Data Management – Vaults**

Vaults

A vault stores structured and revised data that is characterized by lifecycle states.

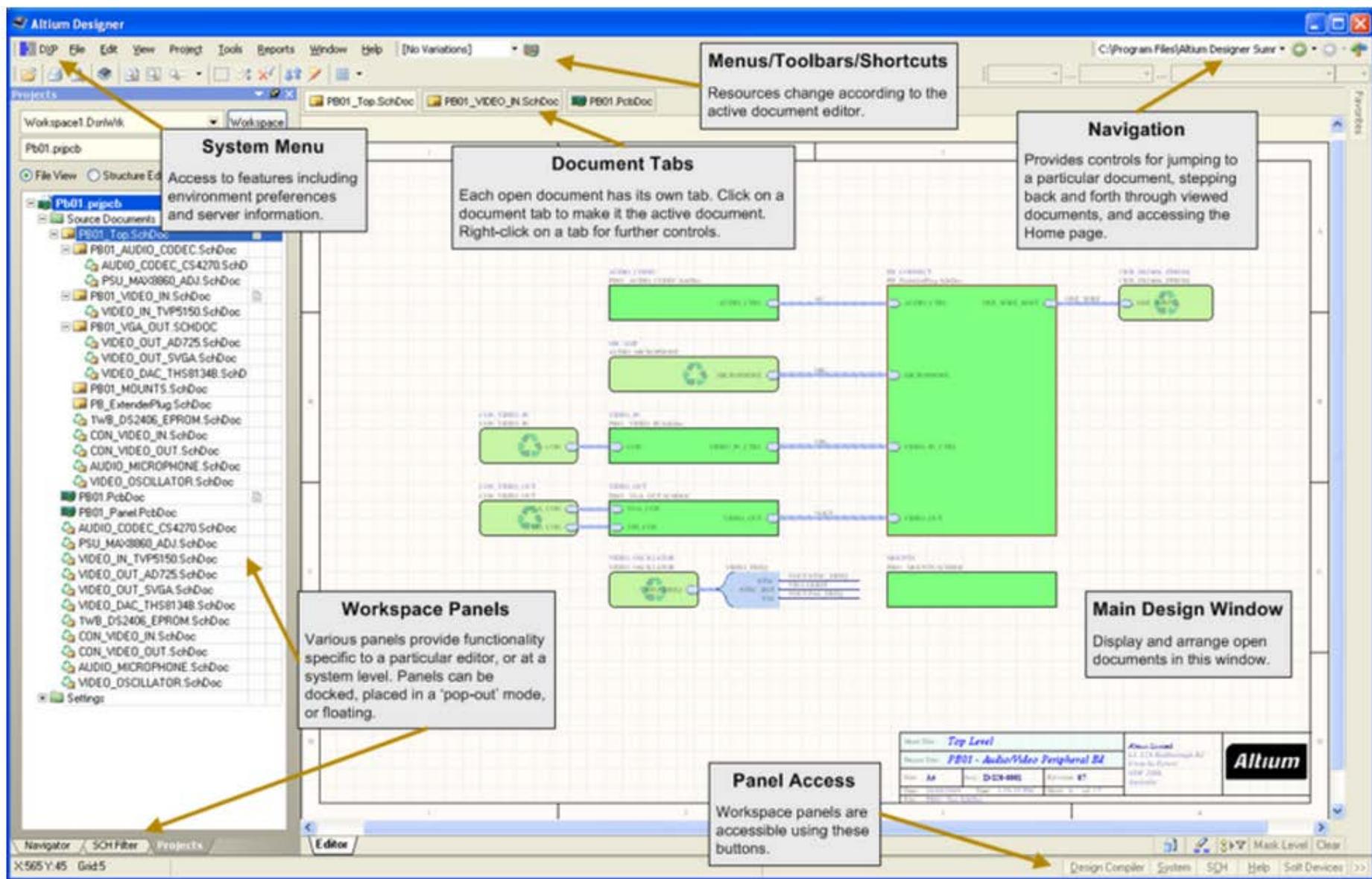
[More Information...](#)

Name	Description	Address	Status	Enab...
Altium Content Vault	Altium Content Vault	http://vault.live.altium.com	✓	<input checked="" type="checkbox"/>

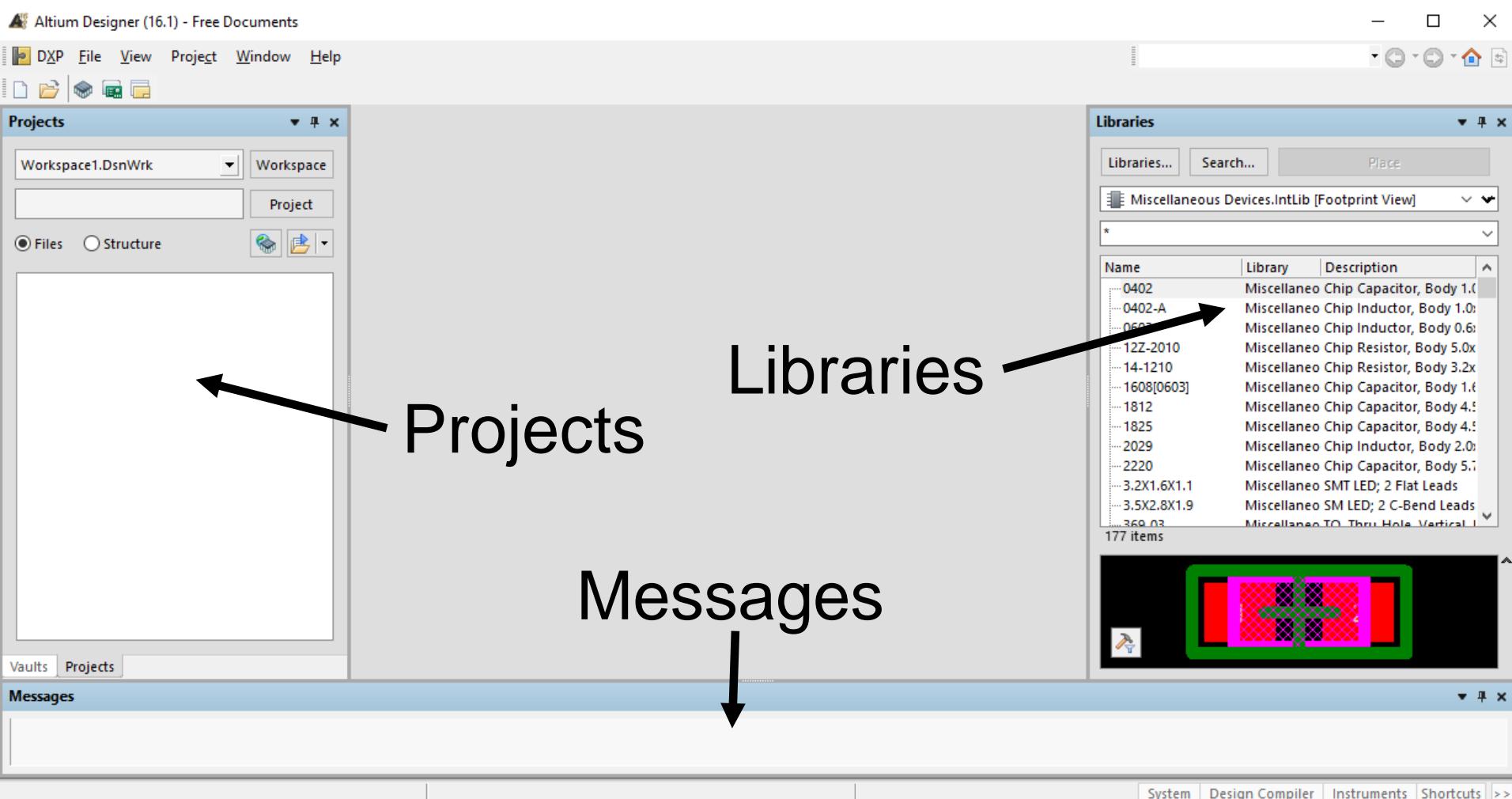
Understanding Altium

- DXP (Design explorer): Unified platform
- Collaborative environment (corporate tool):
 - Multiple users, some with dedicated tasks
 - Design team incremental changes day-by-day
 - Built-in version control (SVN subversion or CVS concurrent versions system)
 - Design repositories / Vaults (accessible by multiple users with different credentials)
- Cloud oriented support:
 - Save preferences online
 - <http://live.altium.com/> (forum, design content, blog)

Altium Design Environment



Recommended basic panels



For more help working with panels read [this](#)

Understanding Altium

(Basics for the single user)



Don't forget :

- Use Keyboard shortcuts
<Shift + F1> while running a command
- <Esc> or Right Click to exit a command
- Save documents to see some changes take effect

Altium Projects

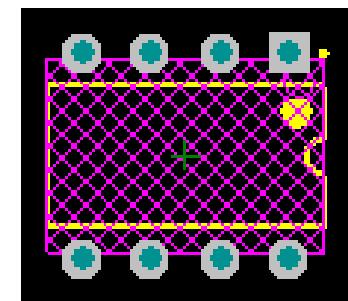
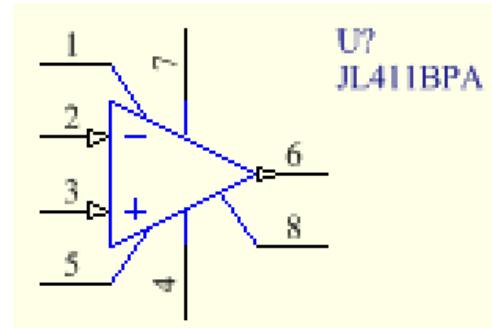
- Project: collection of design documents
 - 1 Project = 1 implementation
 - It stores links to all source documents
 - relative reference: same drive
 - absolute reference: different drive
 - It creates links to all output documents
 - Saves project options
- Create a PCB_Project, Save as: new name
(does not move the file creates a copy)
- The active project is highlighted
- Add/Remove documents to/from a project

Project types

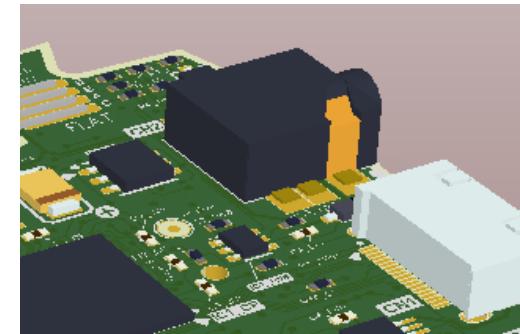
- PCB Project (*.PrjPcb)
 - Schematic, libraries, PCB layout
- FPGA Project (*.PrjFpg)
- Embedded Project (*.PrjEmb)
- Core Project (*.PrjCor)
- Integrated Library (*.LibPkg) & (*.IntLib)
- Script Project (*.PrjScr)

Component, Model and Library Concepts

- Component representations:
 - Schematic symbol
 - PCB footprint
 - SPICE model definitions
 - Signal integrity description
 - 3D graphical description



```
***** INPUT STAGE *****  
*  
IOS 2 1 25.0P  
* ^Input offset current  
CI1 1 0 3P  
CI2 2 0 3P  
R1 1 3 1E12  
R2 3 2 1E12  
I1 99 4 1.0M  
J1 5 2 4 JX  
J2 6 7 4 JX  
R3 5 50 650  
R4 6 50 650  
*Fp2=28 MHZ  
C1 5 6 1 272P
```



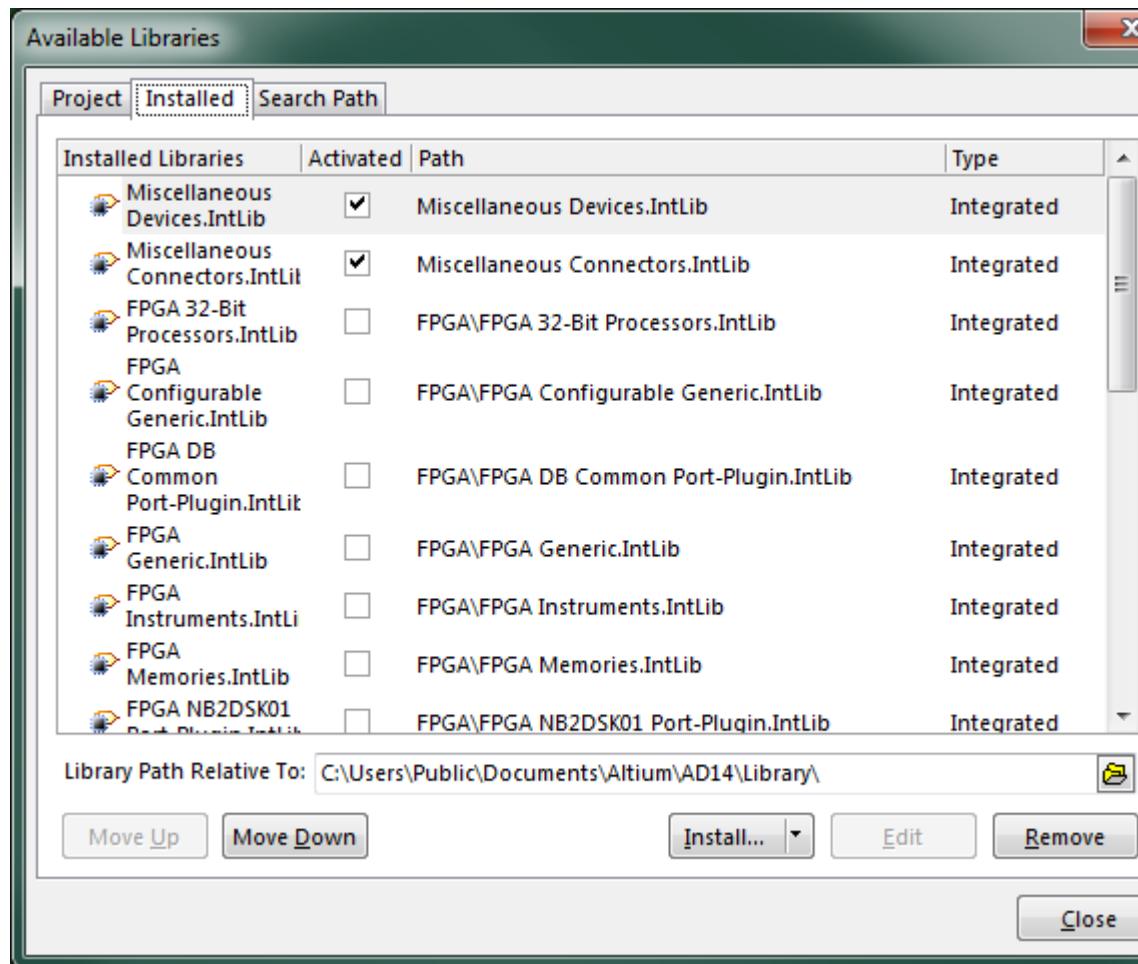
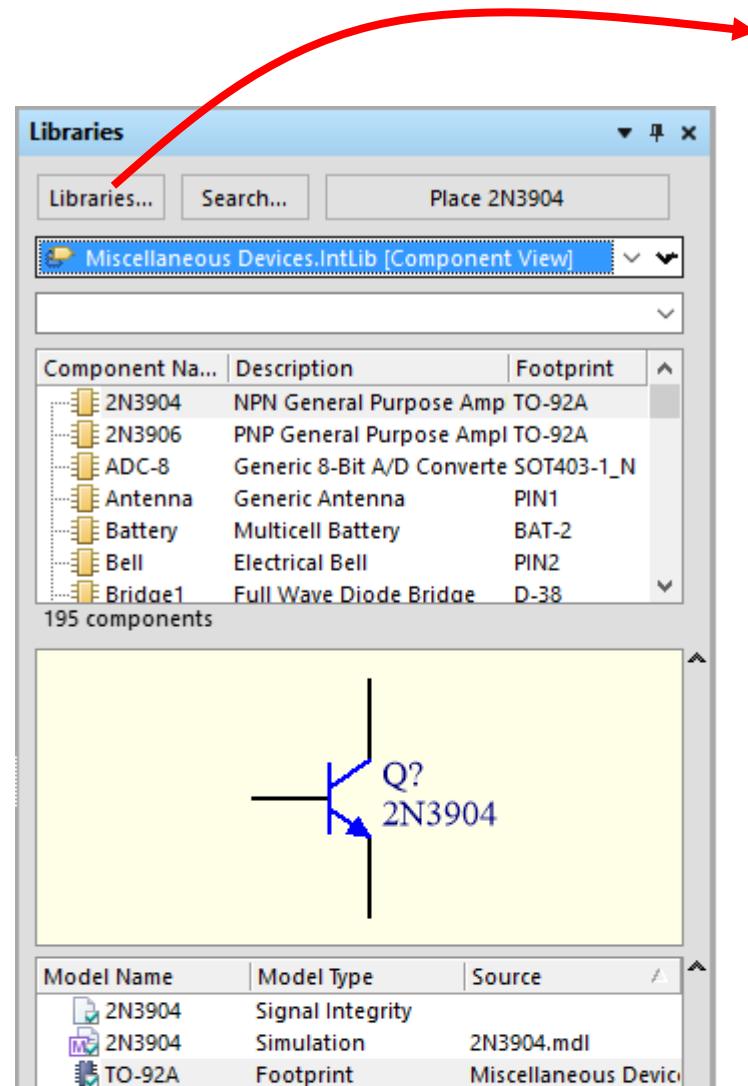
Libraries = collections of components

- Collection of components, models or both
- Model Libraries (*.MDL, *.CKT, *.PCBLib)
 - Simulation models are one file per model
- Schematic Libraries (*SchLib)
 - Symbol and a link to a model library
- Integrated Libraries (*.IntLib)
 - Unified components: Symbol, footprint and other domain models + parametric information are compiled into a single portable file

To setup libraries in Altium

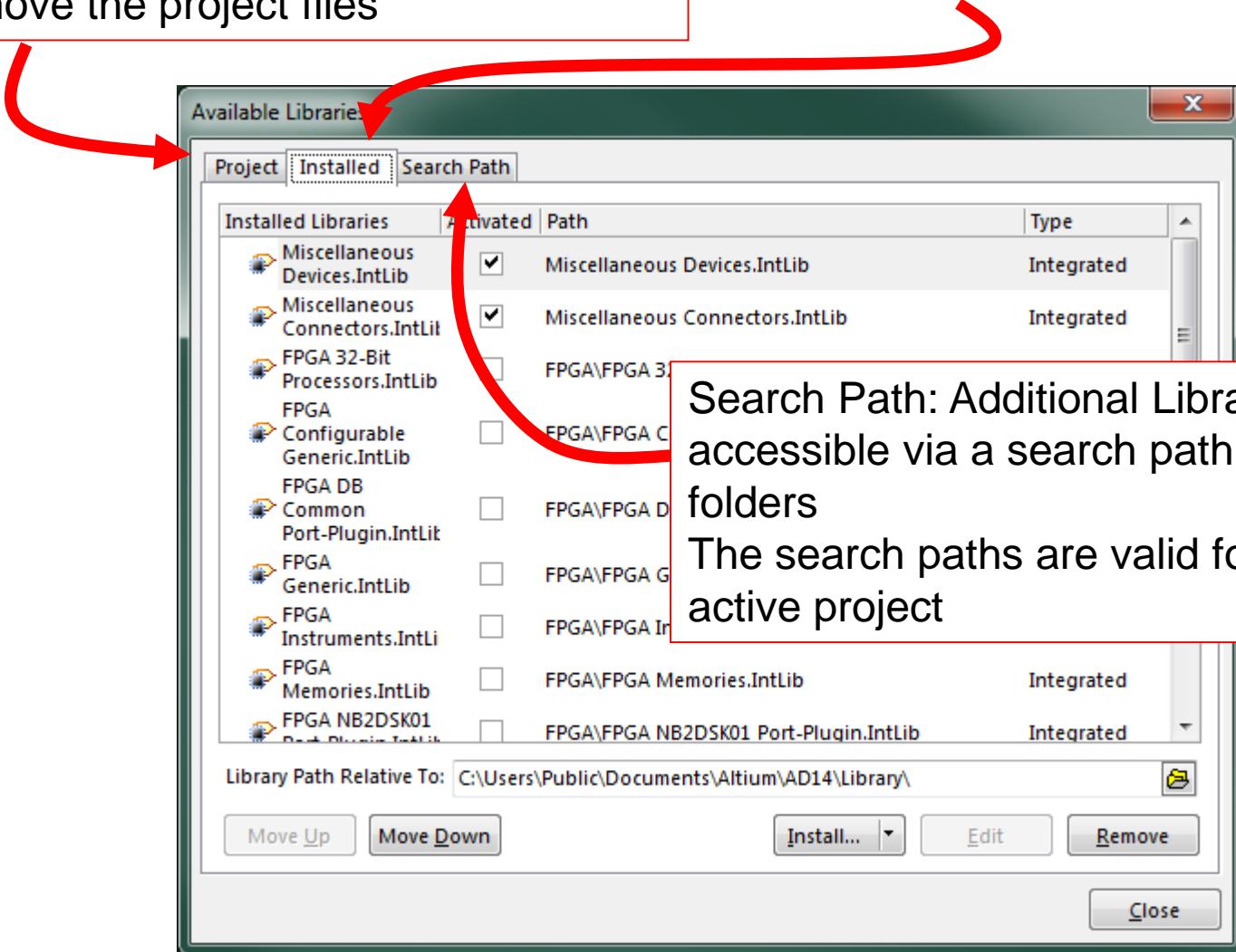
Libraries panel

Available Libraries Dialog



Project: part of and available only to the active project and its documents
You have to keep track of where these are if you move the project files

Installed: All installed libraries.
Components are available to all open projects and list is persistent across design sessions



Search Path: Additional Libraries accessible via a search path and sub-folders
The search paths are valid for the active project

Libraries

Current library

Select a different library

Place 2N3904

Miscellaneous Devices.IntLib [Component View]

Libraries... Search... Place 2N3904

Component Name Description Footprint

- 2N3904 NPN General Purpose Amp TO-92A
- 2N3906 PNP General Purpose Ampl TO-92A
- ADC-8 Generic 8-Bit A/D Converte SOT403-1_N
- Antenna Generic Antenna PIN1
- Battery Multicell Battery BAT-2
- Bell Electrical Bell PIN2
- Bridge1 Full Wave Diode Bridge D-38

195 components

Schematic symbol for selected component

Model Name Model Type Source

- 2N3904 Signal Integrity 2N3904.mdl
- 2N3904 Simulation 2N3904.mdl
- TO-92A Footprint Miscellaneous Device

Graphical display of the selected model

Supplier Manufacturer Description Unit Price

Icons used to show/hide panel sections

Libraries Panel:

All libraries available to the active project

Project + Installed + Search Path

When placing component:

<spacebar> to rotate

<x> or <y> to flip

<Tab> open properties dialog

<L> for PCB footprints
to flip component side

To search across libraries:

Search ...

Obtaining integrated libraries

1. Frozen (legacy) libraries: [from here](#)

you can install anywhere but it is a good idea to make a subfolder under:

C:\Users\Public\Public Documents\Altium\AD16\Library
or a cloud storage service if you work from more than one PC

2. AltiumLive website: [Resources / Design Content](#)



Manufacturer: National Semiconductor

Updated: 3+ months ago

Tags: Analog, Amplifier

National Semiconductor Amplifiers. This collection offers amplifiers from single to quad, up to 1.7GHz with low-distortion, low-power and low-voltage options.

GO TO VAULT

DOWNLOAD LIBRARY

This is useful to preview component

This downloads a .zip file for the complete library

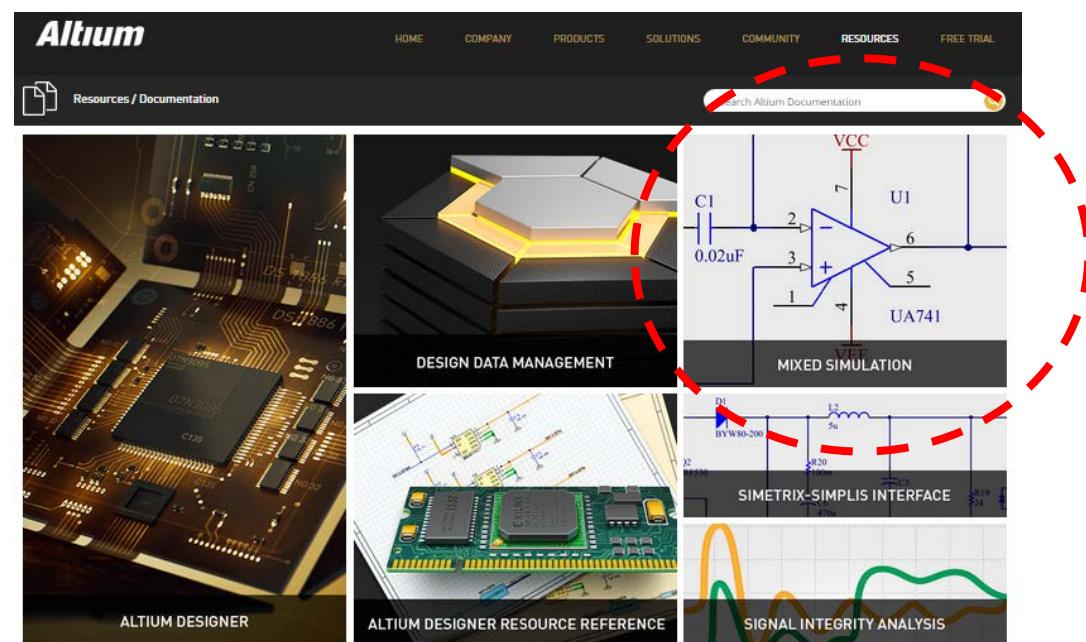
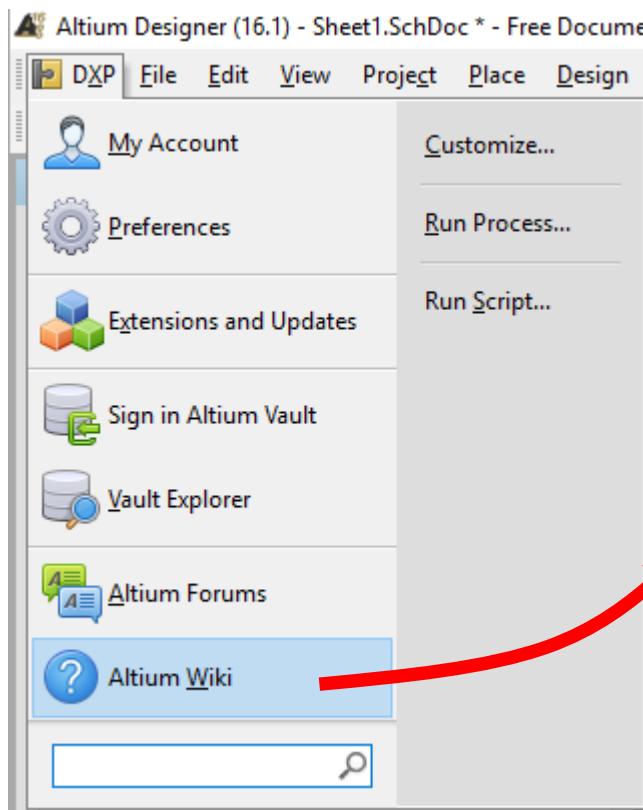
Altium Vault

Altium's cloud library (repository of models)
Also includes real-time supply chain information

The screenshot shows the Altium Designer interface. On the left, a vertical toolbar lists various options: My Account, Preferences, Extensions and Updates, Sign in Altium Vault, **Vault Explorer**, Altium Forums, and Altium Wiki. A large red arrow points from the text above to the 'Vault Explorer' button. On the right, a search results window is open. At the top, a search bar contains the text 'CD4017'. Below the search bar, the results are displayed under the heading 'Search Result [No description]'. The results table has columns for Item, S., Description, C, N, and C. The first result, 'CMP-1619-00769-2', is highlighted with a blue selection bar. At the bottom of the search results window, there is a summary for the selected item: 'CMP-1619-00769-2 [CD40174BE] Released Summary ▾' and 'CMOS Hex D-Type Flip-Flop, N0016A, TUBE'.

Item	S.	Description	C	N	C
CMP-1619-00769-2	R...	CMOS Hex D-Type Flip...	C...	U...	
CMP-1623-00343-2	R...	CMOS Decade Counter...	C...	U...	
CMP-1623-00071-2	R...	CMOS Decade Counter...	C...	U...	
CMP-1623-00072-2	R...	CMOS Decade Counter...	C...	U...	
CMP-1619-00102-2	R...	CMOS Hex D-Type Flip...	C...	U...	
CMP-1616-00133-3	R...	CMOS Quad D-Type Fli...	C...	U...	
CMP-1623-00678-2	R...	CMOS Decade Counter...	C...	U...	

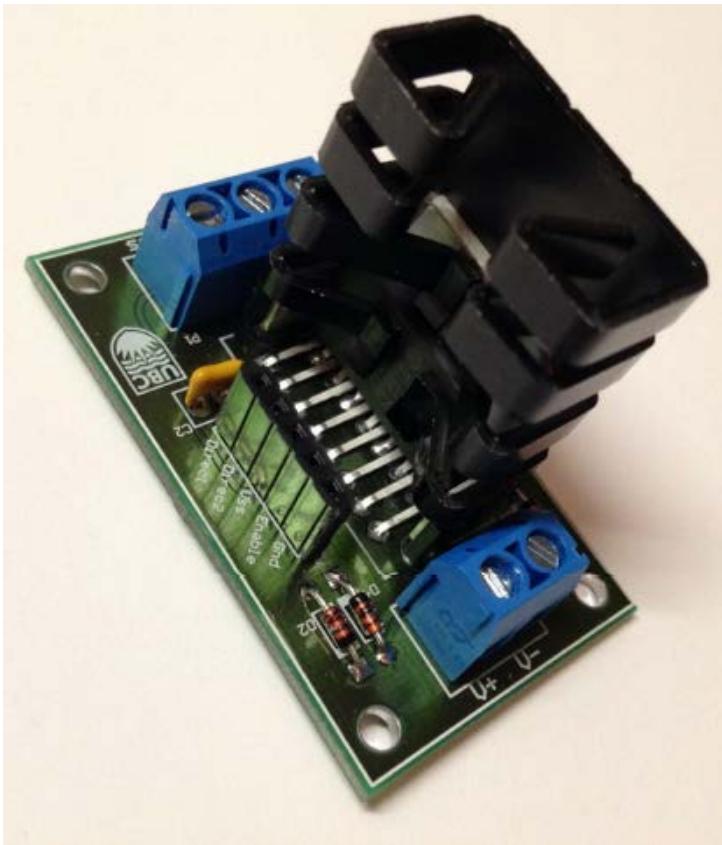
Learning to use Altium



Best training material is on the Altium website
It is updated, but beware that menus and options
slightly change between versions

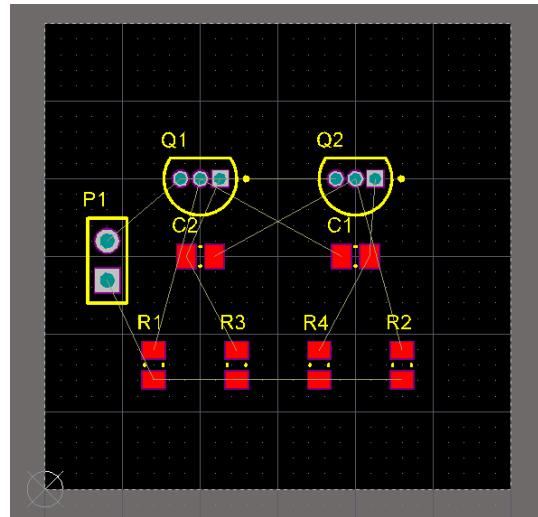
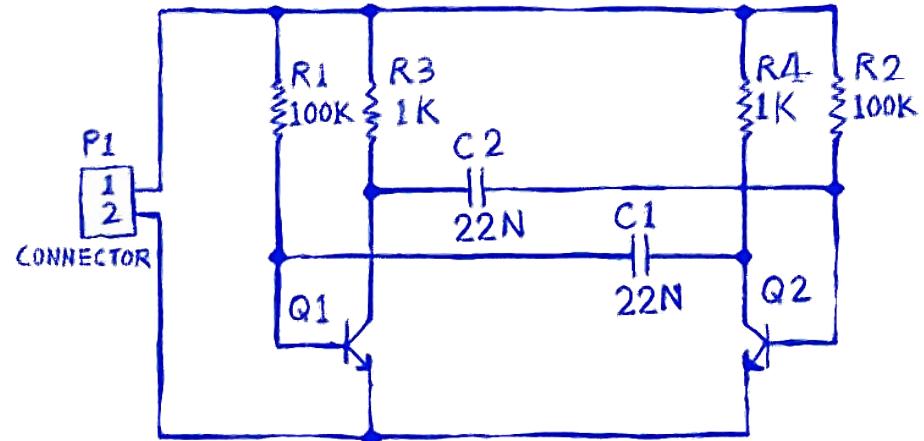
Walk-through example

L298 Motor Driver Board
(by Matt Winship)



[L298_Motor_Driver_Board_Datasheet.pdf](#)

[Altium introductory tutorial](#)

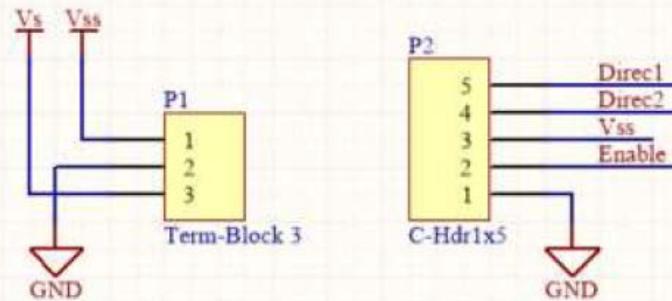


LM298 Motor Driver Board Schematic

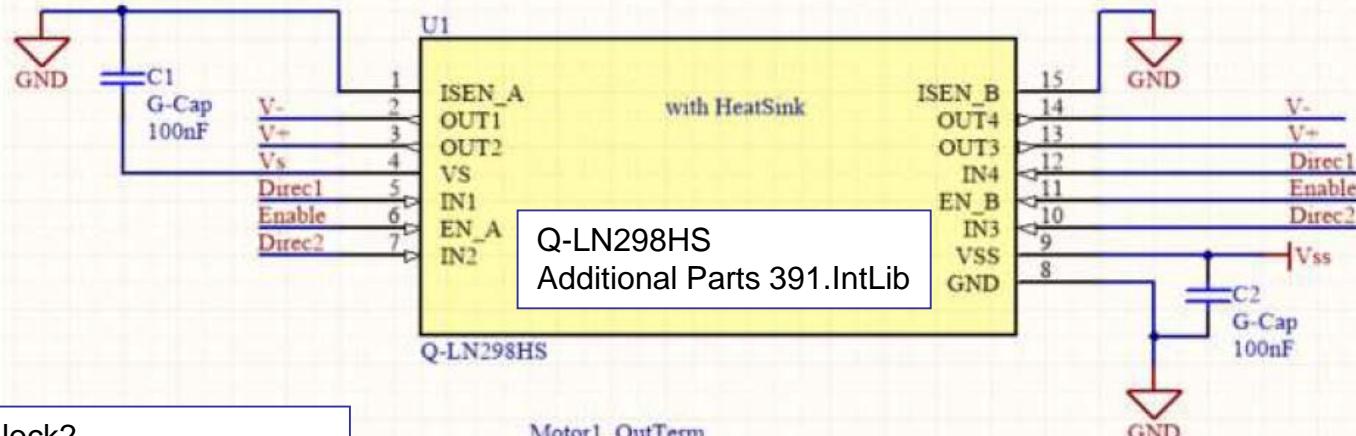
1. Load libraries
2. Draw the schematic
Set electrical type for connector pins
3. Compile Project:
Project → Project Options
4. Place ‘no ERC’ labels if necessary
Modify connection matrix with caution

LM298 Motor Driver Board Schematic

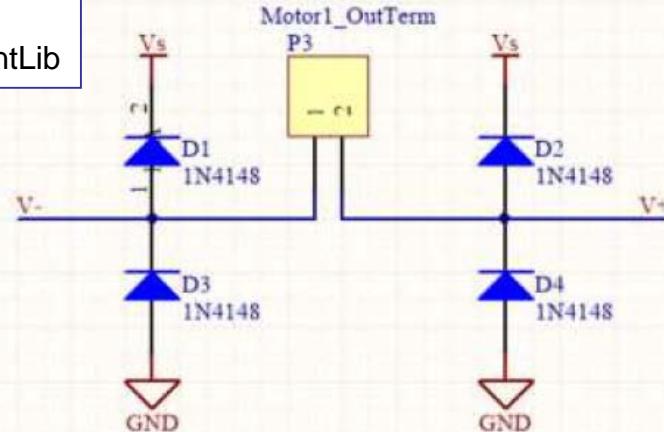
C-Block3
PartsDatabaseV16.1.IntLib



C-Hdr1x5
PartsDatabaseV16.1.IntLib



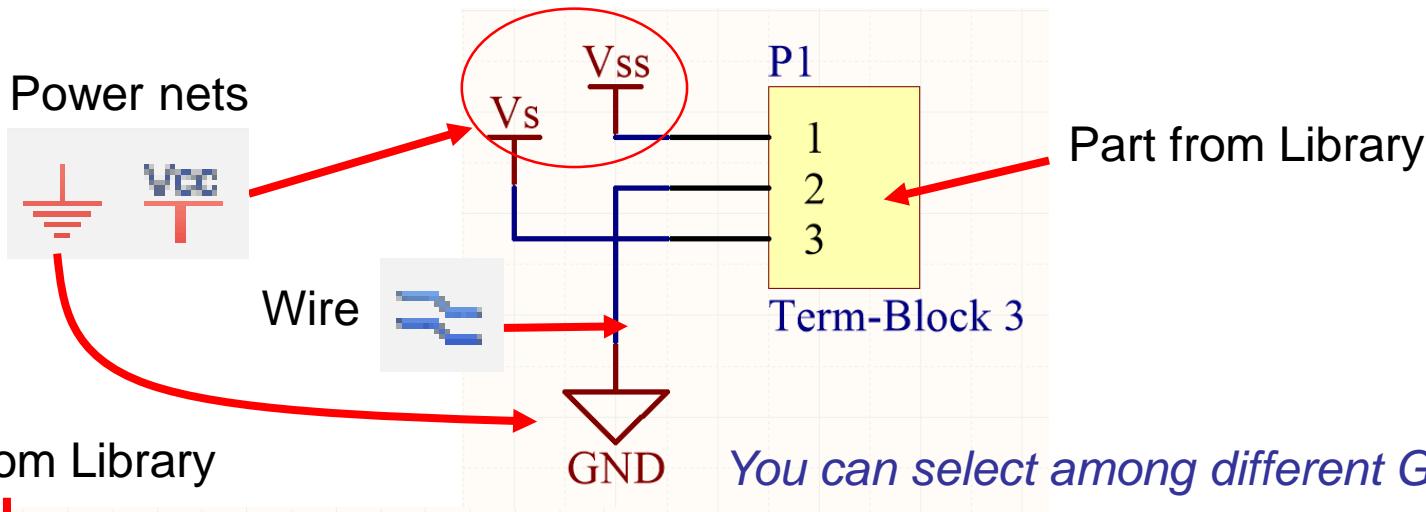
C-Block2
PartsDatabaseV16.1.IntLib



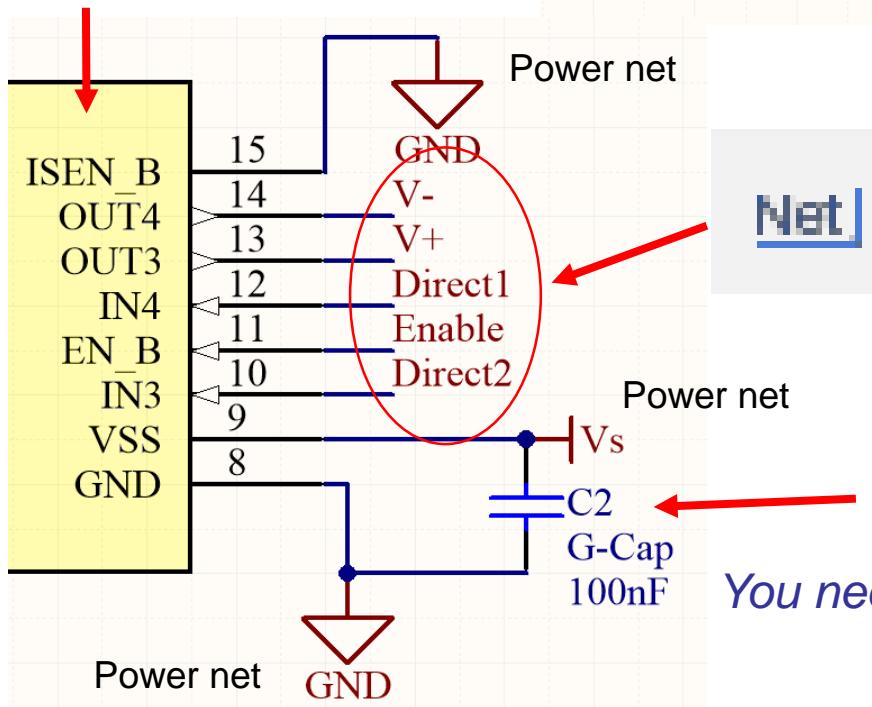
T-DiodeRect
PartsDatabaseV16.1.IntLib

G-Cap
PartsDatabaseV16.1.IntLib

Drawing the schematic



You can select among different GND symbols

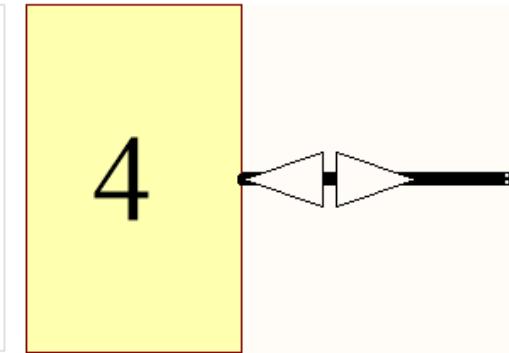
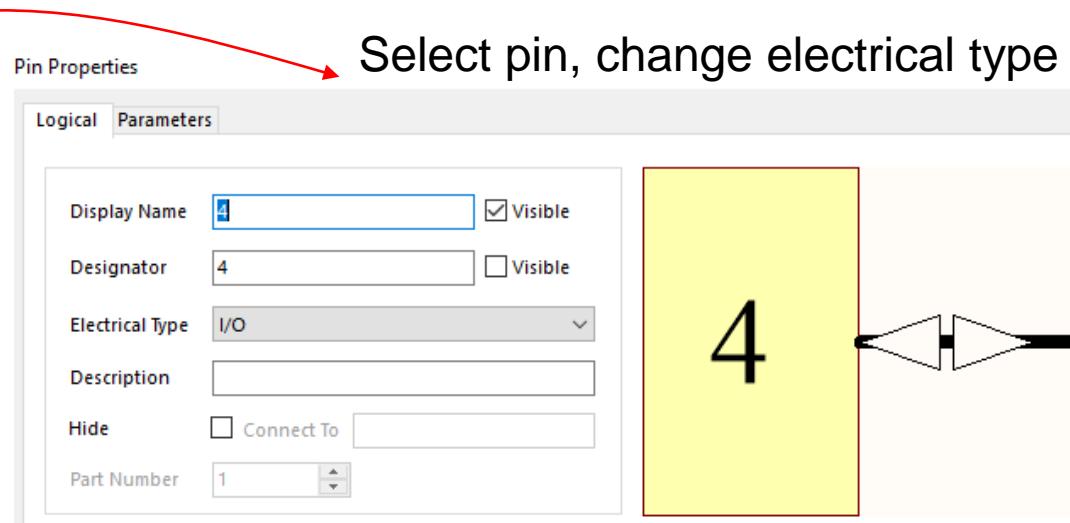
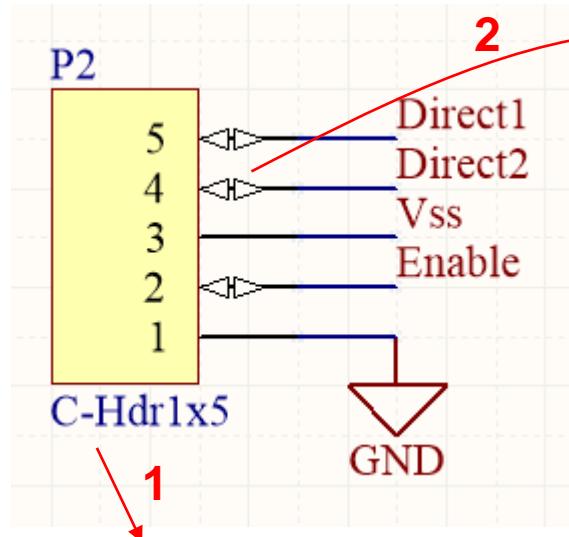


You need to input the capacitance value

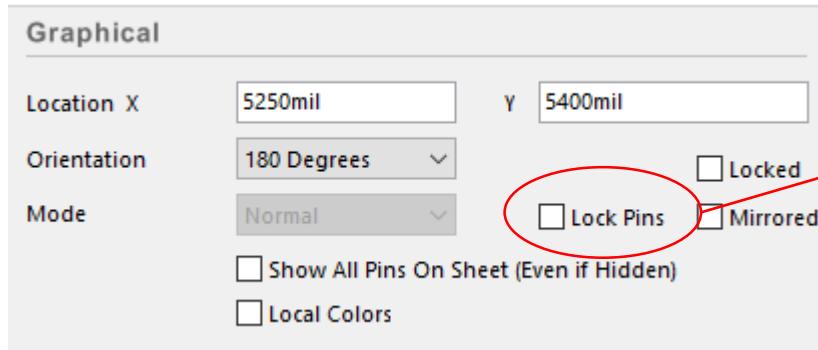
Set the electrical type of pins

On the Q-LN298HS Symbol, pins Direct1, Direct2, and Enable are inputs

You need to set the pins of connector P2 to Output, or I/O, to provide a compatible electrical type net



Properties

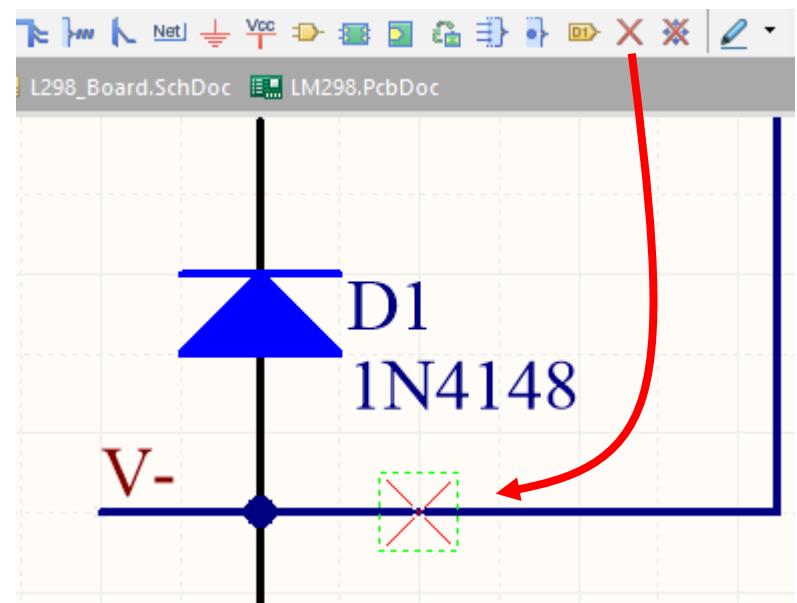


Compile Project

- Project >> Compile Project

Messages			
Class	Document	Source	Message
[Error]	LM298.SchDoc	Compiler	Net V- contains multiple Output Pins (Pin U1-2,Pin U1-14)
[Error]	LM298.SchDoc	Compiler	Net V+ contains multiple Output Pins (Pin U1-3,Pin U1-13)

- This error is caused by having 2 pins of the LM298 connected to V- and 2 pins connected to V+
- In this case this was done intentionally
- To ignore this error place a No ERC label on the net



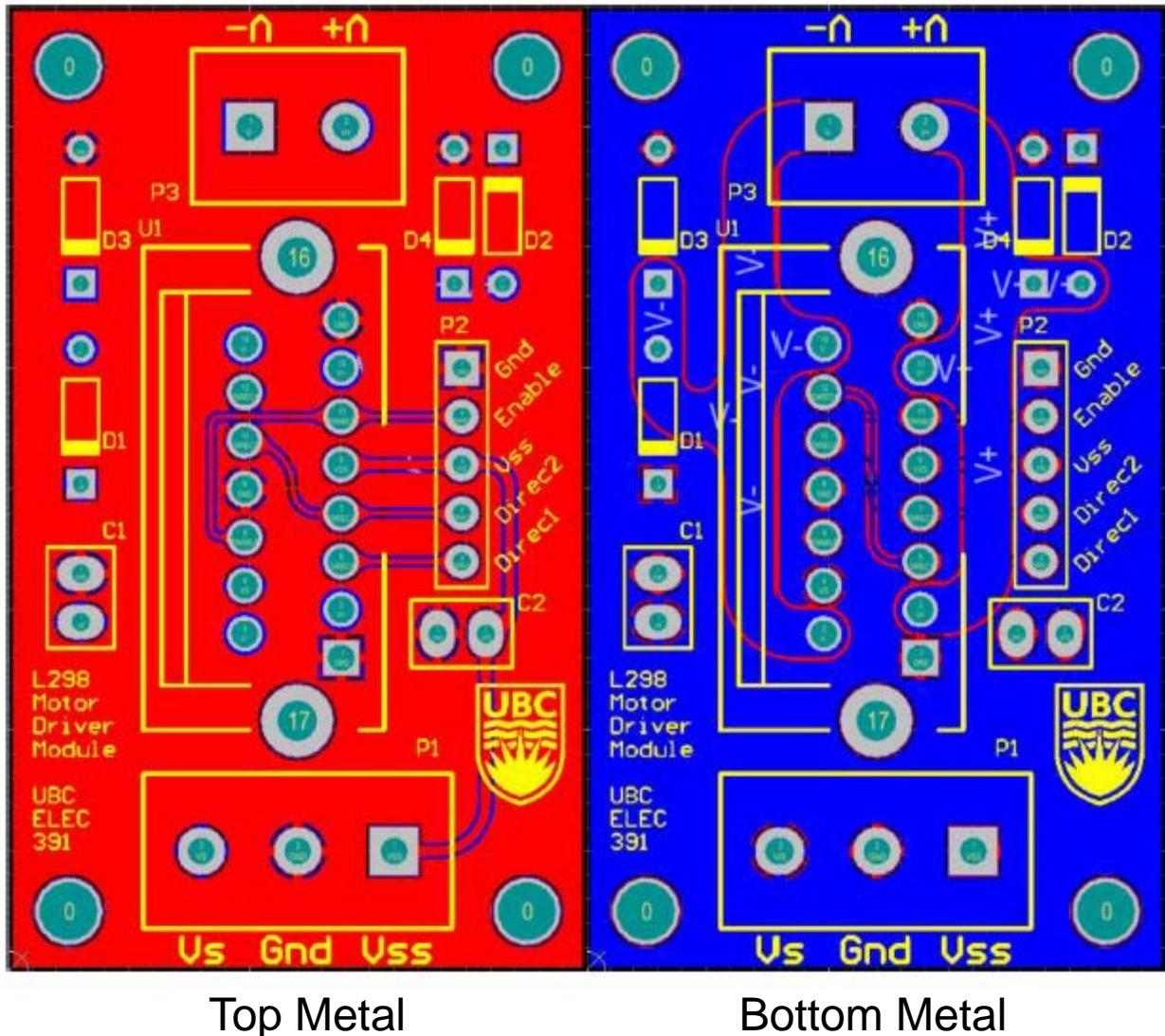
Wiring Tips

- **Left-click** or **<Enter>** to anchor the wire at the cursor position.
- **<Backspace>** (**←**) to remove the last anchor point.
- **<Spacebar>** to toggle the direction of the corner.
- **<Shift+Spacebar>** to cycle through all possible corner modes.
- **Right-click** or **<Esc>** to exit wire placement mode.
- To graphically edit the shape of a wire, Click once to select it first, then Click and hold on a segment or vertex to move it.
- Whenever a wire crosses the connection point of a component, or is terminated on another wire, a junction will automatically be created.
- A wire that crosses the end of a pin will connect to that pin, even if you delete the junction.
- To move a placed component and drag connected wires with it, hold down the **Ctrl** key while moving the component, or select **Move » Drag**.

LM298 Motor Driver Board Layout

Board Layout

- Size 1.2" x 2.1"
- 2 layers
- Mounting holes
- Thick traces for V- and V+
- Power planes for Vs and GND

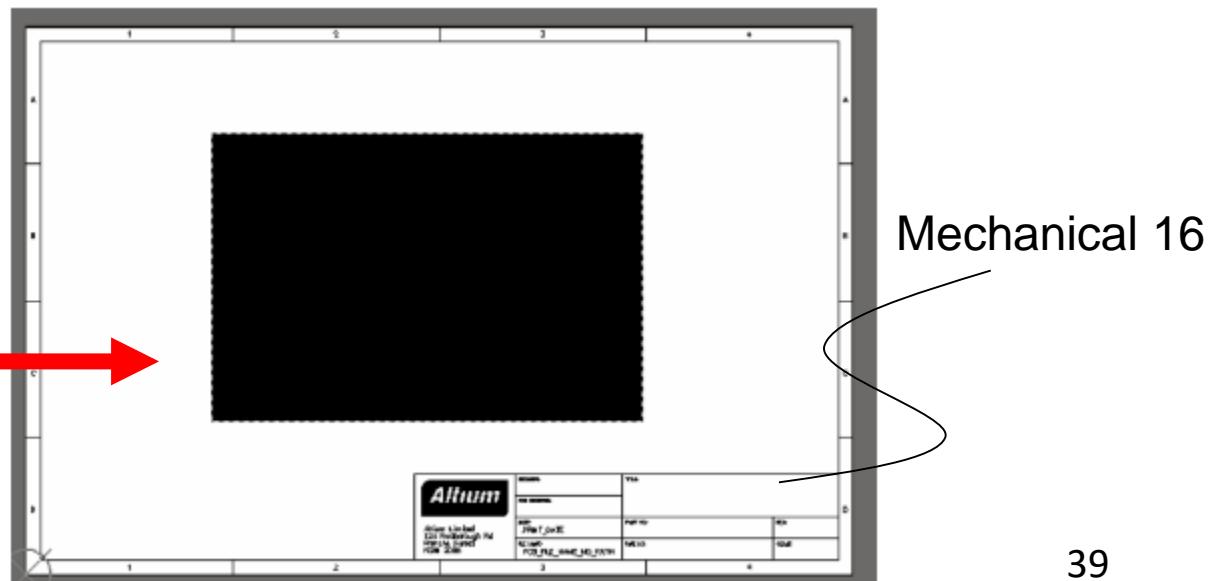
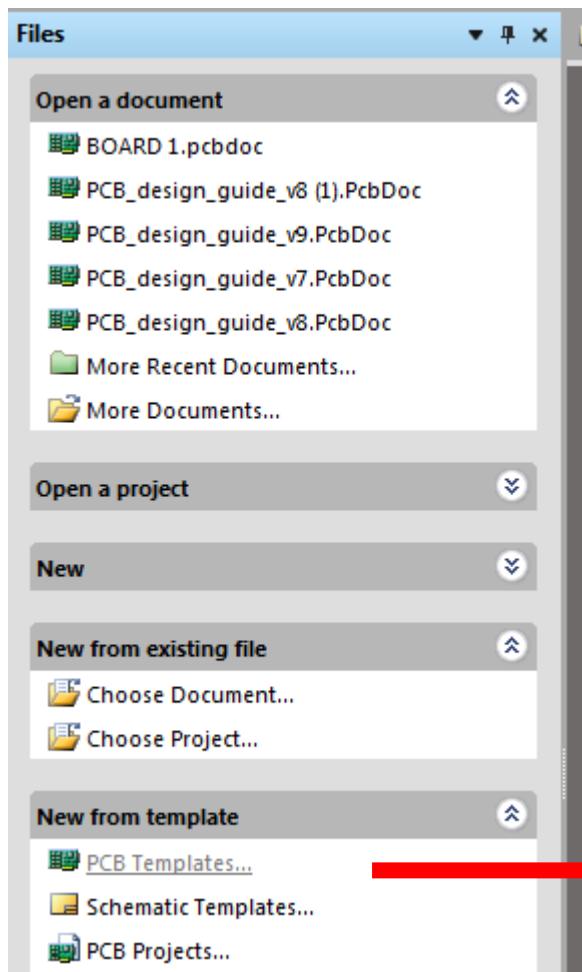


2 starting points for PCB design

1. From a companion schematic package
 - Prepare project schematics
 - Import schematic design
 - Component footprints are added automatically
 - Connectivity is indicated with rats nests
 - Net names are imported from the schematic
2. Directly from the PCB editor
 - You need to select and place manually each component footprint from a library
 - No rats nest – connectivity
 - You must assign nets manually (at least GND)

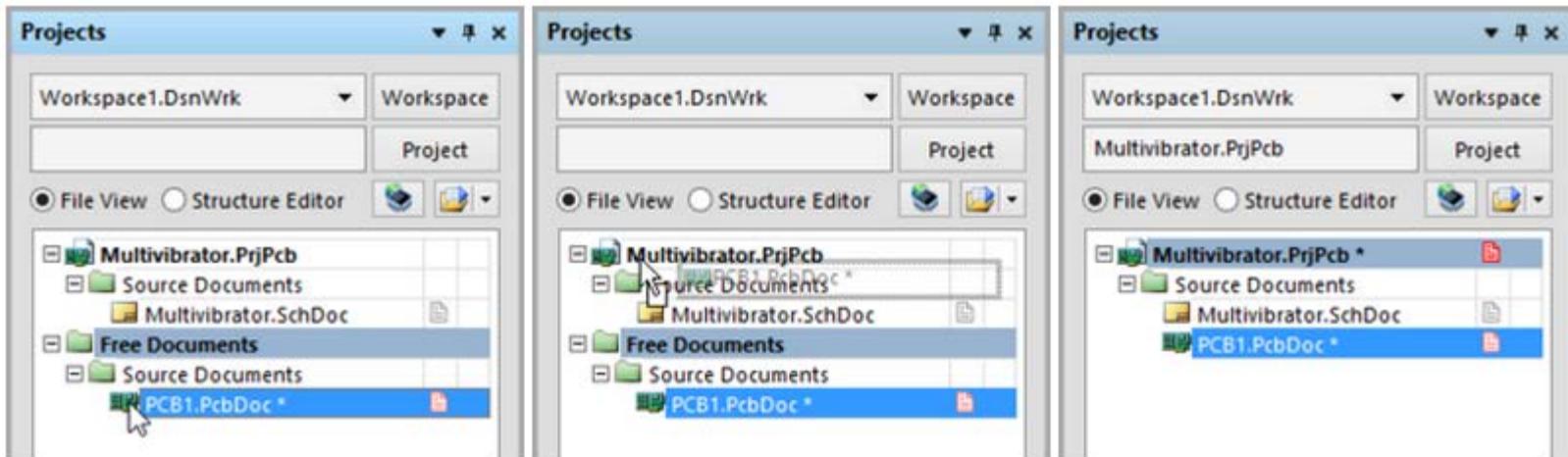
Creating a New Board from a template

- Files Panel:
 - New from template
 - select the A4.PcbDoc template
 - Save as ... same name and directory as SchDoc file



Adding PCB file to project

- Make the PCB board part of the project

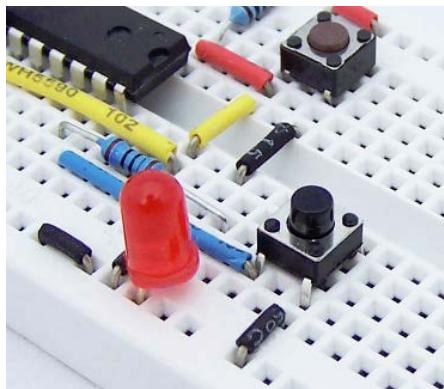


- Rename the file
- Save the PcbDoc file and the project

First things first ... choosing working units

- Imperial (inches)

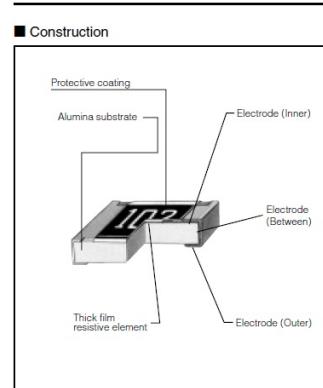
- $1/1000^{\text{th}}$ of an inch = 1 mil = 1 thou
- 100mils (0.1") is a common dimension



- Metric (mm)

- $1 \text{ mm} \neq 1 \text{ mil}$!
- Common unit in SM parts

Panasonic



Thick Film Chip Resistors

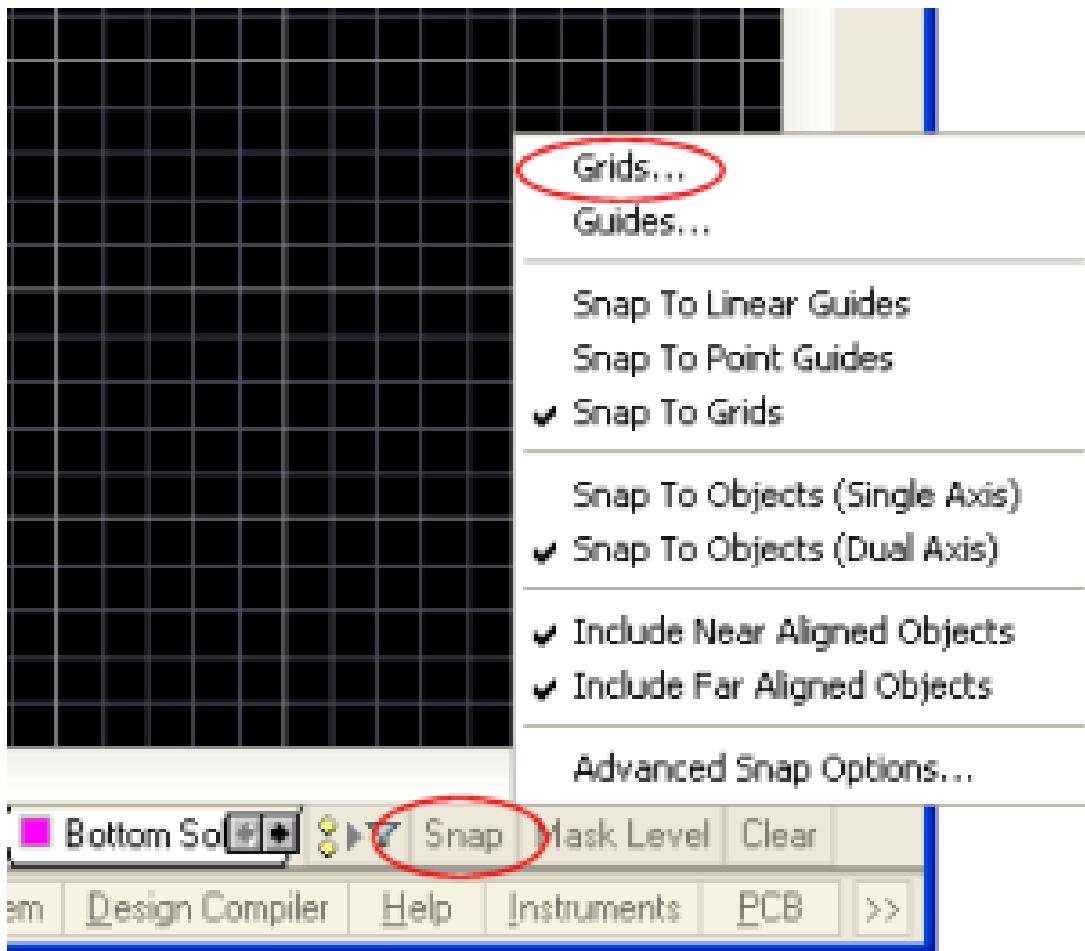
■ Dimensions in mm (not to scale)

Type (inches)	Dimensions (mm)				Mass (Weight) (g/1000 pcs.)
	L	W	a	t	
ERJXG (01005)	0.40 ^{+0.05} _{-0.02}	0.20 ^{+0.02} _{-0.02}	0.10 ^{+0.03} _{-0.02}	0.10 ^{+0.02} _{-0.02}	0.13 ^{+0.02} _{-0.02}
ERJ1G (0201)	0.60 ^{+0.05} _{-0.02}	0.30 ^{+0.03} _{-0.02}	0.10 ^{+0.06} _{-0.02}	0.15 ^{+0.05} _{-0.02}	0.23 ^{+0.03} _{-0.02}
ERJ2G (0402)	1.00 ^{+0.05} _{-0.02}	0.50 ^{+0.06} _{-0.02}	0.20 ^{+0.10} _{-0.02}	0.25 ^{+0.06} _{-0.02}	0.35 ^{+0.05} _{-0.02}
ERJ3G (0603)	1.60 ^{+0.15} _{-0.05}	0.80 ^{+0.15} _{-0.05}	0.30 ^{+0.20} _{-0.05}	0.30 ^{+0.10} _{-0.05}	0.45 ^{+0.10} _{-0.05}
ERJ6G (0906)	2.00 ^{+0.25} _{-0.10}	1.25 ^{+0.20} _{-0.10}	0.40 ^{+0.20} _{-0.10}	0.40 ^{+0.20} _{-0.10}	0.60 ^{+0.30} _{-0.10}
ERJ8G (1206)	3.20 ^{+0.35} _{-0.20}	1.60 ^{+0.30} _{-0.20}	0.50 ^{+0.20} _{-0.10}	0.50 ^{+0.20} _{-0.10}	0.60 ^{+0.30} _{-0.10}
ERJ14 (1612)	3.20 ^{+0.35} _{-0.20}	2.50 ^{+0.35} _{-0.20}	0.50 ^{+0.20} _{-0.10}	0.50 ^{+0.20} _{-0.10}	0.60 ^{+0.30} _{-0.10}
ERJ12 (1612)	4.50 ^{+0.35} _{-0.20}	3.20 ^{+0.30} _{-0.20}	0.50 ^{+0.20} _{-0.10}	0.50 ^{+0.20} _{-0.10}	0.60 ^{+0.30} _{-0.10}
ERJ12Z (2010)	5.00 ^{+0.35} _{-0.20}	2.50 ^{+0.35} _{-0.20}	0.60 ^{+0.20} _{-0.10}	0.60 ^{+0.20} _{-0.10}	0.60 ^{+0.30} _{-0.10}
ERJ17 (2512)	6.40 ^{+0.35} _{-0.20}	3.20 ^{+0.30} _{-0.20}	0.65 ^{+0.20} _{-0.10}	0.60 ^{+0.20} _{-0.10}	0.60 ^{+0.30} _{-0.10}

- Remember: 100mils = 2.54mm
- To switch units in Altium Press <Q>

First things first ... setting the snap grid

- PCBs are grid based objects

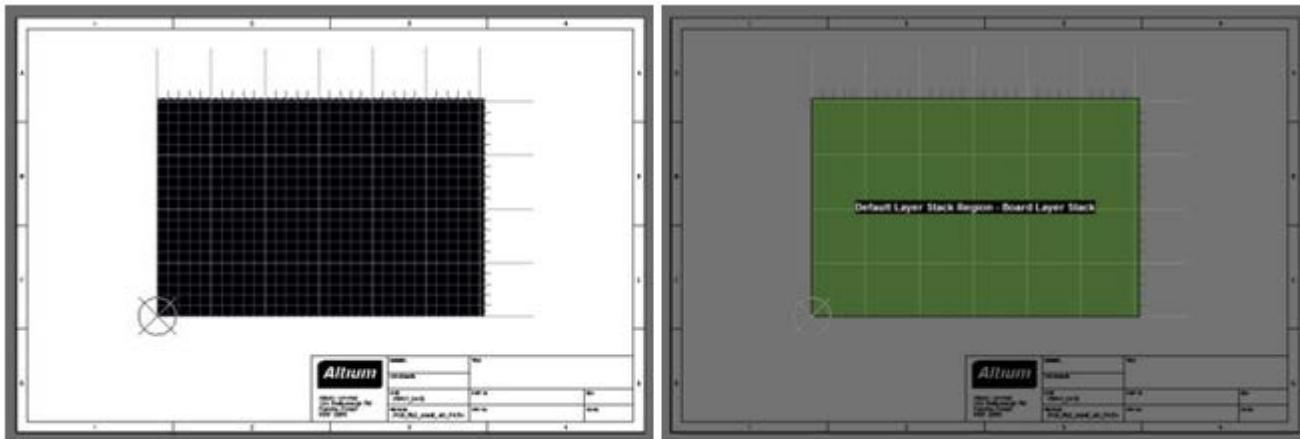


Unified Cursor-Snap System

- Selecting a suitable snap grid:
 - $\text{<Ctrl>} + \text{<G>}$
 - Start with a coarse grid to define board size

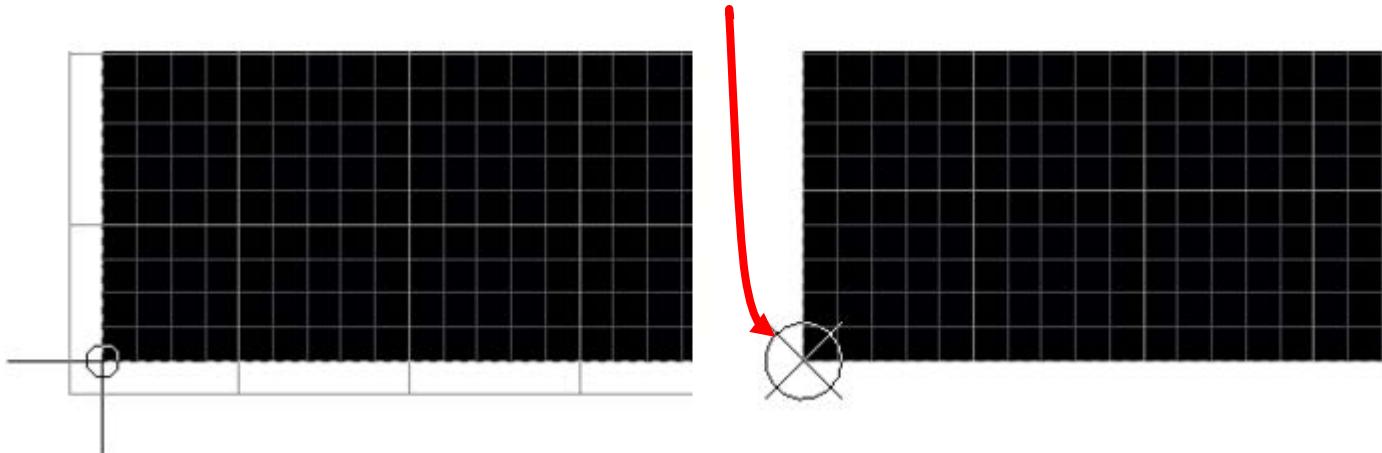
First things first ... redefining the board shape

- Viewing modes:
 - Board Planning Mode (**1**)
 - **Design » Edit Board Shape** (resize to 1.2" x 2.1")
 - **Design >> Move Board Shape** (Relocate the origin)
 - 2D Layout Mode (**2**)
 - 3D Layout Mode (**3**).



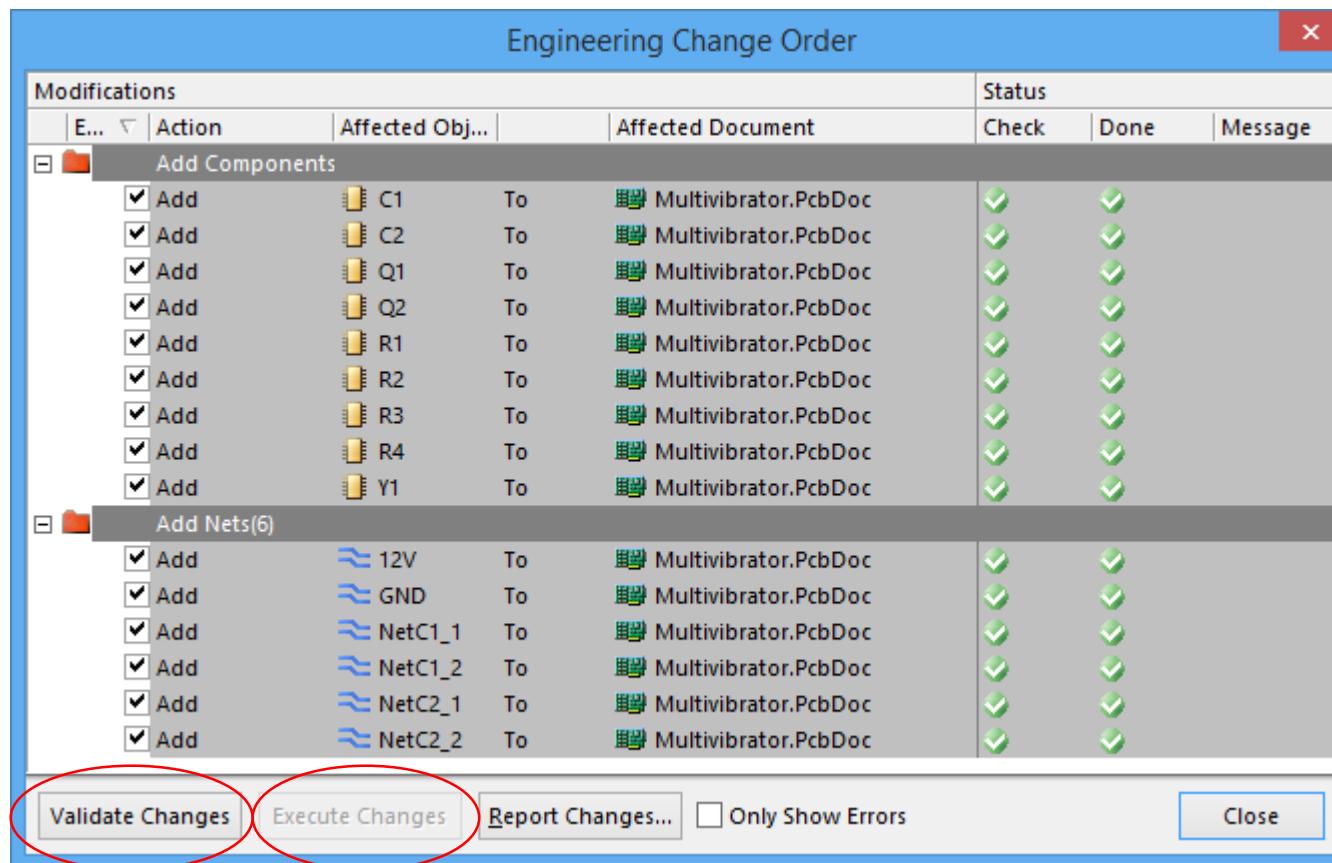
First things first ... setting the board origin

- Absolute origin (lower left corner)
- User-defined relative origin
 - Edit >> Origin >> Set

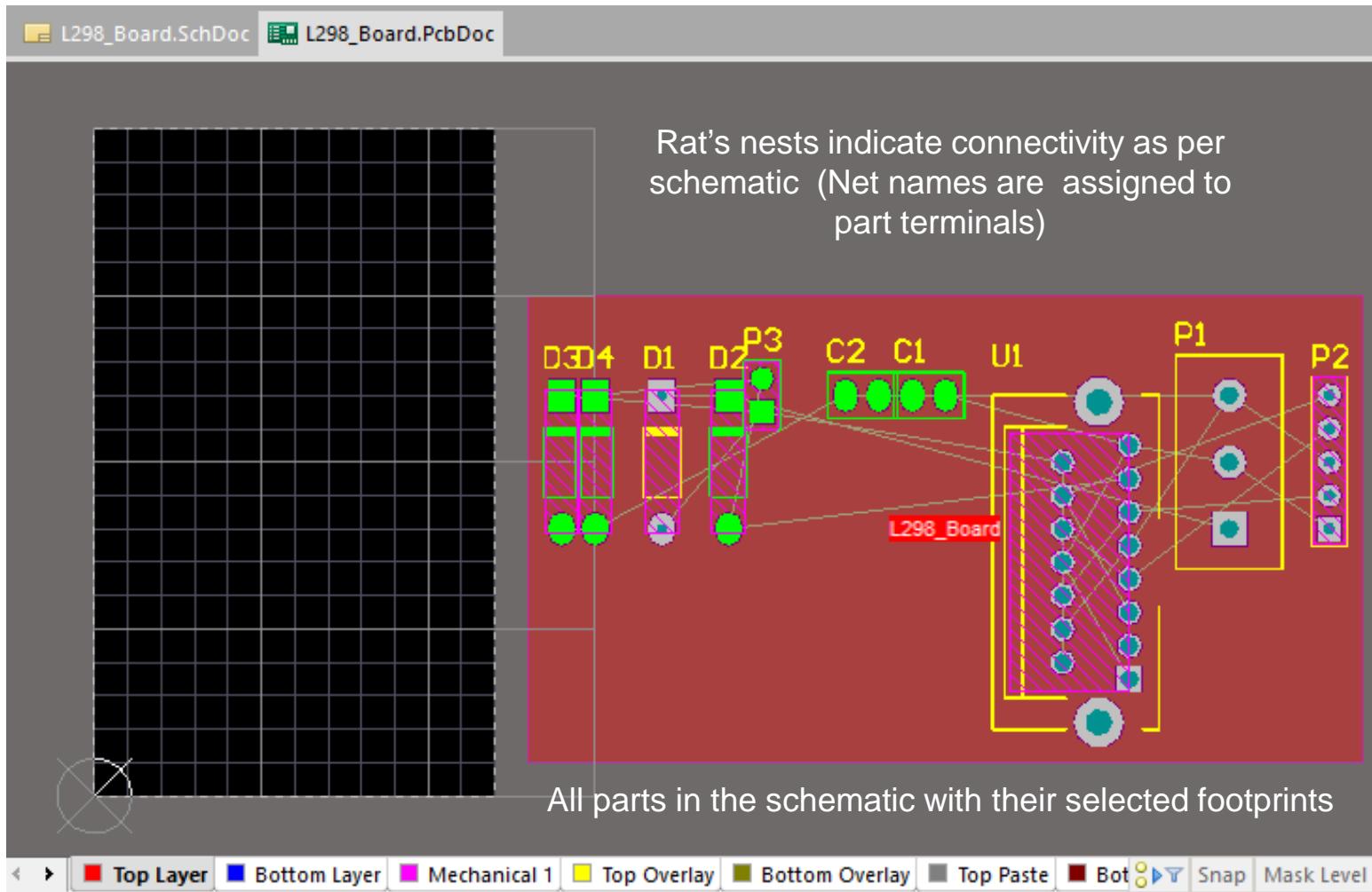


Design transfer

- Design transfer
 - On Schematic file
 - Design >> Update PCB Document ...

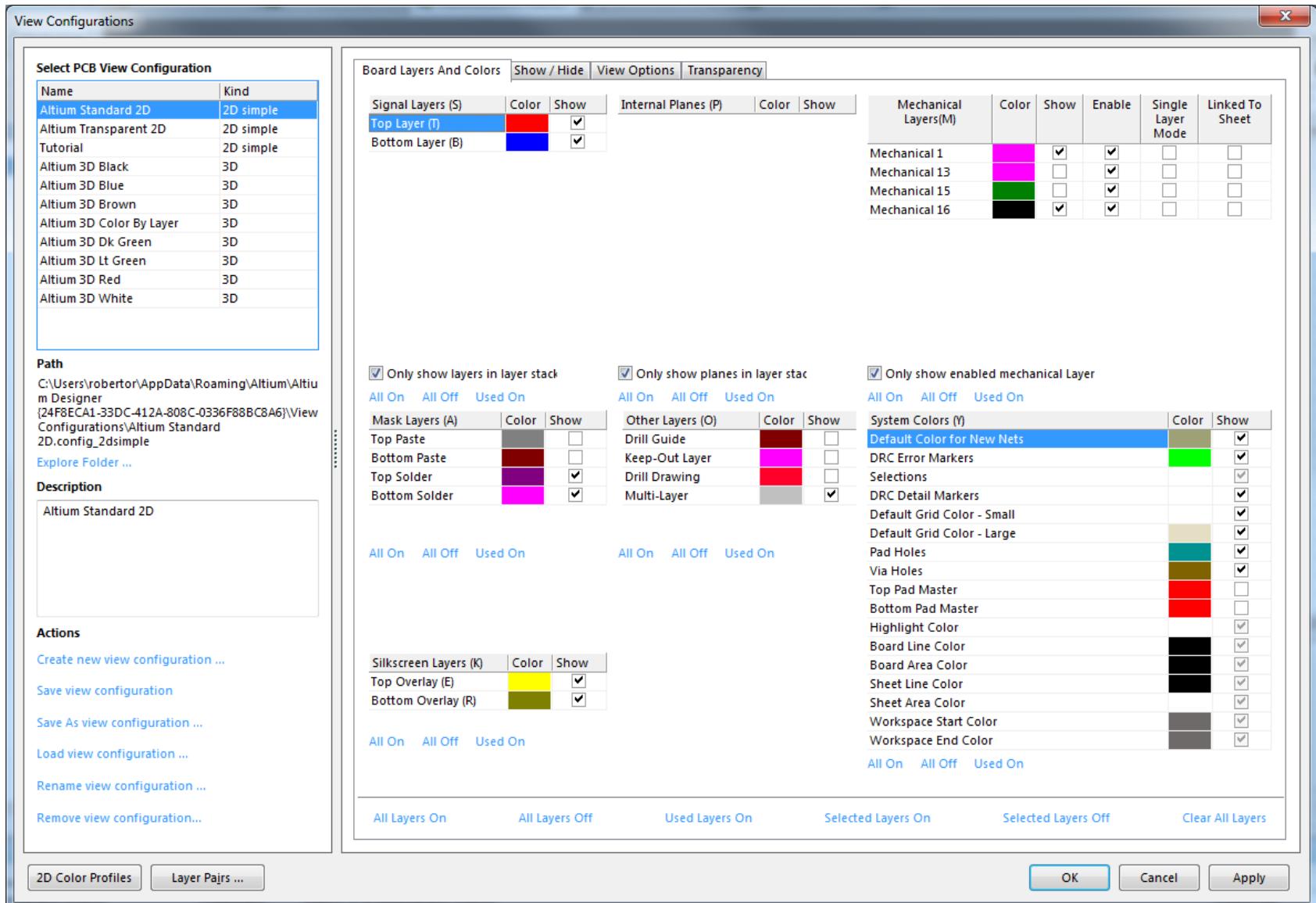


Design transfer



Configuring the Display Layers

- Design » Board Layers and Colors

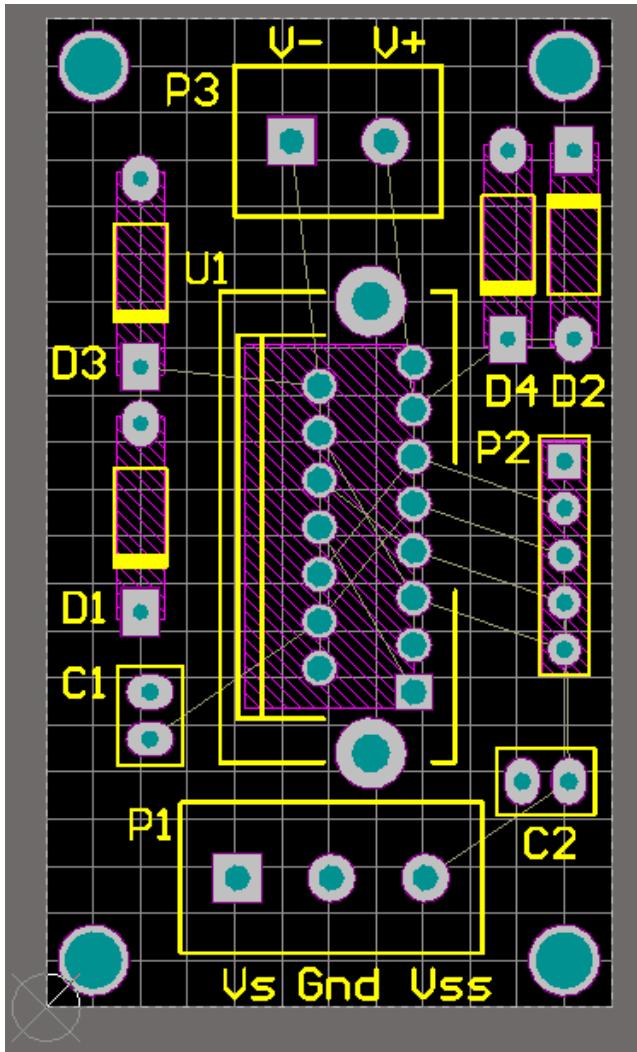


Configuring the Display Layers



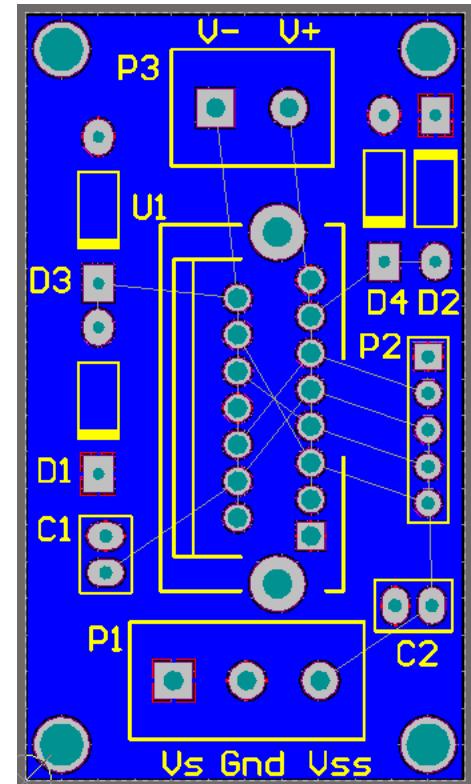
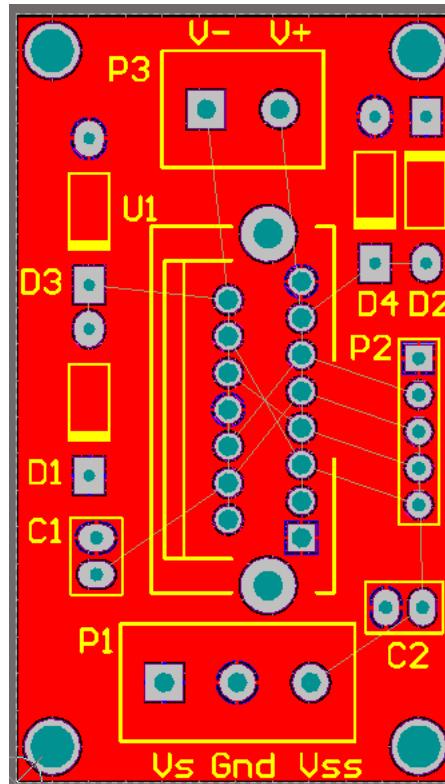
- **Electrical layers**
32 signal layers and 16 internal power plane layers.
- **Mechanical layers**
32 general purpose mechanical layers, used for design tasks such as dimensions, fabrication details, assembly instructions, or special purpose tasks such as glue dot layers. These layers can be selectively included in print and Gerber output generation. They can also be paired, meaning that objects placed on one of the paired layers in the library editor, will flip to the other layer in the pair when the component is flipped to the bottom side of the board.
- **Special layers**
these include the top and bottom silkscreen layers, the solder and paste mask layers, drill layers, the Keep-Out layer (used to define the electrical boundaries), the multilayer (used for multilayer pads and vias), the connection layer, DRC error layer, grid layers, hole layers, and other display-type layers.

Positioning components & routing



122mils mounting holes

Place a plane on top for GND
Place a plane bottom for Vs



Handy shortcuts for routing

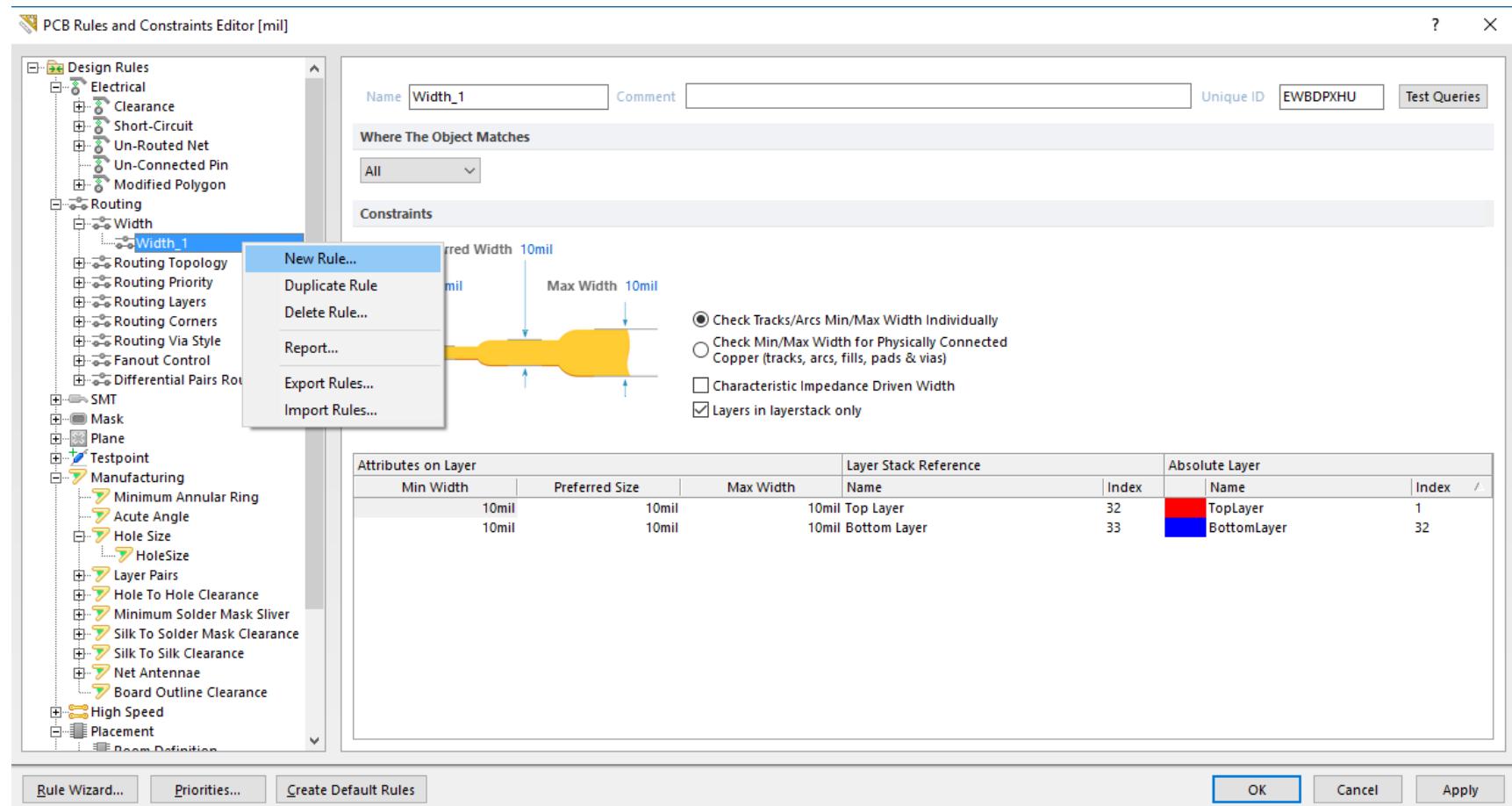
- Press * on the numeric keypad while routing to cycle through the available signal layers. A via will automatically be added, in accordance with the applicable Routing Via Style design rule. Alternatively, use **Ctrl+Shift+Roll** shortcuts to move back and forth through the available signal layers.
- **Shift+R** to cycle through the enabled conflict resolution modes, including Push, Walkaround, Hug and Push, and Ignore. Enable the required modes in the **PCB Editor - Interactive Routing** page of the *Preferences* dialog.
- **Shift+S** to cycle single layer mode on and off, ideal when there are many objects on multiple layers.
- **Spacebar** to toggle the corner direction (for all but any angle mode).
- **Shift+Spacebar** to cycle through the various track corner modes. The styles are: any angle, 45°, 45° with arc, 90° and 90° with arc. There is an option to limit this to 45° and 90° in the **PCB Editor - Interactive Routing** page of the *Preferences* dialog.

Design Rules

- Design >> Rules

Rule	Constrain	Query
Electrical, Clearance	Min clearance = 7mil	All
Routing, Width*	Min width = 7mils Max width = 500mils Preferred = 10mils	All
Routing, Width_IO	Min width = 7mils Max width =500mils Preferred =100mils	Advanced (Query) (InNet('V+') OR InNet('V-'))
Width_Vss	Min width = 7mils Max width =500mils Preferred =20mils	Net Vss

Custom Routing design rules



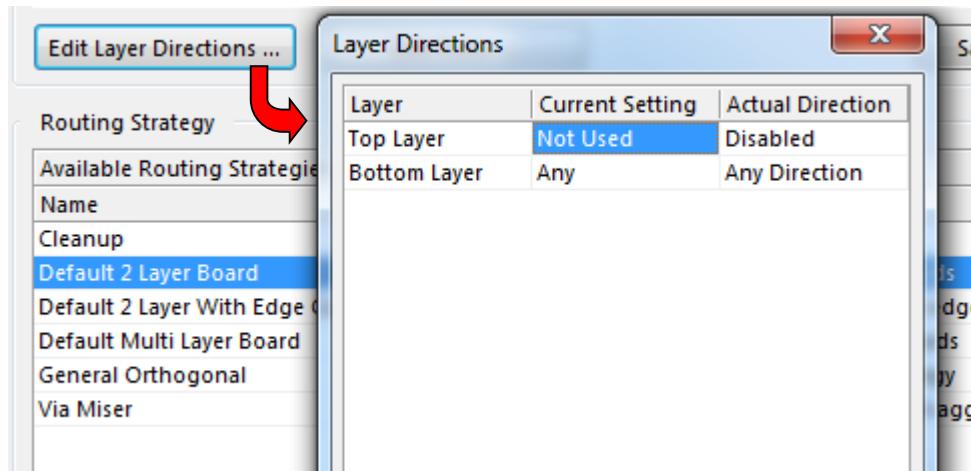
Rename to “Width_IO”

Use ‘Custom Query’ to set
Belongs to net V+
OR
Belongs to V-

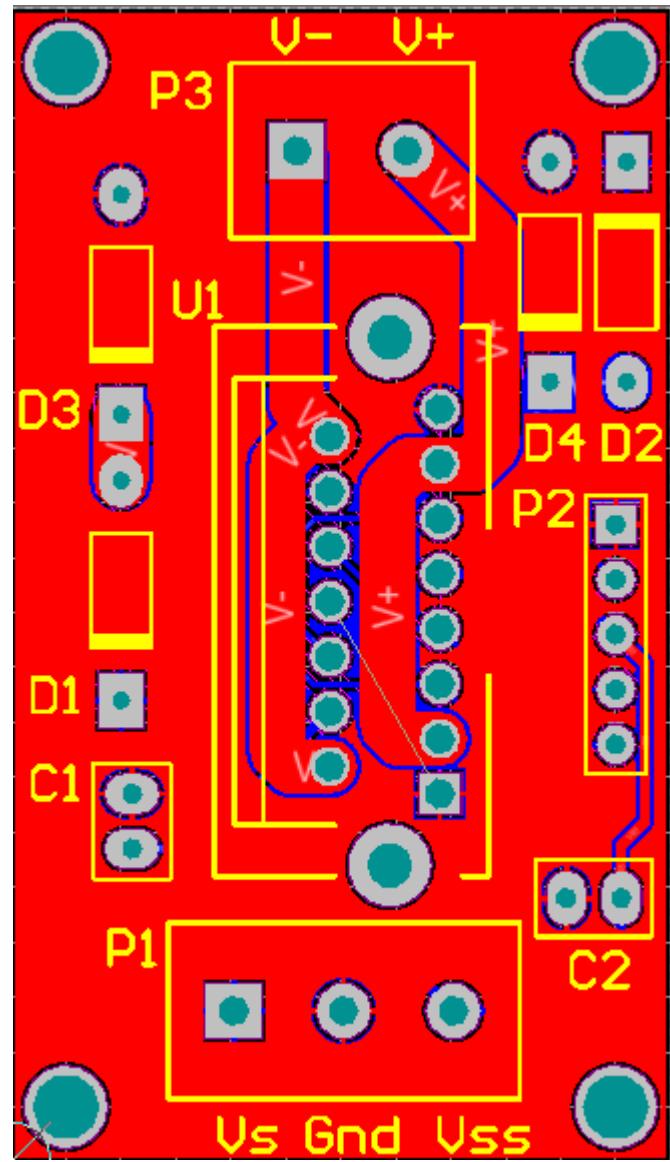
Set rule execution
priority

Auto route

- Tools » Un-Route » All
- Auto Route » All



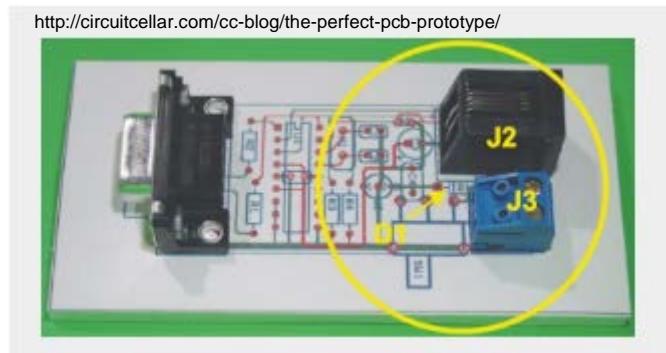
- You can also set single layer routing



PCB Design Best Practices

Best Practices: Estimating board size

- Before starting layout it is good to have an idea of the target size of the PCB board and all other relevant dimensions.
- It is very helpful to have the components at hand to plan the floor-plan.
- An old good trick of the trade is to print the PCB layout at a 1:1 scale, place the printout on a foam and stick on the through hole components.

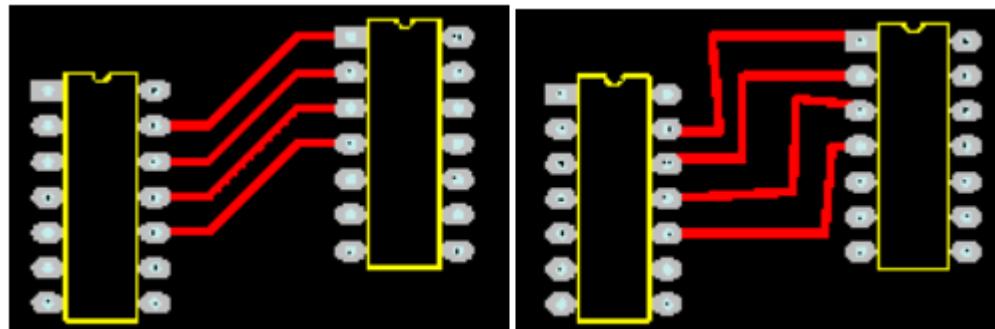


Best Practices: Floor planning

- Choose your units and set the grid
- Carefully plan the placement of components
 - Place analog and digital sections apart
 - Group components into ‘functional blocks’
 - Place ICs in the same direction
 - Align ICs, resistors, labels, capacitors etc.
 - Place de-caps close by their ICs
 - Place Op-amp resistors near the Op-amp
 - Plan for mounting holes and heat sinks
- Aim for symmetry when possible
- Do use Design Rule check

Best Practices: Routing strategy

- On two sided boards keep traces perpendicular as much as possible
- Avoid 90 degree bends in tracks (?) (reduced chances of acid traps)
- Keep traces a short as possible
- Always connect a trace to the center of the pad
- Use teardrops (Tools >> tear drops), and use vias to avoid lockout
- Do not place vias under SMD pads
- Layout first all critical traces
 - e.g. CLK, diff pairs, controlled length
- Polygons as fills:
Connect to GND (EMC), or do not leave 'dead copper' →
- Rout nicely



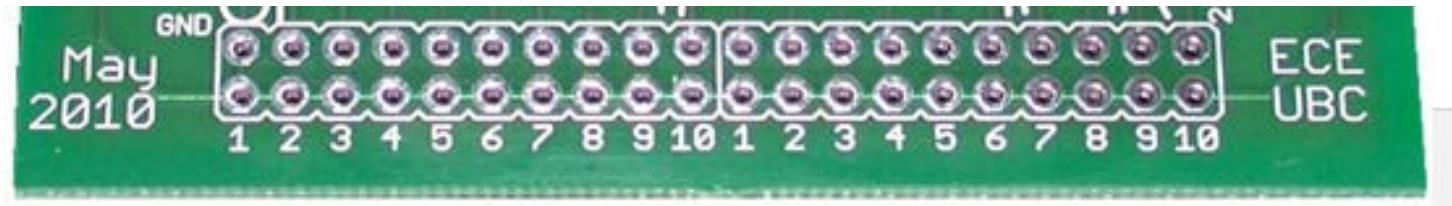
[Ref 3]

An example of GOOD routing (Left) and BAD routing (Right)



Best Practices: Labelling

- Always sign your design: add date, version, and name of board
- Label all relevant inputs and outputs
- Default sizes for comments and designators are 60mils x 10mils
- If you have silkscreen on both sides add a 'TOP' label to the top overlay.



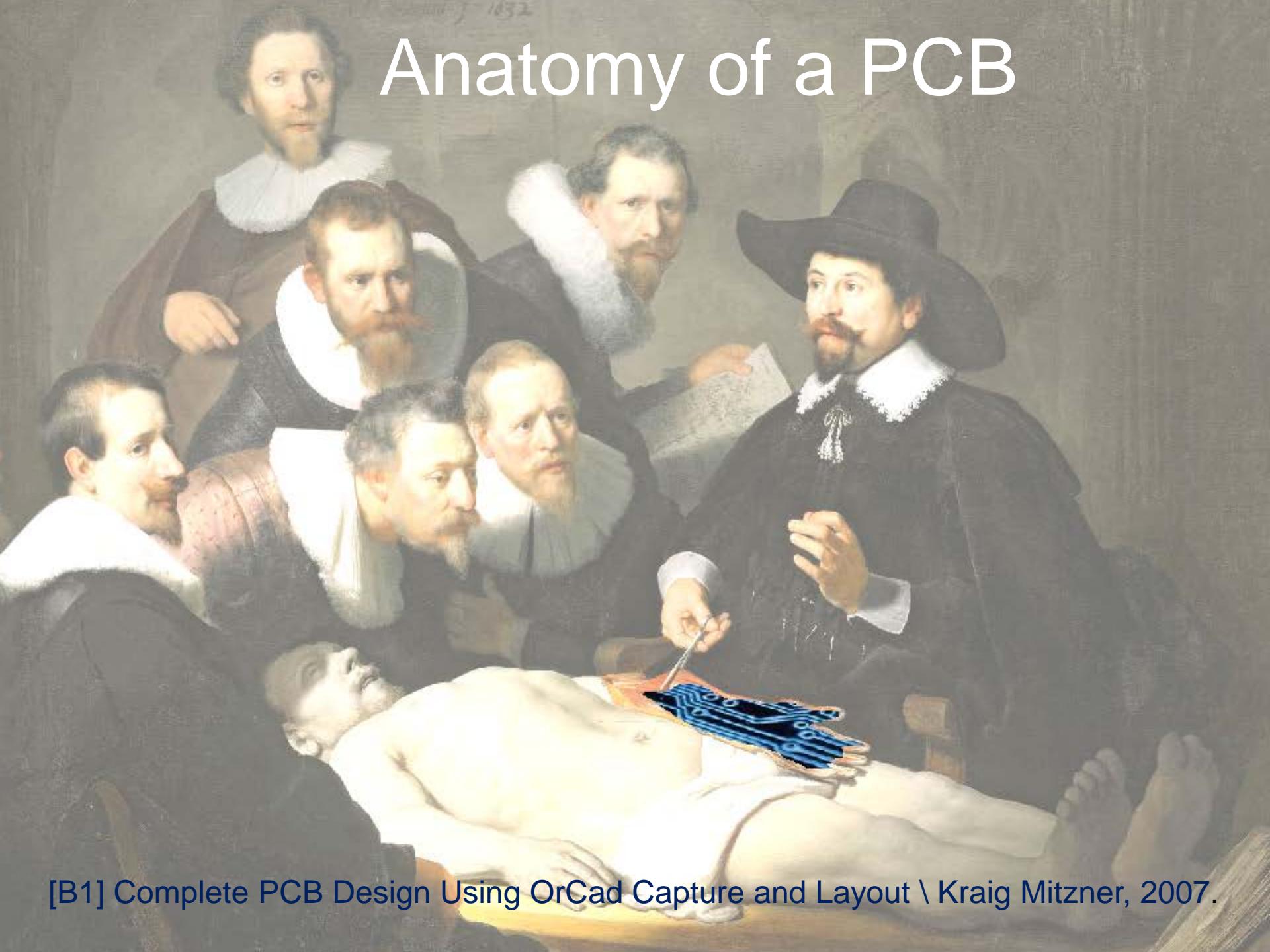
Best Practices: Finishing touches

- Add mounting holes
- Run: Reports >> Board Information
 - Board specification → to confirm board size
 - Non-plated hole size
 - Plated hole size
- Using the hole size editor:
 - Minimize the total number of holes sizes
 - Verify that all vias are the same size (if possible)
- Verify that there are no unwanted leftovers on any Mechanical layer

Online resources

1. Ten best practices of PCB design – EDN Magazine, Edwin Robledo & Mark Toth
2. Circuit Board Layout Techniques – Texas Instruments, Chapter 17 of Op-amps for everyone
3. PCB Design Tutorial – David L. Jones

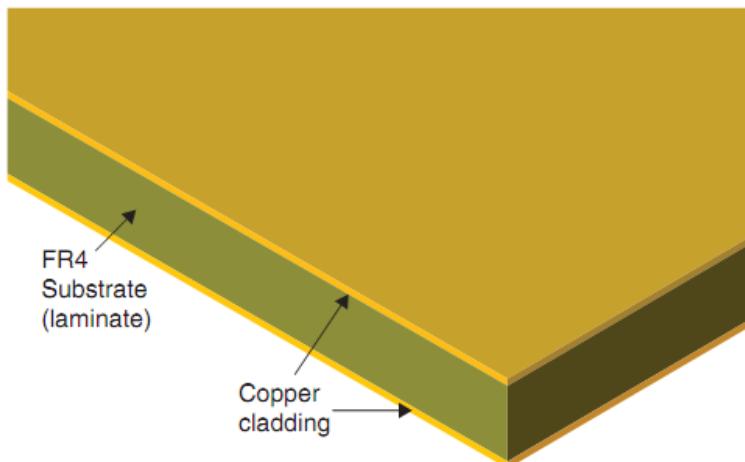
Anatomy of a PCB



[B1] Complete PCB Design Using OrCad Capture and Layout \ Kraig Mitzner, 2007.

PCB Anatomy: Laminate

- **Laminate (substrate)**
 - Rigid board of insulating material
 - Available in different thicknesses & materials
 - Covered with copper foil or cladding
 - Provides structural support and insulation to circuit components
 - Most commonly used material type is FR4, 62-63mils (1.6mm) thick

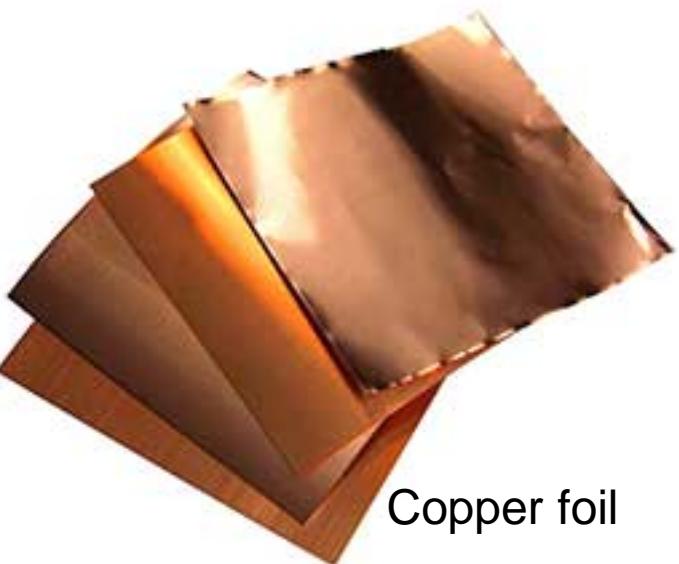


Cu thickness measured in weight oz/ft²
 $\frac{1}{2}$ oz → 0.7mils
1 oz → 1.4mils
2 oz → 2.8mils

1mil = 25μm

Figure 1-2 A double-sided copper clad FR4 substrate.

PCB Anatomy: Laminate



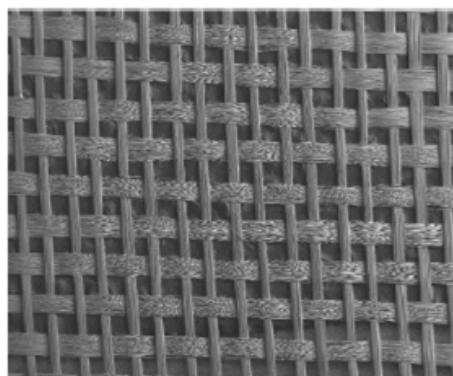
Copper foil



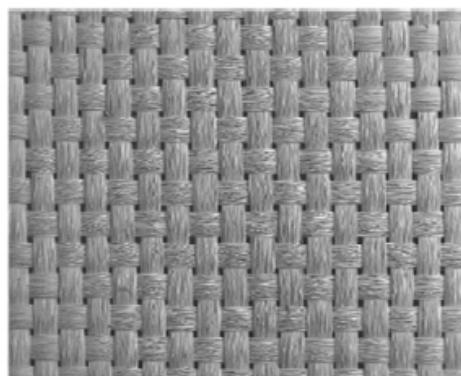
Prepeg



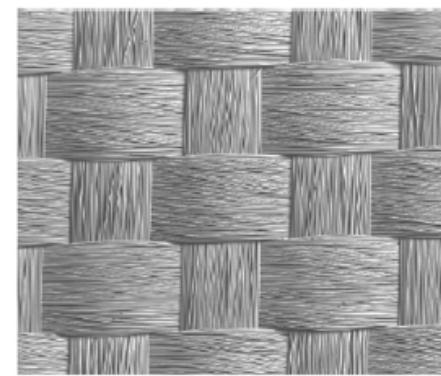
Copper clad



1080



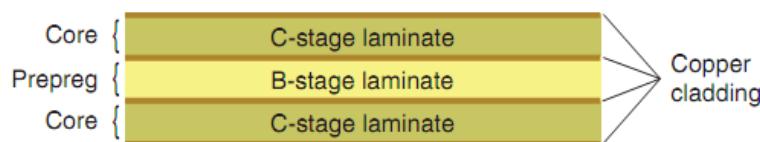
2116



7628

Common glass weaves

PCB Anatomy: Layer Stack-up



Ref [B1] *Figure 1-3 Cores and prepreg.*



 **COFAN**
COFAN-PCB.COM

Design >> Layer Stack Manager ...

A screenshot of the 'Layer Stack Manager' software interface. The window title is 'Layer Stack Manager'. At the top, there are buttons for 'Save', 'Load', 'Presets' (with a dropdown arrow), and a checked '3D' checkbox. To the right of these are several icons: a blue arrow, a red arrow, a green square, a blue square, a yellow square, and a 'Layer Pairs' dropdown menu. Below the toolbar is a preview window showing a 3D perspective of the PCB stack-up. The stack-up consists of several layers: a green 'Top Overlay', a light green 'Top Solder Mask', a grey 'Dielectric1' layer with orange squares representing vias, a grey 'Bottom Layer', a light green 'Bottom Solder Mask', and a green 'Bottom Overlay'. To the right of the preview is a detailed table of the stack-up layers:

Layer Name	Type	Material	Thickness (mil)	Dielectric Material	Dielectric Constant	Pullback (mil)
Top Overlay	Overlay					
Top Solder	Solder Mask/Co...	Surface Material	0.4	Solder Resist	3.5	
Top Layer	Signal	Copper	1.4			
Dielectric1	Dielectric	None	62	FR-4	4.8	
Bottom Layer	Signal	Copper	1.4			
Bottom Solder	Solder Mask/Co...	Surface Material	0.4	Solder Resist	3.5	
Bottom Overlay	Overlay					

PCB Anatomy: Traces / Tracks

- Copper traces are patterned either by:
 - Photolithography: requires photomasks
 - Laser: used to draw patterns on photoresist
 - Mechanical milling: Cu is removed to isolate the traces.
- Trace width and thickness determines:
 - Ampacity (current carrying capacity)
 - Characteristic impedance for RF designs
- Manufacturing limitations:
 - Minimum trace width and gap (e.g. 7/7)

Negative view:

Copper planes, Drill
holes, Solder Masks

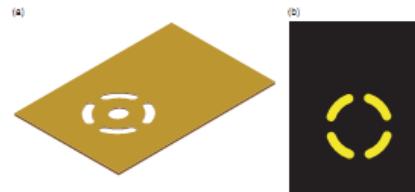


Figure 1-18 Copper in a plane layer (negative view without drill info). (a) Copper plane with thermal relief. (b) Negative view in Layout.

Teardrops:

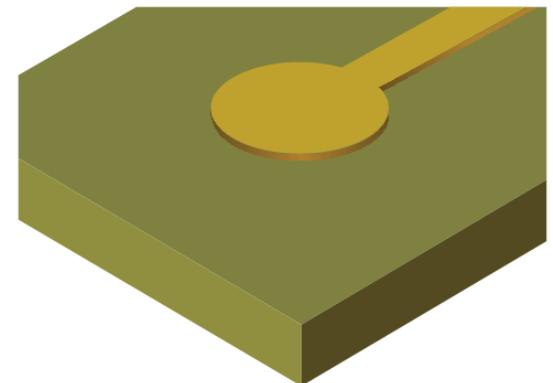
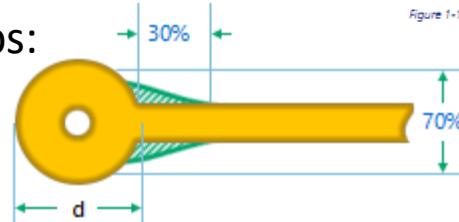


Figure 1-11 Copper pad and trace after etching and resist stripping.

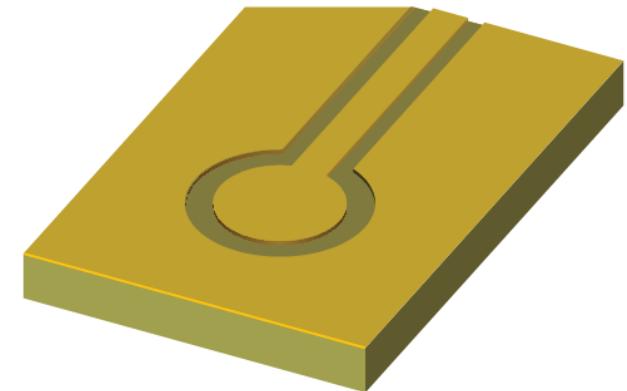
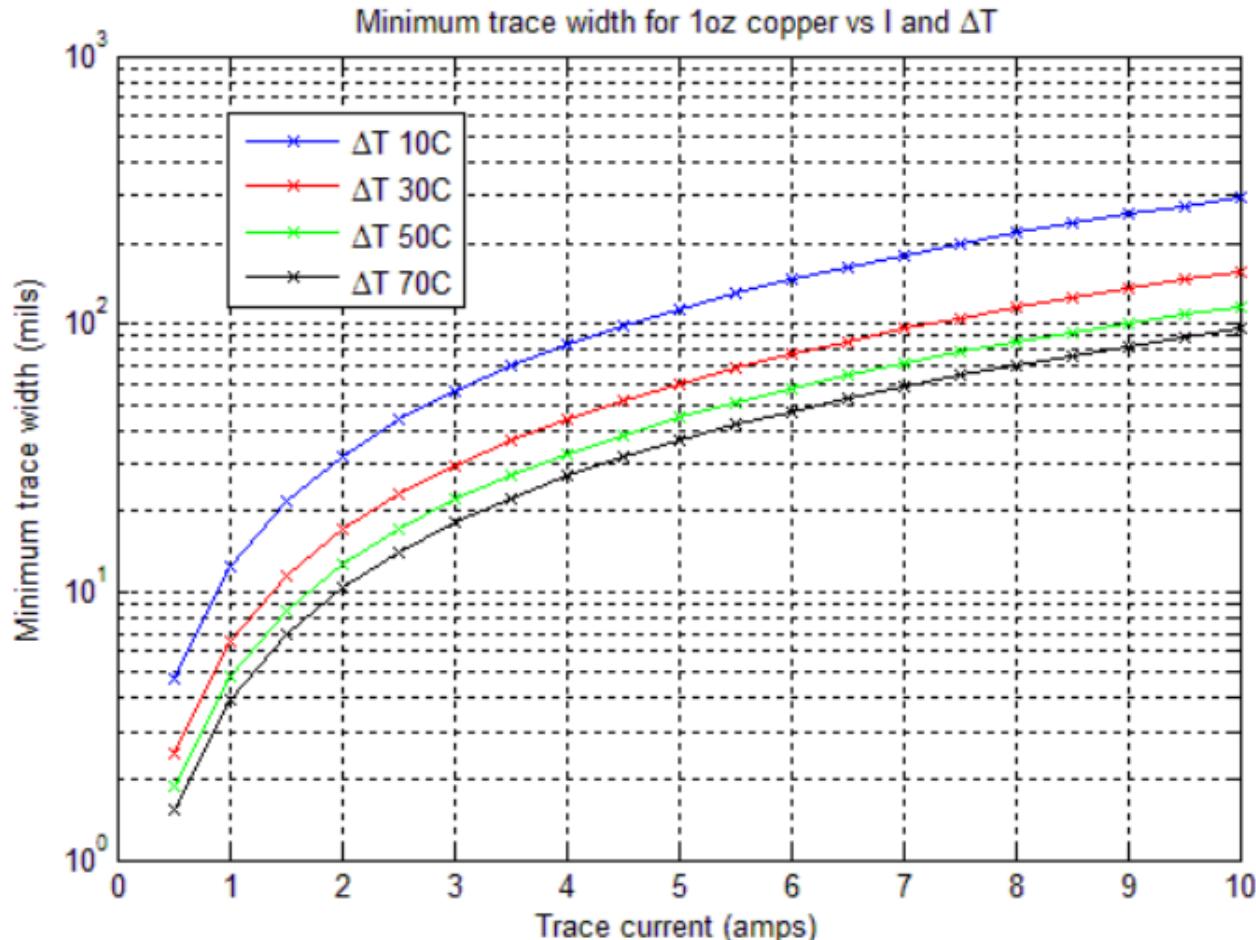


Figure 1-12 A mechanically milled trace.

PCB Anatomy: Trace width



Use the following online trace width calculator:

<http://circuitcalculator.com/wordpress/2006/01/31/pcb-trace-width-calculator>

PCB Anatomy: Vias

- Connection between layers is accomplished with via holes
- After the holes are drilled, their inner walls are plated
- Top and bottom traces are patterned after plating

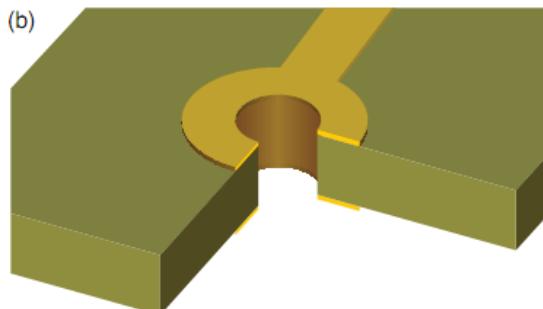
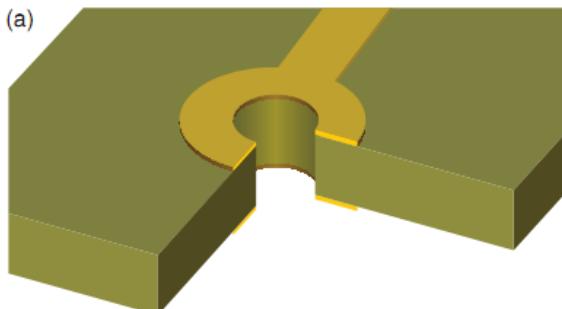
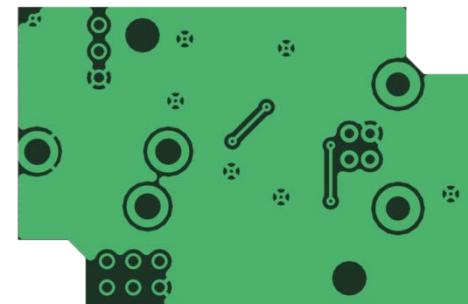


Figure 1-13 Holes are drilled into the board and then copper plated. (a) A nonplated through-hole. (b) A plated through-hole.



Thermal relief is needed when connecting a via to a copper plane

PWR and GND planes
are commonly inner
layers

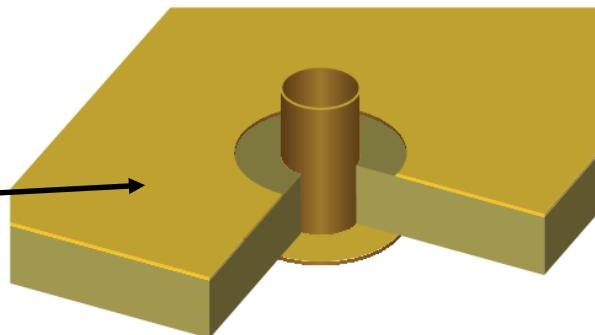


Figure 1-15 A clearance area provides isolation between a plated hole and a plane.

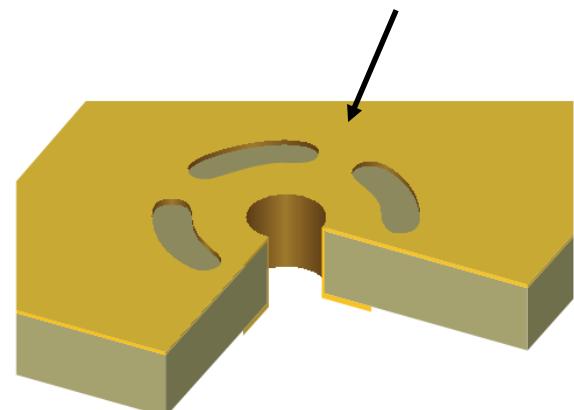


Figure 1-14 A connection to a plane layer through a thermal relief.

PCB Anatomy: Vias

- Types of via holes:
 - Plated and un-plated
 - through-hole, blind, buried

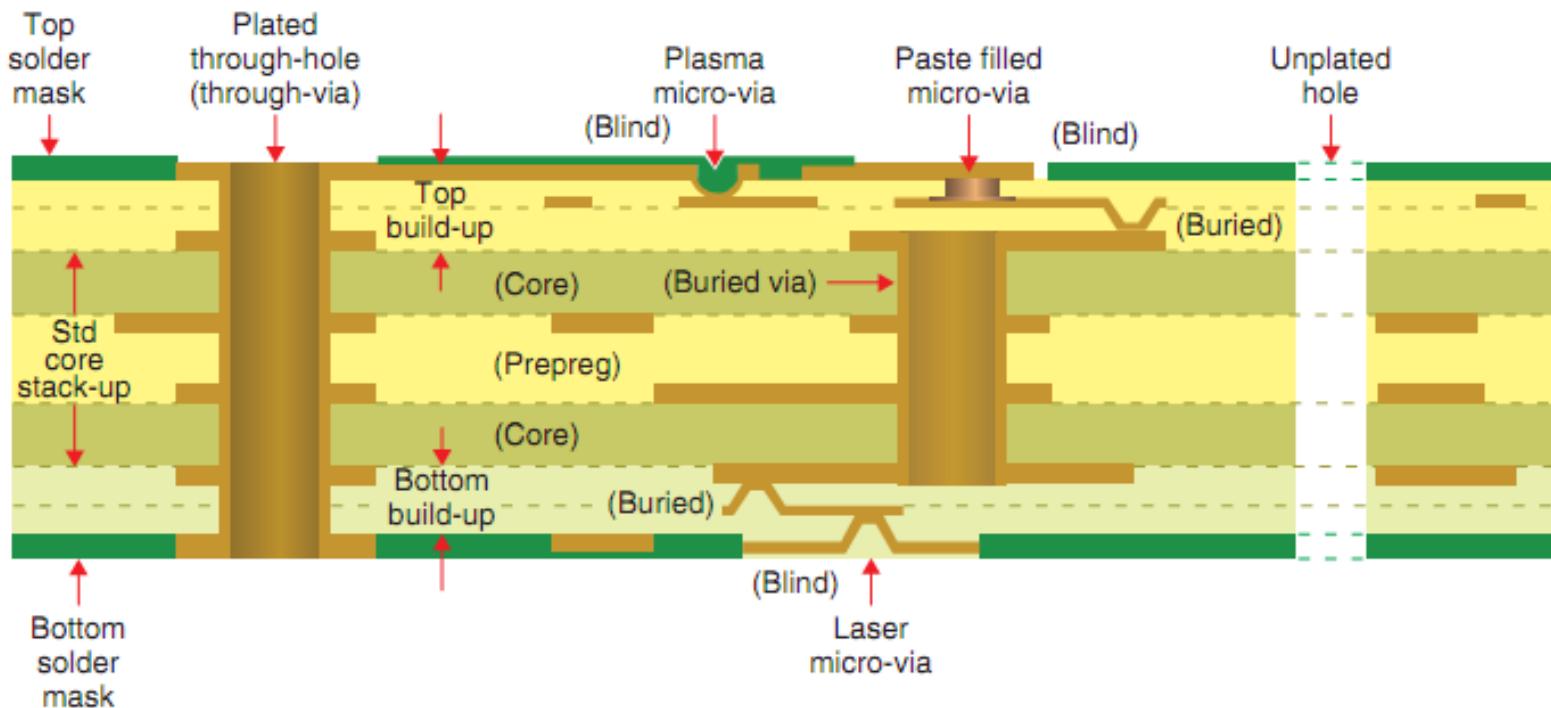


Figure 1-5 A built-up, multitechnology, PCB stack-up.

PCB Anatomy: Holes

Holes can be:

- Vias, multi-layer pads, mounting holes, or cuts
- Plated or non plated

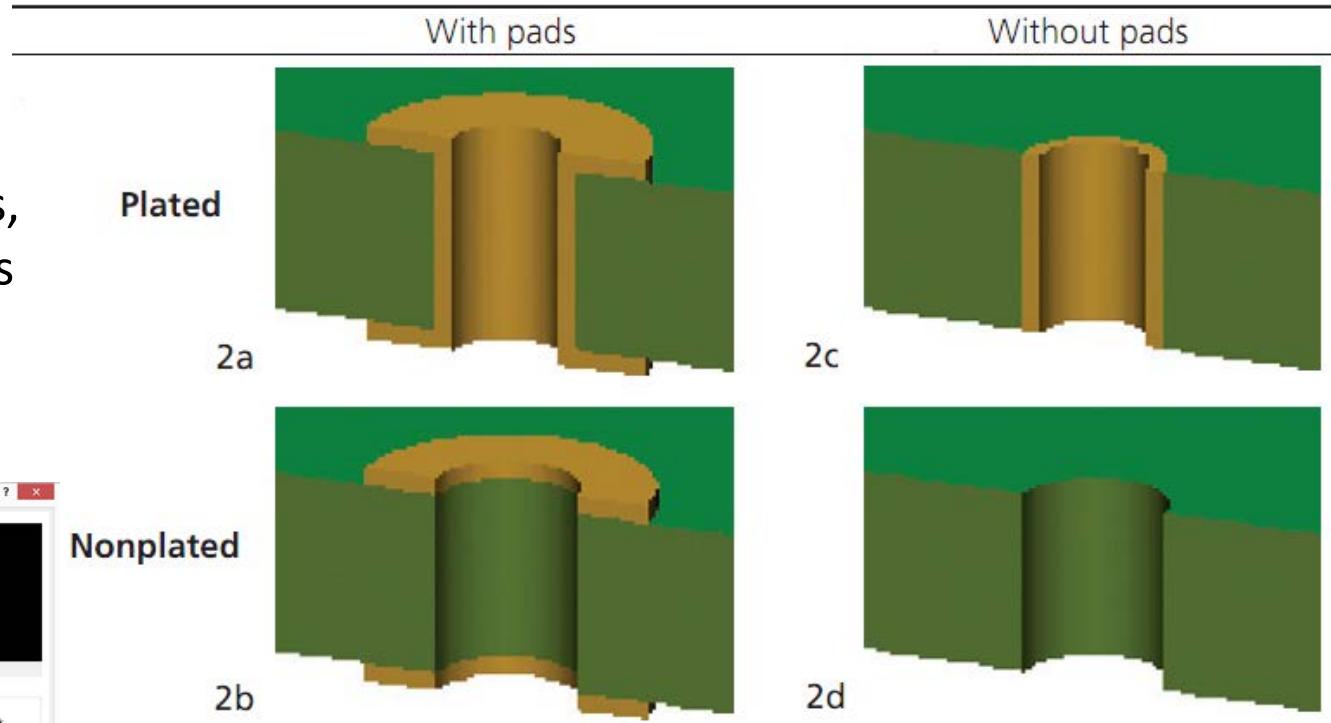
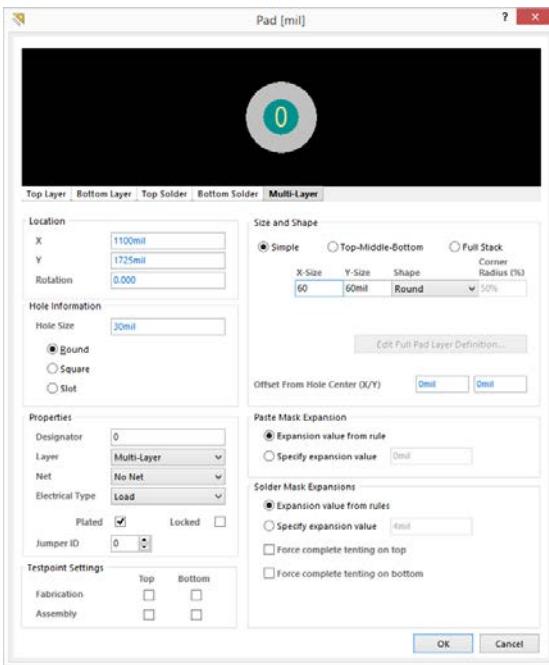


Table 8-2 Basic hole types

You must specify whether a hole is plated or non plated during the design process

Plating reduces hole size by 0.003"

PCB Anatomy: Pads

- Pads: contact areas for soldering components, test points, and solder traps
- Pads can have any shape
- Single layer pads: Top/bottom layer, common for SMT, end launch connectors
- Multi-layer pads: for through hole components
- Footprints are a collection of pads

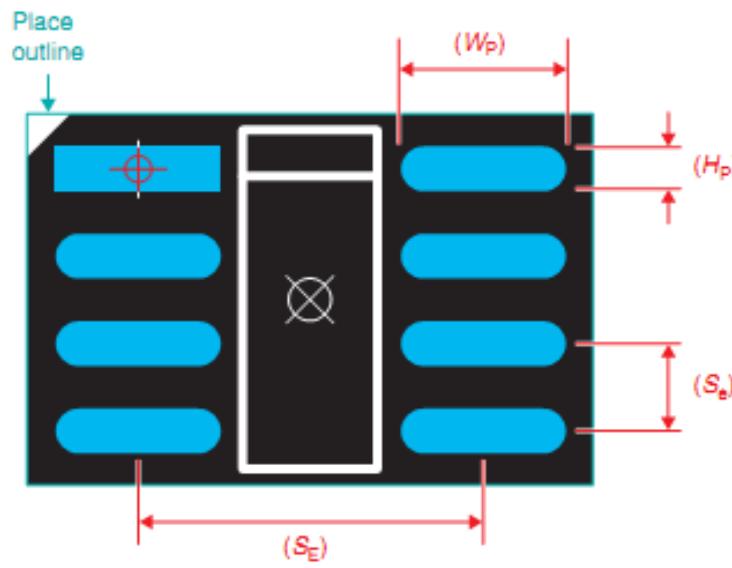


Figure 5-7 Footprint dimensions (typical convention).

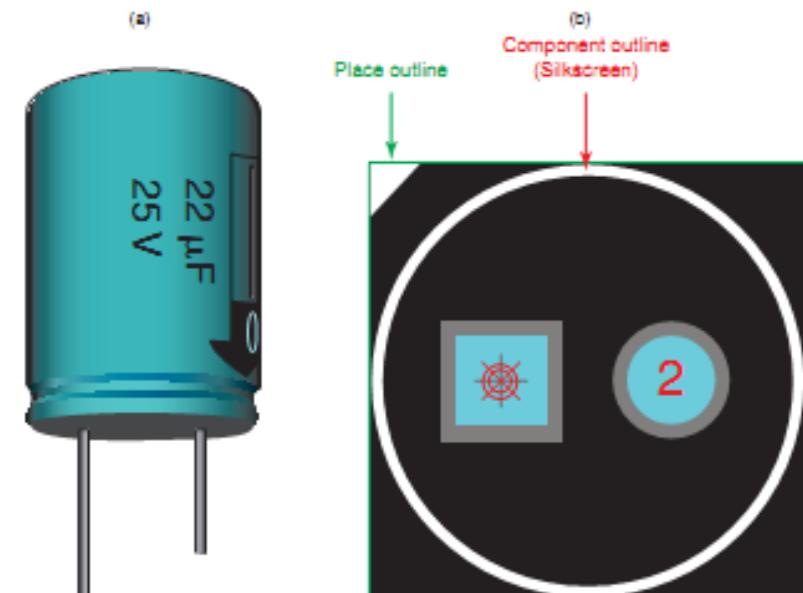


Figure 5-12 Radial-leaded through-hole device. (a) Axial-leaded capacitor. (b) Layout axial footprint

PCB Anatomy: Solder mask

- Solder mask or solder resist:
 - Thin polymer layer deposited on top and bottom layers
 - Protects outer layers from oxidation and prevents solder bridges
 - Allows for wave or reflow soldering of components
 - Holes are opened with photolithography wherever components will be soldered
 - Default color is green, but any other color is possible

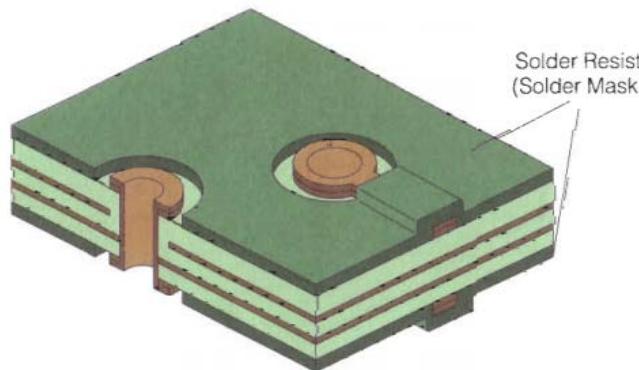


Illustration ML-14. Apply solder resist. The specified resist (either dry film, liquid photoimageable, or screen printed) is applied to the surfaces of the PCB or panel.

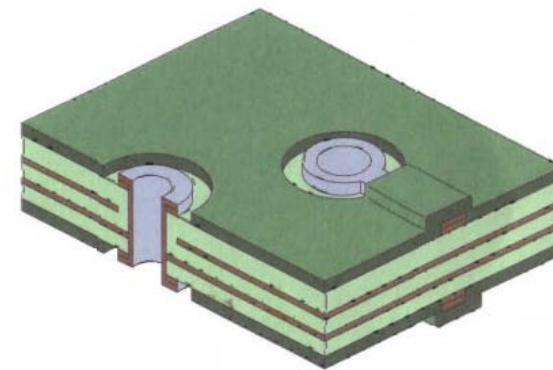
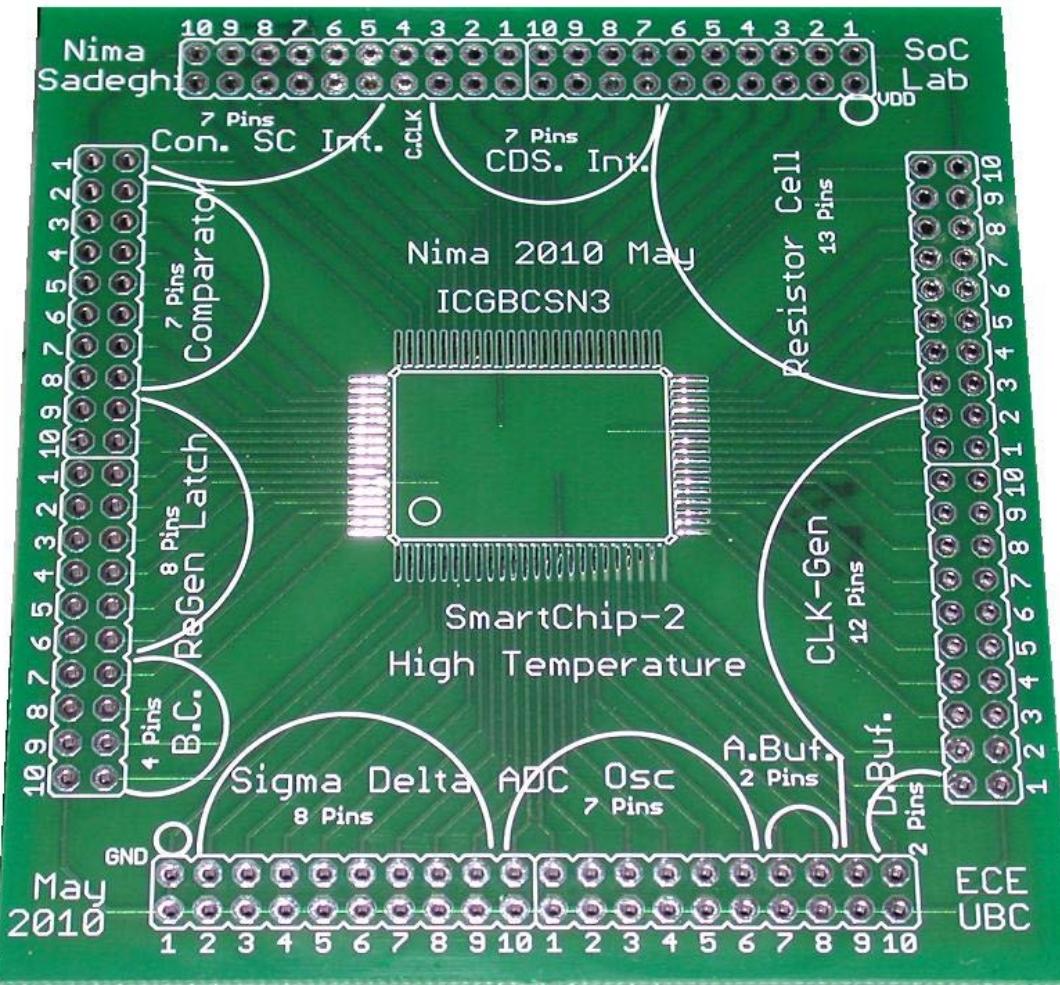


Illustration ML-15. Solder coat. Solder (tin/lead) is applied to the exposed copper areas, and the excess solder is removed.

Source: Printed Circuit Board Basics: An Introduction to the PCB Industry, by: Michael Flatt

PCB Anatomy: Legend / Silkscreen / Overlay



- Legend or silkscreen:
 - Applied on top of the solder resist
 - Can be applied to one or both outer layers
 - Default color is white but any other color is possible

Tip: add (Top) and (Bottom)

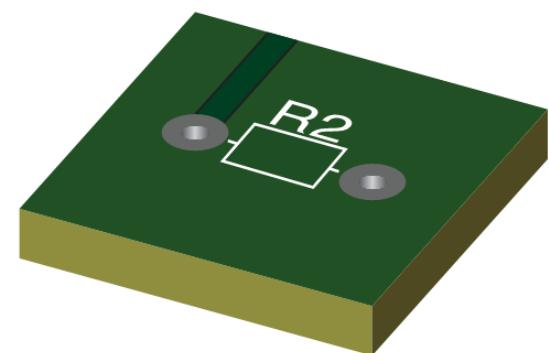
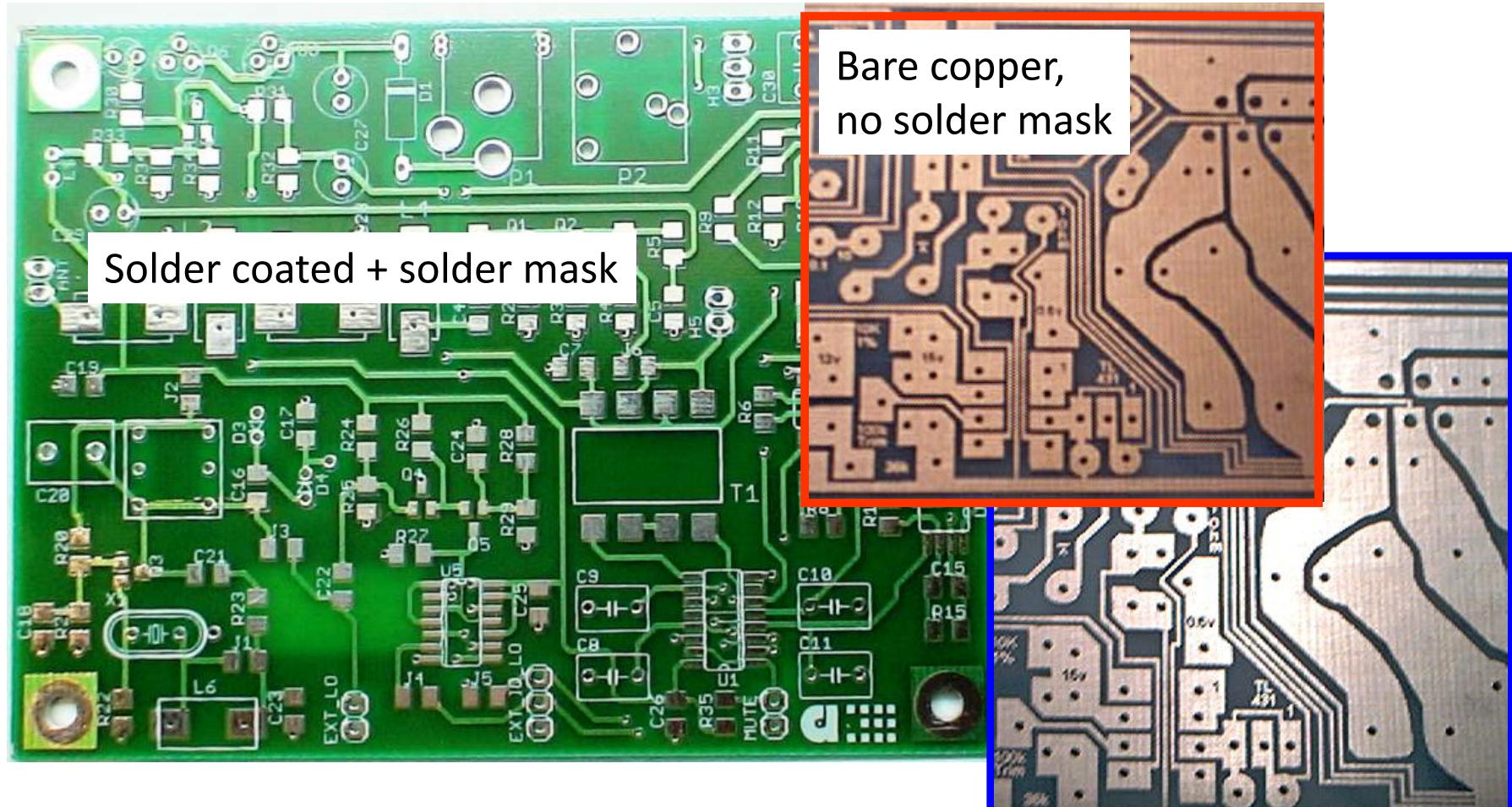


Figure 1-16 Final layers are the soldermask (green) and silk screen (white).

PCB Anatomy: Surface finishing / thinning



There are different types of finishes, eg:

HASL (tin), ENIG (Nickel and Gold), Silver immersion

Solder coated + no solder mask

PCB Anatomy: Mechanical Layers

- Multi-purpose layers
- E.g. Altium supports 32 Mechanical layers: M1 ... M32
- Typically
 - M1 Board outline
 - M2 PCB manufacturing info
 - M11-M12 Top and bottom layer dimensions
 - M13 Top layer 3D models and mechanical outlines
 - M14 Bottom layer 3D models and mechanical outlines
 - M15 Top layer assembly information
 - M16 Bottom layer assembly information

PCB Basic Terminology

- **Laminate / Substrate**
 - Material (FR4, Rogers)
 - Thickness (62-63mil, 16mm)
 - Prepeg, Core, Foil, Clad
 - Stack-up
- **Traces / tracks**
 - Width & gap
 - Ampacity
 - Characteristic impedance
- **Vias & Hole**
 - Types of vias
 - Plated vs non-plated holes
 - Thermal relief
 - Annular ring
- **Pads**
 - Multi-layer, single layer
 - Tear drop
- **Components /Parts**
 - Footprints
 - Symbols
 - Libraries
- **Layers**
 - Mechanical, board outline
 - Top metal, Bottom metal
 - Inner layers / Planes
 - Top / Bottom Solder Mask
 - Legend / Silkscreen / Top overlay
 - Top / Bottom pads
 - Multi-layer
- **Surface Finish**
 - HASL, ENIG
- **Fabrication CAM files**
 - Gerber, 274X
 - Excellon NC drill files