



1. Description

1.1. Project

Project Name	mcb_main
Board Name	custom
Generated with:	STM32CubeMX 6.3.0
Date	08/26/2021

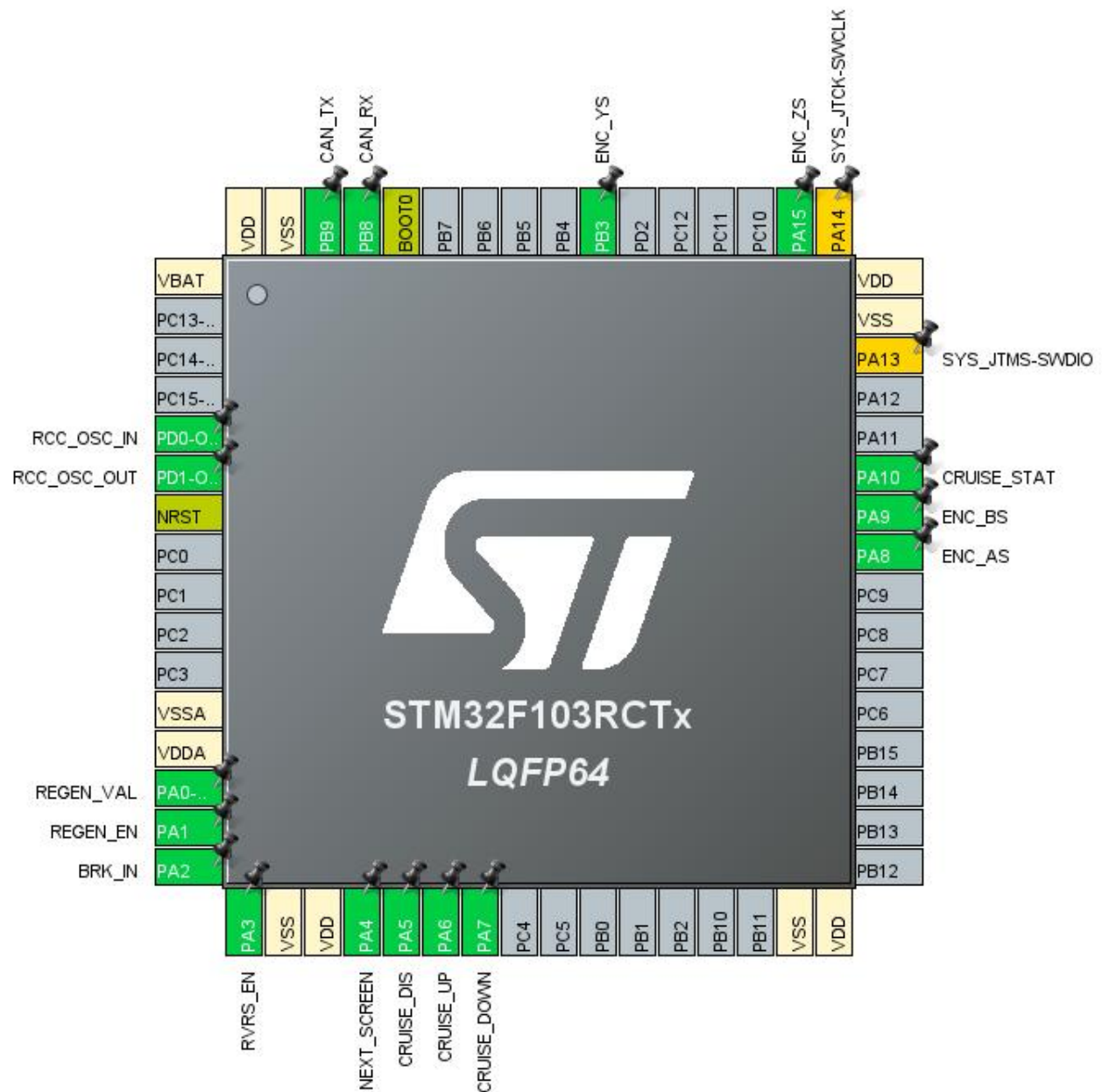
1.2. MCU

MCU Series	STM32F1
MCU Line	STM32F103
MCU name	STM32F103RCTx
MCU Package	LQFP64
MCU Pin number	64

1.3. Core(s) information

Core(s)	Arm Cortex-M3
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2. Pinout Configuration



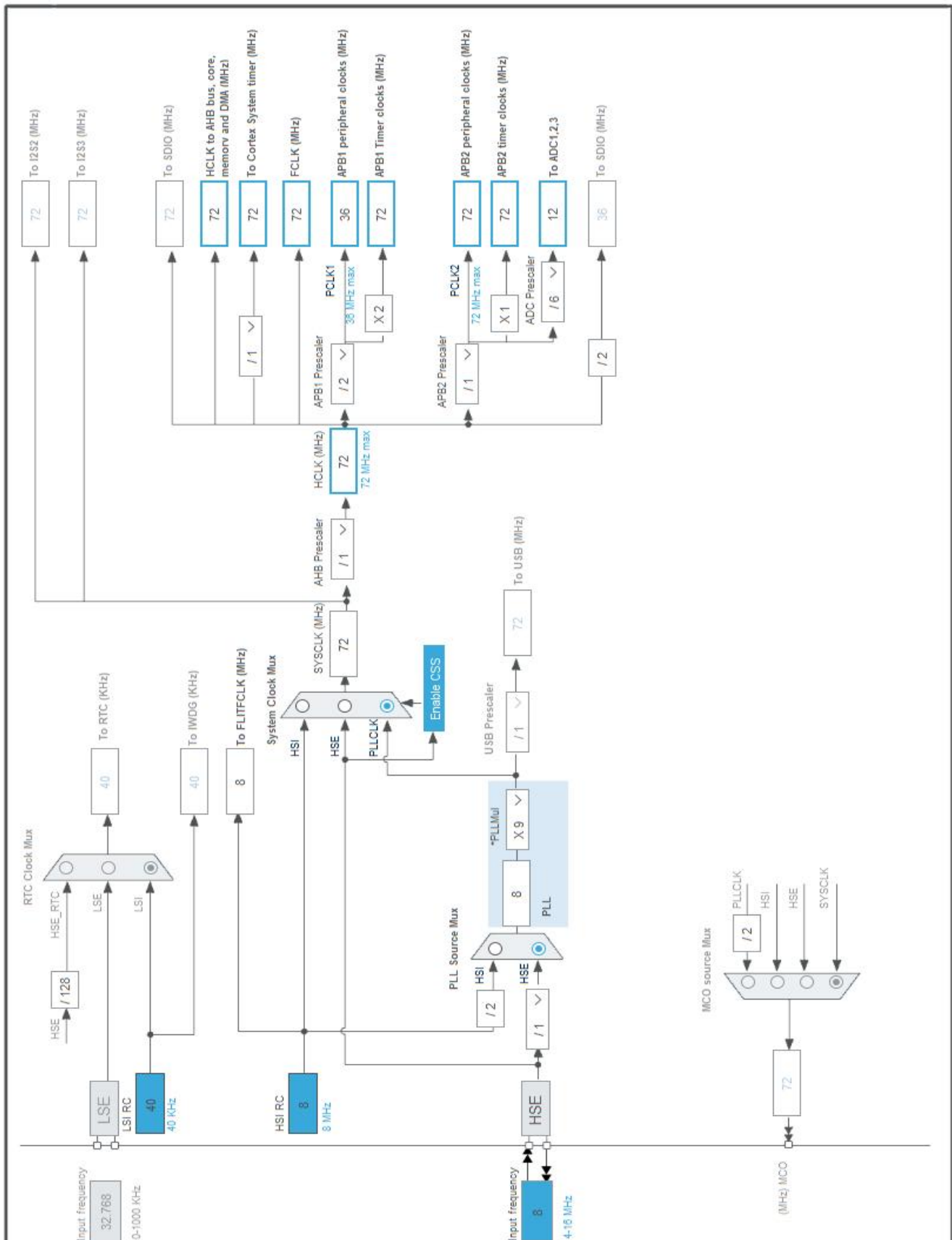
3. Pins Configuration

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
5	PD0-OSC_IN	I/O	RCC_OSC_IN	
6	PD1-OSC_OUT	I/O	RCC_OSC_OUT	
7	NRST	Reset		
12	VSSA	Power		
13	VDDA	Power		
14	PA0-WKUP	I/O	ADC2_IN0, ADC1_IN0	REGEN_VAL
15	PA1	I/O	GPIO_EXTI1	REGEN_EN
16	PA2	I/O	GPIO_EXTI2	BRK_IN
17	PA3	I/O	GPIO_EXTI3	RVRS_EN
18	VSS	Power		
19	VDD	Power		
20	PA4	I/O	GPIO_EXTI4	NEXT_SCREEN
21	PA5	I/O	GPIO_EXTI5	CRUISE_DIS
22	PA6	I/O	GPIO_EXTI6	CRUISE_UP
23	PA7	I/O	GPIO_EXTI7	CRUISE_DOWN
31	VSS	Power		
32	VDD	Power		
41	PA8 *	I/O	GPIO_Input	ENC_AS
42	PA9 *	I/O	GPIO_Input	ENC_BS
43	PA10 *	I/O	GPIO_Output	CRUISE_STAT
46	PA13 **	I/O	SYS_JTMS-SWDIO	
47	VSS	Power		
48	VDD	Power		
49	PA14 **	I/O	SYS_JTCK-SWCLK	
50	PA15 *	I/O	GPIO_Input	ENC_ZS
55	PB3 *	I/O	GPIO_Input	ENC_YS
60	BOOT0	Boot		
61	PB8	I/O	CAN_RX	
62	PB9	I/O	CAN_TX	
63	VSS	Power		
64	VDD	Power		

* The pin is affected with an I/O function

** The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	mcb_main
Project Folder	C:\Users\mihir\Desktop\firmware_v3\components\mcb\mcb_main
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_F1 V1.8.3
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	Yes
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	MX_DMA_Init	DMA
3	SystemClock_Config	RCC
4	MX_CAN_Init	CAN
5	MX_ADC1_Init	ADC1

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F1
Line	STM32F103
MCU	STM32F103RCTx
Datasheet	DS5792_Rev12

6.2. Parameter Selection

Temperature	25
Vdd	3.3

6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

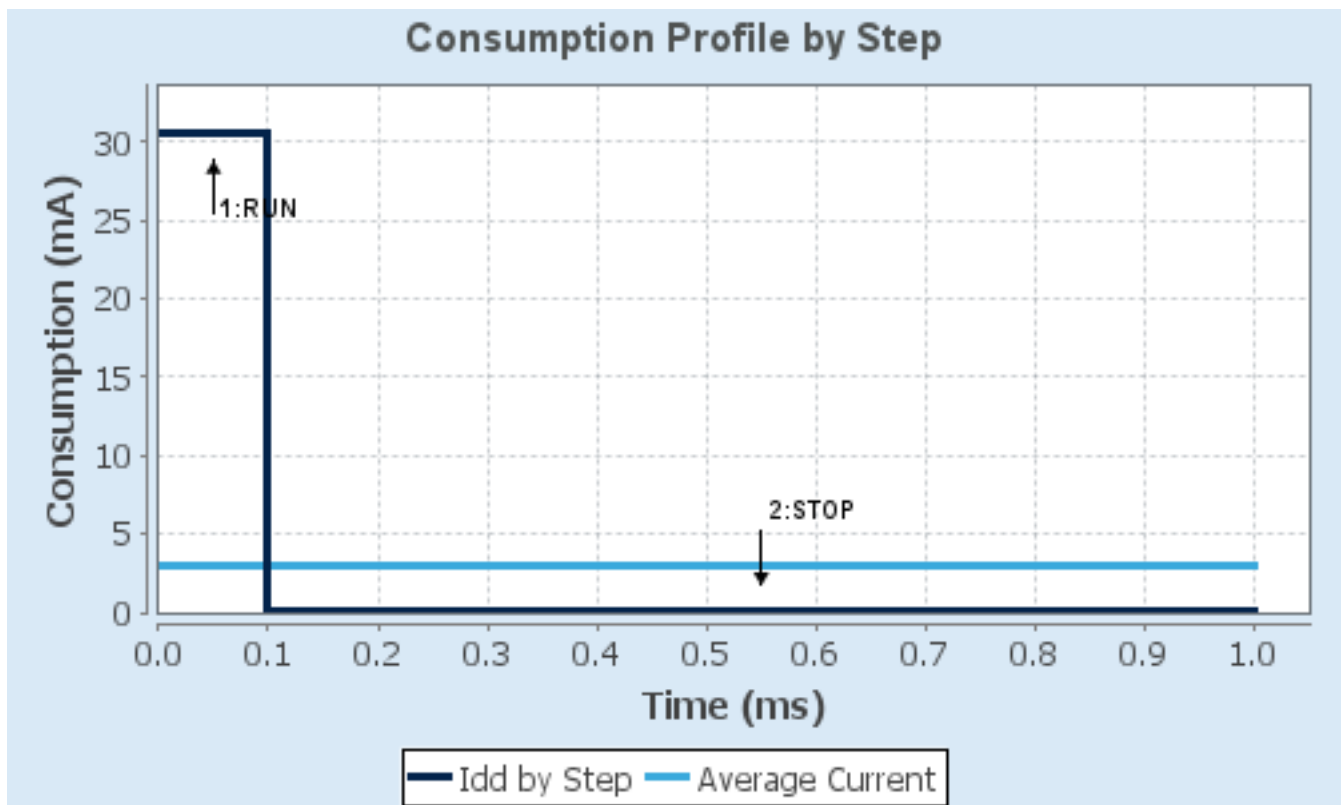
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.3	3.3
Voltage Source	Battery	Battery
Range	No Scale	No Scale
Fetch Type	FLASH	n/a
CPU Frequency	72 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator LP
Clock Source Frequency	8 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	30.5 mA	25 μ A
Duration	0.1 ms	0.9 ms
DMIPS	90.0	0.0
Ta Max	100.47	105
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	3.07 mA
Battery Life	1 month, 15 days, 15 hours	Average DMIPS	61.0 DMIPS

6.6. Chart



7. Peripherals and Middlewares Configuration

7.1. ADC1

mode: IN0

7.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode Independent mode

ADC_Settings:

Data Alignment Right alignment

Scan Conversion Mode Disabled

Continuous Conversion Mode **Enabled ***

Discontinuous Conversion Mode Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions Enable

Number Of Conversion 1

External Trigger Conversion Source Regular Conversion launched by software

Rank 1

Channel Channel 0

Sampling Time 1.5 Cycles

ADC_Injected_ConversionMode:

Enable Injected Conversions Disable

WatchDog:

Enable Analog WatchDog Mode false

7.2. CAN

mode: Activated

7.2.1. Parameter Settings:

Bit Timings Parameters:

Prescaler (for Time Quantum) 16

Time Quantum **444.44444444444446 ***

Time Quanta in Bit Segment 1 **13 Times ***

Time Quanta in Bit Segment 2 **4 Times ***

Time for one Bit **7999.99 ***

Baud Rate **125000 ***

ReSynchronization Jump Width 1 Time

Basic Parameters:

Time Triggered Communication Mode	Enable *
Automatic Bus-Off Management	Enable *
Automatic Wake-Up Mode	Enable *
Automatic Retransmission	Disable
Receive Fifo Locked Mode	Disable
Transmit Fifo Priority	Disable
Advanced Parameters:	
Operating Mode	Normal

7.3. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

7.3.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Prefetch Buffer	Enabled
Flash Latency(WS)	2 WS (3 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
HSE Startup Timeout Value (ms)	100
LSE Startup Timeout Value (ms)	5000

7.4. SYS

Debug: No Debug

Timebase Source: TIM8

7.5. FREERTOS

Interface: CMSIS_V2

7.5.1. Config parameters:

API:

FreeRTOS API	CMSIS v2
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Versions:

FreeRTOS version	10.0.1
CMSIS-RTOS version	2.00

Kernel settings:

USE_PREEMPTION	Enabled
CPU_CLOCK_HZ	SystemCoreClock
TICK_RATE_HZ	1000
MAX_PRIORITIES	56
MINIMAL_STACK_SIZE	128
MAX_TASK_NAME_LEN	16
USE_16_BIT_TICKS	Disabled
IDLE_SHOULD_YIELD	Enabled
USE_MUTEXES	Enabled
USE_RECURSIVE_MUTEXES	Enabled
USE_COUNTING_SEMAPHORES	Enabled
QUEUE_REGISTRY_SIZE	8
USE_APPLICATION_TASK_TAG	Disabled
ENABLE_BACKWARD_COMPATIBILITY	Enabled
USE_PORT_OPTIMISED_TASK_SELECTION	Disabled
USE_TICKLESS_IDLE	Disabled
USE_TASK_NOTIFICATIONS	Enabled
RECORD_STACK_HIGH_ADDRESS	Disabled

Memory management settings:

Memory Allocation	Dynamic / Static
TOTAL_HEAP_SIZE	3072
Memory Management scheme	heap_4

Hook function related definitions:

USE_IDLE_HOOK	Disabled
USE_TICK_HOOK	Disabled
USE_MALLOC_FAILED_HOOK	Disabled
USE_DAEMON_TASK_STARTUP_HOOK	Disabled
CHECK_FOR_STACK_OVERFLOW	Disabled

Run time and task stats gathering related definitions:

GENERATE_RUN_TIME_STATS	Disabled
USE_TRACE_FACILITY	Enabled
USE_STATS_FORMATTING_FUNCTIONS	Disabled

Co-routine related definitions:

USE_CO_ROUTINES	Disabled
MAX_CO_ROUTINE_PRIORITIES	2

Software timer definitions:

USE_TIMERS	Enabled
TIMER_TASK_PRIORITY	2
TIMER_QUEUE_LENGTH	10
TIMER_TASK_STACK_DEPTH	256

Interrupt nesting behaviour configuration:

LIBRARY_LOWEST_INTERRUPT_PRIORITY	15
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LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY 5

7.5.2. Include parameters:

Include definitions:

vTaskPrioritySet	Enabled
uxTaskPriorityGet	Enabled
vTaskDelete	Enabled
vTaskCleanUpResources	Disabled
vTaskSuspend	Enabled
vTaskDelayUntil	Enabled
vTaskDelay	Enabled
xTaskGetSchedulerState	Enabled
xTaskResumeFromISR	Enabled
xQueueGetMutexHolder	Enabled
xSemaphoreGetMutexHolder	Disabled
pcTaskGetTaskName	Disabled
uxTaskGetStackHighWaterMark	Enabled
xTaskGetCurrentTaskHandle	Disabled
eTaskGetState	Enabled
xEventGroupSetBitFromISR	Disabled
xTimerPendFunctionCall	Enabled
xTaskAbortDelay	Disabled
xTaskGetHandle	Disabled

7.5.3. Advanced settings:

Newlib settings (see parameter description first):

USE_NEWLIB_REENTRANT Disabled

Project settings (see parameter description first):

Use FW pack heap file Enabled

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA0-WKUP	ADC1_IN0	Analog mode	n/a	n/a	REGEN_VAL
CAN	PB8	CAN_RX	Input mode	No pull-up and no pull-down	n/a	
	PB9	CAN_TX	Alternate Function Push Pull	n/a	High *	
RCC	PD0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PD1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
Single Mapped Signals	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
GPIO	PA1	GPIO_EXTI1	External Interrupt Mode with Rising/Falling edge	Pull-down *	n/a	REGEN_EN
	PA2	GPIO_EXTI2	External Interrupt Mode with Rising/Falling edge	Pull-down *	n/a	BRK_IN
	PA3	GPIO_EXTI3	External Interrupt Mode with Rising/Falling edge	Pull-down *	n/a	RVRS_EN
	PA4	GPIO_EXTI4	External Interrupt Mode with Rising edge trigger detection	Pull-down *	n/a	NEXT_SCREEN
	PA5	GPIO_EXTI5	External Interrupt Mode with Rising edge trigger detection	Pull-down *	n/a	CRUISE_DIS
	PA6	GPIO_EXTI6	External Interrupt Mode with Rising edge trigger detection	Pull-down *	n/a	CRUISE_UP
	PA7	GPIO_EXTI7	External Interrupt Mode with Rising edge trigger detection	Pull-down *	n/a	CRUISE_DOWN
	PA8	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	ENC_AS
	PA9	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	ENC_BS
	PA10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	CRUISE_STAT
	PA15	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	ENC_ZS
	PB3	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	ENC_YS

8.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC1	DMA1_Channel1	Peripheral To Memory	Low

ADC1: DMA1_Channel1 DMA request Settings:

Mode: Normal
Peripheral Increment: Disable
Memory Increment: **Enable ***
Peripheral Data Width: Half Word
Memory Data Width: Half Word

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	15	0
System tick timer	true	15	0
EXTI line1 interrupt	true	5	0
EXTI line2 interrupt	true	5	0
EXTI line3 interrupt	true	5	0
EXTI line4 interrupt	true	5	0
DMA1 channel1 global interrupt	true	5	0
EXTI line[9:5] interrupts	true	5	0
TIM8 update interrupt	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1 and ADC2 global interrupts	unused		
USB high priority or CAN TX interrupts	unused		
USB low priority or CAN RX0 interrupts	unused		
CAN RX1 interrupt	unused		
CAN SCE interrupt	unused		

8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Prefetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	false	false
Debug monitor	false	true	false
Pendable request for system service	false	false	false
System tick timer	false	false	true

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
EXTI line1 interrupt	false	true	true
EXTI line2 interrupt	false	true	true
EXTI line3 interrupt	false	true	true
EXTI line4 interrupt	false	true	true
DMA1 channel1 global interrupt	false	true	true
EXTI line[9:5] interrupts	false	true	true
TIM8 update interrupt	false	true	true

* User modified value

9. System Views

9.1. Category view

9.1.1. Current

Middleware

FREERTOS 

System Core

Analog

Timers

Connectivity

Multimedia

Computing

DMA 

ADC1 

CAN 

GPIO 

IIVIC 

RCC 

SYS 

10. Docs & Resources

Type	Link
Datasheet	http://www.st.com/resource/en/datasheet/CD00191185.pdf
Reference manual	http://www.st.com/resource/en/reference_manual/CD00171190.pdf
Programming manual	http://www.st.com/resource/en/programming_manual/CD00228163.pdf
Programming manual	http://www.st.com/resource/en/programming_manual/CD00283419.pdf
Errata sheet	http://www.st.com/resource/en/errata_sheet/CD00197763.pdf
Application note	http://www.st.com/resource/en/application_note/CD00160362.pdf
Application note	http://www.st.com/resource/en/application_note/CD00164185.pdf
Application note	http://www.st.com/resource/en/application_note/CD00167594.pdf
Application note	http://www.st.com/resource/en/application_note/CD00200423.pdf
Application note	http://www.st.com/resource/en/application_note/CD00211314.pdf
Application note	http://www.st.com/resource/en/application_note/CD00249778.pdf
Application note	http://www.st.com/resource/en/application_note/CD00259245.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264321.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264342.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00024853.pdf
Application note	http://www.st.com/resource/en/application_note/DM00032987.pdf
Application note	http://www.st.com/resource/en/application_note/DM00033267.pdf
Application note	http://www.st.com/resource/en/application_note/DM00033344.pdf
Application note	http://www.st.com/resource/en/application_note/DM00042534.pdf
Application note	http://www.st.com/resource/en/application_note/DM00052530.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073742.pdf
Application note	http://www.st.com/resource/en/application_note/DM00080497.pdf
Application note	http://www.st.com/resource/en/application_note/DM00129215.pdf

Application note http://www.st.com/resource/en/application_note/DM00156964.pdf
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Application note http://www.st.com/resource/en/application_note/DM00209695.pdf
Application note http://www.st.com/resource/en/application_note/DM00220769.pdf
Application note http://www.st.com/resource/en/application_note/DM00236305.pdf
Application note http://www.st.com/resource/en/application_note/DM00257177.pdf
Application note http://www.st.com/resource/en/application_note/DM00272912.pdf
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Application note http://www.st.com/resource/en/application_note/DM00315319.pdf
Application note http://www.st.com/resource/en/application_note/DM00325582.pdf
Application note http://www.st.com/resource/en/application_note/DM00327191.pdf
Application note http://www.st.com/resource/en/application_note/DM00354244.pdf
Application note http://www.st.com/resource/en/application_note/DM00380469.pdf
Application note http://www.st.com/resource/en/application_note/DM00395696.pdf
Application note http://www.st.com/resource/en/application_note/DM00493651.pdf
Application note http://www.st.com/resource/en/application_note/DM00536349.pdf
Application note http://www.st.com/resource/en/application_note/DM00725181.pdf