1.2-V, 12-/10-/8-BIT, 200-KSPS/100-KSPS, MICRO-POWER, MINIATURE ANALOG-TO-DIGITAL CONVERTER WITH SERIAL INTERFACE

FEATURES

- **Single 1.2-V to 3.6-V Supply Operation**
- **High Throughput**
  - **– 200/240/280KSPS for 12/10/8-Bit $V_{DD} \geq 1.6$ V**
  - **– 100/120/140KSPS for 12/10/8-Bit $V_{DD} \geq 1.2$ V**
- **±1.5LSB INL, 12-Bit NMC (ADS7866)**
- **71 dB SNR, –83 dB THD at f_{IN} = 30 kHz (ADS7866)**
- **Synchronized Conversion with SCLK**
- **SPI Compatible Serial Interface**
- **No Pipeline Delays**
- **Low Power**
  - **– 1.39 mW Typ at 200 KSPS, V_{DD} = 3.6 V**
  - **– 0.39 mW Typ at 200 KSPS, V_{DD} = 1.6 V**
  - **– 0.22 mW Typ at 100 KSPS, V_{DD} = 1.2 V**
- **Auto Power-Down: 8 nA Typ, 300 nA Max**
- **0 V to V_{DD} Unipolar Input Range**
- **6-Pin SOT-23 Package**

APPLICATIONS

- **Battery Powered Systems**
- **Isolated Data Acquisition**
- **Medical Instruments**
- **Portable Communication**
- **Portable Data Acquisition Systems**
- **Automatic Test Equipment**

DESCRIPTION

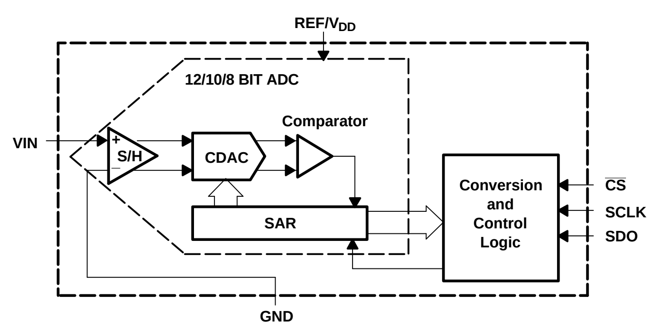
The ADS7866/67/68 are low power, miniature, 12/10/8-bit A/D converters each with a unipolar, single-ended input. These devices can operate from a single 1.6 V to 3.6 V supply with a 200-KSPS throughput for ADS7866. In addition, these devices can maintain at least a 100-KSPS throughput with a supply as low as 1.2 V.

The sampling, conversion, and activation of digital output SDO are initiated on the falling edge of $\overline{CS}$. The serial clock SCLK is used for controlling the conversion rate and shifting data out of the converter. Furthermore, SCLK provides a mechanism to allow digital host processors to synchronize with the converter. These converters interface with micro-processors or DSPs through a high-speed SPI compatible serial interface. There are no pipeline delays associated with the device.

The minimum conversion time is determined by the frequency of the serial clock input, SCLK, while the maximum frequency of SCLK is determined by the minimum sampling time required to charge the input capacitance to 12/10/8-bit accuracy for the ADS7866/67/68, respectively. The maximum throughput is determined by how often a conversion is initiated when the minimum sampling time is met and the maximum SCLK frequency is used. Each device automatically powers down after each conversion, which allows each device to save power when the throughput is reduced while using the maximum SCLK frequency.

The converter reference is taken internally from the supply. Hence, the analog input range for these devices is 0 V to V_{DD}.

These devices are available in a 6-pin SOT-23 package and are characterized over the industrial –40°C to 85°C temperature range.



Micro-Power Miniature SAR Converter Family

RESOLUTION/SPEED	< 200 KSPS	1 MSPS – 1.25 MSPS
12-Bit	ADS7866 (1.2 V_{DD} to 3.6 V_{DD})	ADS7886 (2.35 V_{DD} to 5.25 V_{DD})
10-Bit	ADS7867 (1.2 V_{DD} to 3.6 V_{DD})	ADS7887 (2.35 V_{DD} to 5.25 V_{DD})
8-Bit	ADS7868 (1.2 V_{DD} to 3.6 V_{DD})	ADS7888 (2.35 V_{DD} to 5.25 V_{DD})

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1)

MODEL	MAXIMUM INTEGRAL LINEARITY (LSB)	MAXIMUM DIFFERENTIAL LINEARITY (LSB)	NO MISSING CODES RESOLULTION (BIT)	PACKAGE TYPE	PACKAGE MARKING (SYMBOL)	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS7866I	±1.5	–1/+1.5	12	SOT23-6	A66Y	DBV	–40°C to 85°C	ADS7866IDBVT	Small tape and reel, 250
ADS7866I	±1.5	–1/+1.5	12	SOT23-6	A66Y	DBV	–40°C to 85°C	ADS7866IDBVR	Tape and reel, 3000
ADS7867I	±0.5	±0.5	10	SOT23-6	A67Y	DBV	–40°C to 85°C	ADS7867IDBVT	Small tape and reel, 250
ADS7867I	±0.5	±0.5	10	SOT23-6	A67Y	DBV	–40°C to 85°C	ADS7867IDBVR	Tape and reel, 3000
ADS7868I	±0.5	±0.5	8	SOT23-6	A68Y	DBV	–40°C to 85°C	ADS7868IDBVT	Small tape and reel, 250
ADS7868I	±0.5	±0.5	8	SOT23-6	A68Y	DBV	–40°C to 85°C	ADS7868IDBVR	Tape and reel, 3000

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

			RATING
	V_{DD} to GND		–0.3 V to 4.0 V
	Analog input voltage to GND		–0.3 V to V_{DD} + 0.3 V
	Digital input voltage to GND		–0.3 V to 4.0 V
	Digital output voltage to GND		–0.3 V to V_{DD} + 0.3 V
T_A	Operating free-air temperature range		–40°C to 85°C
$T_{STORAGE}$	Storage temperature range		–65°C to 150°C
T_J	Junction temperature		150°C
	SOT-23 Package	θ_{JA} Thermal impedance	110.9°C/W
		θ_{JC} Thermal impedance	22.31°C/W
	Lead temperature, soldering	Vapor phase (10–40 sec)	250°C
		Infrared (10–30 sec)	260°C
	ESD		3 kV

SPECIFICATIONS, ADS7866

At –40°C to 85°C, f_{SAMPLE} = 200 KSPS and f_{SCLK} = 3.4 MHz if 1.6 V ≤ V_{DD} ≤ 3.6 V; f_{SAMPLE} = 100 KSPS and f_{SCLK} = 1.7 MHz if 1.2 V ≤ V_{DD} < 1.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYSTEM PERFORMANCE						
	Resolution			12		Bits
	No missing codes		12			Bits
	Integral linearity		–1.5		1.5	LSB(1)
	Differential linearity		–1		1.5	LSB
	Offset error(2)	1.2 V ≤ V_{DD} < 1.6 V	–2		2	LSB
		1.6 V ≤ V_{DD} ≤ 3.6 V	–3		3	
	Gain error(3)	1.2 V ≤ V_{DD} < 1.6 V	–2		2	LSB
		1.6 V ≤ V_{DD} ≤ 3.6 V	–2		2	
	Total unadjusted error(4)	1.2 V ≤ V_{DD} < 1.6 V	–2.5		2.5	LSB
		1.6 V ≤ V_{DD} ≤ 3.6 V	–3.5		3.5	
SAMPLING DYNAMICS (See Timing Characteristics Section)						
$t_{CONVERT}$	Conversion time	f_{SCLK} = 3.4 MHz, 13 SCLK cycles	3.82			µs
t_{SAMPLE}	Acquisition time	f_{SCLK} = 3.4 MHz, 1.6 V ≤ V_{DD} ≤ 3.6 V	0.64			µs
f_{SAMPLE}	Throughput rate	f_{SCLK} = 3.4 MHz, 1.6 V ≤ V_{DD} ≤ 3.6 V			200	KSPS
	Aperture delay			10		ns
	Aperture jitter			40		ps
DYNAMIC CHARACTERISTICS						
SINAD	Signal-to-noise and distortion	f_{IN} = 30 kHz, 1.2 V ≤ V_{DD} < 1.6 V		68		dB
		f_{IN} = 30 kHz, 1.6 V ≤ V_{DD} ≤ 3.6 V	69	70		
SNR	Signal-to-noise ratio	f_{IN} = 30 kHz, 1.2 V ≤ V_{DD} < 1.6 V		70		dB
		f_{IN} = 30 kHz, 1.6 V ≤ V_{DD} ≤ 3.6 V	70	71		
THD	Total harmonic distortion(5)	f_{IN} = 30 kHz, 1.2 V ≤ V_{DD} < 1.6 V		–70		dB
		f_{IN} = 30 kHz, 1.6 V ≤ V_{DD} ≤ 3.6 V		–83		
SFDR	Spurious free dynamic range	f_{IN} = 30 kHz, 1.2 V ≤ V_{DD} < 1.6 V		75		dB
		f_{IN} = 30 kHz, 1.6 V ≤ V_{DD} ≤ 3.6 V		85		
	Full-power bandwidth(6)	At 0.1 dB, 1.2 V ≤ V_{DD} < 1.6 V		2		MHz
		At 0.1 dB, 1.6 V ≤ V_{DD} ≤ 3.6 V		4		
		At 3 dB, 1.2 V ≤ V_{DD} < 1.6 V		3		
		At 3 dB, 1.6 V ≤ V_{DD} ≤ 3.6 V		8		
ANALOG INPUT						
	Full-scale input span(7)	VIN – GND	0		V_{DD}	V
C_S	Input capacitance			12		pF
	Input leakage current		–1		1	µA
DIGITAL INPUT						
	Logic family , CMOS					
V_{IH}	Input logic high level	1.2 V ≤ V_{DD} < 1.6 V	0.7×V_{DD}		3.6	V
		1.6 V ≤ V_{DD} < 1.8 V	0.7×V_{DD}		3.6	
		1.8 V ≤ V_{DD} < 2.5 V	0.7×V_{DD}		3.6	
		2.5 V ≤ V_{DD} ≤ 3.6 V	2		3.6	

(1) LSB = Least Significant BIt
(2) The difference in the first code transition 000...000 to 000...001 from the ideal value of GND + 1 LSB.
(3) The difference in the last code transition 011...111 to 111...111 from the ideal value of V_{DD} - 1 LSB with the offset error removed.
(4) The absolute difference from the ideal transfer function of the converter. This specification is similar to INL error except the effects of offset error and gain error are included.
(5) The 2nd through 10th harmonics are used to determine THD.
(6) Input frequency where the amplitude of the digitized signal has decreased by 0.1 dB or 3 dB.
(7) Ideal input span which does not include gain or offset errors.

SPECIFICATIONS, ADS7866 (continued)

At –40°C to 85°C, f_{SAMPLE} = 200 KSPS and f_{SCLK} = 3.4 MHz if 1.6 V ≤ V_{DD} ≤ 3.6 V; f_{SAMPLE} = 100 KSPS and f_{SCLK} = 1.7 MHz if 1.2 V ≤ V_{DD} < 1.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IL}	Input logic low level	1.2 V ≤ V_{DD} < 1.6 V		–0.2		0.2×V_{DD}	V
		1.6 V ≤ V_{DD} < 1.8 V		–0.2		0.2×V_{DD}	
		1.8 V ≤ V_{DD} < 2.5 V		–0.2		0.3×V_{DD}	
		2.5 V ≤ V_{DD} ≤ 3.6 V		–0.2		0.8	
I_{SCLK}	SCLK pin leakage current	Digital input = 0 V or V_{DD}		–1	0.02	1	µA
I_{CS}	$\overline{CS}$ pin leakage current				±1		µA
C_{IN}	Digital input pin capacitance					10	pF
DIGITAL OUTPUT							
V_{OH}	Output logic high level	I_{SOURCE} = 200 µA		V_{DD}–0.2		V_{DD}	V
V_{OL}	Output logic low level	I_{SINK} = 200 µA		0		0.2	V
I_{SDO}	SDO pin leakage current	Floating output		–1		1	µA
C_{OUT}	Digital output pin capacitance	Floating output				10	pF
	Data format, straight binary						
POWER SUPPLY REQUIREMENTS							
V_{DD}	Supply voltage			1.2		3.6	V
I_{DD}	Supply current, normal operation	Digital inputs = 0 V or V_{DD}	f_{SAMPLE} = 200 KSPS, f_{SCLK} = 3.4 MHz, V_{DD} = 3.6 V		385	500	µA
			f_{SAMPLE} = 100 KSPS, f_{SCLK} = 3.4 MHz, V_{DD} = 3.6 V		193		
			f_{SAMPLE} = 50 KSPS, f_{SCLK} = 3.4 MHz, V_{DD} = 3.6 V		97		
			f_{SAMPLE} = 20 KSPS, f_{SCLK} = 3.4 MHz, V_{DD} = 3.6 V		39		
			f_{SAMPLE} = 200 KSPS, f_{SCLK} = 3.4 MHz, V_{DD} = 3 V		340		µA
			f_{SAMPLE} = 100 KSPS, f_{SCLK} = 3.4 MHz, V_{DD} = 3 V		170		
			f_{SAMPLE} = 50 KSPS, f_{SCLK} = 3.4 MHz, V_{DD} = 3 V		85		
			f_{SAMPLE} = 20 KSPS, f_{SCLK} = 3.4 MHz, V_{DD} = 3 V		35		
			f_{SAMPLE} = 200 KSPS, f_{SCLK} = 3.4 MHz, V_{DD} = 2.5 V		305		µA
			f_{SAMPLE} = 100 KSPS, f_{SCLK} = 3.4 MHz, V_{DD} = 2.5 V		153		
			f_{SAMPLE} = 50 KSPS, f_{SCLK} = 3.4 MHz, V_{DD} = 2.5 V		77		
			f_{SAMPLE} = 20 KSPS, f_{SCLK} = 3.4 MHz, V_{DD} = 2.5 V		31		
			f_{SAMPLE} = 200 KSPS, f_{SCLK} = 3.4 MHz, V_{DD} = 1.8 V		256		µA
			f_{SAMPLE} = 100 KSPS, f_{SCLK} = 3.4 MHz, V_{DD} = 1.8 V		128		
			f_{SAMPLE} = 50 KSPS, f_{SCLK} = 3.4 MHz, V_{DD} = 1.8 V		65		
			f_{SAMPLE} = 20 KSPS, f_{SCLK} = 3.4 MHz, V_{DD} = 1.8 V		26		
			f_{SAMPLE} = 200 KSPS, f_{SCLK} = 3.4 MHz, V_{DD} = 1.6 V		241	330	µA
			f_{SAMPLE} = 100 KSPS, f_{SCLK} = 3.4 MHz, V_{DD} = 1.6 V		121		
			f_{SAMPLE} = 50 KSPS, f_{SCLK} = 3.4 MHz, V_{DD} = 1.6 V		61		
			f_{SAMPLE} = 20 KSPS, f_{SCLK} = 3.4 MHz, V_{DD} = 1.6 V		25		
			f_{SAMPLE} = 100 KSPS, f_{SCLK} = 1.7 MHz, V_{DD} = 1.2 V		186	250	µA
			f_{SAMPLE} = 50 KSPS, f_{SCLK} = 1.7 MHz, V_{DD} = 1.2 V		93		
			f_{SAMPLE} = 20 KSPS, f_{SCLK} = 1.7 MHz, V_{DD} = 1.2 V		37		
I_{DD}	Power-down mode	SCLK on or off			0.008	0.3	µA
POWER DISSIPATION							
	Normal operation	f_{SAMPLE} = 200 KSPS, f_{SCLK} = 3.4 MHz, V_{DD} = 3.6 V			1.39	1.80	mW
		f_{SAMPLE} = 200 KSPS, f_{SCLK} = 3.4 MHz, V_{DD} = 1.6 V			0.39	0.53	
		f_{SAMPLE} = 100 KSPS, f_{SCLK} = 1.7 MHz, V_{DD} = 1.2 V			0.22	0.3	
	Power-down mode	SCLK on or off, V_{DD} = 3.6 V			1.08		µW
TEMPERATURE RANGE							
	Specified performance			–40		85	°C

SPECIFICATIONS, ADS7867

At –40°C to 85°C, f_{SAMPLE} = 240 KSPS and f_{SCLK} = 3.4 MHz if 1.6 V ≤ V_{DD} ≤ 3.6 V; f_{SAMPLE} = 120 KSPS and f_{SCLK} = 1.7 MHz if 1.2 V ≤ V_{DD} < 1.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYSTEM PERFORMANCE						
	Resolution			10		Bits
	No missing codes		10			Bits
	Integral linearity		–0.5		0.5	LSB[1]
	Differential linearity		–0.5		0.5	LSB
	Offset error[2]	1.2 V ≤ V_{DD} < 1.6 V	–0.75		0.75	LSB
		1.6 V ≤ V_{DD} ≤ 3.6 V	–1		1	
	Gain error[3]	1.2 V ≤ V_{DD} < 1.6 V	–0.5		0.5	LSB
		1.6 V ≤ V_{DD} ≤ 3.6 V	–0.5		0.5	
	Total unadjusted error[4]	1.2 V ≤ V_{DD} < 1.6 V	–2		2	LSB
		1.6 V ≤ V_{DD} ≤ 3.6 V	–2		2	
SAMPLING DYNAMICS (See Timing Characteristics Section)						
$t_{CONVERT}$	Conversion time	f_{SCLK} = 3.4 MHz, 11 SCLK cycles	3.235			µs
t_{SAMPLE}	Acquisition time	f_{SCLK} = 3.4 MHz, 1.6 V ≤ V_{DD} ≤ 3.6 V	0.64			µs
f_{SAMPLE}	Throughput rate	f_{SCLK} = 3.4 MHz, 1.6 V ≤ V_{DD} ≤ 3.6 V			240	KSPS
	Aperture delay			10		ns
	Aperture jitter			40		ps
DYNAMIC CHARACTERISTICS						
SINAD	Signal-to-noise and distortion	f_{SAMPLE} = 100 KSPS, f_{IN} = 30 kHz, 1.2 V ≤ V_{DD} < 1.6 V		61		dB
		f_{SAMPLE} = 200 KSPS, f_{IN} = 30 kHz, 1.6 V ≤ V_{DD} ≤ 3.6 V	61	61.7		
SNR	Signal-to-noise ratio	f_{SAMPLE} = 100 KSPS, f_{IN} = 30 kHz, 1.2 V ≤ V_{DD} < 1.6 V		61.5		dB
		f_{SAMPLE} = 200 KSPS, f_{IN} = 30 kHz, 1.6 V ≤ V_{DD} ≤ 3.6 V		61.8		
THD	Total harmonic distortion[5]	f_{SAMPLE} = 100 KSPS, f_{IN} = 30 kHz, 1.2 V ≤ V_{DD} < 1.6 V		-68		dB
		f_{SAMPLE} = 200 KSPS, f_{IN} = 30 kHz, 1.6 V ≤ V_{DD} ≤ 3.6 V		-78	-72	
SFDR	Spurious free dynamic range	f_{SAMPLE} = 100 KSPS, f_{IN} = 30 kHz, 1.2 V ≤ V_{DD} < 1.6 V		73		dB
		f_{SAMPLE} = 200 KSPS, f_{IN} = 30 kHz, 1.6 V ≤ V_{DD} ≤ 3.6 V	74	80		
	Full-power bandwidth[6]	At 0.1 dB, 1.2 V ≤ V_{DD} < 1.6 V		2		MHz
		At 0.1 dB, 1.6 V ≤ V_{DD} ≤ 3.6 V		4		
		At 3 dB, 1.2 V ≤ V_{DD} < 1.6 V		3		
		At 3 dB, 1.6 V ≤ V_{DD} ≤ 3.6 V		8		
ANALOG INPUT						
	Full-scale input span[7]	VIN – GND	0		V_{DD}	V
C_S	Input capacitance			12		pF
	Input leakage current		–1		1	µA
DIGITAL INPUT						
	Logic family, CMOS					
V_{IH}	Input logic high level	1.2 V ≤ V_{DD} < 1.6 V	0.7×V_{DD}		3.6	V
		1.6 V ≤ V_{DD} < 1.8 V	0.7×V_{DD}		3.6	
		1.8 V ≤ V_{DD} < 2.5 V	0.7×V_{DD}		3.6	
		2.5 V ≤ V_{DD} ≤ 3.6 V	2		3.6	

(1) LSB = Least Significant BIt
(2) The difference in the first code transition 000...000 to 000...001 from the ideal value of GND + 1 LSB.
(3) The difference in the last code transition 011...111 to 111...111 from the ideal value of V_{DD} - 1 LSB with the offset error removed.
(4) The absolute difference from the ideal transfer function of the converter. This specification is similar to INL error except the effects of offset error and gain error are included.
(5) The 2nd through 10th harmonics are used to determine THD.
(6) Input frequency where the amplitude of the digitized signal has decreased by 0.1 dB or 3 dB.
(7) Ideal input span which does not include gain or offset errors.

SPECIFICATIONS, ADS7867 (continued)

At –40°C to 85°C, f_{SAMPLE} = 240 KSPS and f_{SCLK} = 3.4 MHz if 1.6 V ≤ V_{DD} ≤ 3.6 V; f_{SAMPLE} = 120 KSPS and f_{SCLK} = 1.7 MHz if 1.2 V ≤ V_{DD} < 1.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IL}	Input logic low level	1.2 V ≤ V_{DD} < 1.6 V		–0.2		0.2×V_{DD}	V
		1.6 V ≤ V_{DD} < 1.8 V		–0.2		0.2×V_{DD}	
		1.8 V ≤ V_{DD} < 2.5 V		–0.2		0.3×V_{DD}	
		2.5 V ≤ V_{DD} ≤ 3.6 V		–0.2		0.8	
I_{SCLK}	SCLK pin leakage current	Digital input = 0 V or V_{DD}		–1	0.02	1	µA
I_{CS}	$\overline{CS}$ pin leakage current				±1		µA
C_{IN}	Digital input pin capacitance					10	pF
DIGITAL OUTPUT							
V_{OH}	Output logic high level	I_{SOURCE} = 200 µA		V_{DD}–0.2		V_{DD}	V
V_{OL}	Output logic low level	I_{SINK} = 200 µA		0		0.2	V
I_{SDO}	SDO pin leakage current	Floating output		–1		1	µA
C_{OUT}	Digital output pin capacitance	Floating output				10	pF
	Data format, straight binary						
POWER SUPPLY REQUIREMENTS							
V_{DD}	Supply voltage			1.2		3.6	V
I_{DD}	Supply current, normal operation	Digital Inputs = 0 V or V_{DD}	f_{SAMPLE} = 240 KSPS, f_{SCLK} = 3.4 MHz, V_{DD} = 3.6 V		420	500	µA
			f_{SAMPLE} = 100 KSPS, f_{SCLK} = 3.4 MHz, V_{DD} = 3.6 V		172		
			f_{SAMPLE} = 240 KSPS, f_{SCLK} = 3.4 MHz, V_{DD} = 1.6 V		261	330	µA
			f_{SAMPLE} = 100 KSPS, f_{SCLK} = 3.4 MHz, V_{DD} = 1.6 V		107		
			f_{SAMPLE} = 120 KSPS, f_{SCLK} = 1.7 MHz, V_{DD} = 1.2 V		202	250	µA
			f_{SAMPLE} = 50 KSPS, f_{SCLK} = 1.7 MHz, V_{DD} = 1.2 V		83		
I_{DD}	Power-down mode	SCLK on or off			0.008	0.3	µA
POWER DISSIPATION							
	Normal operation	f_{SAMPLE} = 240 KSPS, f_{SCLK} = 3.4 MHz, V_{DD} = 3.6 V			1.51	1.80	mW
		f_{SAMPLE} = 240 KSPS, f_{SCLK} = 3.4 MHz, V_{DD} = 1.6 V			0.42	0.53	
		f_{SAMPLE} = 120 KSPS, f_{SCLK} = 1.7 MHz, V_{DD} = 1.2 V			0.24	0.30	
	Power-down mode	SCLK on or off, V_{DD} = 3.6 V				1.08	µW
TEMPERATURE RANGE							
	Specified performance			–40		85	°C

SPECIFICATIONS, ADS7868

At –40°C to 85°C, f_{SAMPLE} = 280 KSPS and f_{SCLK} = 3.4 MHz if 1.6 V ≤ V_{DD} ≤ 3.6 V; f_{SAMPLE} = 140 KSPS and f_{SCLK} = 1.7 MHz if 1.2 V ≤ V_{DD} < 1.6 V (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYSTEM PERFORMANCE						
	Resolution			8		Bits
	No missing codes		8			Bits
	Integral linearity		–0.5		0.5	LSB(1)
	Differential linearity		–0.5		0.5	LSB
	Offset error(2)	1.2 V ≤ V_{DD} < 1.6 V	–0.5		0.5	LSB
		1.6 V ≤ V_{DD} ≤ 3.6 V	–0.5		0.5	
	Gain error(3)	1.2 V ≤ V_{DD} < 1.6 V	–0.5		0.5	LSB
		1.6 V ≤ V_{DD} ≤ 3.6 V	–0.5		0.5	
	Total unadjusted error(4)	1.2 V ≤ V_{DD} < 1.6 V	–1		1	LSB
		1.6 V ≤ V_{DD} ≤ 3.6 V	–1		1	
SAMPLING DYNAMICS (See Timing Characteristics Section)						
$t_{CONVERT}$	Conversion time	f_{SCLK} = 3.4 MHz, 9 SCLK cycles	2.647			µs
t_{SAMPLE}	Acquisition time	f_{SCLK} = 3.4 MHz, 1.6 V ≤ V_{DD} ≤ 3.6 V	0.64			µs
f_{SAMPLE}	Throughput rate	f_{SCLK} = 3.4 MHz, 1.6 V ≤ V_{DD} ≤ 3.6 V			280	KSPS
	Aperture delay			10		ns
	Aperture jitter			40		ps
DYNAMIC CHARACTERISTICS						
SINAD	Signal-to-noise and distortion	f_{SAMPLE} = 100 KSPS, f_{IN} = 30 kHz, 1.2 V ≤ V_{DD} < 1.6 V		49		dB
		f_{SAMPLE} = 200 KSPS, f_{IN} = 30 kHz, 1.6 V ≤ V_{DD} ≤ 3.6 V	49	49.4		
SNR	Signal-to-noise ratio	f_{SAMPLE} = 100 KSPS, f_{IN} = 30 kHz, 1.2 V ≤ V_{DD} < 1.6 V		49.4		dB
		f_{SAMPLE} = 200 KSPS, f_{IN} = 30 kHz, 1.6 V ≤ V_{DD} ≤ 3.6 V		49.8		
THD	Total harmonic distortion(5)	f_{SAMPLE} = 100 KSPS, f_{IN} = 30 kHz, 1.2 V ≤ V_{DD} < 1.6 V		–65		dB
		f_{SAMPLE} = 200 KSPS, f_{IN} = 30 kHz, 1.6 V ≤ V_{DD} ≤ 3.6 V		–72	-66	
SFDR	Spurious free dynamic range	f_{SAMPLE} = 100 KSPS, f_{IN} = 30 kHz, 1.2 V ≤ V_{DD} < 1.6 V		67		dB
		f_{SAMPLE} = 200 KSPS, f_{IN} = 30 kHz, 1.6 V ≤ V_{DD} ≤ 3.6 V	66	67		
	Full-power bandwidth(6)	At 0.1 dB, 1.2 V ≤ V_{DD} < 1.6 V		2		MHz
		At 0.1 dB, 1.6 V ≤ V_{DD} ≤ 3.6 V		4		
		At 3 dB, 1.2 V ≤ V_{DD} < 1.6 V		3		
		At 3 dB, 1.6 V ≤ V_{DD} ≤ 3.6 V		8		
ANALOG INPUT						
	Full-scale input span(7)	VIN – GND	0		V_{DD}	V
C_S	Input capacitance			12		pF
	Input leakage current		–1		1	µA
DIGITAL INPUT						
	Logic family, CMOS					
V_{IH}	Input logic high level	1.2 V ≤ V_{DD} < 1.6 V	$0.7{\times}V_{DD}$		3.6	V
		1.6 V ≤ V_{DD} < 1.8 V	$0.7{\times}V_{DD}$		3.6	
		1.8 V ≤ V_{DD} < 2.5 V	$0.7{\times}V_{DD}$		3.6	
		2.5 V ≤ V_{DD} ≤ 3.6 V	2		3.6	

(1) LSB = Least Significant BIt
(2) The difference in the first code transition 000...000 to 000...001 from the ideal value of GND + 1 LSB.
(3) The difference in the last code transition 011...111 to 111...111 from the ideal value of V_{DD} - 1 LSB with the offset error removed.
(4) The absolute difference from the ideal transfer function of the converter. This specification is similar to INL error except the effects of offset error and gain error are included.
(5) The 2nd through 10th harmonics are used to determine THD.
(6) Input frequency where the amplitude of the digitized signal has decreased by 0.1 dB or 3 dB.
(7) Ideal input span which does not include gain or offset errors.

SPECIFICATIONS, ADS7868 (continued)

At –40°C to 85°C, f_{SAMPLE} = 280 KSPS and f_{SCLK} = 3.4 MHz if 1.6 V ≤ V_{DD} ≤ 3.6 V; f_{SAMPLE} = 140 KSPS and f_{SCLK} = 1.7 MHz if 1.2 V ≤ V_{DD} < 1.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IL}	Input logic low level	1.2 V ≤ V_{DD} < 1.6 V		–0.2		0.2×V_{DD}	V
		1.6 V ≤ V_{DD} < 1.8 V		–0.2		0.2×V_{DD}	
		1.8 V ≤ V_{DD} < 2.5 V		–0.2		0.3×V_{DD}	
		2.5 V ≤ V_{DD} ≤ 3.6 V		–0.2		0.8	
I_{SCLK}	SCLK pin leakage current	Digital input = 0 V or V_{DD}		–1	0.02	1	µA
I_{CS}	$\overline{CS}$ pin leakage current				±1		µA
C_{IN}	Digital input pin capacitance					10	pF
DIGITAL OUTPUT							
V_{OH}	Output logic high level	I_{SOURCE} = 200 µA		V_{DD}–0.2		V_{DD}	V
V_{OL}	Output logic low level	I_{SINK} = 200 µA		0		0.2	V
I_{SDO}	SDO pin leakage current	Floating output		–1		1	µA
C_{OUT}	Digital output pin capacitance	Floating output				10	pF
	Data format, straight binary						
POWER SUPPLY REQUIREMENTS							
V_{DD}	Supply voltage			1.2		3.6	V
I_{DD}	Supply current, normal operation	Digital Inputs = 0 V or V_{DD}	f_{SAMPLE} = 280 KSPS, f_{SCLK} = 3.4 MHz, V_{DD} = 3.6 V		439	500	µA
			f_{SAMPLE} = 100 KSPS, f_{SCLK} = 3.4 MHz, V_{DD} = 3.6 V		154		
			f_{SAMPLE} = 280 KSPS, f_{SCLK} = 3.4 MHz, V_{DD} = 1.6 V		264	330	µA
			f_{SAMPLE} = 100 KSPS, f_{SCLK} = 3.4 MHz, V_{DD} = 1.6 V		93		
			f_{SAMPLE} = 140 KSPS, f_{SCLK} = 1.7 MHz, V_{DD} = 1.2 V		201	250	µA
			f_{SAMPLE} = 50 KSPS, f_{SCLK} = 1.7 MHz, V_{DD} = 1.2 V		70		
I_{DD}	Power-down mode	SCLK on or off			0.008	0.3	µA
POWER DISSIPATION							
	Normal operation	f_{SAMPLE} = 280 KSPS, f_{SCLK} = 3.4 MHz, V_{DD} = 3.6 V			1.58	1.8	mW
		f_{SAMPLE} = 280 KSPS, f_{SCLK} = 3.4 MHz, V_{DD} = 1.6 V			0.42	0.53	
		f_{SAMPLE} = 140 KSPS, f_{SCLK} = 1.7 MHz, V_{DD} = 1.2 V			0.24	0.3	
	Power-down mode	SCLK on or off, V_{DD} = 3.6 V				1.08	µW
TEMPERATURE RANGE							
	Specified performance			–40		85	°C

TIMING REQUIREMENTS[1][2]

At –40°C to 85°C, f_{SCLK} = 3.4 MHz if 1.6 V ≤ V_{DD} ≤ 3.6 V; f_{SCLK} = 1.7 MHz if 1.2 V ≤ V_{DD} < 1.6 V, 50-pF Load on SDO Pin, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{sample}	Sample time			$t_{SU(CSF-FSCLKF)} + 2 \times t_{C(SCLK)}$		μs
$t_{convert}$	Conversion time	ADS7866		$13 \times t_{C(SCLK)}$		μs
		ADS7867		$11 \times t_{C(SCLK)}$		
		ADS7868		$9 \times t_{C(SCLK)}$		
$t_{C(SCLK)}$	Cycle time	1.2 V ≤ V_{DD} < 1.6 V	See (3)		100	μs
		1.6 V ≤ V_{DD} < 1.8 V	See (3)		100	
		1.8 V ≤ V_{DD} < 2.5 V	See (3)		50	
		2.5 V ≤ V_{DD} ≤ 3.6 V	See (3)		6.7	
$t_{WH(SCLK)}$	Pulse duration		$0.4 \times t_{C(SCLK)}$		$0.6 \times t_{C(SCLK)}$	ns
$t_{WL(SCLK)}$	Pulse duration		$0.4 \times t_{C(SCLK)}$		$0.6 \times t_{C(SCLK)}$	ns
$t_{SU(CSF-FSCLKF)}$	Setup time	1.2 V ≤ V_{DD} < 1.6 V	192			ns
		1.6 V ≤ V_{DD} < 1.8 V	55			
		1.8 V ≤ V_{DD} ≤ 3.6 V	55			
$t_{D(CSF-SDOVALID)}$	Delay time	1.2 V ≤ V_{DD} < 1.6 V			65	ns
		1.6 V ≤ V_{DD} < 1.8 V			55	
		1.8 V ≤ V_{DD} ≤ 3.6 V			55	
$t_{H(SCLKF-SDOVALID)}$	Hold time	1.2 V ≤ V_{DD} < 1.6 V	20			ns
		1.6 V ≤ V_{DD} < 1.8 V	10			
		1.8 V ≤ V_{DD} ≤ 3.6 V	10			
$t_{D(SCLKF-SDOVALID)}$	Delay time	1.2 V ≤ V_{DD} < 1.6 V			140	ns
		1.6 V ≤ V_{DD} < 1.8 V			140	
		1.8 V ≤ V_{DD} ≤ 3.6 V			140	
$t_{DIS(EOC-SDOZ)}$	Disable time	1.2 V ≤ V_{DD} < 1.6 V	10		80	ns
		1.6 V ≤ V_{DD} < 1.8 V	7		60	
		1.8 V ≤ V_{DD} ≤ 3.6 V	7		60	
$t_{WH(CS)}$	Pulse duration	1.2 V ≤ V_{DD} < 1.6 V	20			ns
		1.6 V ≤ V_{DD} < 1.8 V	10			
		1.8 V ≤ V_{DD} ≤ 3.6 V	10			
$t_{SU(LSBZ-CSF)}$	Setup time	1.2 V ≤ V_{DD} < 1.6 V	20			ns
		1.6 V ≤ V_{DD} < 1.8 V	10			
		1.8 V ≤ V_{DD} ≤ 3.6 V	10			

(1) All input signals are specified with $t_r = t_f$ = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.
(2) See timing diagram in Figure 1.
(3) Min $t_{C(SCLK)}$ is determined by the Min t_{SAMPLE} of the specific resolution and supply voltage. See *Acquisition Time, Conversion Time, and Total Cycle Time* section for further details.

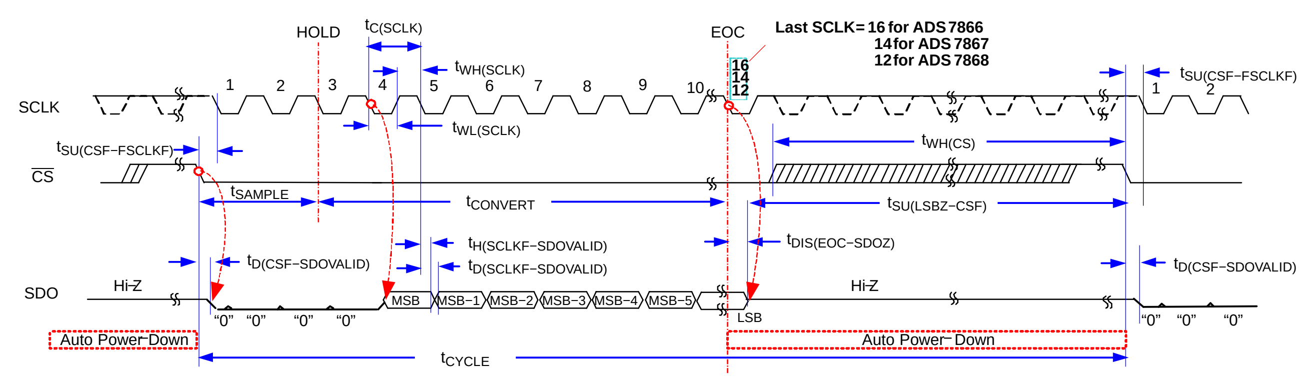
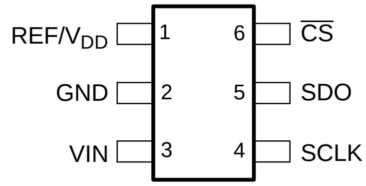


Figure 1. Timing Diagram

PIN CONFIGURATION

ADS7866/67/68
DBV PACKAGE
(TOP VIEW)



TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
NAME	**NO.**	
REF/V_{DD}	1	External reference input and power supply
GND	2	Ground for signal and power supply. All analog and digital signals are referred with respect to this pin.
VIN	3	Analog signal input
SCLK	4	Serial clock input. This clock is used for clocking data out, and it is the source of conversion clock.
SDO	5	This is the serial data output of the conversion result. The serial stream comes with MSB first. The MSB is clocked out (changed) on the falling edge one SCLK after the sampling period ends. This results in four leading zeros after $\overline{CS}$ becomes active. SDO is 3-stated once all the valid bits are clocked out (12 for ADS7866, 10 for ADS7867, and 8 for ADS7868).
$\overline{CS}$	6	This is an active low input signal. It is used as a chip select to gate the SCLK input, to initiate a conversion, and to frame output data.

TYPICAL CHARACTERISTICS ADS7866

FFT (8192 Points)

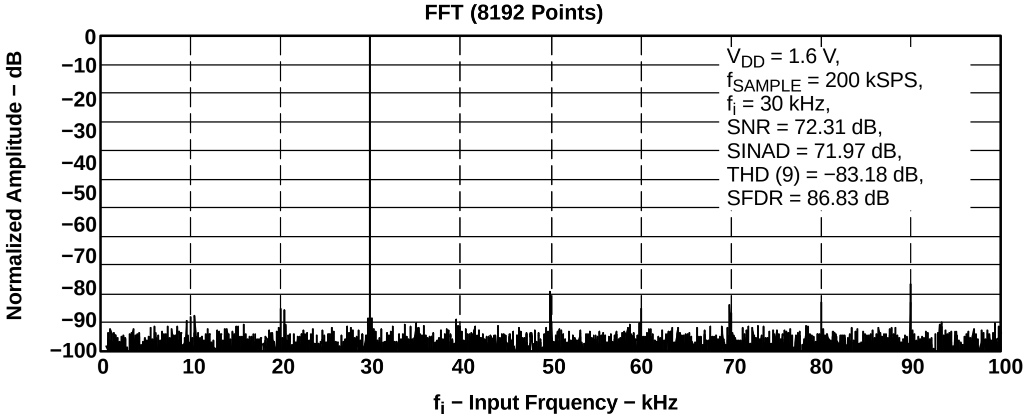


Figure 2.

FFT (8192 Points)

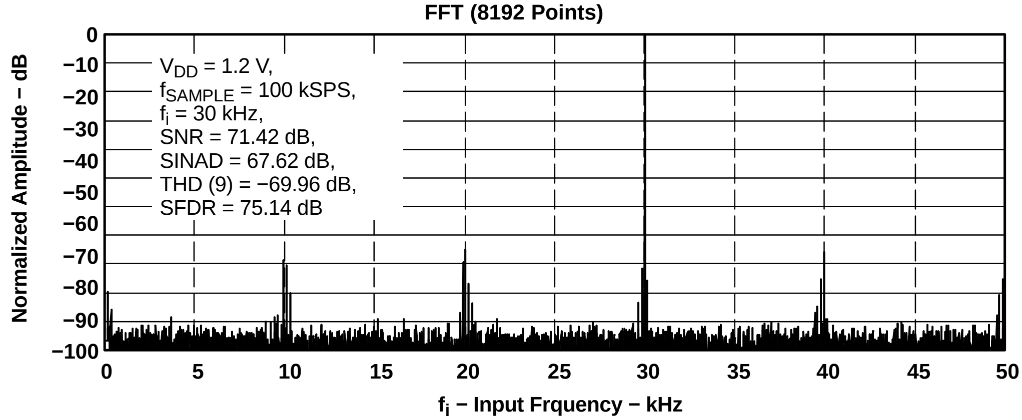


Figure 3.

SIGNAL-TO-NOISE RATIO
vs
INPUT FREQUENCY

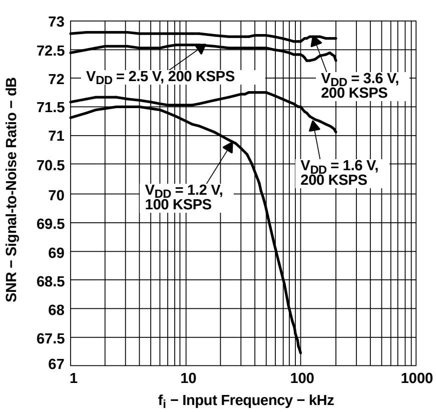


Figure 4.

SIGNAL-TO-NOISE
AND DISTORTION
vs
INPUT FREQUENCY

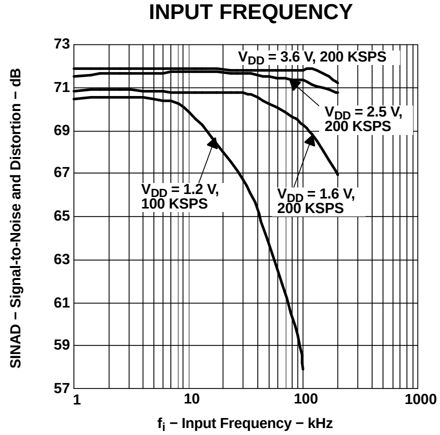


Figure 5.

TOTAL HARMONIC DISTORTION
vs
INPUT FREQUENCY

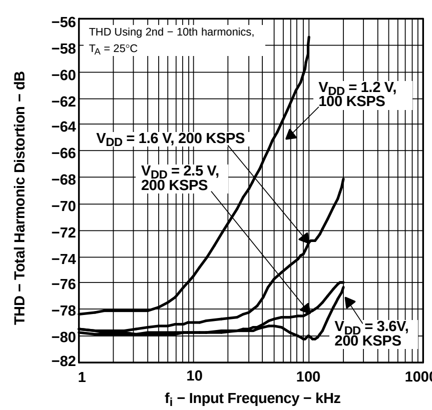


Figure 6.

TYPICAL CHARACTERISTICS ADS7866 (continued)

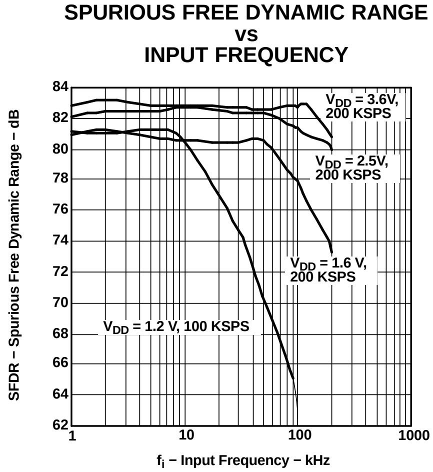


Figure 7.

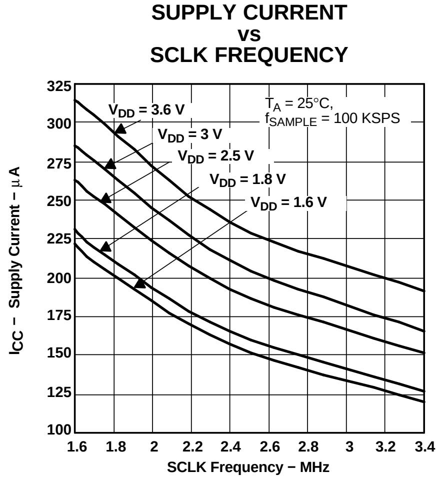


Figure 8.

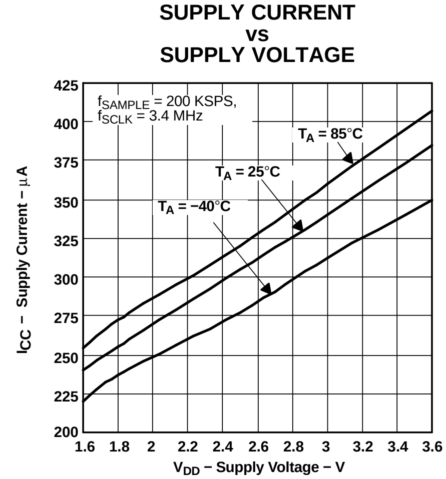


Figure 9.

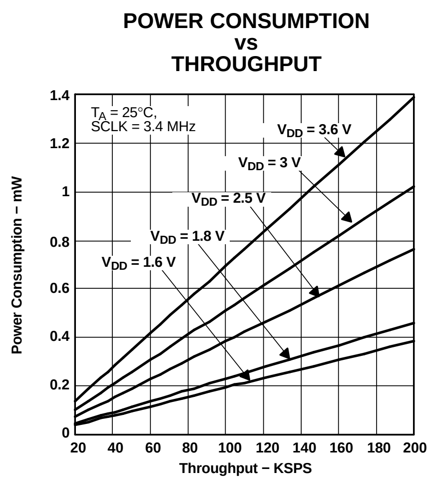


Figure 10.

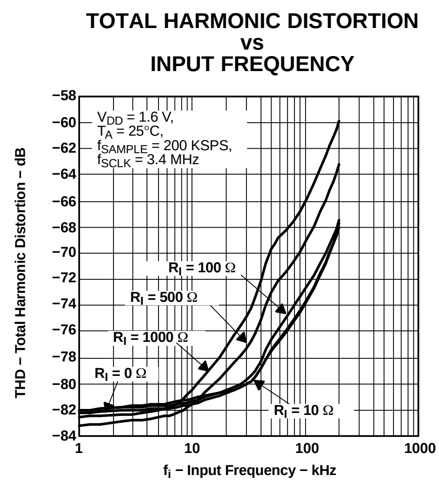


Figure 11.

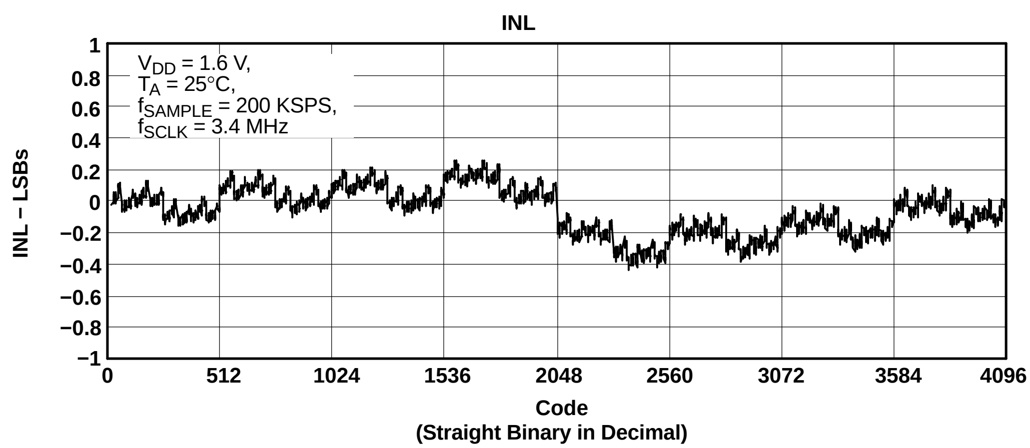


Figure 12.

TYPICAL CHARACTERISTICS ADS7866 (continued)

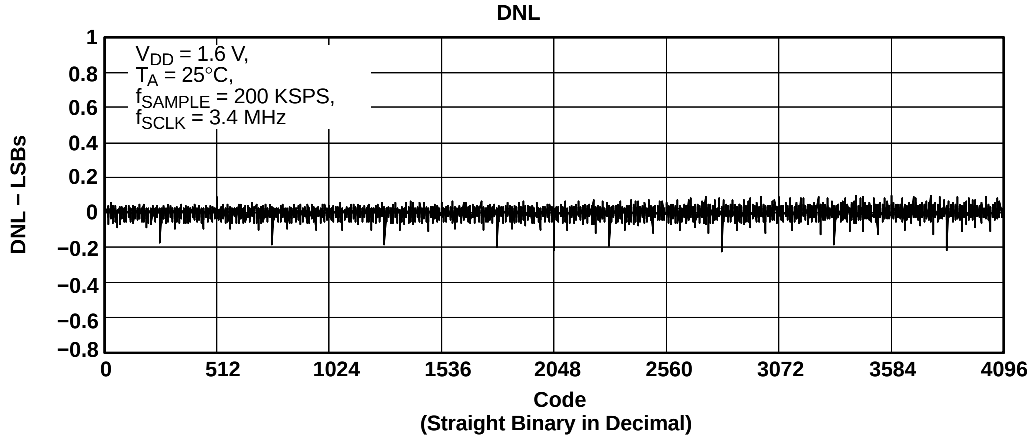


Figure 13.

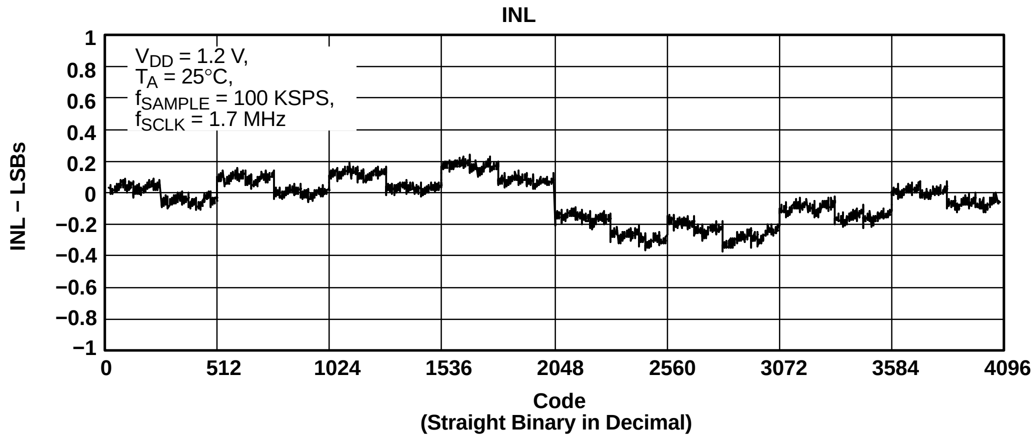


Figure 14.

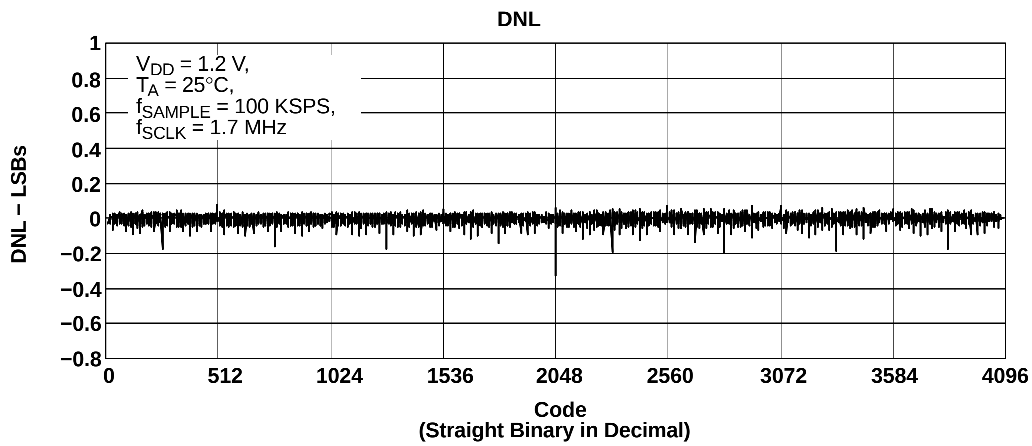


Figure 15.

TYPICAL CHARACTERISTICS ADS7866 (continued)

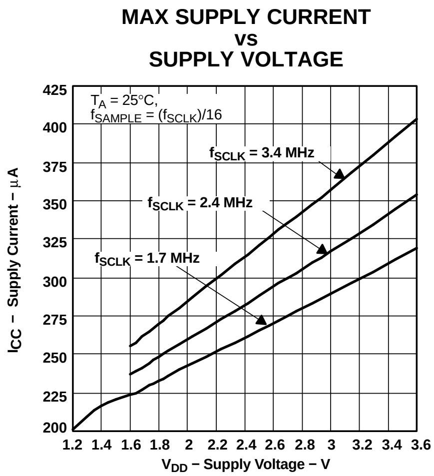


Figure 16.

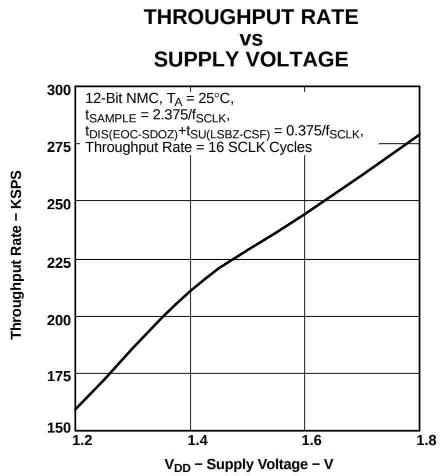


Figure 17.

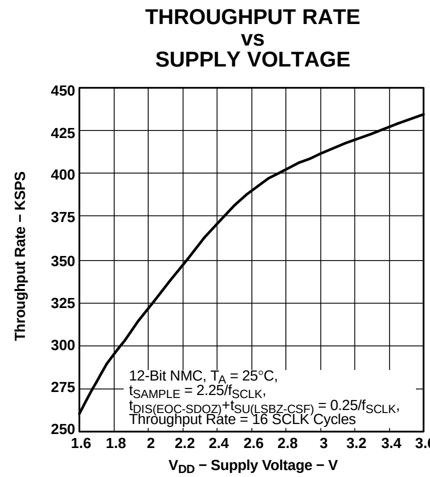


Figure 18.

TYPICAL CHARACTERISTICS ADS7867

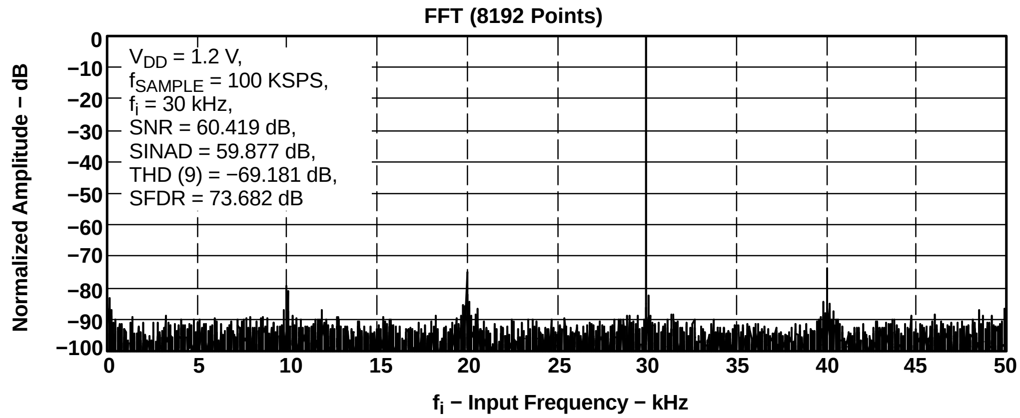


Figure 19.

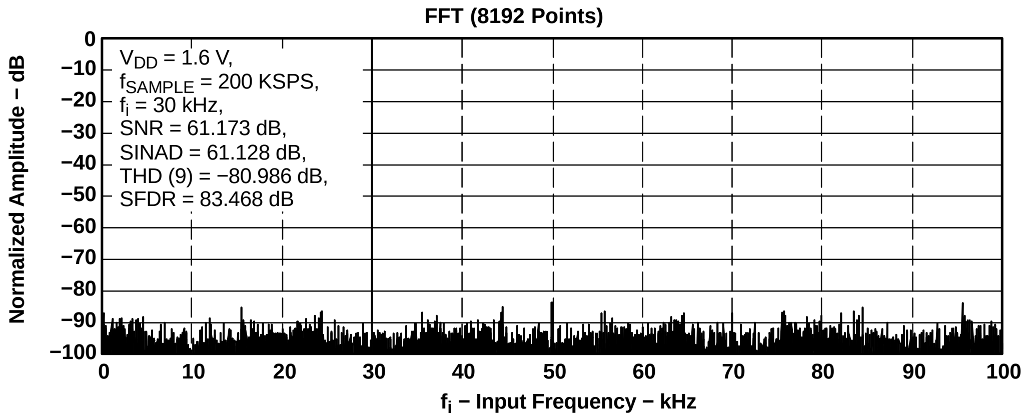


Figure 20.

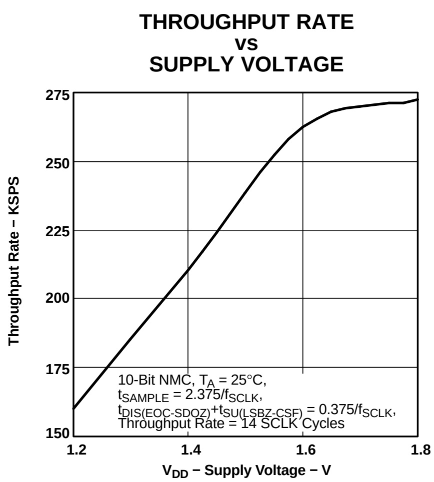


Figure 21.

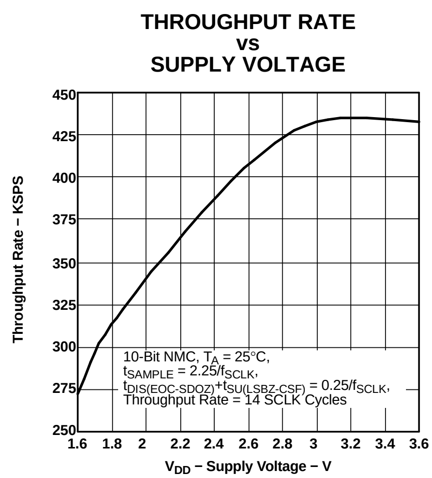


Figure 22.

TYPICAL CHARACTERISTICS ADS7868

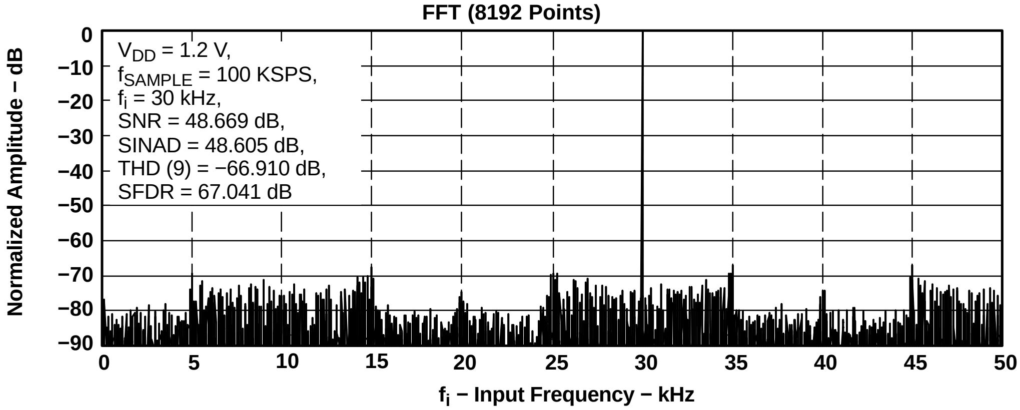


Figure 23.

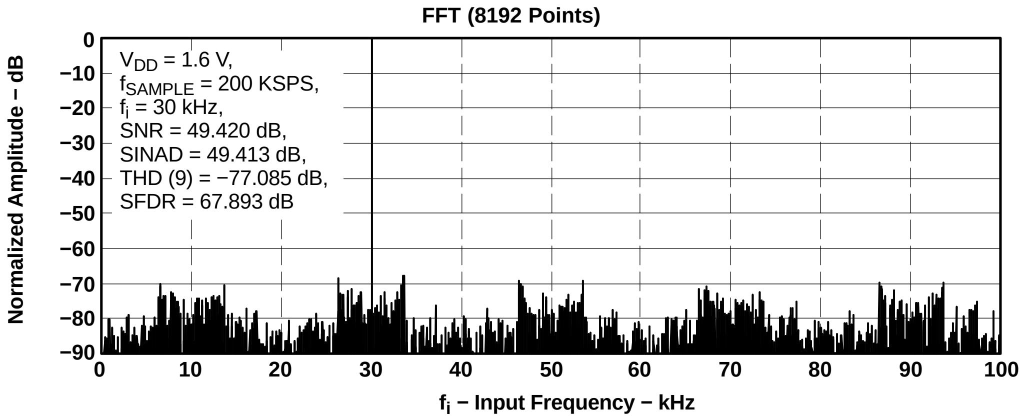


Figure 24.

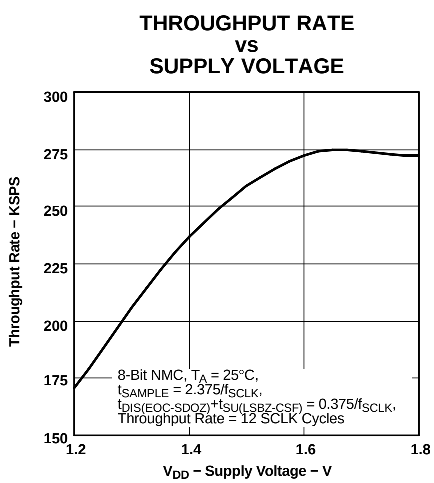


Figure 25.

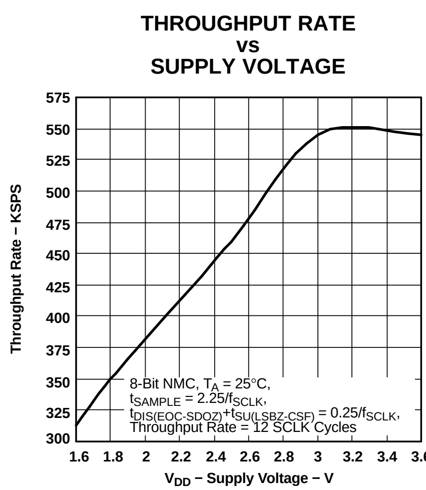


Figure 26.

THEORY OF OPERATION

The ADS7866/67/68 is a family of low supply voltage, low power, high-speed successive approximation register (SAR) analog-to-digital converters (ADCs). The devices can be operated from a supply range from 1.2 V to 3.6 V. There is no need for an external reference. The reference is derived internally from the supply voltage, so the analog input range can be from 0 V to V_{DD}. These ADCs use a charge redistribution architecture, which inherently includes a sample/hold function.

START OF A CONVERSION CYCLE

A conversion cycle is initiated by bringing the $\overline{CS}$ pin low and supplying the serial clock SCLK. The time between the falling edge of $\overline{CS}$ and the third falling edge of SCLK after $\overline{CS}$ falls is used to acquire the input signal. This must be greater than or equal to the minimum acquisition time (MIN t_{SAMPLE} in Table 1) specified for the desired resolution and supply voltage. On the third falling edge of SCLK after $\overline{CS}$ falls, the device goes into hold mode and the process of digitizing the sampled input signal starts.

Acquisition Time, Conversion Time, and Total Cycle Time

The maximum SCLK frequency is determined by the minimum acquisition time (MIN t_{SAMPLE}) specified for the specific resolution and supply voltage of the device. The conversion time is determined by the frequency of SCLK since this is a synchronous converter. The conversion time is 13 times the SCLK cycle time $t_{C(SCLK)}$ for the ADS7866, 11 times for the ADS7867, and 9 times for the ADS7868. The acquisition time, which is also the power up time, is the set-up time between the first falling edge of SCLK after $\overline{CS}$ falls ($t_{SU(CSF\text{-}FSCLKF)}$) plus 2 times $t_{C(SCLK)}$.

The total cycle time, t_{CYCLE}, which is the inverse of the maximum sample rate, can be calculated as follows:

$$t_{CYCLE} = t_{SAMPLE} + t_{CONVERT} + 0.5 \times t_{C(SCLK)}$$

$$\text{if } t_{DIS(EOC\text{-}SDOZ)} + t_{SU(LSBZ\text{-}CSF)} \le 0.5 \times t_{C(SCLK)}$$

$$t_{CYCLE} = t_{SAMPLE} + t_{CONVERT} + t_{DIS(EOC\text{-}SDOZ)} + t_{SU(LSBZ\text{-}CSF)}$$

$$\text{if } t_{DIS(EOC\text{-}SDOZ)} + t_{SU(LSBZ\text{-}CSF)} > 0.5 \times t_{C(SCLK)}$$

THEORY OF OPERATION (continued)

Table 1. Acquisition, Conversion, SCLK, and Potential Throughput Calculation

PARAMETER		SUPPLY VOLTAGE	ADS7866	ADS7867	ADS7868	UNIT
MIN $t_{SU(CSF-FSCLKF)}$	Setup time	1.2 V ≤ V_{DD} < 1.6 V	192	192	192	ns
		1.6 V ≤ V_{DD} < 1.8 V	55	55	55	
		1.8 V ≤ V_{DD} ≤ 3.6 V	55	55	55	
MAX $t_{DIS(EOC-SDOZ)}$	Disable time	1.2 V ≤ V_{DD} < 1.6V	80	80	80	ns
		1.6 V ≤ V_{DD} < 1.8 V	60	60	60	
		1.8 V ≤ V_{DD} ≤ 3.6 V	60	60	60	
MIN $t_{SU(LSBZ-CSF)}$	Setup time	1.2 V ≤ V_{DD} < 1.6 V	20	20	20	ns
		1.6 V ≤ V_{DD} < 1.8 V	10	10	10	
		1.8 V ≤ V_{DD} ≤ 3.6 V	10	10	10	
MAX f_{SCLK}	Frequency	1.2 V ≤ V_{DD} < 1.6 V	1.7	1.7	1.7	MHz
		1.6 V ≤ V_{DD} < 1.8 V	3.4	3.4	3.4	
		1.8 V ≤ V_{DD} ≤ 3.6 V	3.4	3.4	3.4	
MIN t_{sample}	Sample time	1.2 V ≤ V_{DD} < 1.6 V	1368	1368	1368	ns
		1.6 V ≤ V_{DD} < 1.8 V	643	643	643	
		1.8 V ≤ V_{DD} ≤ 3.6 V	643	643	643	
MIN $t_{convert}$	Conversion time	1.2 V ≤ V_{DD} < 1.6 V	7647	6471	5294	ns
		1.6 V ≤ V_{DD} < 1.8 V	3824	3235	2647	
		1.8 V ≤ V_{DD} ≤ 3.6 V	3824	3235	2647	
MIN t_{CYCLE}	Cycle time	1.2 V ≤ V_{DD} < 1.6 V	9116	7939	6763	ns
		1.6 V ≤ V_{DD} < 1.8 V	4537	3949	3360	
		1.8 V ≤ V_{DD} ≤ 3.6 V	4537	3949	3360	
f_{sample}	Theoretical sample frequency	1.2 V ≤ V_{DD} < 1.6 V	110	126	148	KSPS
		1.6 V ≤ V_{DD} < 1.8 V	220	253	298	
		1.8 V ≤ V_{DD} ≤ 3.6 V	220	253	298	

TYPICAL CONNECTION

For a typical connection circuit for the ADS7866/67/68 see Figure 27. A REF3112 is used to supply 1.2 V to the device. A 0.1-µF decoupling capacitor is required between the REF/V_{DD} and GND pins of the converter. This capacitor should be placed as close as possible to the pins of the device. Designers should strive to minimize the routing length of the traces that connect the terminals of the capacitor to the pins of the converter.

Keep in mind the converter offers no inherent rejection of noise or voltage variation in regards to the reference input. This is of particular concern because the reference input is tied to the power supply. Any noise and ripple from the supply appears directly in the digital results. While high frequency noise can be filtered out as described in the previous paragraph, voltage variation due to the line frequency (50 Hz or 60 Hz) can be difficult to remove.

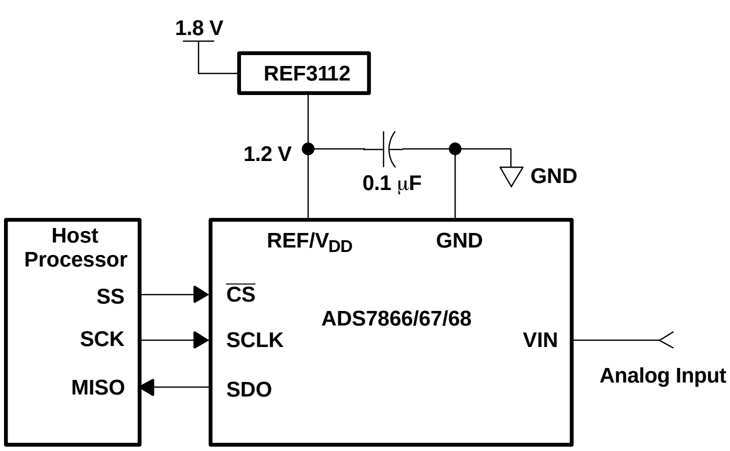


Figure 27. Typical Circuit Configuration

ANALOG INPUT

Figure 28 shows the analog input equivalent circuit for the ADS7866/67/68. The analog input is provided between the VIN and GND pins. When a conversion is initiated, the input signal is sampled on the internal capacitor array. When the converter enters hold mode, the input signal is captured on the internal capacitor array. The VIN input range is limited to 0 V to V_{DD} because the reference is derived from the supply.

The current flowing into the analog input depends upon a number of factors, such as the sample rate, the input voltage, and the input source impedance. The current from the input source charges the internal capacitor array during the sample period. After this capacitance has been fully charged, there is no further input current. The source of the analog input voltage must be able to charge the input capacitance C_S (12 pF typical) within the minimum acquisition time (MIN t_{SAMPLE}) specified for the desired resolution and supply voltage. In the case of the ADS7866, the MIN t_{SAMPLE} for 12-bit resolution is 643 ns (V_{DD} between 1.6 V and 3.6 V). When the converter goes into hold mode, the input impedance is greater than 1 GΩ.

Care must be taken regarding the absolute analog input voltage. In order to maintain the linearity of the converter, the span (VIN – GND) should be within the limits specified. Outside of these limits, the converter's linearity may not meet specifications. Noise introduced into the converter from the input source may be minimized by using low bandwidth input signals along with low-pass filters.

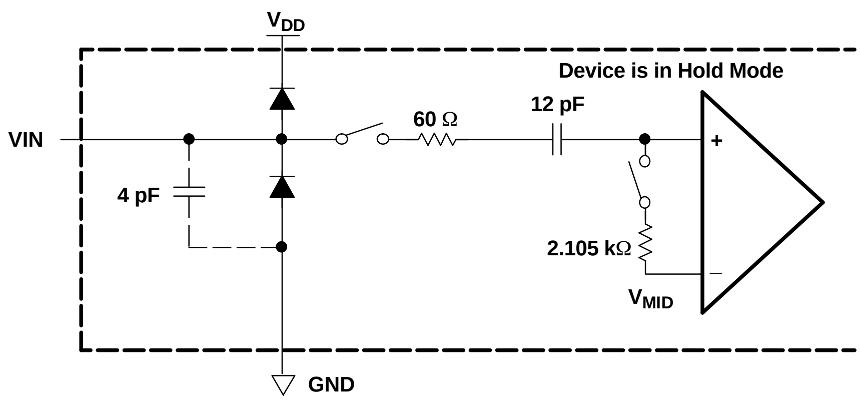


Figure 28. Analog Input Equivalent Circuit (Typical Impedance Values at V_{DD} = 1.6 V, T_A = 27°C)

Choice of Input Driving Amplifier

The analog input to the converter needs to be driven with a low noise, low voltage op amp like the OPA364 or OPA333. An RC filter is recommended at the input pin to low-pass filter the noise from the source. The input to the converter is a unipolar input voltage in the range 0 V to V_{DD}.

DIGITAL INTERFACE

The ADS7866/67/68 interface with microprocessors or DSPs through a high-speed SPI compatible serial interface with CPOL = 1 (inactive SCLK returns to logic high or SCLK leading edge is the rising edge), CPHA = 1 (output data changes on falling edge of SCLK and is available on the rising edge of SCLK). The sampling, conversion, and activation of SDO are initiated on the falling edge of $\overline{CS}$. The serial clock (SCLK) is used for controlling the rate of conversion. It also provides a mechanism allowing synchronization with digital host processors.

The digital inputs, $\overline{CS}$ and SCLK, can exceed the supply voltage V_{DD} as long as they do not exceed the maximum V_{IH} of 3.6 V. This allows the ADS7866/67/68 family to interface with host processors which use a different supply voltage than the converter without requiring external level-shifting circuitry. Furthermore, the digital inputs can be applied to $\overline{CS}$ and SCLK before the supply voltage of the converter is activated without the risk of creating a latch-up condition.

Conversion Result

The ADS7866/67/68 outputs 12/10/8-bit data after 4 leading zeros, respectively. These codes are in straight binary format as shown in Table 2.

The serial output SDO is activated on the falling edge of $\overline{CS}$. The first leading zero is available on SDO until the first falling edge of SCLK after $\overline{CS}$ falls. The remaining 3 leading zeros are shifted out on SDO on the first, second, and third falling edges of SCLK after $\overline{CS}$ falls. The MSB of the converted result follows 4 leading zeros and is clocked out on the fourth falling edge of SCLK. The rising edge of $\overline{CS}$ or the falling edge of SCLK when the EOC occurs puts SDO output into 3-state. Refer to Table 2 for ideal output codes versus input voltages.

Table 2. ADS7866/67/68 Ideal Output Codes Versus Input Voltages

DESCRIPTION	ANALOG INPUT VOLTAGE	DIGITAL OUTPUT STRAIGHT BINARY	
		BINARY CODE	HEX CODE
ADS7866			
Least Significant Bit (LSB)	$V_{DD}/4096$		
Full Scale	V_{DD} – 1LSB	1111 1111 1111	FFF
Midscale	$V_{DD}/2$	1000 0000 0000	800
Midscale – 1LSB	$V_{DD}/2$ – 1LSB	0111 1111 1111	7FF
Zero	0V	0000 0000 0000	000
ADS7867			
Least Significant Bit (LSB)	$V_{DD}/1024$		
Full Scale	V_{DD} – 1LSB	11 1111 1111	3FF
Midscale	$V_{DD}/2$	10 0000 0000	200
Midscale – 1LSB	$V_{DD}/2$ – 1LSB	01 1111 1111	1FF
Zero	0V	00 0000 0000	000
ADS7868			
Least Significant Bit (LSB)	$V_{DD}/256$		
Full Scale	V_{DD} – 1LSB	1111 1111	FF
Midscale	$V_{DD}/2$	1000 0000	80
Midscale – 1LSB	$V_{DD}/2$ – 1LSB	0111 1111	7F
Zero	0V	0000 0000	00

POWER DISSIPATION

The ADS7866/67/68 family is capable of operating with very low supply voltages while drawing a fraction of a milliamp. Furthermore, there is an auto power-down mode to reduce the power dissipation between conversion cycles. Carefully selected system design can take advantage of these features to achieve optimum power performance.

Auto Power-Down Mode

The ADS7866/67/68 family has an auto power-down feature. Besides powering down all circuitry, the converter consumes only 8 nA typically in this mode. The device automatically wakes up when $\overline{CS}$ falls. However, not all of the functional blocks are fully powered until sometime before the third falling edge of SCLK. The device powers down once it reaches the end of conversion (EOC) which is the 16th falling edge of SCLK for the ADS7866 (the 14th and 12th for the ADS7867 and ADS7868, respectively). If $\overline{CS}$ is pulled high before the device reaches the EOC, the converter goes into power-down mode and the ongoing conversion is aborted. Refer to the timing diagram in Figure 1 for further information.

Power Saving: SCLK Frequency and Throughput

These converters achieve lower power dissipation for a fixed throughput rate $f_{sample} = 1/t_{cycle}$ by using higher SCLK frequencies. Higher SCLK frequencies reduce the acquisition time (t_{sample}) and conversion time ($t_{convert}$). This means the converters spend more time in auto power-down mode per conversion cycle. This can be observed in Figure 8 which shows the ADS7866 supply current versus SCLK frequency for f_{sample} = 100 KSPS. For a particular SCLK frequency, the acquisition time and conversion time are fixed. Therefore, a lower throughput increases the proportion of the time the converters are in power down. Figure 10 shows this case for the ADS7866 power consumption versus throughput rate for f_{SCLK} = 3.4 MHz.

Power-On Initialization

There is no specific initialization requirement for these converters after power-on, but the first conversion might not yield a valid result. In order to set the converter in a known state, $\overline{CS}$ should be toggled low then high after V_{DD} has stabilized during power-on. By doing this, the converter is placed in auto power-down mode, and the serial data output (SDO) is 3-stated.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
ADS7866IDBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Purchase Samples
ADS7866IDBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Purchase Samples
ADS7866IDBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Request Free Samples
ADS7866IDBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Request Free Samples
ADS7867IDBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Purchase Samples
ADS7867IDBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Purchase Samples
ADS7867IDBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-250C-1 YEAR	Request Free Samples
ADS7867IDBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-250C-1 YEAR	Request Free Samples
ADS7868IDBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Purchase Samples
ADS7868IDBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Purchase Samples
ADS7868IDBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Request Free Samples
ADS7868IDBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Request Free Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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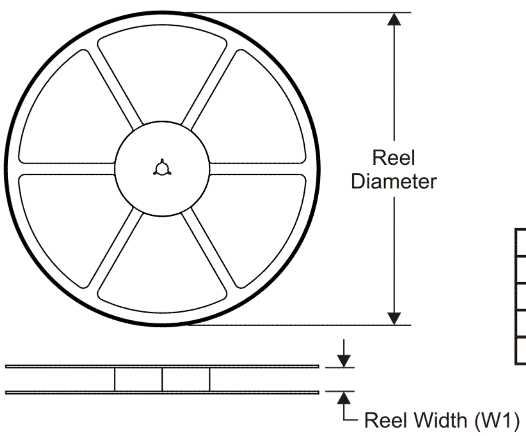
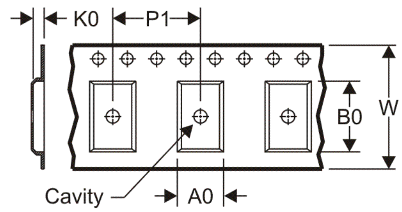
TAPE AND REEL INFORMATION

REEL DIMENSIONS

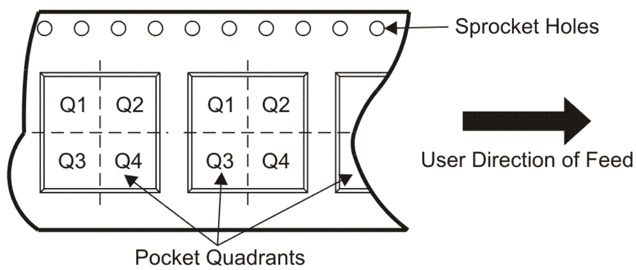


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

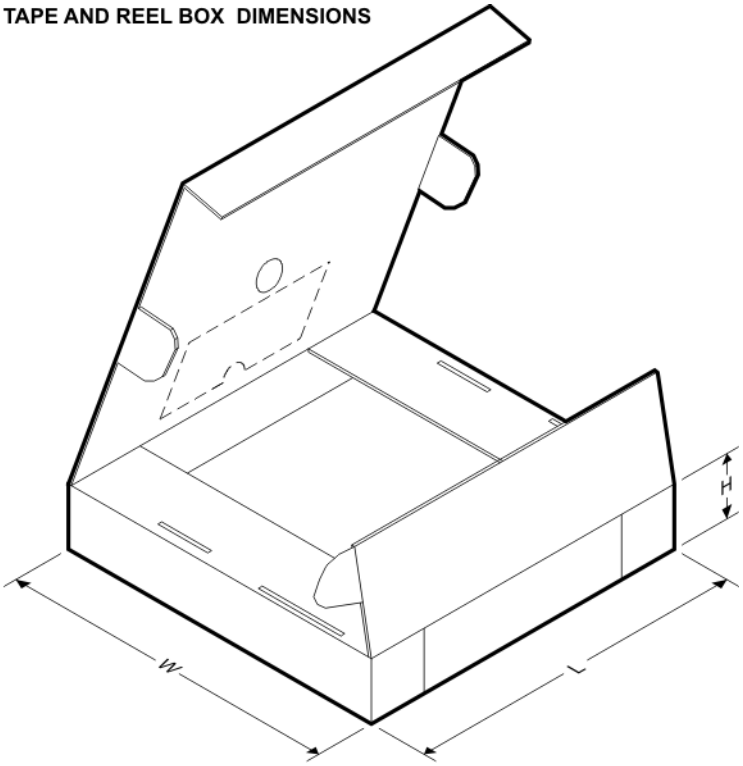
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS7866IDBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.1	1.39	4.0	8.0	Q3
ADS7866IDBVT	SOT-23	DBV	6	250	180.0	8.4	3.2	3.1	1.39	4.0	8.0	Q3
ADS7867IDBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.1	1.39	4.0	8.0	Q3
ADS7867IDBVT	SOT-23	DBV	6	250	180.0	8.4	3.2	3.1	1.39	4.0	8.0	Q3
ADS7868IDBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.1	1.39	4.0	8.0	Q3
ADS7868IDBVT	SOT-23	DBV	6	250	180.0	8.4	3.2	3.1	1.39	4.0	8.0	Q3

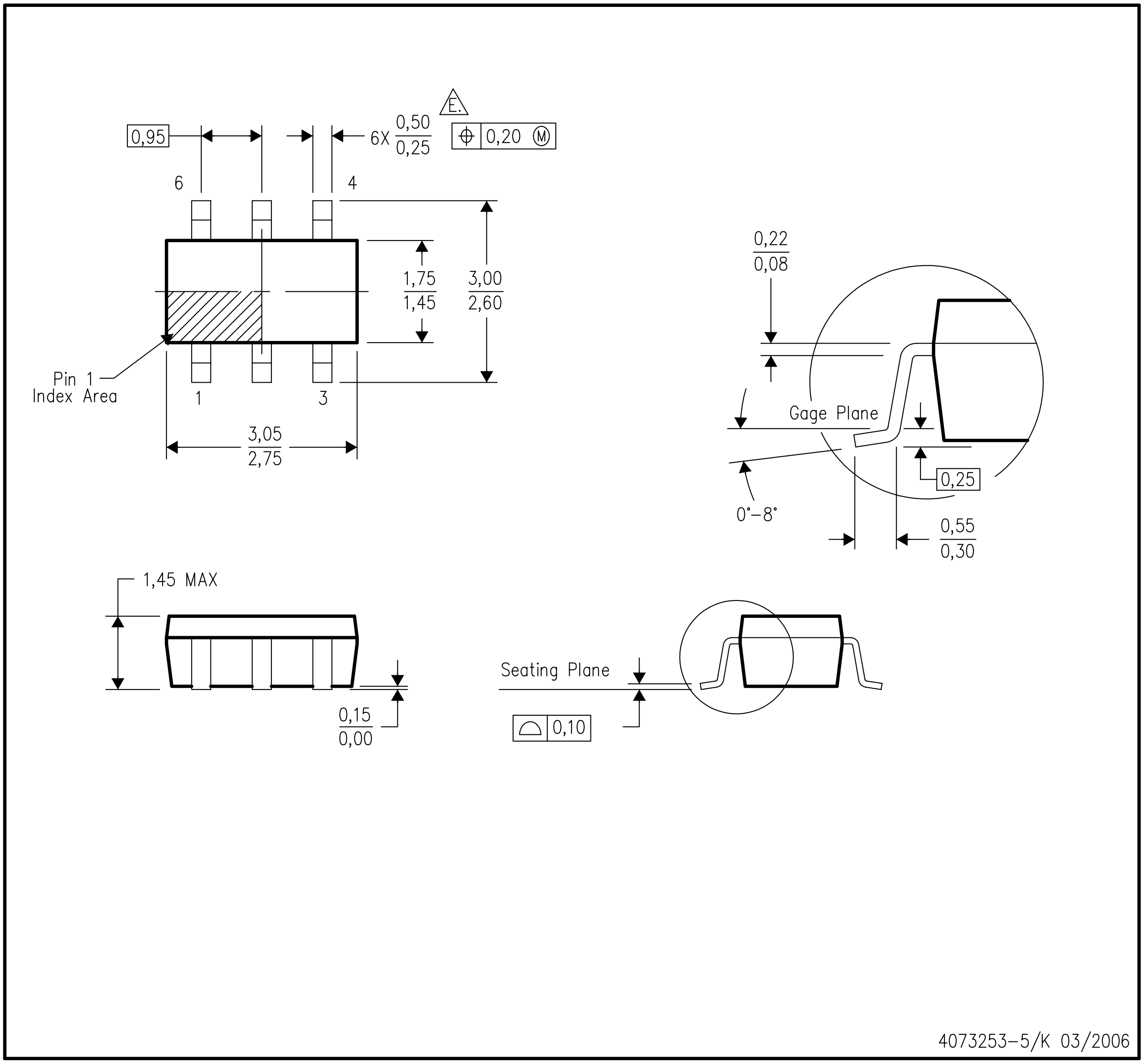
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS7866IDBVR	SOT-23	DBV	6	3000	190.5	212.7	31.8
ADS7866IDBVT	SOT-23	DBV	6	250	190.5	212.7	31.8
ADS7867IDBVR	SOT-23	DBV	6	3000	190.5	212.7	31.8
ADS7867IDBVT	SOT-23	DBV	6	250	190.5	212.7	31.8
ADS7868IDBVR	SOT-23	DBV	6	3000	190.5	212.7	31.8
ADS7868IDBVT	SOT-23	DBV	6	250	190.5	212.7	31.8

DBV (R-PDSO-G6) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
E. Falls within JEDEC MO-178 Variation AB, except minimum lead width.

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