Introduction

Thank you for designing with the Lower Power Spartan®-6 FPGAs. Although Xilinx has made every effort to ensure the highest possible quality, the devices in Table 1 are subject to the limitations described in the following errata.

Devices

These errata apply to the Lower Power Spartan-6 devices shown in Table 1.

Table 1: **Devices Affected by These Errata**

Devices	XC6SLX4	JTAG ID (Revision Code) 2 or higher
	XC6SLX9	JTAG ID (Revision Code) 2 or higher
	XC6SLX16	JTAG ID (Revision Code) 4 or higher
	XC6SLX25	JTAG ID (Revision Code) 2 or higher
	XC6SLX45	JTAG ID (Revision Code) 4 or higher
	XC6SLX75	JTAG ID (Revision Code) 2 or higher
	XC6SLX100	JTAG ID (Revision Code) 2 or higher
	XC6SLX150	JTAG ID (Revision Code) 4 or higher
Packages	All	
Speed Grades	-1L	

Hardware Errata Details

This section provides a detailed description of each hardware issue known at the release time of this document.

IODELAY2

The devices in Table 1 do not support the IODELAY2 block except when using tap 0. Table 2 shows the supported attributes for the IODELAY2 block.

Table 2: **Supported IODELAY2 Attributes**

Mode	IDELAY_TYPE	Tap Selection
IDELAY (Input)	FIXED	IDELAY_VALUE=0
	DEFAULT	N/A
ODELAY (Output)	N/A	ODELAY_VALUE=0

MCB interfaces are not affected by the IODELAY2 errata.

See Answer Record 41356 for additional information.

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Block RAM

Dual Port Block RAM Address Overlap in READ_FIRST and Simple Dual Port Mode

When using the block RAM in True Dual Port (TDP) READ_FIRST mode or Simple Dual Port (SDP) mode, with different clocks on ports A and B, the user must ensure certain addresses do not occur simultaneously on both ports when both ports are enabled and one port is being written to. Failure to observe this restriction can result in read and/or memory array corruption.

The description is found in the Conflict Avoidance section in v1.2 of UG383, *Spartan-6 FPGA Block RAM Resources User Guide*.

This description was originally added to the *Spartan-6 FPGA Block RAM Resources User Guide*, v1.1, published 10/28/09. This errata is being provided to highlight this change and ensure that all users are aware of this design restriction. ISE® 12.1 software provides appropriate warnings for possible violations of these restrictions.

This issue will not be fixed in the devices listed in Table 1.

Work-around

The recommended work-around to avoid memory array corruption issue is to configure the block RAM in WRITE_FIRST mode. WRITE_FIRST mode is available in block RAMs configured in TDP mode in all ISE software versions. WRITE_FIRST mode is available in block RAMs configured in SDP mode from ISE v12.3 and later.

See Answer Record 34533.

9K Simple Dual Port Block RAM Width Restriction

The Spartan-6 FPGA RAMB8BWER in Simple Dual Port (SDP) mode (RAM_MODE=SDP) only supports the 36-bit data width on both ports. Failure to set both ports to 36 bits (DATA_WIDTH_A=36, DATA_WIDTH_B=36) can result in data corruption.

The description is found in the Possible Configurations section in v1.2 of UG383, *the Spartan-6 FPGA Block RAM Resources User Guide*.

This description was originally added to the *Spartan-6 FPGA Block RAM Resources User Guide*, v1.2, published 02/23/10. This errata is being provided to highlight this change and ensure that all users are aware of this design restriction. ISE 12.1 software provides appropriate warnings for possible violations of these restrictions.

This issue will not be fixed in the devices listed in Table 1.

Work-around

See Answer Record 34541.

9K Block RAM Initialization

Block RAM used in the 9K mode (RAMB8BWER) can fail to initialize user data or default values during configuration in the devices listed in Table 1. This description is found in the Additional Block RAM Primitive Design Considerations section in v1.3 of UG383, *the Spartan-6 FPGA Block RAM Resources User Guide*.

This issue will not be fixed in the devices listed in Table 1.

Work-arounds

Use ISE 13.2 or later to generate the bitstream and do not use encryption. If using ISE 13.1 or earlier or using encryption, then either use 18K block RAM or write to the 9K block RAM to initialize it after configuration.

See Answer Record 39999.

Configuration

BPI Configuration Not Supported in LX25 Devices

Master BPI mode for configuration is not supported in the XC6SLX25 device listed in Table 1. The other devices in Table 1 that support Master BPI configuration are not affected. This description is found in the Master BPI Configuration Interface section in v2.2 of UG380, *Spartan-6 FPGA Configuration User Guide*.

See Answer Record 36521 for additional information.

This issue will not be fixed in the XC6SLX25 device listed in Table 1.

Work-around

Alternative configuration modes include Master SelectMAP mode with a Xilinx Platform Flash PROM or Master SPI mode, including x4 mode with a quad SPI Flash.

Configuration Readback When Using 9K Block RAM

Configuration readback can corrupt 9K block RAM (RAMB8BWER) data. Configuration readback (including iMPACT Verify) is not supported when 9K block RAM is used in the devices listed in Table 1. However, readback CRC (POST_CRC), which is typically used for SEU detection, is supported. This description is found in the Additional Block RAM Primitive Design Considerations section in v1.3 of UG383, *Spartan-6 FPGA Block RAM Resources User Guide*.

This issue will not be fixed in the devices listed in Table 1.

Work-around

Use 18K block RAM if configuration readback will be used.

See Answer Record 39977.

Operational Guidelines

Design Software Requirements

The devices listed in Table 1, unless otherwise specified, require the following Xilinx development software installation:

- Refer to the Spartan-6 Device Production Software and Speed Specification Release table in DS162, *Spartan-6 FPGA Data Sheet: DC and Switching Characteristics* for the Xilinx ISE Design Suite version required for the selected part. Upgrading to ISE 13.2 or later is recommended.
- See Software Known Issues with regards to Spartan-6 FPGAs in Answer Record 40000.

Additional Questions or Clarifications

For additional questions regarding these errata, contact Xilinx Technical Support: http://www.xilinx.com/support/clearexpress/websupport.htm or your Xilinx Sales Representative: http://www.xilinx.com/company/contact.htm.

Revision History

Date	Version	Description
04/01/11	1.0	Initial Xilinx release.
07/11/11	1.1	Updated 9K Block RAM Initialization, BPI Configuration Not Supported in LX25 Devices, Configuration Readback When Using 9K Block RAM, and Design Software Requirements.

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