Introduction

Thank you for designing with the Spartan®-6 family of devices. Although Xilinx has made every effort to ensure the highest possible quality, the devices in Table 1 are subject to the limitations described in the following errata.

Devices

These errata apply to the Spartan-6 devices shown in Table 1.

Table 1: **Devices Affected by These Errata**

Devices	Previous Mask Revision	New Mask Revision(1)
	JTAG ID (Revision Code)	
XC6SLX4	0	2 or higher
XC6SLX9	0	2 or higher
XC6SLX16	2, 3	4 or higher
XC6SLX25	0	2 or higher
XC6SLX25T	0	2 or higher
XC6SLX45	2, 3	4 or higher
XC6SLX45T	3	4 or higher
XC6SLX75	0	2 or higher
XC6SLX75T	0	2 or higher
XC6SLX100	0	2 or higher
XC6SLX100T	0	2 or higher
XC6SLX150	3	4 or higher
XC6SLX150T	3	4 or higher
Package	All	
Speed Grades	-2, -3, -3N, -4	-2, -3, -3N

Notes:

1. See XCN11012 for additional information on mask revision change. IODELAY2 errata is different for previous and new mask revisions.

Hardware Errata Details

This section provides a detailed description of each hardware issue known at the release time of this document.

IODELAY2 (New Mask Revision)

In the devices listed in Table 1 with the JTAG ID (Revision Code) listed under New Mask Revision, the IODELAY2 block can experience single data bit corruption. MCB interfaces are not affected by the IODELAY2 errata.

Single Data Bit Corruption in IDELAY and ODELAY Modes

The IODELAY2 block can corrupt a single data bit for some IDELAY_VALUE and ODELAY_VALUE settings.

Work-arounds

IDELAY_TYPE=FIXED, VARIABLE_FROM_ZERO, VARIABLE_FROM_HALF_MAX or DIFF_PHASE_DETECTOR, or when used in ODELAY mode

Limit the data rate through the IODELAY2 to the maximum specifications in Table 2.

Table 2: **Maximum IODELAY2 Data Rate**

V_{CCINT} Range	Temperature	Maximum Data Rate (Mb/s)[1]		
		-3	-3N	-2
Standard Performance (Standard V_{CCINT})	Commercial	800	667	667
	Industrial	740	625	625
Extended Performance (Requires Extended Performance V_{CCINT})	Commercial	900	740	740
	Industrial	860	700	700

Notes:

1. Higher data rates are achievable when certain system design restrictions or considerations are taken into account. See Answer Record 41083 for additional information.

IDELAY_TYPE=FIXED or VARIABLE_FROM_ZERO or when used in ODELAY mode, with tap limit

When using a fixed tap value and requiring higher performance than specified in Table 2, restricting the maximum IDELAY_VALUE or ODELAY_VALUE can avoid data corruption at the higher indicated data rates. Table 3 provides a summary of these higher data rates for fixed tap values.

Table 3: **Maximum IDELAY_VALUE or ODELAY_VALUE**

Maximum DELAY Value	Maximum Data Rate (Mb/s)		
	-3	-3N	-2
6	1,080	1,050	950
7	1,050		
8	1,000	1,000	
9	950	950	
14	800	800	800
18	See Table 2	700	700
20	See Table 2	667	667

IODELAY2 (Previous Mask Revision)

In the devices listed in Table 1 with the JTAG ID (Revision Code) listed under Previous Mask Revision, the IODELAY2 block can experience late data edge delays, early data edge delays, and single data bit corruption. MCB interfaces are not affected by the IODELAY2 errata.

Late Data Edge Delay in IDELAY and ODELAY Modes

The IODELAY2 block can add up to 350 ps of delay on the rising or falling edge transitions when the IDELAY_VALUE or ODELAY_VALUE is 4 or higher for all IDELAY_TYPE settings or when used as output delay. This behavior can be present at all data rates and should be included in system timing margin analysis.

Early Data Edge Delay in ODELAY Mode

The IODELAY2 block used in the ODELAY mode can generate a data edge up to 350 ps early on the rising or falling edge transitions. This behavior can be present at data rates higher than 533 Mb/s and for all ODELAY_VALUE settings and should be included in system timing margin analysis.

Single Data Bit Corruption in IDELAY and ODELAY Modes

The IODELAY2 block can corrupt a single data bit for all IDELAY_TYPE settings or when used in ODELAY mode.

Work-arounds

IDELAY_TYPE=DEFAULT

The data rate must not exceed 250 Mb/s to avoid data corruption.

IDELAY_TYPE=FIXED or VARIABLE_FROM_ZERO or When Used in ODELAY Mode

The IDELAY_VALUE or ODELAY_VALUE must not exceed the values in Table 4 to avoid data corruption at the indicated data rate.

Table 4: **Maximum IDELAY_VALUE or ODELAY_VALUE**

Data Rate (Mb/s)	Bit Time (ps)	Maximum DELAY Value
1,080	926	6
1,050	952	7
1,000	1,000	8
945	1,058	9
800	1,250	14
667	1,499	20
625	1,600	22
533	1,876	28
400	2,500	43
333	3,003	54
266	3,759	72
200	5,000	101
188	5,319	107

IDELAY_TYPE=VARIABLE_FROM_HALF_MAX

The data rate must not exceed 400 Mb/s, the IODELAY2 IOCLK frequency must be equal to the data rate, and the positive increment must not exceed 5 to avoid data corruption.

IDELAY_TYPE=DIFF_PHASE_DETECTOR

The data rate must not exceed 400 Mb/s and data to clock skew, including package trace difference, must not exceed 0.15 UI to avoid data corruption.

See Answer Record 38408 for additional information.

Block RAM

Dual Port Block RAM Address Overlap in READ_FIRST and Simple Dual Port Mode

When using the block RAM in True Dual Port (TDP) READ_FIRST mode or Simple Dual Port (SDP) mode, with different clocks on ports A and B, the user must ensure certain addresses do not occur simultaneously on both ports when both ports are enabled and one port is being written to. Failure to observe this restriction can result in read and/or memory array corruption.

The description is found in the Conflict Avoidance section in v1.2 of UG383, *Spartan-6 FPGA Block RAM Resources User Guide*.

This description was originally added to the *Spartan-6 FPGA Block RAM Resources User Guide*, v1.1, published 10/28/09. This errata is being provided to highlight this change and ensure that all users are aware of this design restriction. ISE® 12.1 software provides appropriate warnings for possible violations of these restrictions.

This issue will not be fixed in the devices listed in Table 1.

Work-around

The recommended work-around to avoid memory array corruption issue is to configure the block RAM in WRITE_FIRST mode. WRITE_FIRST mode is available in block RAMs configured in TDP mode in all ISE software versions. WRITE_FIRST mode is available in block RAMs configured in SDP mode from ISE v12.3 and later.

See Answer Record 34533.

9K Simple Dual Port Block RAM Width Restriction

The Spartan-6 FPGA RAMB8BWER in Simple Dual Port (SDP) mode (RAM_MODE=SDP) only supports the 36-bit data width on both ports. Failure to set both ports to 36 bits (DATA_WIDTH_A=36, DATA_WIDTH_B=36) can result in data corruption.

The description is found in the Possible Configurations section in v1.2 of UG383, *the Spartan-6 FPGA Block RAM Resources User Guide*.

This description was originally added to the *Spartan-6 FPGA Block RAM Resources User Guide*, v1.2, published 02/23/10. This errata is being provided to highlight this change and ensure that all users are aware of this design restriction. ISE 12.1 software provides appropriate warnings for possible violations of these restrictions.

This issue will not be fixed in the devices listed in Table 1.

Work-around

See Answer Record 34541.

9K Block RAM Initialization

Block RAM used in the 9K mode (RAMB8BWER) can fail to initialize user data or default values during configuration in the devices listed in Table 1. This description is found in the Additional Block RAM Primitive Design Considerations section in v1.3 of UG383, *Spartan-6 FPGA Block RAM Resources User Guide*.

This issue will not be fixed in the devices listed in Table 1.

Work-arounds

Use ISE 13.2 or later to generate the bitstream and do not use encryption. If using ISE 13.1 or earlier or using encryption, then either use 18K block RAM or write to the 9K block RAM to initialize it after configuration.

See Answer Record 39999.

Memory Controller Block (MCB)

MCB Performance (Does Not Apply to LX16 JTAG ID Revision Code 2 and LX45 JTAG ID Revision Code 2 Devices)

DS162, *Spartan-6 FPGA Data Sheet: DC and Switching Characteristics* includes new data rate specifications for DDR2 interfaces implemented with the MCB. This applies to all devices in Table 1, with the exception of the Spartan-6 FPGA LX16 JTAG ID Revision Code 2 and LX45 JTAG ID Revision Code 2 devices. The new data rates are supported in the Standard MCB performance mode when operating within the standard V_{CCINT} recommended operating conditions. In addition, a new Extended MCB performance mode has been introduced with V_{CCINT} operating conditions that allow the MCB to operate at the originally specified performance.

Table 5: **MCB Performance Specification Comparison**

Performance Specification	V_{CCINT} Operating Range	DDR2 Performance	
		-2	-3/-4
Original (No Longer Supported)	1.14V – 1.26V	667 Mb/s	800 Mb/s
New (Standard Performance)	1.14V – 1.26V	625 Mb/s	667 Mb/s
New (Extended Performance)	1.2V – 1.26V	667 Mb/s	800 Mb/s

This errata is being provided to highlight this change and ensure that all MCB users are aware of the new performance modes and specifications. The ISE 12.2 software (with MIG 3.5) will provide support for selection and timing validation of the new Standard and Extended MCB performance modes. Prior to the ISE 12.2 software release, these modes can be used by adhering to the correct V_{CCINT} range and ensuring that MIG tool selections are made in compliance with the new performance specifications.

Answer Record 35818 contains additional information. Also, refer to Product Change Notice (PCN) document XCN10024 for details on Spartan-6 LX16 and LX45 devices in production at the time of the PCN's release.

Configuration

BPI Configuration Not Supported in LX25/T Devices

Master BPI mode for configuration is not supported in the XC6SLX25 and XC6SLX25T devices listed in Table 1. The other devices in Table 1 that support Master BPI configuration are not affected. This description is found in the Master BPI Configuration Interface section in v2.2 of UG380, *Spartan-6 FPGA Configuration User Guide*.

See Answer Record 36521 for additional information.

This issue will not be fixed in the XC6SLX25 and XC6SLX25T devices listed in Table 1.

Work-around

Alternative configuration modes include Master SelectMAP mode with a Xilinx Platform Flash PROM or Master SPI mode, including x4 mode with a quad SPI Flash.

16-Bit SelectMAP Configuration Maximum CCLK Frequency for LX100/T Devices

The maximum CCLK configuration frequency has been revised from 40 MHz to 35 MHz for 16-bit-wide SelectMAP mode for the XC6SLX100/T devices listed in Table 1. SelectMAP mode is also known as slave parallel or BPI mode. The parameters affected are F_{SMCCK} for slave mode (x16 only) and F_{MCCK} for master mode (SelectMAP/BPI x16 only). This change is included in DS162, *Spartan-6 FPGA Data Sheet: DC and Switching Characteristics*, v1.10, November 4, 2010. All designs using 16-bit SelectMAP in the XC6SLX100/T devices should use a configuration frequency of less than 35 MHz. No software changes are associated with this revision.

See Answer Record 38733 for additional information.

Configuration Readback When Using 9K Block RAM

Configuration readback can corrupt 9K block RAM (RAMB8BWER) data. Configuration readback (including iMPACT Verify) is not supported when 9K block RAM is used in the devices listed in Table 1. However, readback CRC (POST_CRC), which is typically used for SEU detection, is supported. This description is found in the Additional Block RAM Primitive Design Considerations section in v1.3 of UG383, *Spartan-6 FPGA Block RAM Resources User Guide*.

This issue will not be fixed in the devices listed in Table 1.

Work-around

Use 18K block RAM if configuration readback will be used.

See Answer Record 39977.

Operational Guidelines

Design Software Requirements

The devices listed in Table 1, unless otherwise specified, require the following Xilinx development software installation:

- Refer to the Spartan-6 Device Production Software and Speed Specification Release table in DS162, *Spartan-6 FPGA Data Sheet: DC and Switching Characteristics* for the Xilinx ISE Design Suite version required for the selected part. Upgrading to ISE 13.2 or later is recommended.
- See Software Known Issues with regards to Spartan-6 FPGAs in Answer Record 35180 (ISE 12.4) and Answer Record 40000 (ISE 13.x).

Additional Questions or Clarifications

For additional questions regarding these errata, contact Xilinx Technical Support: http://www.xilinx.com/support/clearexpress/websupport.htm or your Xilinx Sales Representative: http://www.xilinx.com/company/contact.htm.

Revision History

Date	Version	Description
05/12/10	1.0	Initial Xilinx release.
06/14/10	1.1	Added MCB Performance (Does Not Apply to LX16 JTAG ID Revision Code 2 and LX45 JTAG ID Revision Code 2 Devices).
06/25/10	1.2	Added the Spartan-6 LX45T device. Updated Table 1 and MCB Performance (Does Not Apply to LX16 JTAG ID Revision Code 2 and LX45 JTAG ID Revision Code 2 Devices).
07/16/10	1.3	Added the Spartan-6 LX75/T and LX150/T devices. Added -4 speed grade to Table 5.
07/23/10	1.4	Added the Spartan-6 LX25/T and LX100/T devices. Added Configuration errata and an Operational Guidelines section.
10/15/10	1.5	Added LX4 and LX9 devices to document; updated Table 1. Updated speed grade information in Table 1. Added IODELAY2 (Previous Mask Revision) section, including Late Data Edge Delay in IDELAY and ODELAY Modes, Early Data Edge Delay in ODELAY Mode, and Single Data Bit Corruption in IDELAY and ODELAY Modes. Updated Dual Port Block RAM Address Overlap in READ_FIRST and Simple Dual Port Mode work-around.
12/20/10	1.6	Added 16-Bit SelectMAP Configuration Maximum CCLK Frequency for LX100/T Devices.
01/31/11	1.7	Added 9K Block RAM Initialization and Configuration Readback When Using 9K Block RAM.
04/15/11	1.8	Condensed document title. Updated Table 1. Added IODELAY2 (New Mask Revision). DDR3 was removed from the Memory Controller Block (MCB) errata per XCN10024. Updated Design Software Requirements.
07/11/11	1.9	Updated Table 3, 9K Block RAM Initialization, BPI Configuration Not Supported in LX25/T Devices, Configuration Readback When Using 9K Block RAM, and Design Software Requirements.

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