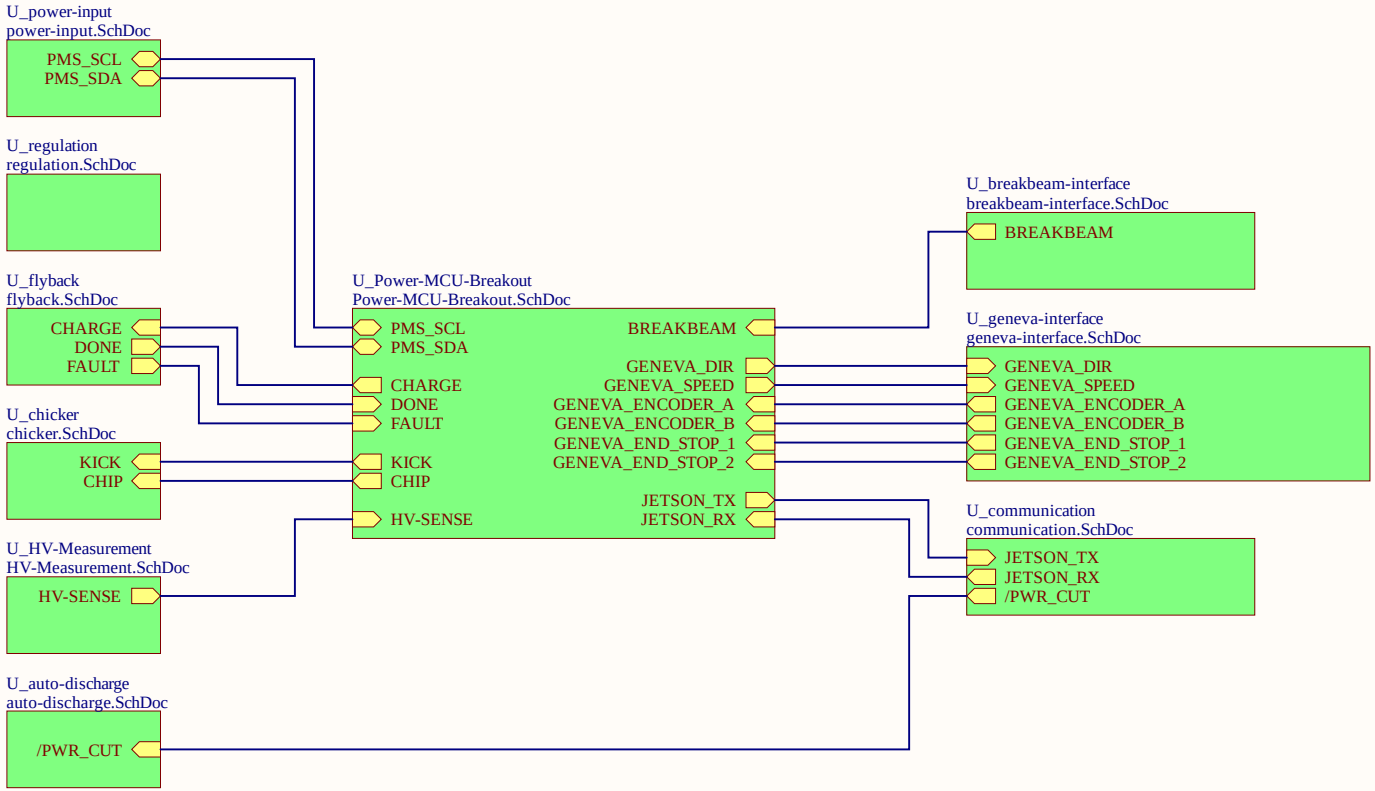
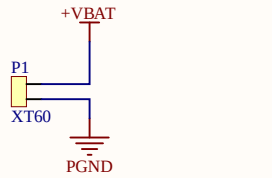


Title		
Size A4	Number	Revision 3
Date: 1-29-2022		Sheet of
File: C:\Users\..\power-v3.3.SchDoc		Drawn By: Simon Zheng

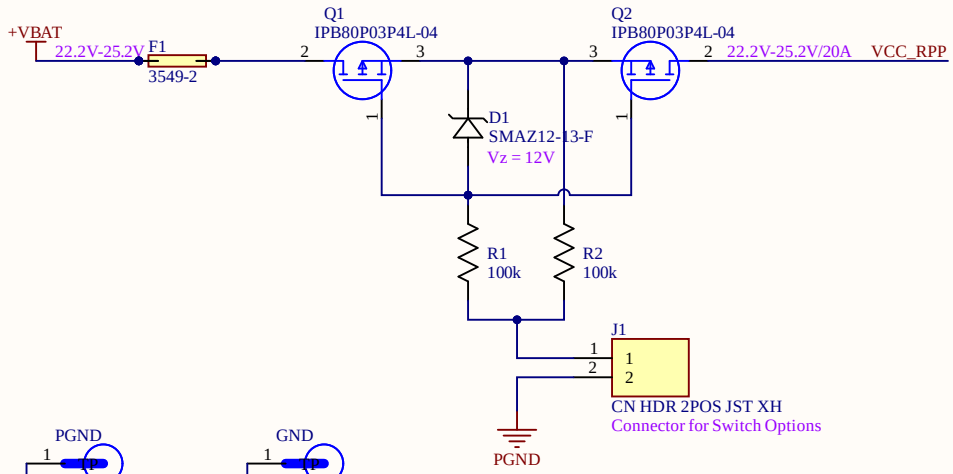
Power Input and Monitoring

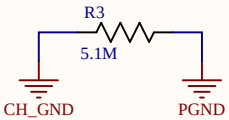
Battery Connector

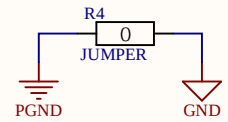
Breakout to 2 x 3S LiPo: 22.2V-25.2V

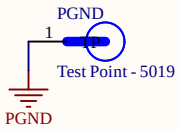


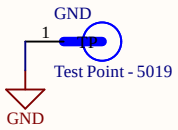
Reverse Polarity Protection



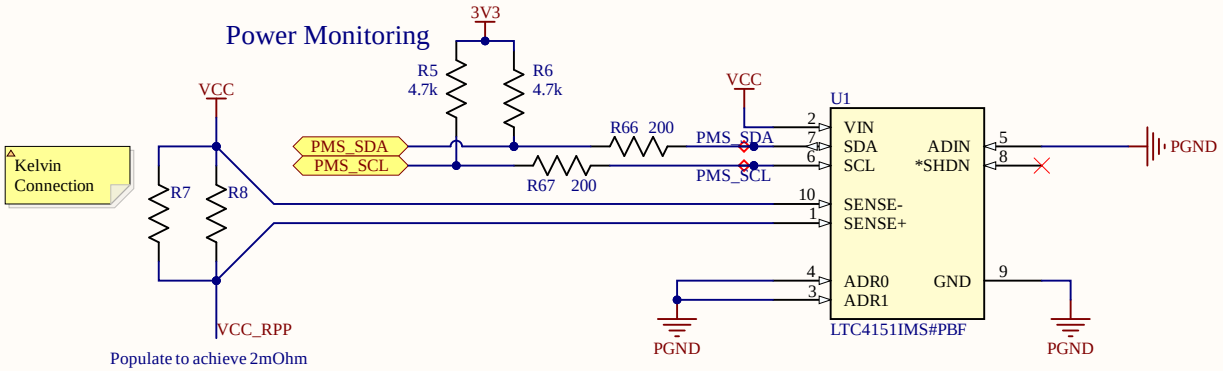








Power Monitoring



****
Reverse Polarity Protection Design Specifications
****

Reverse Polarity

Under the condition that a negative potential is applied across the battery input, current flow will be blocked. This is because the reverse polarity causes the body diode of the MOSFET to be reverse biased. Then, VG = |VBAT| > 0V and so P-Channel MOSFET will be in the cut-off region.

Note: no matter the switch state for the reverse polarity condition, the MOSFETs will remain in cut-off.

S1 Closed

---

the gates of Q1 and Q2 are pulled to ground. This places the P-Channel in ohmic region (e.g. conducting) once fully turned on. The zener diode, D1, clamps VGS > -10V and this ensures that VGS always sits within its safe bounds of VGS < +5/-16V.

****
Power Monitoring Specification
****

Specifications

- Vin = 0.0V - 80.0V

Slave Address

The values of A1 and A0 select the slave address of the device. Both selection inputs are pulled down, mapping to the address __ (update this).

Max Supported I2C Clock Frequency: 400kHz

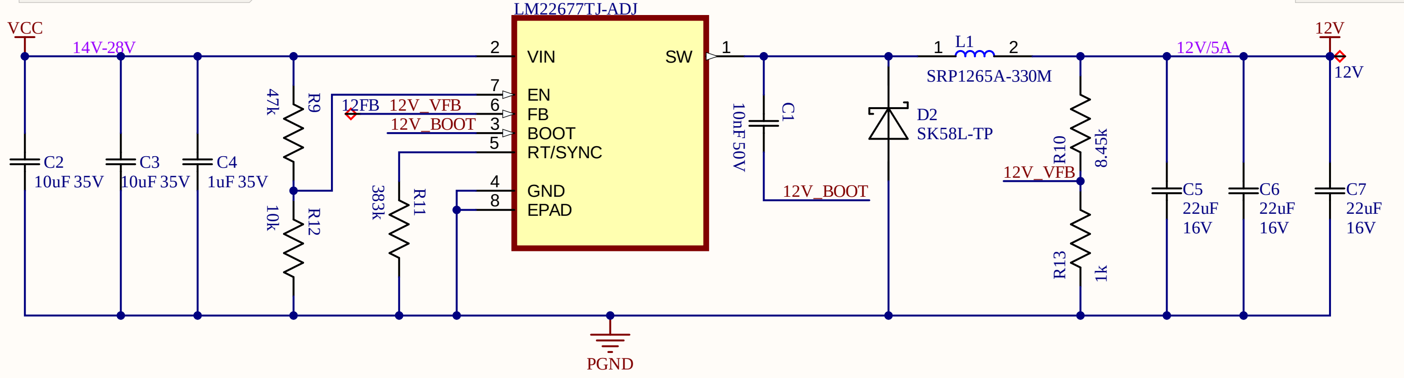
Title		
Size: A4	Number	Revision
Date: 1-29-2022		Sheet of
File: C:\Users\..\power-input.SchDoc		Drawn By: Hannah Sawiuk, Dannon Sturn

Additional capacitance provided by the capacitors in the flyback schematic

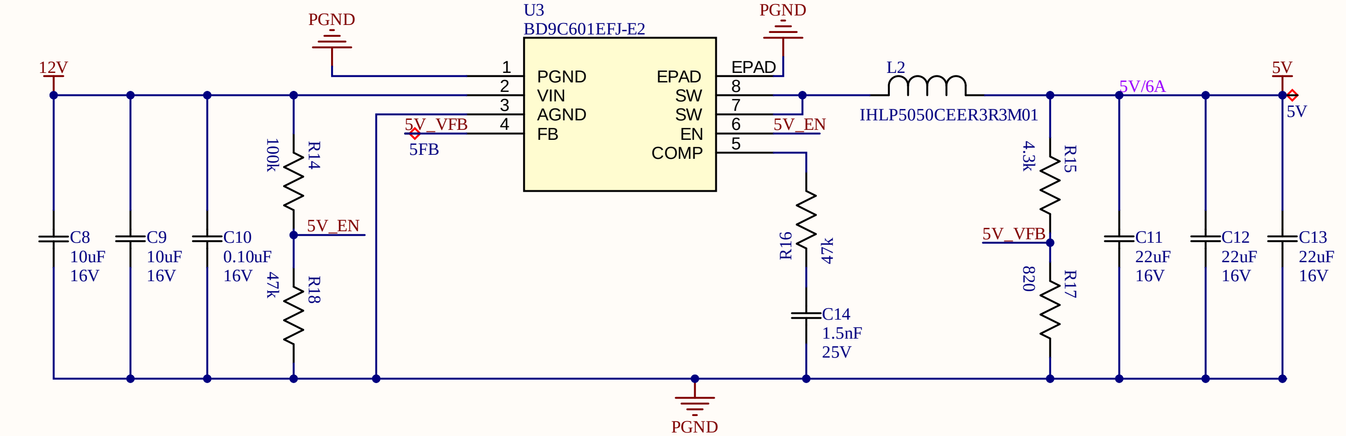
Voltage Conversion and Regulation

Verify Diode footprint

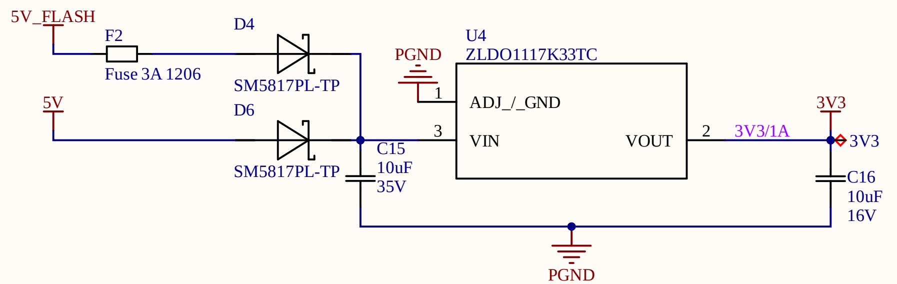
12V DC/DC Converter



5V DC/DC Converter



3.3V Fixed LDO



****
3.3V LDO
****

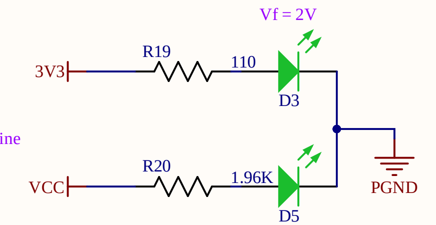
Simple 3.3V fixed LDO for supplying the MCU and various sensors.

Specifications

- Vin = 1.35V - 18.0V
- Vout = 3.3V
- Iout = 1.0A
- Pout = 3.3W

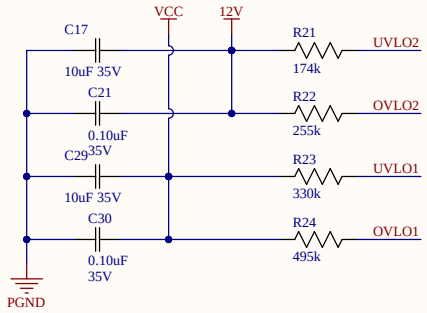
Power LEDs

~10mA to 15mA through each line



Dannon Stum

Overvoltage and Undervoltage Pins



****
OVLO/UVLO Configuration
****
The LT3751 provides user-programmable under and overvoltage lockouts for both VCC and VTRANS.

Note: typical UVLOx/OVLOx pin current = 50uA

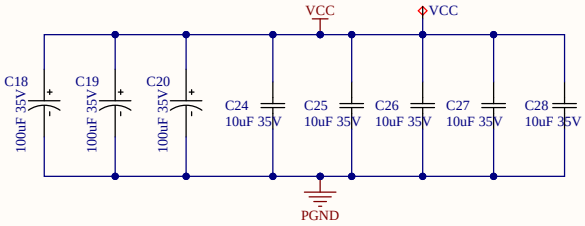
12V

VCC_Min = 10V
VCC_Max = 14V
Ruvlo2 = (VCC_MIN-1.225V)/50uA = 175.5k
Rovlo2 = (VCC_MAX-1.225V)/50uA = 255.5k

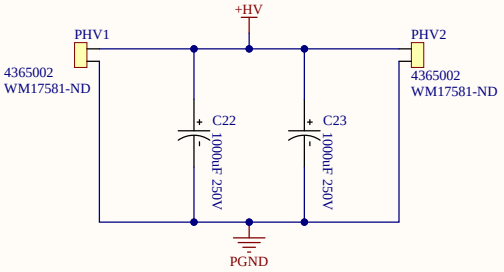
VCC

VBAT_Min = 18V
VBAT_Max = 26V
Ruvlo1 = (VBAT_MIN-1.225V)/50uA = 335.5k
Rovlo1 = (VBAT_MAX-1.225V)/50uA = 495.5k

Supply Bypass Capacitors

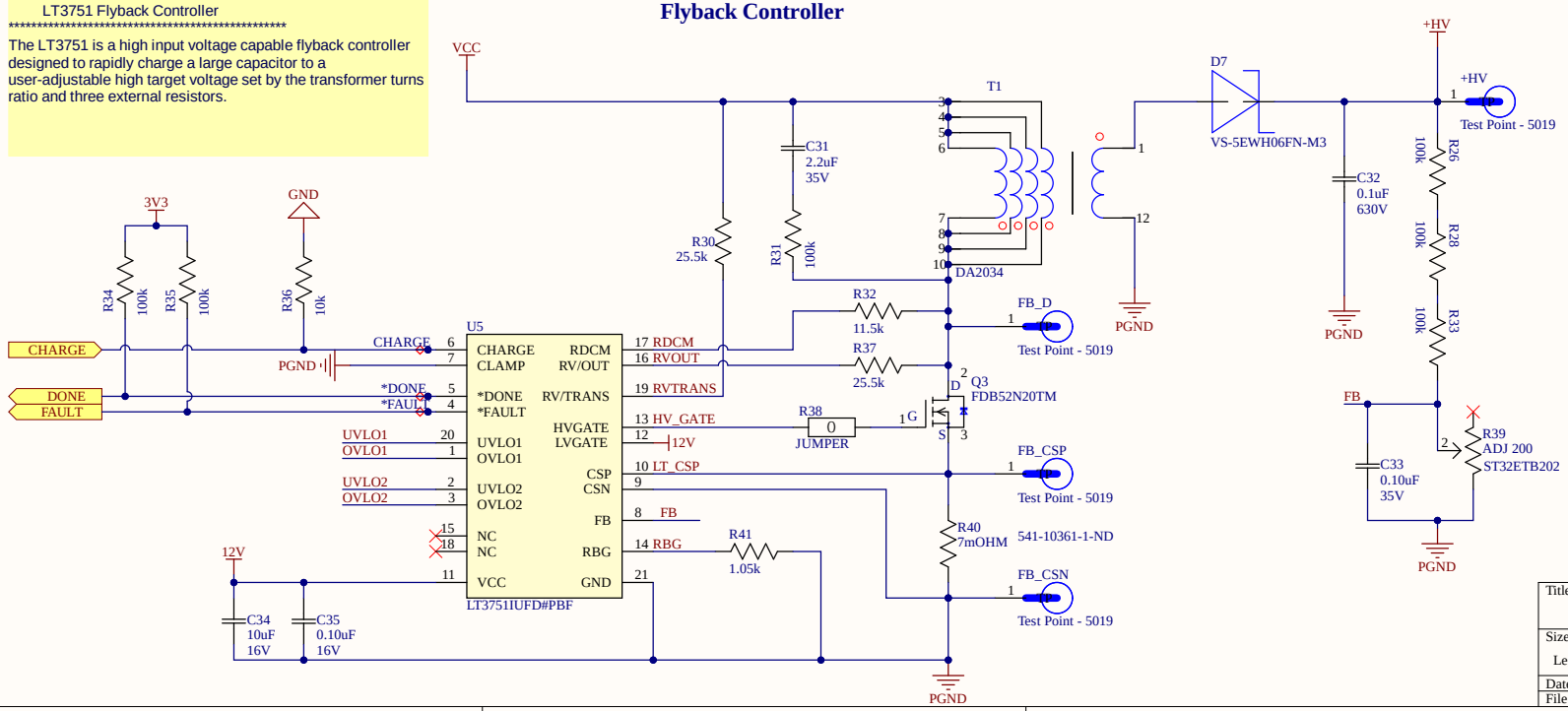


HV Capacitor Bank



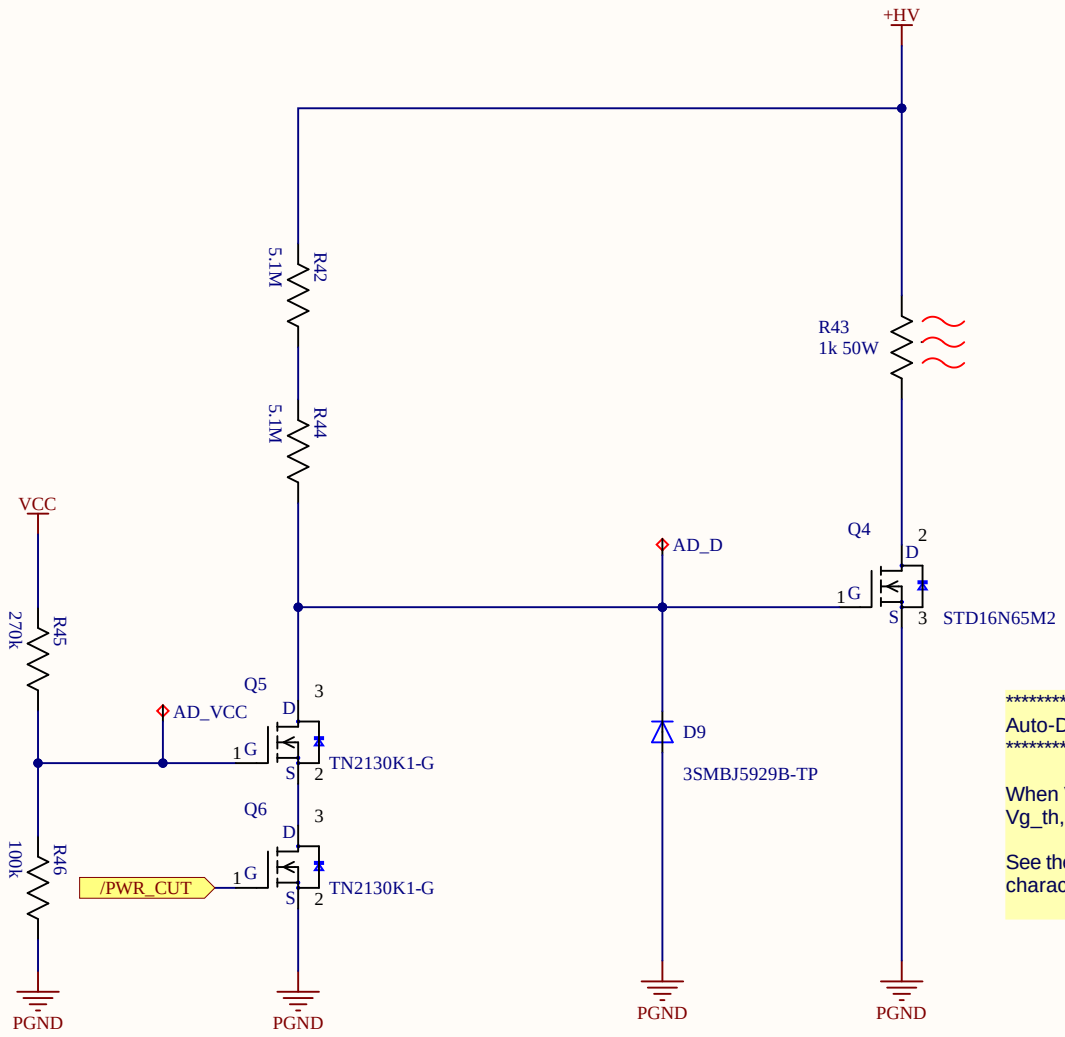
****
LT3751 Flyback Controller
****
The LT3751 is a high input voltage capable flyback controller designed to rapidly charge a large capacitor to a user-adjustable high target voltage set by the transformer turns ratio and three external resistors.

Flyback Controller



Title		
Size: Legal	Number	Revision
Date: 1-29-2022		Sheet of
File: C:\Users\..\flyback.SchDoc		Drawn By:Graham Whyte

Automatic High Voltage Discharge



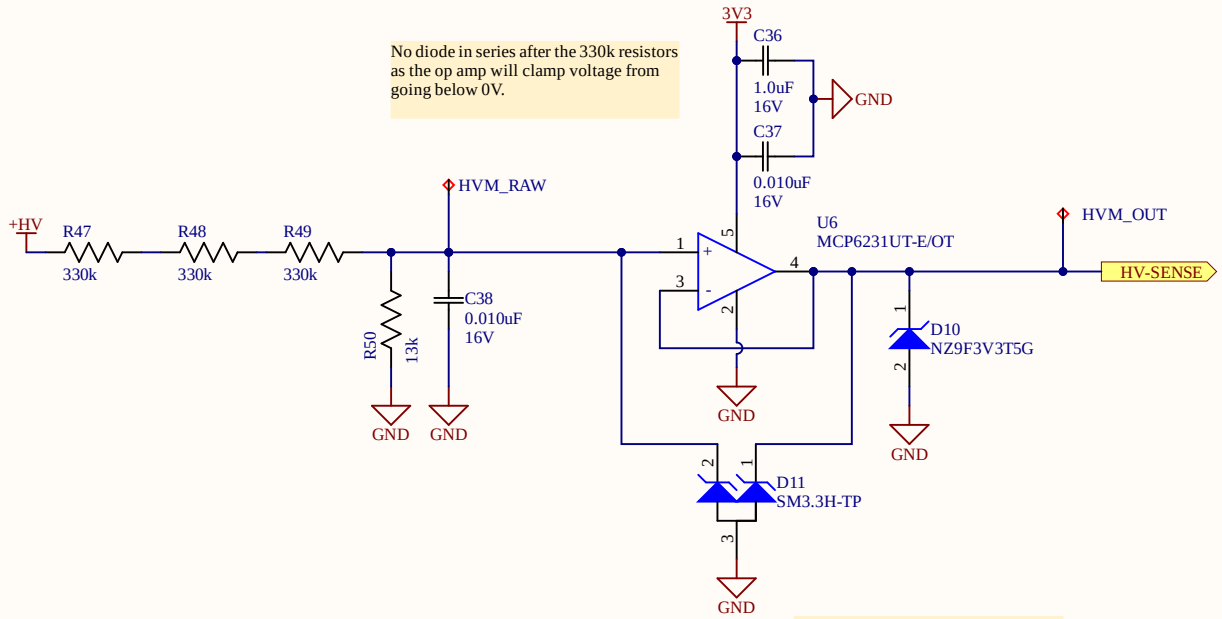
****
Auto-Discharge Circuit
****

When VCC drops such that the divided voltage is below BSS127 Vg_th, the STD11 gate is clamped to <15V, draining the +HV rail.

See the auto-discharge spice simulation for discharge characteristics.

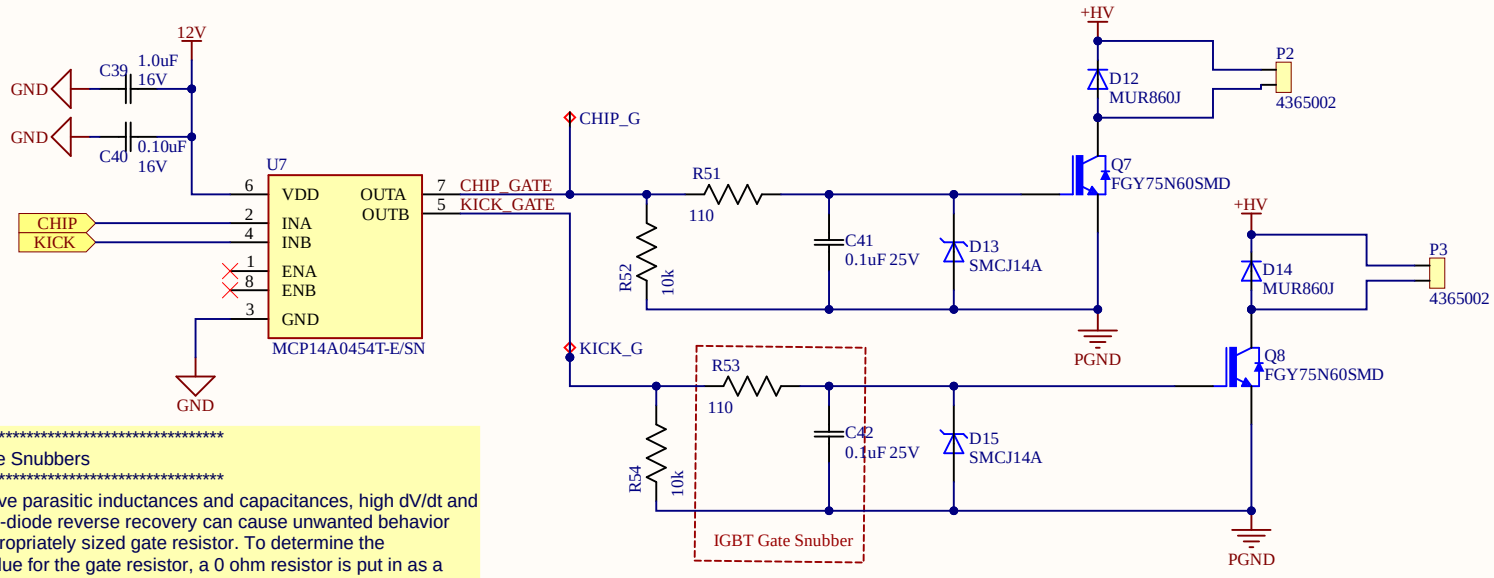
Title		
Size: A	Number	Revision
Date: 1-29-2022		Sheet of
File: C:\Users\..\auto-discharge.SchDoc		Drawn By: Simon Zheng

High Voltage Feedback



Title		
Size: A4	Number	Revision
Date: 1-29-2022		Sheet of
File: C:\Users\..\HV-Measurement.SchDoc		Drawn By: Dannon Sturn

Kick/Chip Solenoid Switch Control



****
Gate Snubbers
****
Transistors have parasitic inductances and capacitances, high dV/dt and di/dt, and body-diode reverse recovery can cause unwanted behavior without an appropriately sized gate resistor. To determine the appropriate value for the gate resistor, a 0 ohm resistor is put in as a placeholder and then ringing frequency is measured.

(1) Rg = R(hi or lo) + Rgate + Rg,i
(2) Ls = 1/Ciss(2*pi*f_r)^2
(3) Q = pi*Ls/Rg

Choose quality factor, Q, between 0.5 (critical damping) and 1.0 (underdamped)

See TI's document on "External Gate Resistor Design Guide for Gate Driver"

****
TVS Diodes
****
The IGBT gates are rated for Vge +/- 20V. To ensure transients > 20V do not damage the transistors, TVS diodes with a Reverse Working Voltage (VRWM) <= 20V is used.

Reverse Working Voltage (VRWM) is the specified voltage at which the device will draw only a very small leakage current.

****
10k Pulldown Resistors
****
In the case where the chip is not enabled but the HV capacitors are fully charged to 238V, then the gate of the IGBTs would be floating, and there could be the case where the gate rises above 12V, turning the IGBTs on. This could lead to a safety hazard due to the uncontrolled kicker/chipper action. By pulling down the gates with a 10k resistor, the IGBTs will remain off whenever the gate driver is not enabled.

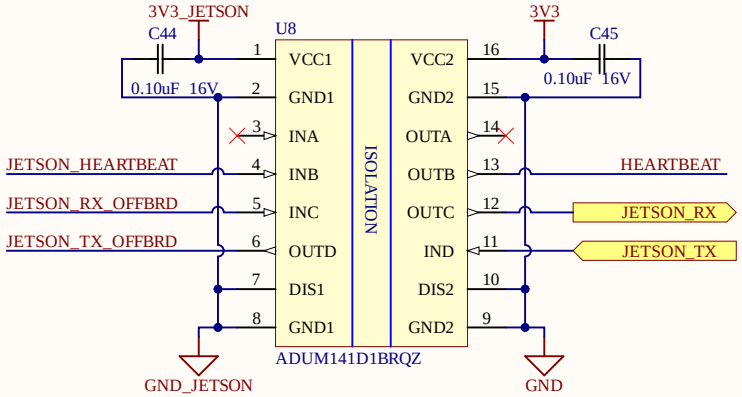
****
IGBTs: FGY75N60
****
IGBT Field Stop 600V 150A 750W

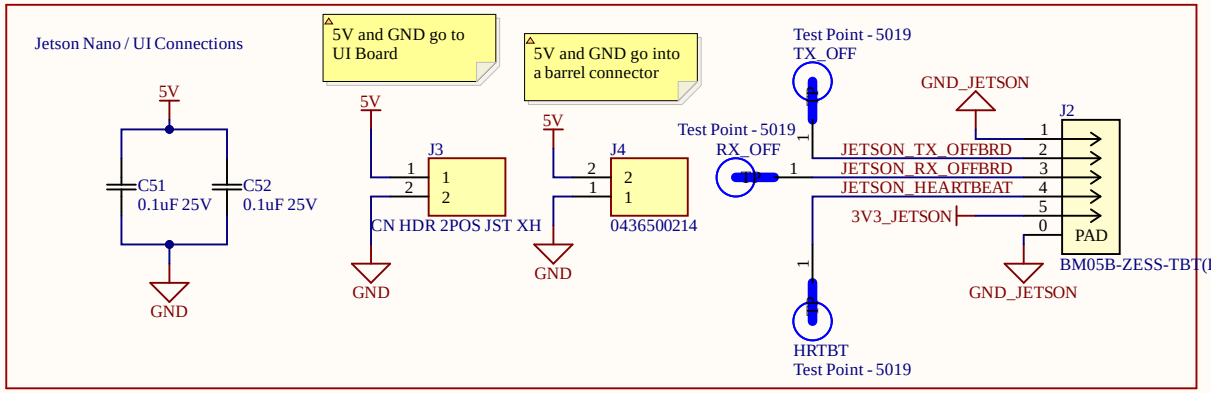
Figure 10:
Qg = 200nC @ Vge = 12V, Vcc = 250V

Title		
Size: A4	Number	Revision
Date: 1-29-2022		Sheet of
File: C:\Users\..\chicker.SchDoc		Drawn By: Hannah Sawiuk

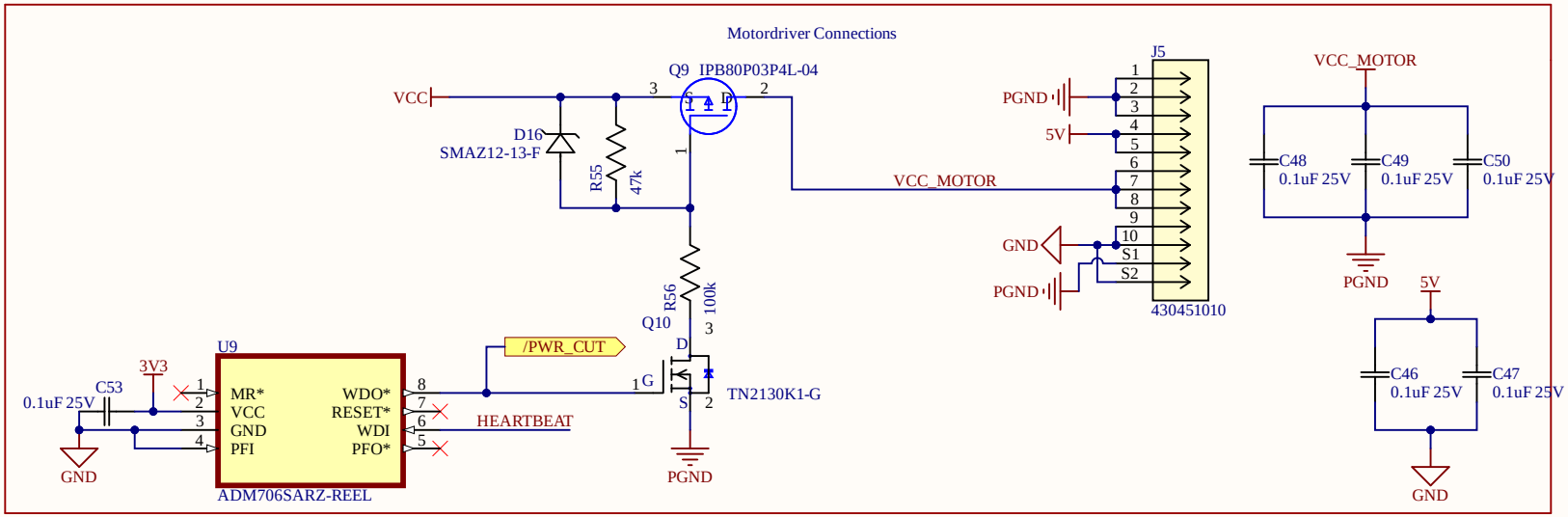
Interboard Signals/Rails

JETSON_TX is from the ESP to the Jetson.
JETSON_RX is from the Jetson to the ESP.
JETSON_TX_OFFBRD is the signal routed to the off board connector and JETSON_RX_OFFBRD is the signal routed from the off board connector.





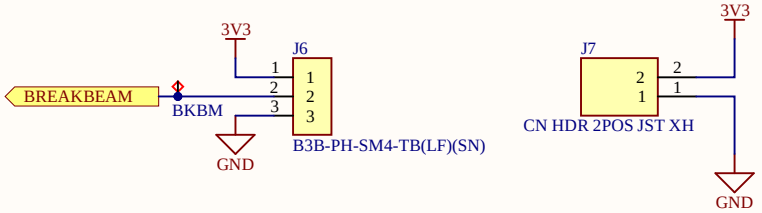
****
Isolation
****
Needed for the communication lines between the power monitor and the MCU given they are on seperate boards. GND return current passes through a seperate wire. This gives the freedom of placing this digital connector anywhere.



Capacitors are to filter and maintain the power rails before leaving the power board. This helps prevent the noise from the power board having an impact on other boards.

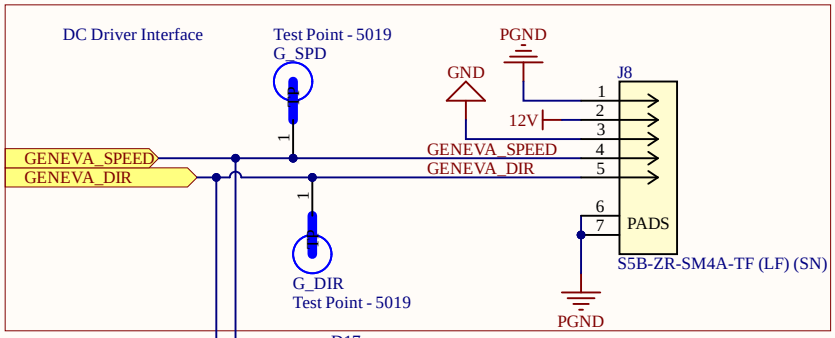
Title		
Size A4	Number	Revision
Date: 1-29-2022		Sheet of
File: C:\Users\..\communication.SchDoc		Drawn By: Simon Zheng, Dannon Sturn

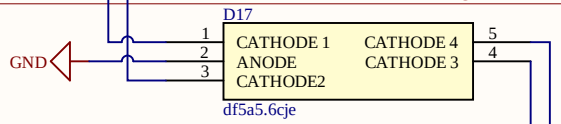
Breakbeam Interface

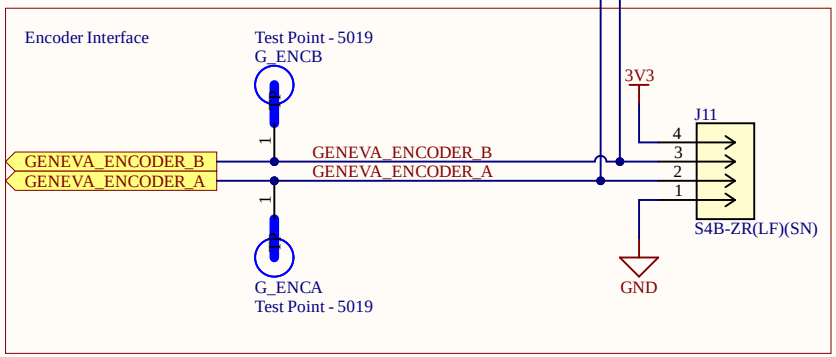


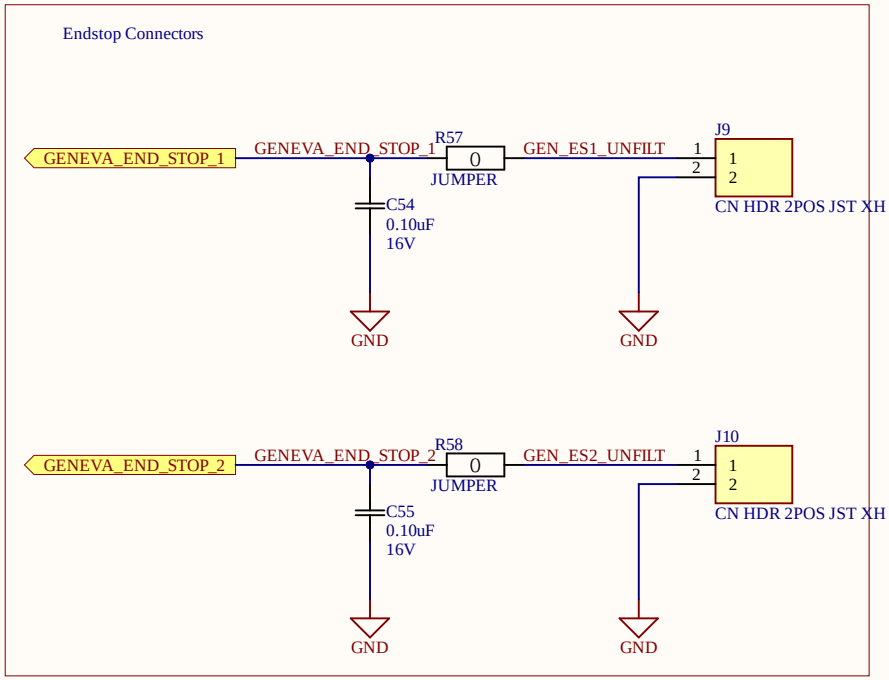
Title		
Size: A4	Number	Revision
Date: 1-29-2022		Sheet of
File: C:\Users\..\breakbeam-interface.SchDoc		Drawn By:

Geneva Interface

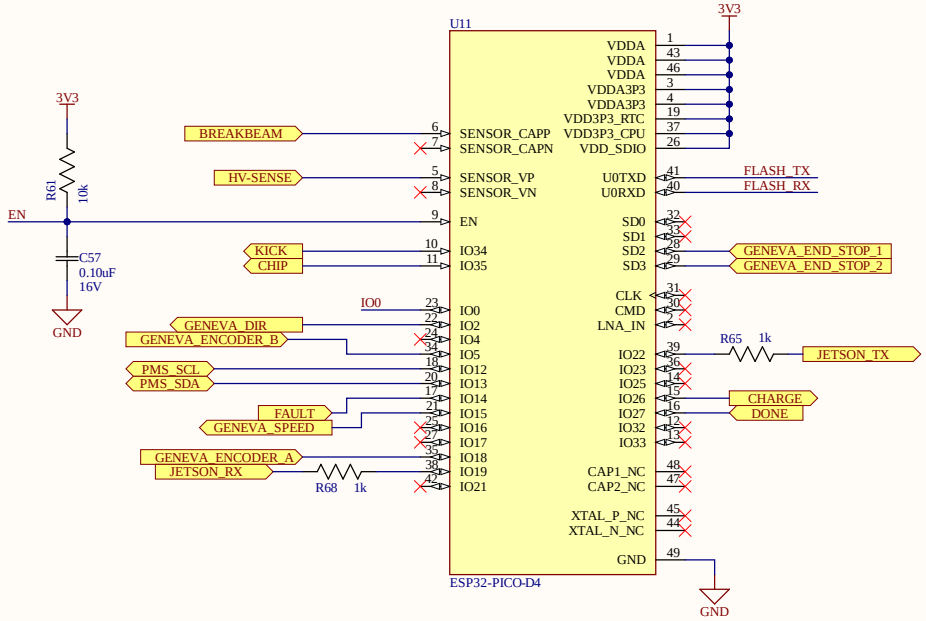


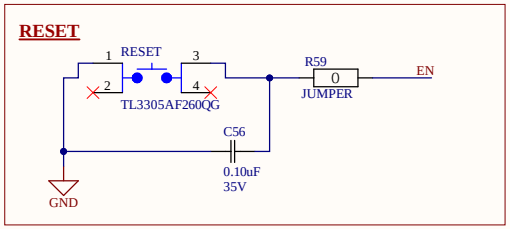


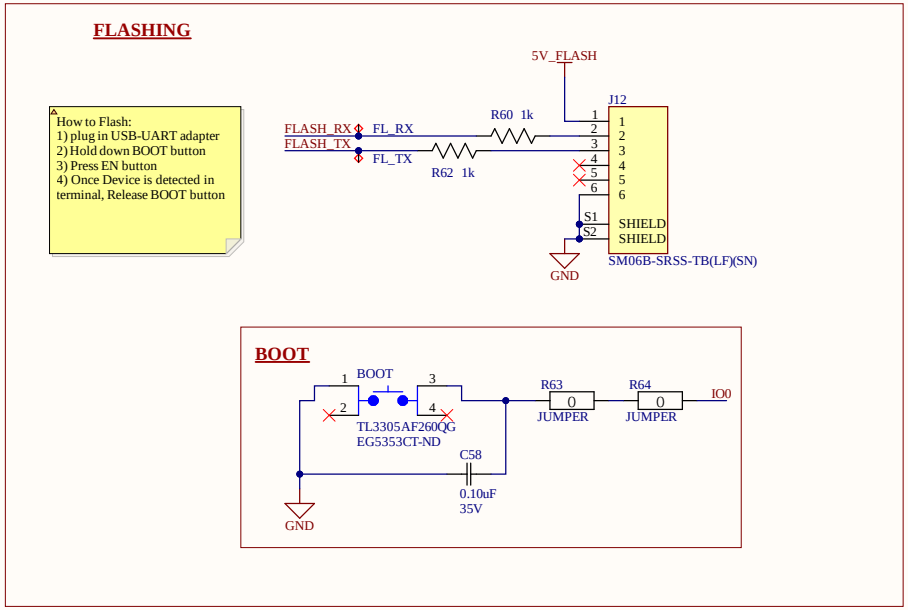


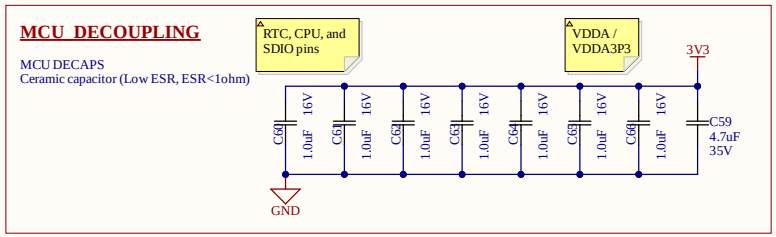


Title		
Size: A4	Number	Revision
Date: 1-29-2022		Sheet of
File: C:\Users\..\geneva-interface.SchDoc		Drawn By:

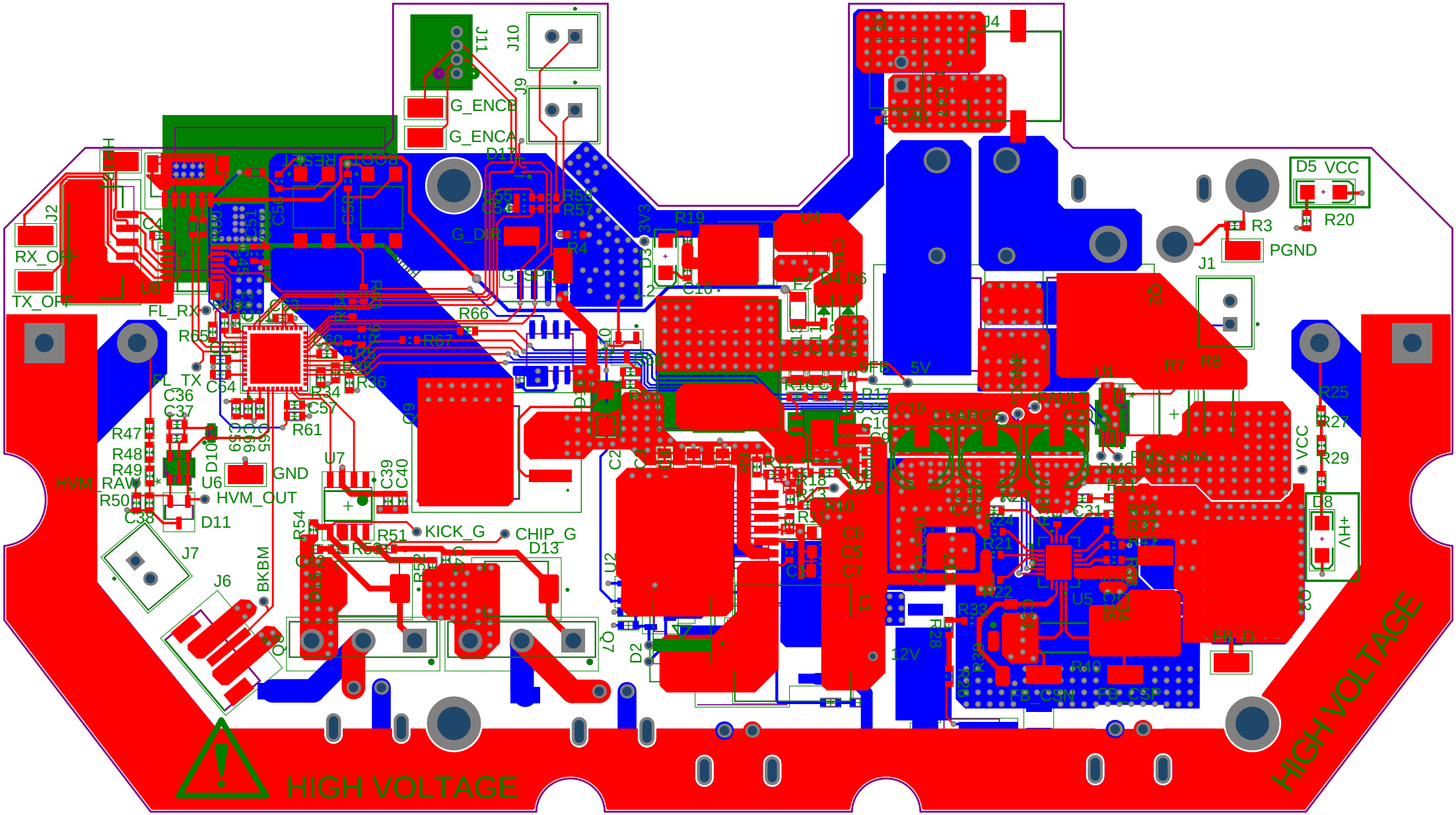








Title		
Size: B	Number	Revision
Date: 1-29-2022		Sheet of
File: C:\Users\..\Power-MCU-Breakout.SchDoc		Drawn By: Dannon Stum


G_ENCB
G_ENCA
RX_OFF
TX_OFF
FL_RX
FL_TX
HVM_RAW
HVM_OUT
GND
KICK_G
CHIP_G
BKBM
D5 VCC
PGND
5V
12V
CHARGE
FAULT
PMS_SDA
PMS_SCL
VCC
+HV
FB_D
HIGH VOLTAGE
HIGH VOLTAGE