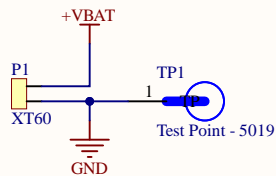


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File:	D:\Users\...\power-v3.1.SchDoc	Drawn By: Simon Zheng

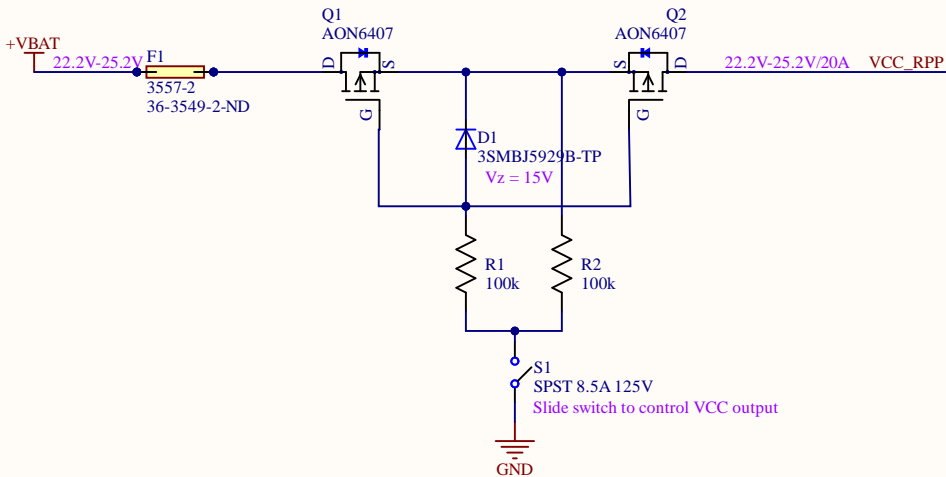
Power Input and Monitoring

Battery Connector

Breakout to 2 x 3S LiPo: 22.2V-25.2V



Reverse Polarity Protection



Reverse Polarity Protection Design Specifications

Reverse Polarity

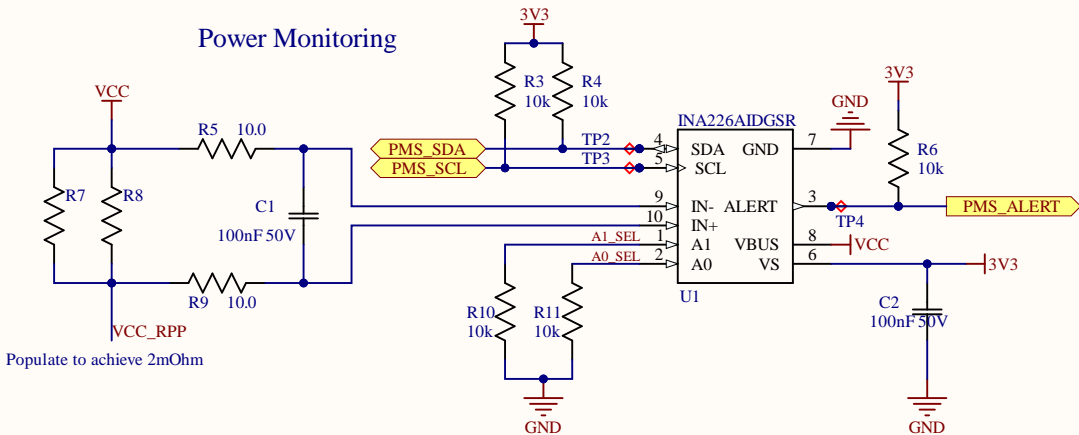
Under the condition that a negative potential is applied across the battery input, current flow will be blocked. This is because the reverse polarity causes the body diode of the MOSFET to be reverse biased. Then,  $V_G = |V_{BAT}| > 0V$  and so P-Channel MOSFET will be in the cut-off region.

Note: no matter the switch state for the reverse polarity condition, the MOSFETs will remain in cut-off.

S1 Closed

the gates of Q1 and Q2 are pulled to ground. This places the P-Channel in ohmic region (e.g. conducting) once fully turned on. The zener diode, D1, clamps  $V_{GS} < \pm 15V$  and this ensures that  $V_{GS}$  always sits within its safe bounds of  $V_{GS} < \pm 25V$ .

Power Monitoring



Power Monitoring Specification

The INA226 is a current shunt and power monitor with an I2C interface. The device monitors both a shunt voltage drop and bus supply voltage.

Specifications

- $V_{in} = 0.0V - 36.0V$
- $V_{supply} = 2.7V - 5V$

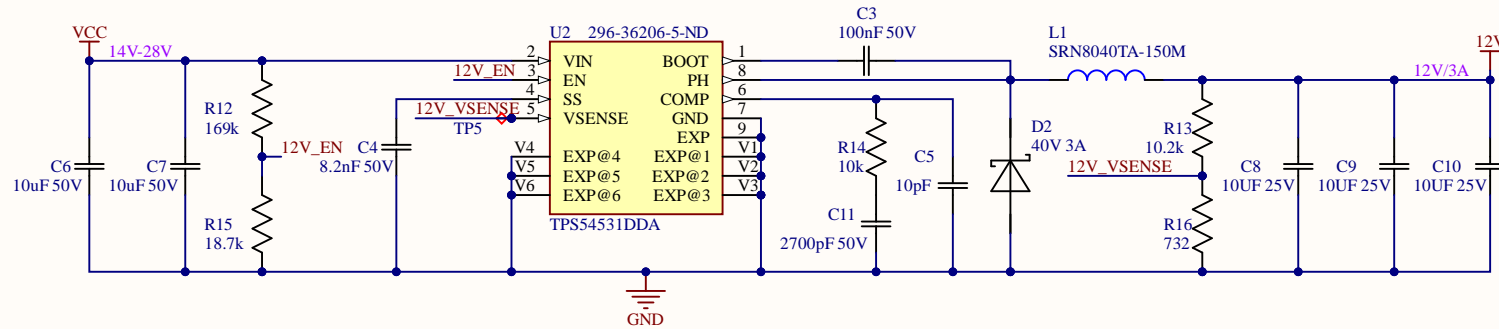
Slave Address

The values of A1 and A0 select the slave address of the device. Both selection inputs are pulled down, mapping to the address 1000000.

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# Voltage Conversion and Regulation

## 12V DC/DC Converter



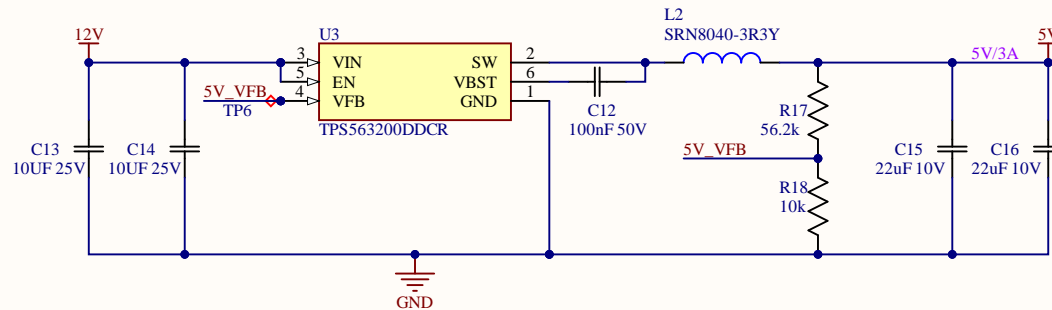
### 12V DC/DC Converter Specifications

Designed using Texas Instruments WEBENCH software. The design report, charts, BOMs, simulation exports, and more can be found in doc/12V-dc\_dc-converter-design/. The converter takes in the batter/supply voltage and steps it down to 12V.

### Specifications

- Vin = 14.0V - 28.0V
- Vout = 12.0V
- Iout = 3.0A
- Vripple = 5%
- Frequency = 570.0 kHz
- Pout = 36.0 W

## 5V DC/DC Converter



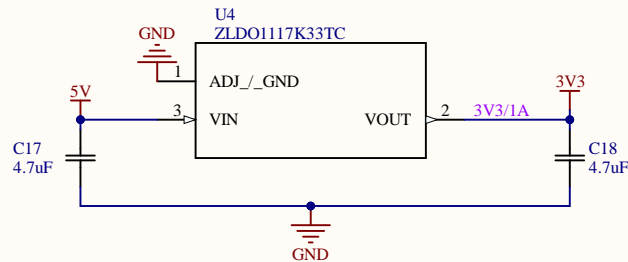
### 5V DC/DC Converter Specifications

Designed using Texas Instruments WEBENCH software. The full design report can be found in doc/5V-dc\_dc-converter-design/. The converter takes the 12V and steps it down to 5V.

### Specifications

- Vin = 11.0V - 13.0V
- Vout = 5.0V
- Iout = 3.0A
- Frequency = 791.515 kHz
- Pout = 15.0 W

## 3.3V Fixed LDO



### 3.3V LDO

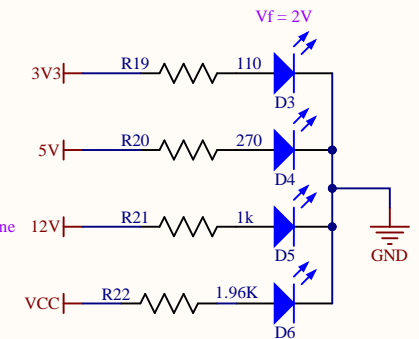
Simple 3.3V fixed LDO for supplying the MCU and various sensors.

### Specifications

- Vin = 1.35V - 18.0V
- Vout = 3.3V
- Iout = 1.0A
- Pout = 3.3W

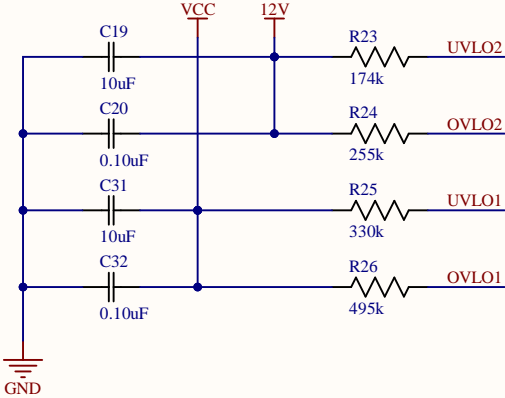
## Power LEDs

~10mA to 15mA through each line



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Overvoltage and Undervoltage Pins



OVLO/UVLO Configuration

The LT3751 provides user-programmable under and overvoltage lockouts for both VCC and VTRANS.

Note: typical UVLOx/OVLOx pin current = 50uA

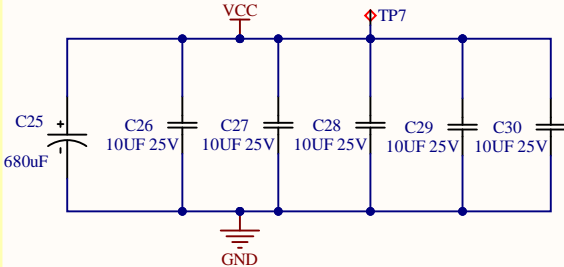
12V

VCC\_Min = 10V  
VCC\_Max = 14V  
Ruvlo2 = (VCC\_MIN-1.225V)/50uA = 175.5k  
Rovlo2 = (VCC\_MAX-1.225V)/50uA = 255.5k

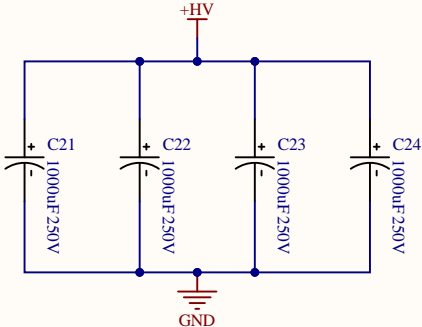
VCC

VBAT\_Min = 18V  
VBAT\_Max = 26V  
Ruvlo1 = (VBAT\_MIN-1.225V)/50uA = 335.5k  
Rovlo1 = (VBAT\_MAX-1.225V)/50uA = 495.5k

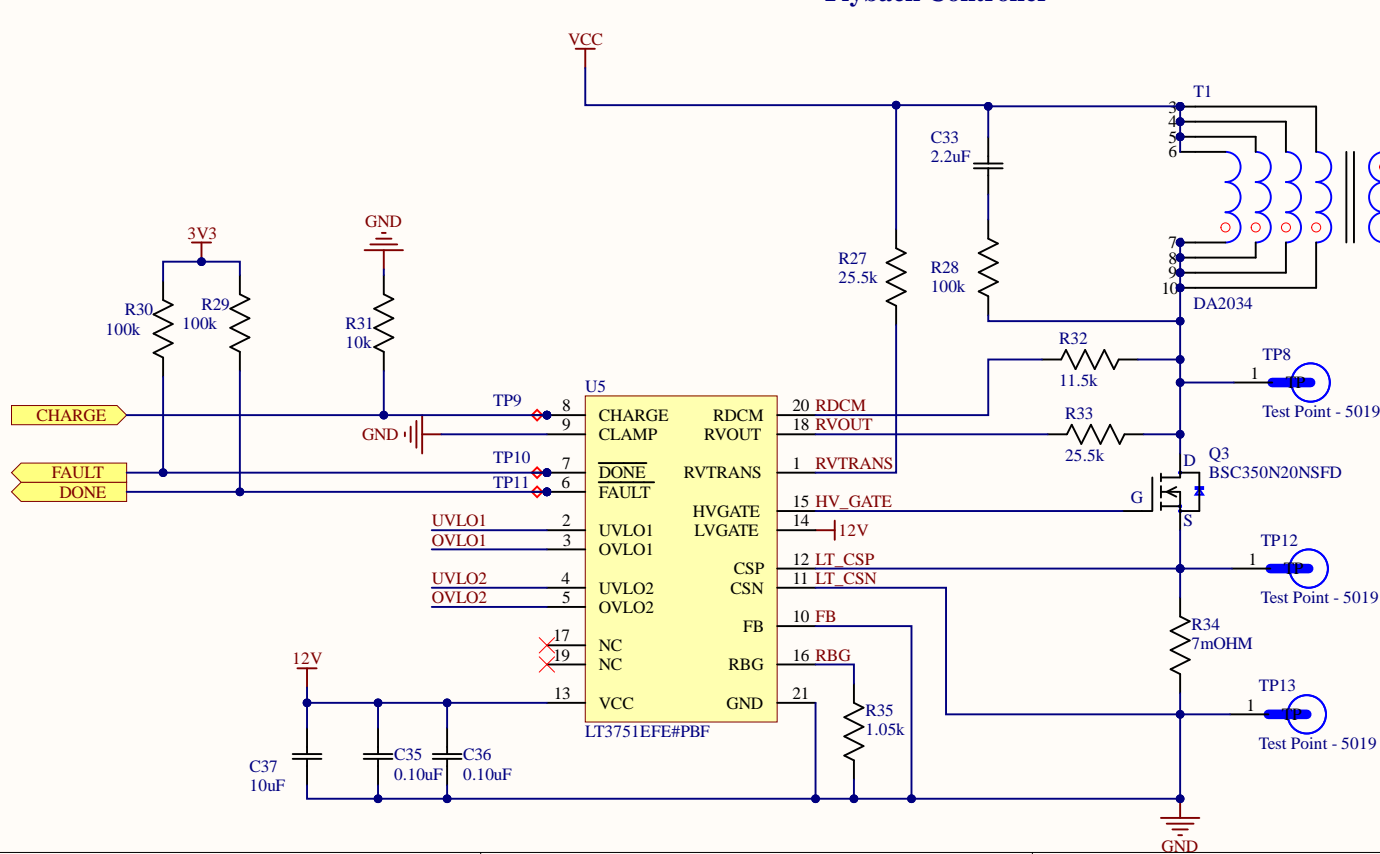
Supply Bypass Capacitors



HV Capacitor Bank



Flyback Controller

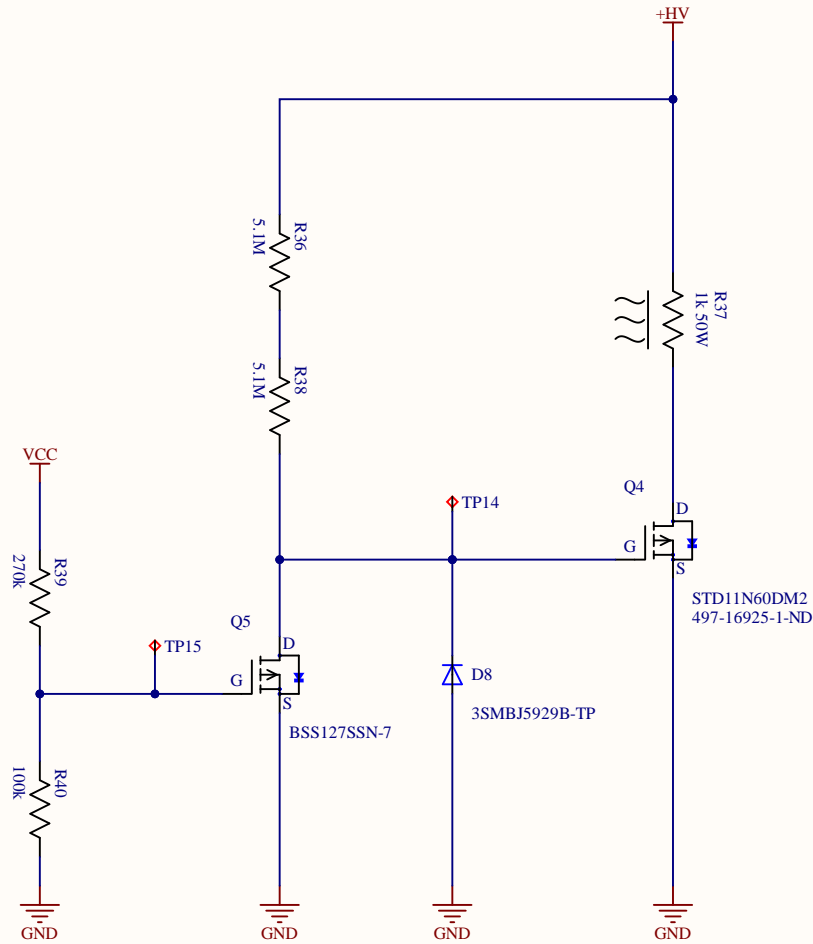


LT3751 Flyback Controller

The LT3751 is a high input voltage capable flyback controller designed to rapidly charge a large capacitor to a user-adjustable high target voltage set by the transformer turns ratio and three external resistors.

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Date: 1/07/2021	Sheet of	
File: D:\Users\...\flyback.SchDoc	Drawn By: Graham Whyte	

Automatic High Voltage Discharge



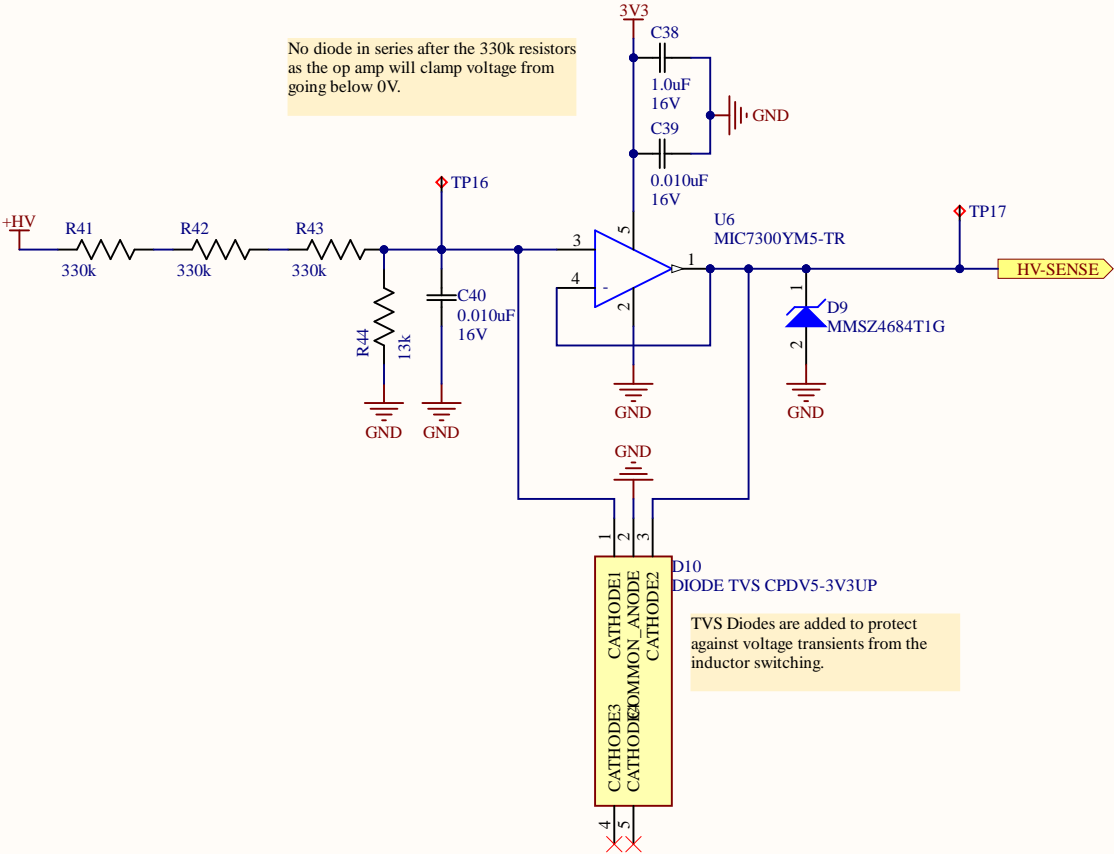
\*\*\*\*\*  
Auto-Discharge Circuit  
\*\*\*\*\*

When VCC drops such that the divided voltage is below BSS127 Vg\_th, the STD11 gate is clamped to <15V, draining the +HV rail.

See the auto-discharge spice simulation for discharge characteristics.

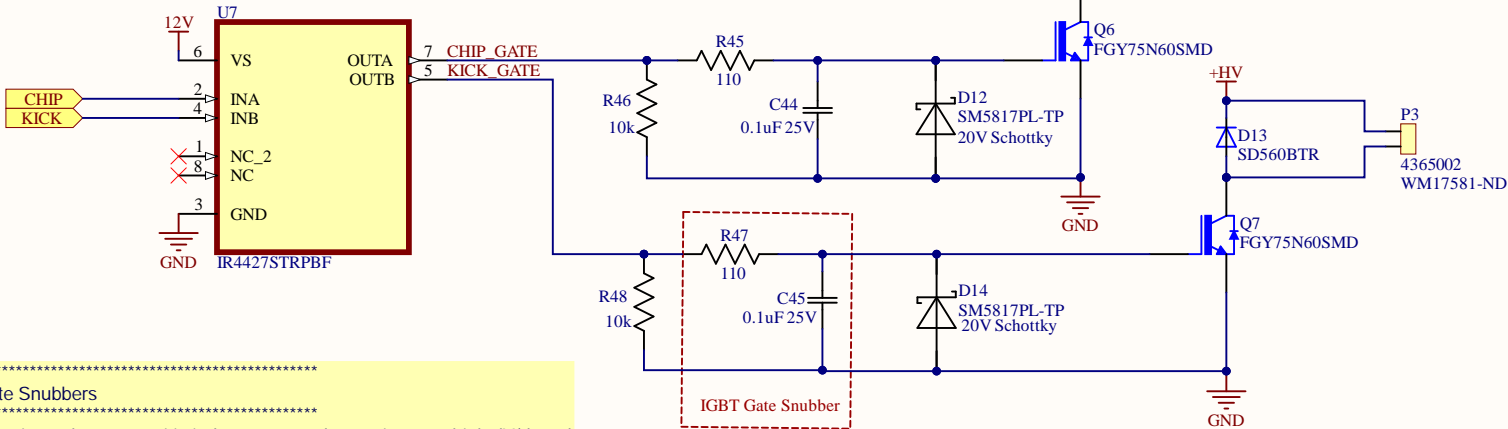
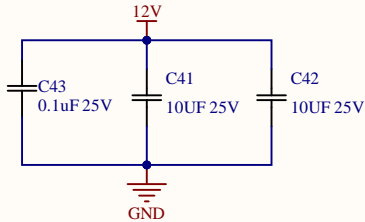
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File:	D:\Users\...\auto-discharge.SchDoc	Drawn By: Simon Zheng

High Voltage Feedback



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File:	D:\Users\...\HV-Measurement.SchDoc	Drawn By: Dannon Sturn

Kick/Chip Solenoid Switch Control



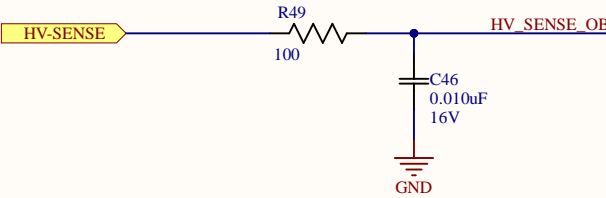
\*\*\*\*\*  
Gate Snubbers  
\*\*\*\*\*  
Transistors have parasitic inductances and capacitances, high dV/dt and di/dt, and body-diode reverse recovery can cause unwanted behavior without an appropriately sized gate resistor. To determine the appropriate value for the gate resistor, a 0 ohm resistor is put in as a placeholder and then ringing frequency is measured.  
  
(1)  $R_g = R(h_i \text{ or } l_o) + R_{gate} + R_{g,i}$   
(2)  $L_s = 1/C_{iss}(2\pi f_r)^2$   
(3)  $Q = \pi L_s / R_g$   
  
Choose quality factor, Q, between 0.5 (critical damping) and 1.0 (underdamped)  
  
See TI's document on "External Gate Resistor Design Guide for Gate Driver"  
  
\*\*\*\*\*  
TVS Diodes  
\*\*\*\*\*  
The IGBT gates are rated for  $V_{ge} \pm 20V$ . To ensure transients > 20V do not damage the transistors, TVS diodes with a Reverse Working Voltage (VRWM) <= 20V is used.  
  
Reverse Working Voltage (VRWM) is the specified voltage at which the device will draw only a very small leakage current.

\*\*\*\*\*  
IGBTs: FG75N60  
\*\*\*\*\*  
IGBT Field Stop 600V 150A 750W  
  
Figure 10:  
 $Q_g = 200nC @ V_{ge} = 12V, V_{cc} = 250V$

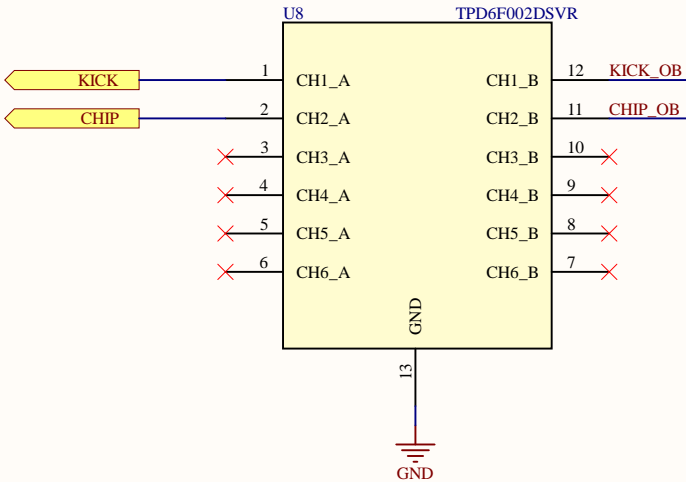
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File:	D:\Users\...\chicker.SchDoc	Drawn By: Hannah Sawiuk

Interboard Signals/Rails

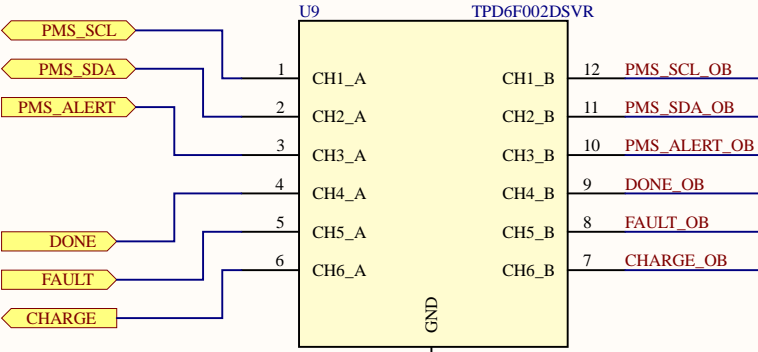
HV Feedback



Solenoid Gate Control

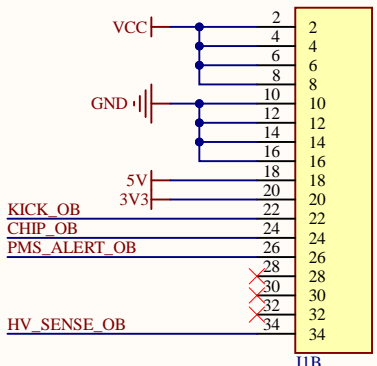
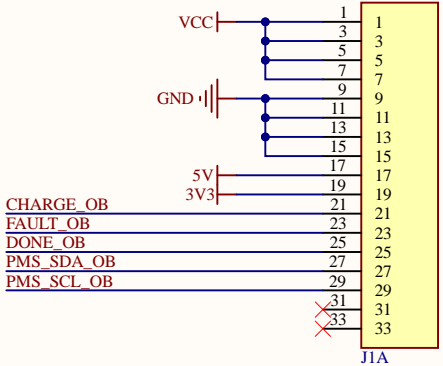


PMIC Signals



Flyback Logic Signals

EMI Filters  
\*\*\*\*\*  
Needed for the communication lines between the power monitor and the MCU given they are on separate boards,  
\*\*\*\*\*



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