



## 1. Description

### 1.1. Project

Project Name	h5dev
Board Name	custom
Generated with:	STM32CubeMX 6.15.0
Date	02/07/2026

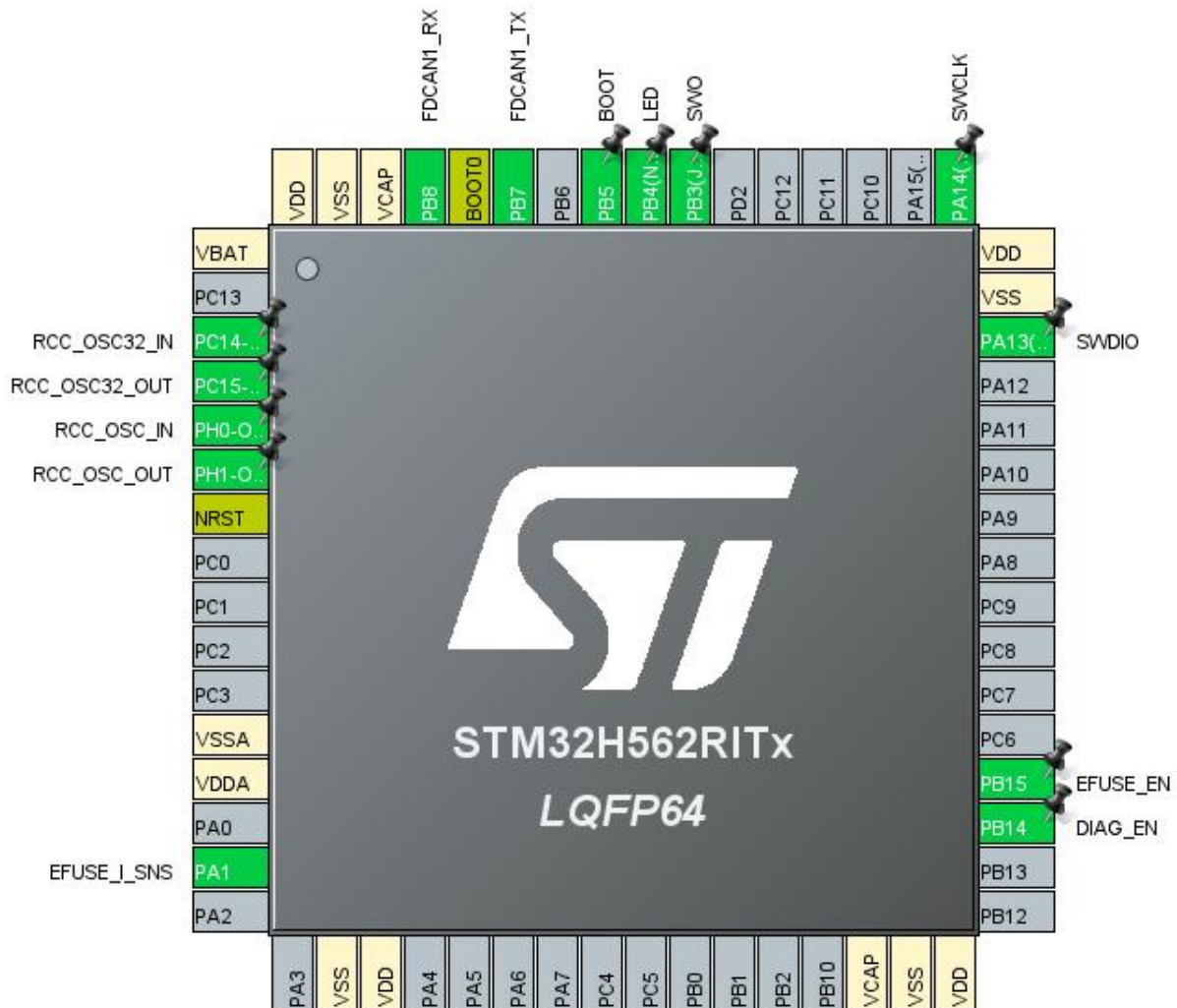
### 1.2. MCU

MCU Series	STM32H5
MCU Line	STM32H562
MCU name	STM32H562RITx
MCU Package	LQFP64
MCU Pin number	64

### 1.3. Core(s) information

Core(s)	ARM Cortex-M33
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## 2. Pinout Configuration

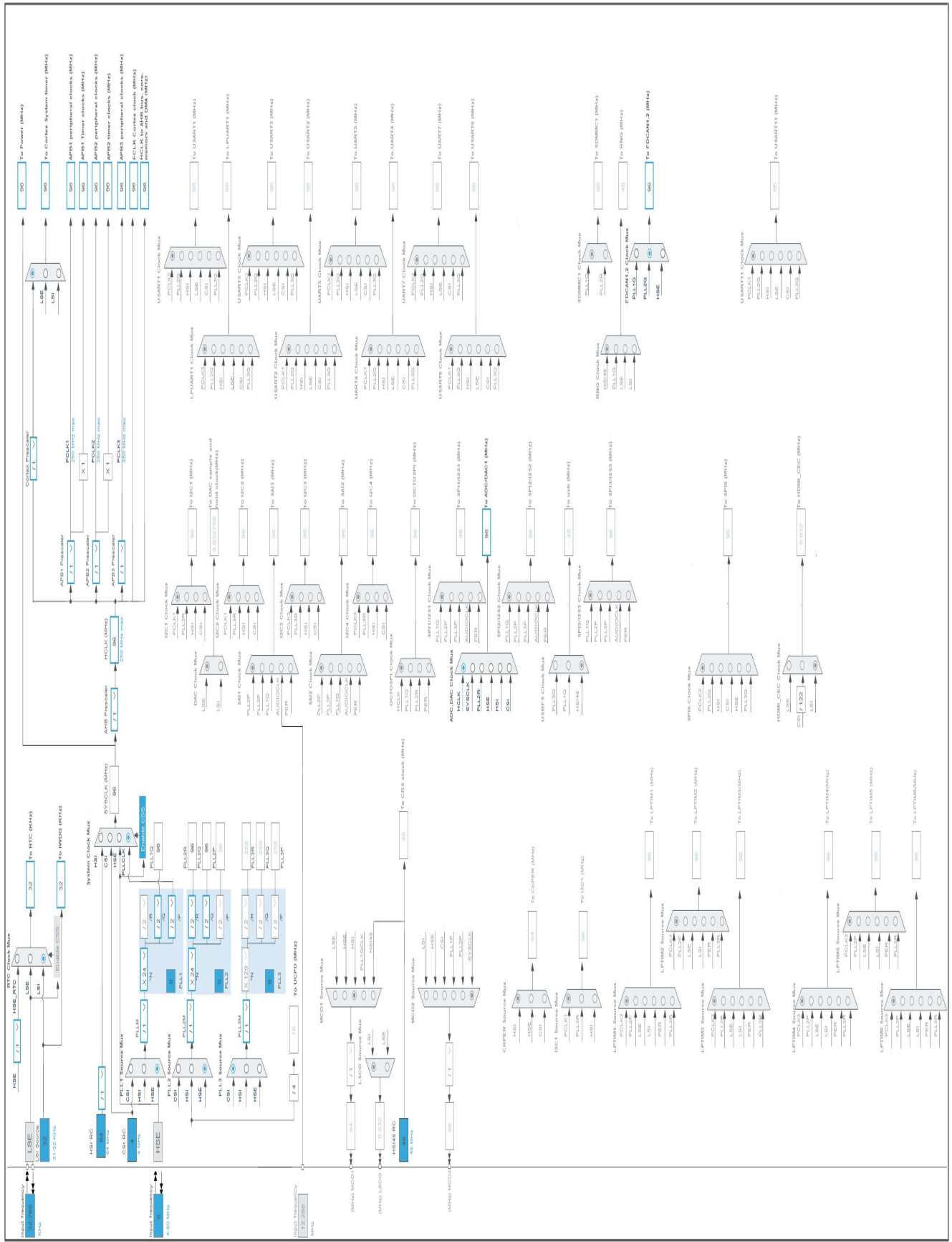


### 3. Pins Configuration

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
3	PC14- OSC32_IN(OSC32_IN)	I/O	RCC_OSC32_IN	
4	PC15- OSC32_OUT(OSC32_OUT)	I/O	RCC_OSC32_OUT	
5	PH0-OSC_IN(PH0)	I/O	RCC_OSC_IN	
6	PH1-OSC_OUT(PH1)	I/O	RCC_OSC_OUT	
7	NRST	Reset		
12	VSSA	Power		
13	VDDA	Power		
15	PA1	I/O	ADC1_INP1	EFUSE_I_SNS
18	VSS	Power		
19	VDD	Power		
30	VCAP	Power		
31	VSS	Power		
32	VDD	Power		
35	PB14 *	I/O	GPIO_Output	DIAG_EN
36	PB15 *	I/O	GPIO_Output	EFUSE_EN
46	PA13(JTMS/SWDIO)	I/O	DEBUG_JTMS-SWDIO	SWDIO
47	VSS	Power		
48	VDD	Power		
49	PA14(JTCK/SWCLK)	I/O	DEBUG_JTCK-SWCLK	SWCLK
55	PB3(JTDO/TRACESWO)	I/O	DEBUG_JTDO-SWO	SWO
56	PB4(NJTRST) *	I/O	GPIO_Output	LED
57	PB5 *	I/O	GPIO_Output	BOOT
59	PB7	I/O	FDCAN1_TX	
60	BOOT0	Boot		
61	PB8	I/O	FDCAN1_RX	
62	VCAP	Power		
63	VSS	Power		
64	VDD	Power		

\* The pin is affected with an I/O function

## 4. Clock Tree Configuration



## 1. Power Consumption Calculator report

### 1.1. Microcontroller Selection

Series	STM32H5
Line	STM32H562
MCU	STM32H562RITx
Datasheet	DS00000_Rev0

### 1.2. Parameter Selection

Temperature	25
Vdd	3.0

### 1.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

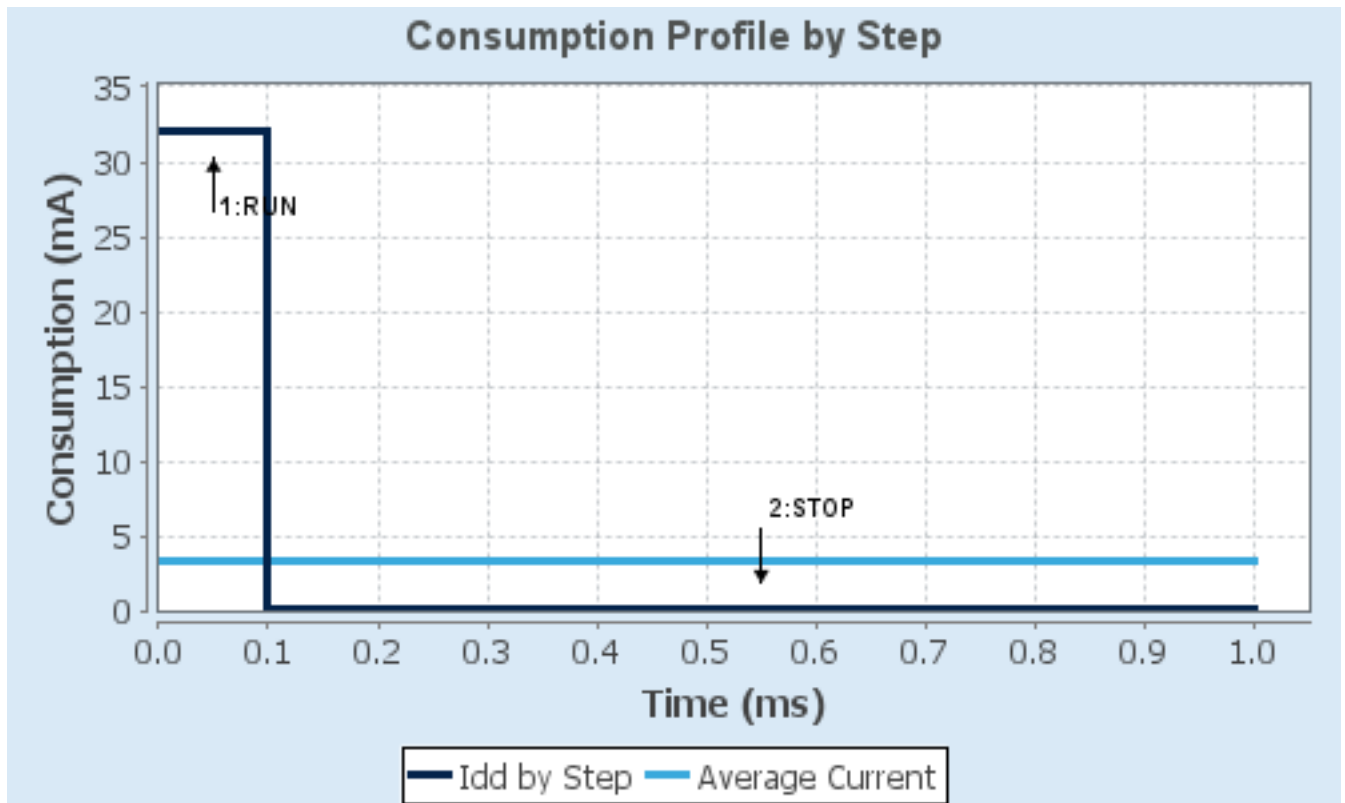
#### 1.4. Sequence

<b>Step</b>	Step1	Step2
<b>Mode</b>	RUN	STOP
<b>Vdd</b>	3.0	3.0
<b>Voltage Source</b>	Battery	Battery
<b>Range</b>	VOS0: Scale0	SVOS5: System-Scale5/SMPS
<b>Fetch Type</b>	FLASH_ON/Cache2Ways_A LL RAM RETENTION	Flash- PwrDwn PwrDwnStop OFF
<b>CPU Frequency</b>	250 MHz	0 Hz
<b>Clock Configuration</b>	HSE BYP PLL	ALL CLOCKS OFF
<b>Clock Source Frequency</b>	8 MHz	0 Hz
<b>Peripherals</b>		
<b>Additional Cons.</b>	0 mA	0 mA
<b>Average Current</b>	32 mA	51.5 $\mu$ A
<b>Duration</b>	0.1 ms	0.9 ms
<b>DMIPS</b>	535.0	0.0
<b>Ta Max</b>	120.68	124.99
<b>Category</b>	In DS Table	In DS Table

#### 1.5. Results

Sequence Time	1 ms	Average Current	3.25 mA
Battery Life	1 month, 13 days, 4 hours	Average DMIPS	535.0 DMIPS

#### 1.6. Chart





## 2. Software Project

### 2.1. Project Settings

Name	Value
Project Name	h5dev
Project Folder	C:\programs\Formula-Electric\Consolidated-
Toolchain / IDE	EWARM V9.20
Firmware Package Name and Version	STM32Cube FW_H5 V1.5.0
Application Structure	Advanced
Generate Under Root	No
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

### 2.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

### 2.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_GPDMA1_Init	GPDMA1
4	MX_FDCAN1_Init	FDCAN1
5	MX_IWDG_Init	IWDG
6	MX_RTC_Init	RTC
7	MX_TIM3_Init	TIM3
8	MX_ADC1_Init	ADC1

## 3. Peripherals and Middlewares Configuration

### 3.1. ADC1

#### IN1: IN1 Single-ended

##### 3.1.1. Parameter Settings:

##### ADCs\_Common\_Settings:

Mode Independent mode

##### ADC\_Settings:

Clock Prescaler	Asynchronous clock mode divided by 2
Resolution	ADC 12-bit resolution
Scan Conversion Mode	Disabled
Data Alignment	Right alignment
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data preserved
Conversion Data Management Mode	Regular Conversion data stored in DR register only
Low Power Auto Wait	Disabled

##### ADC\_Regular\_ConversionMode:

Enable Regular Conversions	Enable
Enable Regular Oversampling	Disable
Number Of Conversion	1
External Trigger Conversion Source	<b>Timer 3 Trigger Out event *</b>
External Trigger Conversion Edge	Trigger detection on the rising edge
Sampling Mode	Normal
<u>Rank</u>	1
Channel	Channel 1
Sampling Time	2.5 Cycles
Offset Number	No offset
Monitored by	None

##### ADC\_Injected\_ConversionMode:

Enable Injected Conversions Disable

##### Analog Watchdog 1:

Enable Analog WatchDog1 Mode false

##### Analog Watchdog 2:

Enable Analog WatchDog2 Mode false

##### Analog Watchdog 3:

Enable Analog WatchDog3 Mode false

### 3.2. BOOTPATH

mode: Activated

### 3.3. DEBUG

Debug: Trace Asynchronous Sw

### 3.4. FDCAN1

mode: Activated

#### 3.4.1. Parameter Settings:

##### Basic Parameters:

Clock Divider	Divide kernel clock by 1
Frame Format	<b>FD mode without BitRate Switching *</b>
Mode	Normal mode
Auto Retransmission	<b>Enable *</b>
Transmit Pause	Disable
Protocol Exception	Disable
Nominal Sync Jump Width	<b>2 *</b>
Data Prescaler	<b>3 *</b>
Data Sync Jump Width	<b>2 *</b>
Data Time Seg1	<b>5 *</b>
Data Time Seg2	<b>2 *</b>
Std Filters Nbr	<b>1 *</b>
Ext Filters Nbr	<b>1 *</b>
Tx Fifo Queue Mode	FIFO mode

##### Bit Timings Parameters:

Nominal Prescaler	<b>6 *</b>
Nominal Time Quantum	<b>62.5 *</b>
Nominal Time Seg1	<b>13 *</b>
Nominal Time Seg2	<b>2 *</b>
Nominal Time for one Bit	1000
Nominal Baud Rate	<b>1000000 *</b>

### 3.5. IWDG

**mode: Activated**

#### 3.5.1. Parameter Settings:

**Watchdog Clocking:**

IWDG counter clock prescaler	4
IWDG window value	4095
IWDG down-counter reload value	4095

**Watchdog Interrupt:**

IWDG Early Wakeup Interrupt	0
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### 3.6. MEMORYMAP

**mode: Activated**

### 3.7. PWR

**mode: Power saving mode**

**mode: Privilege attributes**

#### 3.7.1. PWR Privilege :

**Privilege PWR:**

PWR Privilege	Disable
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### 3.8. RCC

**High Speed Clock (HSE): Crystal/Ceramic Resonator**

**Low Speed Clock (LSE) : Crystal/Ceramic Resonator**

#### 3.8.1. RCC Privilege :

**Privilege RCC:**

Privilege of RCC Non-Secure Items	Disable
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#### 3.8.2. Parameter Settings:

**System Parameters:**

VDD voltage (V)	3.3
Flash Latency(WS)	4 WS (5 CPU cycle)

Flash Programming Delay	2
<b>RCC Parameters:</b>	
HSI Calibration Value	64
CSI Calibration Value	32
HSE Startup Timeout Value (ms)	100
LSE Startup Timeout Value (ms)	5000
TIM Prescaler Selection	Disabled
<b>Power Parameters:</b>	
Power Regulator Voltage Scale	Power Regulator Voltage Scale 3
<b>PLL1/2/3 Parameters:</b>	
PLL1 input frequency range	Between 8 and 16 MHz
PLL2 input frequency range	Between 8 and 16 MHz

### 3.9. RTC

#### mode: Activate Clock Source

##### 3.9.1. Parameter Settings:

<b>General:</b>	
Hour Format	Hourformat 24
Asynchronous Predivider value	127
Synchronous Predivider value	255
Bin Mode	Free running BCD calender mode

##### 3.9.2. RTC Privilege:

<b>Privilege RTC:</b>	
RTC full privilege	Disable
<b>Backup register:</b>	
Start zone 1	RTC_BKP_DR0
Start Zone 2	RTC_BKP_DR0
start zone 3	RTC_BKP_DR0
<b>Privilege Backup register :</b>	
Backup Register PrivZone	Non-privilege
<b>Privilege RTC Feature:</b>	
RTC Initialisation	Non-Privilege
RTC Alarm A	Non-Privilege
RTC Alarm B	Non-Privilege
RTC Calibration	Non-Privilege
RTC TimeStamp	Non-Privilege

RTC WakeUpTimer

Non-Privilege

### 3.10. SYS

#### Timebase Source: TIM6

### 3.11. TIM3

#### Channel1: Output Compare No Output

##### 3.11.1. Parameter Settings:

###### Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Dithering	Disable
Counter Period (AutoReload Register - 16 bits value )	65535
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

###### Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

###### Clear Input:

Clear Input Source	Disable
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###### Output Compare No Output Channel 1:

Mode	Frozen (used for Timing base)
Pulse (16 bits value)	0
Output compare preload	Disable
CH Polarity	High

\* User modified value

## 4. System Configuration

### 4.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA1	ADC1_INP1	Analog mode	No pull-up and no pull-down	n/a	EFUSE_I_SNS
DEBUG	PA13(JTMS/SWDIO)	DEBUG_JTMS-SWDIO	n/a	n/a	n/a	SWDIO
	PA14(JTCK/SWCLK)	DEBUG_JTCK-SWCLK	n/a	n/a	n/a	SWCLK
	PB3(JTDO/TRACESWO)	DEBUG_JTDO-SWO	n/a	n/a	n/a	SWO
FDCAN1	PB7	FDCAN1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB8	FDCAN1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
RCC	PC14-OSC32_IN(OSC32_IN)	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15-OSC32_OUT(OSC32_OUT)	RCC_OSC32_OUT	n/a	n/a	n/a	
	PH0-OSC_IN(PH0)	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-OSC_OUT(PH1)	RCC_OSC_OUT	n/a	n/a	n/a	
GPIO	PB14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DIAG_EN
	PB15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	EFUSE_EN
	PB4(NJTRST)	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED
	PB5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	BOOT

### 4.2. GPDMA1

**Channel 0 - 2 Words Internal FIFO**

**: Standard Request Mode**

#### 4.2.1. All Channels:

##### Channel 0:

Request

GPDMA1\_REQUEST\_ADC1

#### 4.2.2. SECURITY:

**CH0:**

Enable Channel as Privileged

NON PRIVILEGED

### 4.2.3. CH0:

#### **Circular configuration:**

Circular Mode

**Enable \***

Circular Port

Port 0

#### **Request Configuration:**

Request

**ADC1 \***

DMA Handle in IP Structure

DMA\_Handle

Block HW request protocol

Single/Burst Level

#### **Channel configuration:**

Priority

Low

Transaction Mode

Normal

Direction

Peripheral To Memory

Node Type

GPDMA Linear Addressing

#### **Source Data Setting:**

Source Address Increment After Transfer

Disabled

Data Width

**Half Word \***

Burst Length

1

Allocated Port for Transfer

Port 0

#### **Destination Data Setting:**

Destination Address Increment After Transfer

Disabled

Data Width

**Half Word \***

Burst Length

1

Allocated Port for Transfer

Port 0

#### **Data Handling:**

Data Handling Configuration

Disable

#### **Trigger:**

Trigger Configuration

Disable

#### **Channel Configuration for Linked List:**

Execution Mode (circular/linear) of the Linked List

Circular

Linked List Execution Mode

The List is fully executed

#### **Transfer Event Configuration:**

Transfer Event Generation

The TC (and the HT) event is generated at the (respectively half) end of each block

### **4.3. GPDMA2**



#### 4.4. LINKEDLIST

## 4.5. NVIC configuration

### 4.5.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	15	0
System tick timer	true	15	0
RCC non-secure global interrupt	true	5	0
GPDMA1 Channel 0 global interrupt	true	0	0
FDCAN1 interrupt 0	true	5	0
FDCAN1 interrupt 1	true	5	0
TIM6 global interrupt	true	15	0
Flash non-secure global interrupt	unused		
IWDG global interrupt	unused		
ADC1 global interrupt	unused		
TIM3 global interrupt	unused		
FPU global interrupt	unused		

### 4.5.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	false	false
Debug monitor	false	true	false
Pendable request for system service	false	false	false
System tick timer	false	false	false
RCC non-secure global interrupt	false	true	false
GPDMA1 Channel 0 global interrupt	false	true	true
FDCAN1 interrupt 0	false	true	true
FDCAN1 interrupt 1	false	true	true
TIM6 global interrupt	false	true	false

\* User modified value

## 5. System Views

### 5.1. Category view

#### 5.1.1. Current

Middleware										
System Core	Analog	Timers	Connectivity	Multimedia	Security	Computing	Trace and Debug	Power and Thermal	Utilities	Other
CORTEX_M33	ADC1 ✓	RTC ✓	FDCAH1 ✓				DEBUG ✓	PWR ✓	LINKEDLIST	
GPDMA1 ✓		TIM3 ✓								
GPDMA2										
GPIO ✓										
IWDG ✓										
NVIC ✓										
RCC ✓										
SYS ✓										

## 6. Docs & Resources

Type	Link
BSDL files	<a href="https://www.st.com/resource/en/bsdl_model/stm32h5-bsdl.zip">https://www.st.com/resource/en/bsdl_model/stm32h5-bsdl.zip</a>
IBIS models	<a href="https://www.st.com/resource/en/ibis_model/stm32h5-ibis.zip">https://www.st.com/resource/en/ibis_model/stm32h5-ibis.zip</a>
System View Description	<a href="https://www.st.com/resource/en/svd/stm32h5-svd.zip">https://www.st.com/resource/en/svd/stm32h5-svd.zip</a>
Presentations	<a href="https://www.st.com/resource/en/product_presentation/stm32-stm8_embedded_software_solutions.pdf">https://www.st.com/resource/en/product_presentation/stm32-stm8_embedded_software_solutions.pdf</a>
Presentations	<a href="https://www.st.com/resource/en/product_presentation/stm32_eval_tools_portfolio.pdf">https://www.st.com/resource/en/product_presentation/stm32_eval_tools_portfolio.pdf</a>
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Presentations	<a href="https://www.st.com/resource/en/product_presentation/microcontrollers-stm32-family-overview.pdf">https://www.st.com/resource/en/product_presentation/microcontrollers-stm32-family-overview.pdf</a>
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Brochures	<a href="https://www.st.com/resource/en/brochure/products-and-solutions-for-plcs-and-smart-i-os.pdf">https://www.st.com/resource/en/brochure/products-and-solutions-for-plcs-and-smart-i-os.pdf</a>
Flyers	<a href="https://www.st.com/resource/en/flyer/flstm32nucleo.pdf">https://www.st.com/resource/en/flyer/flstm32nucleo.pdf</a>
Flyers	<a href="https://www.st.com/resource/en/flyer/flstm32h5.pdf">https://www.st.com/resource/en/flyer/flstm32h5.pdf</a>
Security Bulletin	<a href="https://www.st.com/resource/en/technical_note/tn1474-security-bulletin-tn1474stpsirt-information-on-softwarebased--microarchitectural-timing-sidechannel-attacks-on-mcus-with-trustzone-for--armv8m-stmicroelectronics.pdf">https://www.st.com/resource/en/technical_note/tn1474-security-bulletin-tn1474stpsirt-information-on-softwarebased--microarchitectural-timing-sidechannel-attacks-on-mcus-with-trustzone-for--armv8m-stmicroelectronics.pdf</a>
Security Bulletin	<a href="https://www.st.com/resource/en/technical_note/tn1489-security-bulletin-tn1489stpsirt-physical-attacks-on-stm32-and-stm32cube-firmware-stmicroelectronics.pdf">https://www.st.com/resource/en/technical_note/tn1489-security-bulletin-tn1489stpsirt-physical-attacks-on-stm32-and-stm32cube-firmware-stmicroelectronics.pdf</a>
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