1. Description

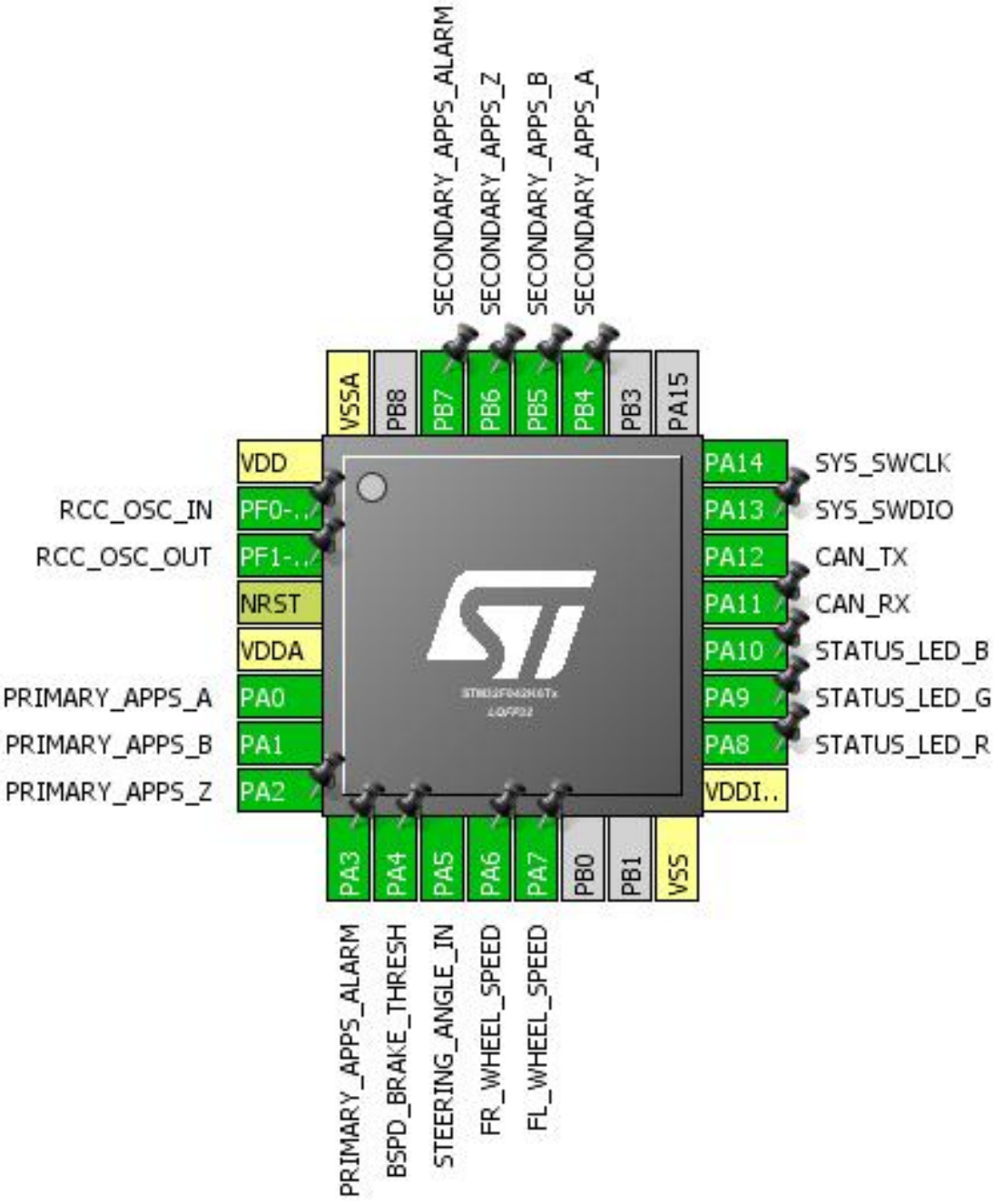
1.1. Project

Project Name	FSM2018
Board Name	custom
Generated with:	STM32CubeMX 4.27.0
Date	11/16/2018

1.2. MCU

MCU Series	STM32F0
MCU Line	STM32F0x2
MCU name	STM32F042K6Tx
MCU Package	LQFP32
MCU Pin number	32

2. Pinout Configuration

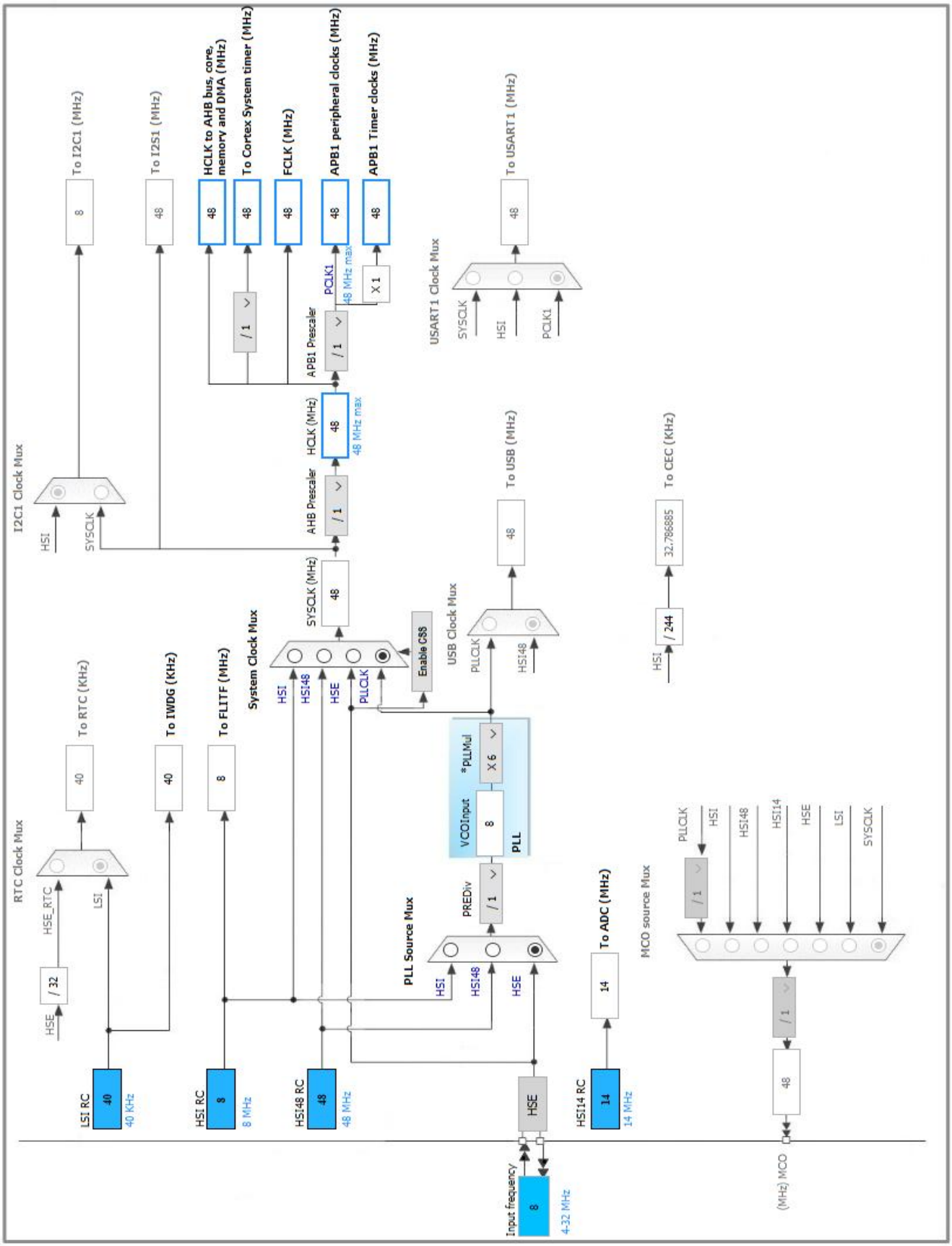


3. Pins Configuration

Pin Number LQFP32	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VDD	Power		
2	PF0-OSC_IN	I/O	RCC_OSC_IN	
3	PF1-OSC_OUT	I/O	RCC_OSC_OUT	
4	NRST	Reset		
5	VDDA	Power		
6	PA0	I/O	TIM2_CH1	PRIMARY_APPS_A
7	PA1	I/O	TIM2_CH2	PRIMARY_APPS_B
8	PA2 *	I/O	GPIO_Input	PRIMARY_APPS_Z
9	PA3 *	I/O	GPIO_Input	PRIMARY_APPS_ALARM
10	PA4 *	I/O	GPIO_Input	BSPD_BRAKE_THRESH
11	PA5	I/O	ADC_IN5	STEERING_ANGLE_IN
12	PA6	I/O	TIM16_CH1	FR_WHEEL_SPEED
13	PA7	I/O	TIM17_CH1	FL_WHEEL_SPEED
16	VSS	Power		
17	VDDIO2	Power		
18	PA8 *	I/O	GPIO_Output	STATUS_LED_R
19	PA9 *	I/O	GPIO_Output	STATUS_LED_G
20	PA10 *	I/O	GPIO_Output	STATUS_LED_B
21	PA11	I/O	CAN_RX	
22	PA12	I/O	CAN_TX	
23	PA13	I/O	SYS_SWDIO	
24	PA14	I/O	SYS_SWCLK	
27	PB4	I/O	TIM3_CH1	SECONDARY_APPS_A
28	PB5	I/O	TIM3_CH2	SECONDARY_APPS_B
29	PB6 *	I/O	GPIO_Input	SECONDARY_APPS_Z
30	PB7 *	I/O	GPIO_Input	SECONDARY_APPS_ALARM
32	VSSA	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. IPs and Middleware Configuration

5.1. ADC

mode: IN5

mode: Vrefint Channel

5.1.1. Parameter Settings:

ADC_Settings:

Clock Prescaler	Asynchronous clock mode
Resolution	ADC 12-bit resolution
Data Alignment	Right alignment
Scan Conversion Mode	**Backward ***
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	**Enabled ***
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data preserved
Low Power Auto Wait	Disabled
Low Power Auto Power Off	Disabled

ADC_Regular_ConversionMode:

Sampling Time	**7.5 Cycles ***
External Trigger Conversion Source	**Timer 1 Trigger Out event ***
External Trigger Conversion Edge	Trigger detection on the rising edge

WatchDog:

Enable Analog WatchDog Mode	false

5.2. CAN

mode: Mode

5.2.1. Parameter Settings:

Bit Timings Parameters:

Prescaler (for Time Quantum)	**8 ***
Time Quantum	**166.66666666666666 ***
Time Quanta in Bit Segment 1	**5 Times ***
Time Quanta in Bit Segment 2	**2 Times ***
ReSynchronization Jump Width	**2 Times ***

Basic Parameters:

Time Triggered Communication Mode	**Enable ***
Automatic Bus-Off Management	Disable
Automatic Wake-Up Mode	Disable
No-Automatic Retransmission	Disable
Receive Fifo Locked Mode	**Enable ***
Transmit Fifo Priority	**Enable ***

Advanced Parameters:

Operating Mode	Normal

5.3. IWDG

mode: Activated

5.3.1. Parameter Settings:

Watchdog Clocking:

IWDG counter clock prescaler	**32 ***
IWDG window value	4095
IWDG down-counter reload value	**200 ***

5.4. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

5.4.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Prefetch Buffer	Enabled
Flash Latency(WS)	1 WS (2 CPU cycle)

RCC Parameters:

HSI14 Calibration Value	16
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

5.5. SYS

mode: Debug Serial Wire

Timebase Source: SysTick

5.6. TIM1

Clock Source : Internal Clock

5.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**4999 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	**Update Event ***

5.7. TIM2

Combined Channels: Encoder Mode

5.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	**65535 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode	**Encoder Mode TI1 and TI2 ***
____ Parameters for Channel 1 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0

____ Parameters for Channel 2 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0

5.8. TIM3

Combined Channels: Encoder Mode

5.8.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**65535 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode	**Encoder Mode TI1 and TI2 ***
____ Parameters for Channel 1 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0
____ Parameters for Channel 2 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0

5.9. TIM14

mode: Activated

5.9.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**7 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**((SystemCoreClockCube / 8) / CONTROL_LOOP_FREQUENCY_CUBE) - 1 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

5.10. TIM16

mode: Activated

Channel1: Input Capture direct mode

5.10.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**WHEEL_SPEED_TIMER_PRESCALER_CUBE ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**65535 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Disable

Input Capture Channel 1:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

5.11. TIM17

mode: Activated

Channel1: Input Capture direct mode

5.11.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**WHEEL_SPEED_TIMER_PRESCALER_CUBE ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**65535 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0

auto-reload preload	Disable

Input Capture Channel 1:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

*** User modified value**

6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC	PA5	ADC_IN5	Analog mode	No pull-up and no pull-down	n/a	STEERING_ANGLE_IN
CAN	PA11	CAN_RX	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
	PA12	CAN_TX	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
RCC	PF0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PF1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA13	SYS_SWDIO	n/a	n/a	n/a	
	PA14	SYS_SWCLK	n/a	n/a	n/a	
TIM2	PA0	TIM2_CH1	Alternate Function Push Pull	**Pull-up ***	Low	PRIMARY_APPS_A
	PA1	TIM2_CH2	Alternate Function Push Pull	**Pull-up ***	Low	PRIMARY_APPS_B
TIM3	PB4	TIM3_CH1	Alternate Function Push Pull	**Pull-up ***	Low	SECONDARY_APPS_A
	PB5	TIM3_CH2	Alternate Function Push Pull	**Pull-up ***	Low	SECONDARY_APPS_B
TIM16	PA6	TIM16_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	FR_WHEEL_SPEED
TIM17	PA7	TIM17_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	FL_WHEEL_SPEED
GPIO	PA2	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	PRIMARY_APPS_Z
	PA3	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	PRIMARY_APPS_ALARM
	PA4	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	BSPD_BRAKE_THRESH
	PA8	GPIO_Output	**Output Open Drain ***	**Pull-up ***	Low	STATUS_LED_R
	PA9	GPIO_Output	**Output Open Drain ***	**Pull-up ***	Low	STATUS_LED_G
	PA10	GPIO_Output	**Output Open Drain ***	**Pull-up ***	Low	STATUS_LED_B
	PB6	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	SECONDARY_APPS_Z
	PB7	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	SECONDARY_APPS_ALARM

6.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC	DMA1_Channel1	Peripheral To Memory	**Medium ***

ADC: DMA1_Channel1 DMA request Settings:

Mode:	**Circular ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
System service call via SWI instruction	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
DMA1 channel 1 interrupt	true	0	0
TIM14 global interrupt	true	0	0
TIM16 global interrupt	true	0	0
TIM17 global interrupt	true	0	0
PVD and VDDIO2 supply comparator interrupts through EXTI lines 16 and 31	unused		
Flash global interrupt	unused		
RCC and CRS global interrupts	unused		
ADC interrupt	unused		
TIM1 break, update, trigger and commutation interrupts	unused		
TIM1 capture compare interrupt	unused		
TIM2 global interrupt	unused		
TIM3 global interrupt	unused		
HDMI-CEC and CAN global interrupts / HDMI-CEC wake-up interrupt through EXTI line 27	unused		

*** User modified value**

7. Power Consumption Calculator report

7.1. Microcontroller Selection

Series	STM32F0
Line	STM32F0x2
MCU	STM32F042K6Tx
Datasheet	025832_Rev5

7.2. Parameter Selection

Temperature	25
Vdd	3.6

8. Software Project

8.1. Project Settings

Name	Value
Project Name	FSM2018
Project Folder	C:\Users\Ahmad\Documents\Formula\Consolidated-Firmware\src\FSM
Toolchain / IDE	MDK-ARM V5
Firmware Package Name and Version	STM32Cube FW_F0 V1.9.0

8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No

9. Software Pack Report