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Rockchip RK3528 Hardware Design Guide

(Fuzhou Hardware Development Center)

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Preface

Overview

This document mainly introduces the key points and precautions of RK3528 processor hardware design, aiming to help RK customers shorten the product design cycle, improve product design stability and reduce failure rate. Please refer to the requirements of this guide for hardware design and try to use the RK released Related core templates. If changes are required due to special reasons, please strictly follow the high-speed digital circuit design requirements and RK product PCB design requirements. conduct.

Chip model

The chip model corresponding to this document is: RK3528

Applicable Targets

This document is primarily intended for the following engineers:

- ÿ Hardware development engineer
- ÿ Layout Engineer
- ÿ Technical support engineer
- ÿ Test Engineer

Change Log

The revision history accumulates the descriptions of each document update. The latest version of the document contains the updated contents of all previous document versions.

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1 System Overview

1.1 Overview

The RK3528 is a high-performance, highly integrated, and low-cost quad-core application processor designed for Smart IPTV/OTT/DBS and high-end multimedia applications. The quad-core Cortex-A53 integrates separate Neon and FPU coprocessors, along with a shared L2 cache, significantly improving system performance. The built-

in ARM Mali-450 GPU supports high-resolution displays and is fully compatible with graphics programs such as OpenGL ES 1.1/2.0 and OpenVG.

RK3528 has a high-performance 32-bit external memory interface and supports LPDDR3/DDR3/DDR3L/DDR4/LPDDR4/LPDDR4X.

Advanced video decoder supports up to 10-bit pixel 4K/60FPS ultra-high-definition video playback, compatible with H.265, H.264, VP9, AVS2, etc. Video standards. The advanced video encoder supports 1080P/60FPS high-definition video capture and H.265 and H.264 encoding.

The display controller can flexibly switch between HDMI output (supporting HDR10, VIVID HDR, CEC, HDCP2.2) and CVBS output.

Live switching.

RK3528 also provides a rich set of peripheral interfaces SDMMC/SDIO/PCIE2.0/USB3.0/RGMII/I2S/PDM/UART/I2C/PWM/SPI, etc., can flexibly support various application scenarios.

1.2 Chip Block Diagram

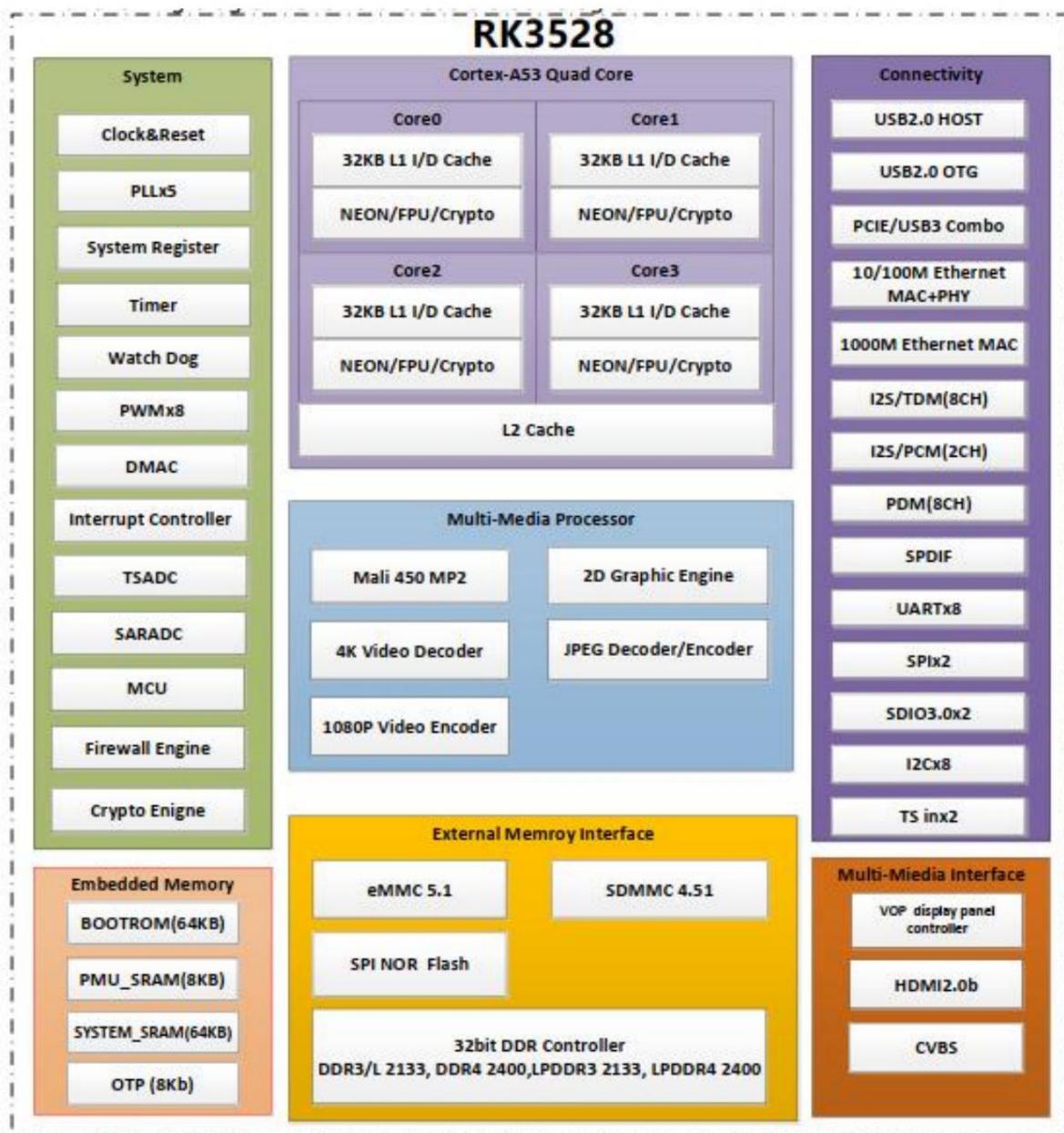


Figure 1-1 RK3528 chip block diagram

1.3 Application Block Diagram

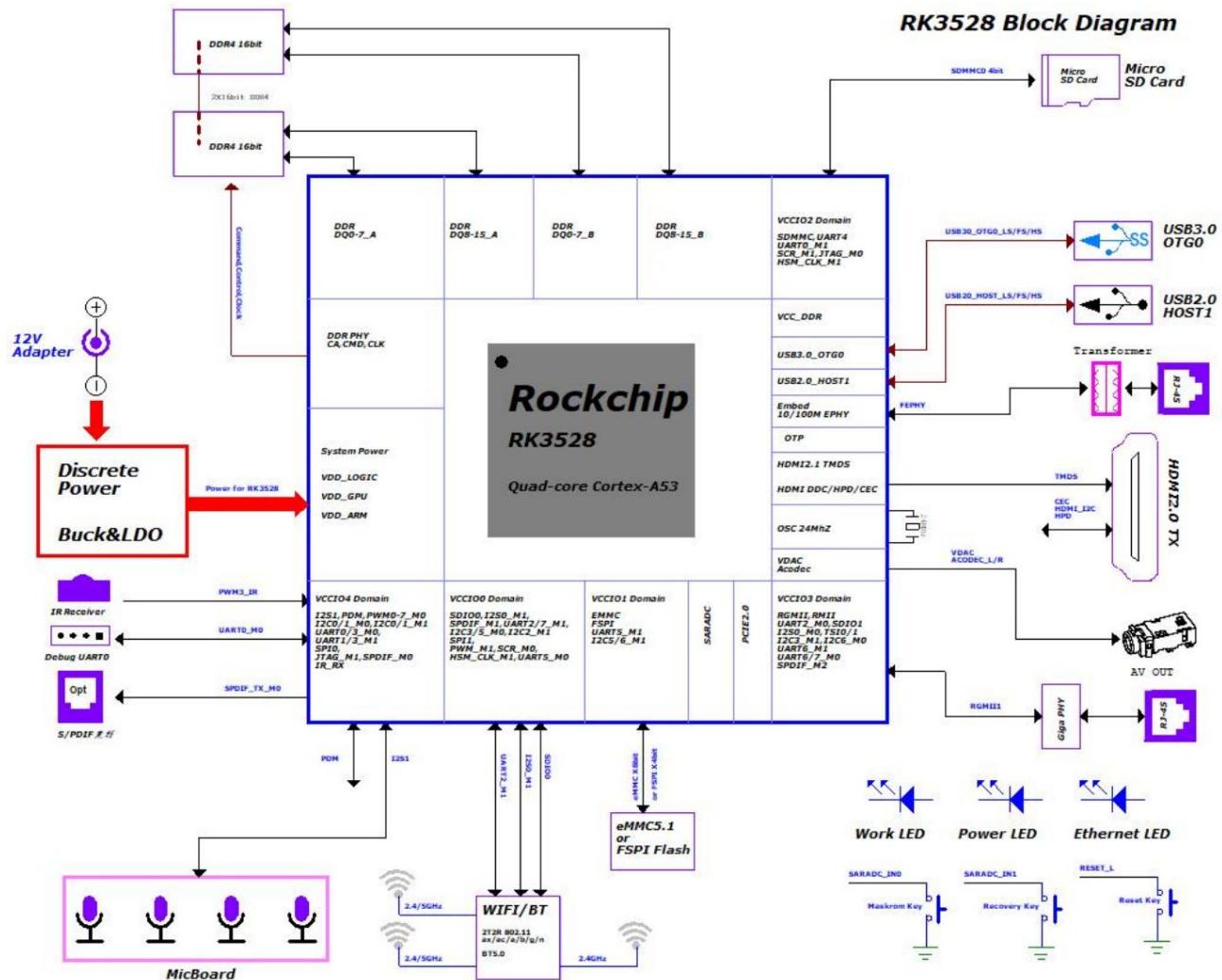


Figure 1-2 RK3528 OTT application block diagram

The above is an example application block diagram of the RK3528 chip solution. For more details, please refer to the reference design schematic diagram released by RK.

2 Schematic Design Suggestions

2.1 Minimum System Design

2.1.1 Clock Circuit

The oscillator circuit inside the RK3528 chip and the external 24MHz crystal together form the system clock, as shown in Figure 2-1.

The network must be connected in series with a 22ohm resistor to limit current and prevent overdrive. The 1M resistor between the XOUT24M and XIN24M networks cannot be modified arbitrarily. change.

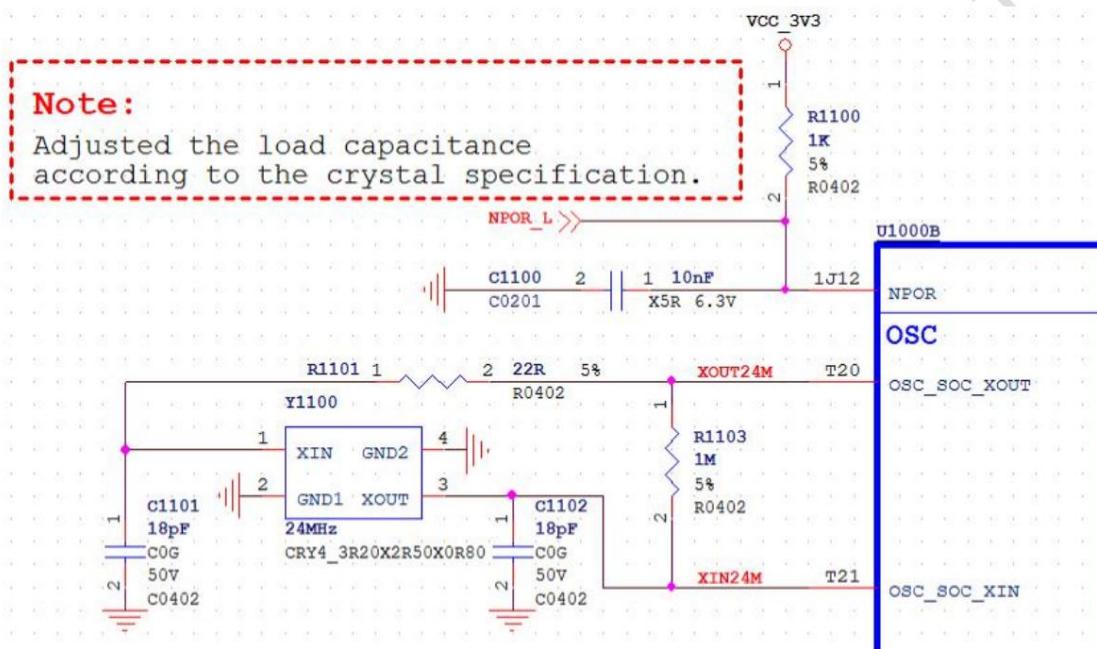


Figure 2-1 RK3528 crystal connection method and device parameters



Notice

Note1 Crystal selection C_L Value not exceeding $12pF$

Note2 Crystal load capacitance should be based on the actual crystal used C_L Capacitor value selection and control the frequency tolerance at room temperature $20ppm$ Within;

$18pF$ The capacitance value corresponding to the crystal selected by our company is not a universal value. The load capacitor material is recommended to be COG or NPO

It is recommended to use patch 4Pin crystals, of which 2 individual GND Pins and PCB The ground of the board is fully connected to enhance the clock resistance ESD Interference capability.

In addition, the system clock can also be directly generated by an external active crystal circuit and input through the OSC_SOC_XIN pin.

The parameters are shown in Table 2-1 below:

Table 2-1 RK3528 24MHz clock requirements

parameter	specification			describe
	Minimum	maximum	unit	
frequency	24.000000		MHz	
Frequency deviation	+/-20		ppm	Frequency tolerance
Clock amplitude	1.8		In	Peak-to-peak value
Operating temperature	-20	80	°C	
ESR	/	40	Ohm	

RK3528 can provide working clock to peripherals:

REF_CLK_OUT_M0/M1: Reserved clock output pin, output clock is 24MHz;

TEST_CLK_OUT: Clock test pin, which can test the CLK frequency of some modules inside the chip;

CLK_32K_OUT_M0/M1: 32.768KHz clock output, can be provided to WIFI/BT, PCIe and other devices when sleeping or working clock;

ETH_CLK_25M_OUT: 25MHz clock output, which can be provided to Ethernet PHY and other devices as working clock;

HSM_CLK_OUT_M0/M1: Default 4.5MHz clock output, Hardware Secure Module working clock;

RGMII1_CLK: can output 125Mhz or 50Mhz clock frequency to provide working clock for external Ethernet PHY;



Notice

The above clock

IO Domain

With peripherals/IT

The voltage levels must match. If they do not match, a level conversion circuit must be added. Please evaluate whether the requirements can be met based on the clock requirements of the peripheral devices.

2.1.2 NPOR Circuit

The RK3528 chip has an internal integrated POR (Power on Reset) circuit, whose main function is to generate the power-on reset signal of the SOC and the power status.

As shown in Figure 2-3, the chip PIN 1J12 is pulled up to the VCC_3V3 power supply through the resistor R1110, which serves as the internal NPOR.

The input reference of the voltage comparator, capacitor C1100 is used for debounce.

The chip's hardware reset detection input is input through PIN 1J12 (NPOR) pin and must be controlled externally, with low level valid.

The pull-up power supply of the NPOR_L network must be consistent with the IO power domain (PMUIO_VCC3V3) where the NPOR pin is located.

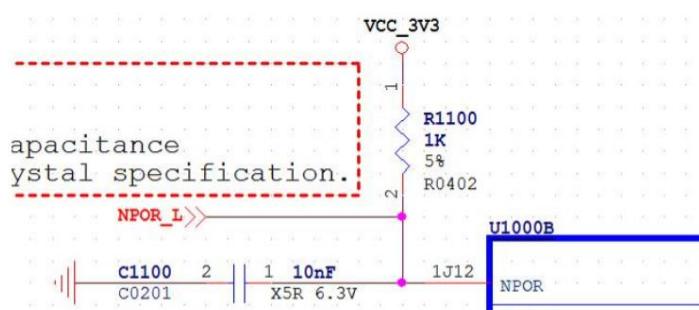


Figure 2-3 RK3528 reset detection input

2.1.3 System boot sequence

The RK3528 chip supports multiple boot modes. After the chip is reset, the boot code integrated in the chip can be used in the following interfaces:

The device boots, and the specific boot order can be selected according to actual application requirements (see the description of "Boot Order Selection" below)

ÿ Serial Flash(FSPI)

ÿ eMMC

ÿ SDMMC Card

If there is no boot code in the above devices, the system code can be downloaded to these devices through the USB2.0 OTG interface signal.

Boot order selection:

The boot sequence of RK3528 can be set through SARADC_IN0 Pin (PIN AA10), starting from the peripherals corresponding to different interfaces.

As shown in the table below, the hardware is configured with different pull-up and pull-down resistor values to design the peripheral boot sequence of ten modes from LEVEL1 to LEVEL10.

The corresponding configuration can be made according to the actual application requirements. For details, please refer to Section 2.3.2.

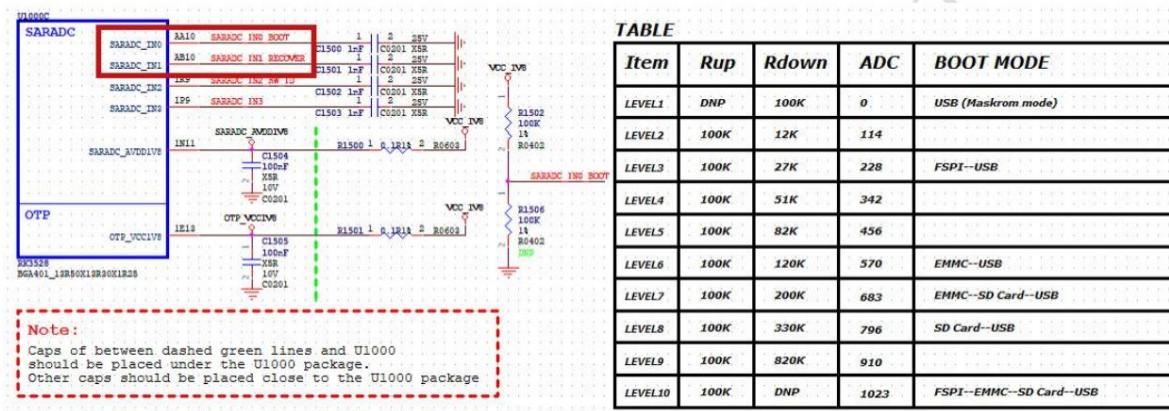


Figure 2-2 RK3528 boot order selection

According to the above LEVEL1 setting, SARADC_IN0_BOOT is short-circuited to ground, which can make the device enter the Maskrom state without going through

Short circuit EMMC_CLK/DATA to enter Maskrom; SARADC_IN1 is used to short circuit to ground to enter Recovery state; other SARADC

The port can be configured according to application requirements.



Notice

Note1 ÿ SARADC_IN0 for BOOT Configuration dedicated pins, cannot be used for other functions

2.1.4 System initialization configuration signal

There is an important signal in RK3528 that affects the system startup configuration. It needs to be configured and kept stable before powering on:

ÿ SDMMC_DET pin (Pin D21): determines whether the IO related to the VCCIO2_VCC power domain is SDMMC or JTAG function;

After the system reset is completed, the chip will configure the default power-on function of the corresponding module according to the input level of this pin.

The CPU JTAG function of RK3528 is multiplexed with the SDMMC function, and the IOMUX is switched through the SDMMC_DET pin.

Therefore, this pin also needs to be configured before power-on, otherwise the CPU JTAG function will have no output, which will affect the debugging during the boot phase.

The lack of SDMMC output will affect the SDMMC boot function.

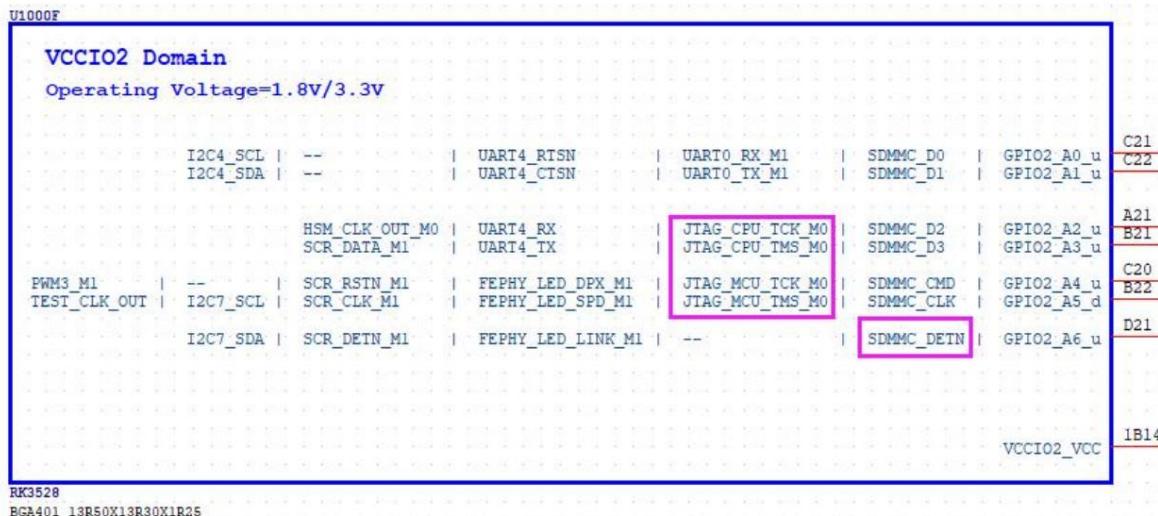


Figure 2-3 RK3528 SDMMC/CPU JTAG multiplexing pins and SDMMC DET pins

- ÿ If the SDMMC_DET pin is detected as high level, the corresponding IO switches to the CPU JTAG function;
- ÿ When it is detected as low level (most SD cards will pull down this pin if inserted, if no special processing is required), the corresponding IO switches to SDMMC functionality;
- ÿ After the system is up, the IOMUX can be controlled by the register, and the pin can be released;
- ÿ For easy query, the configuration status and function of this pin correspond to the following table:

Table 2-2 RK3528 system initialization configuration signal description

Signal Name	Internal pull-up and pull-down	describe
SDMMC_DET	Pull-up	SDMMC/CPU JATG pin multiplexing selection control signal: 0: Identify as SD card insertion, SDMMC/CPU JATG pin multiplexed to SDMMC function; 1: Not recognized as SD card insertion, SDMMC/CPU JATG pin multiplexed as CPU JTAG function ÿDefaultÿ

2.1.5 JTAG and UART Debug Circuits

The ARM JTAG interface of the RK3528 chip complies with the IEEE1149.1 standard, and the PC can be connected via SWD mode (two-wire mode)

DSTREAM emulator, debugs the ARM Core inside the chip.

When connecting to the emulator during the boot phase, you need to ensure that the SDMMC_DET pin is at a high level, otherwise you will not be able to enter the JTAG debugger.

Test mode, the configuration of this management is described in the previous section.

After the system starts up, it will switch to register-controlled IOMUX. The CPU JTAG interface description is shown in the following table:

Table 2-3 RK3528 JTAG Debug Interface Signals

Signal Name	describe
JTAG_CPU_TCK_M0/M1	ARM Cortex-A53 SWD clock input
JTAG_CPU_TMS_M0/M1	ARM Cortex-A53 SWD mode select input
JTAG MCU_TCK_M0/M1	MCU SWD clock input
JTAG MCU_TMS_M0/M1	MCU SWD mode selection input

The JTAG connection method and standard connector pin definition are shown in the figure below:

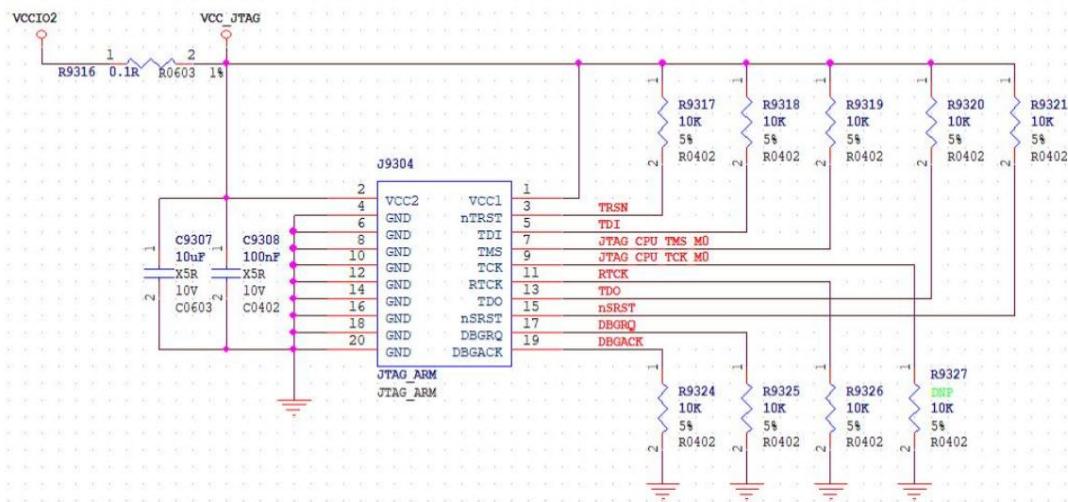


Figure 2-4 RK3528 JTAG connection diagram

If there is no SD Card function, it is recommended to reserve the CPU JTAG function for debugging convenience.

Reserved IO can be selected from any of the following, distributed between VCCIO2_VCC (PIN 1B14) and VCCIO4_VCC (PIN 1J3)

In the source domain, the JTAG peripheral level is generally 3.3V, so you need to pay attention to the IO level consistency.

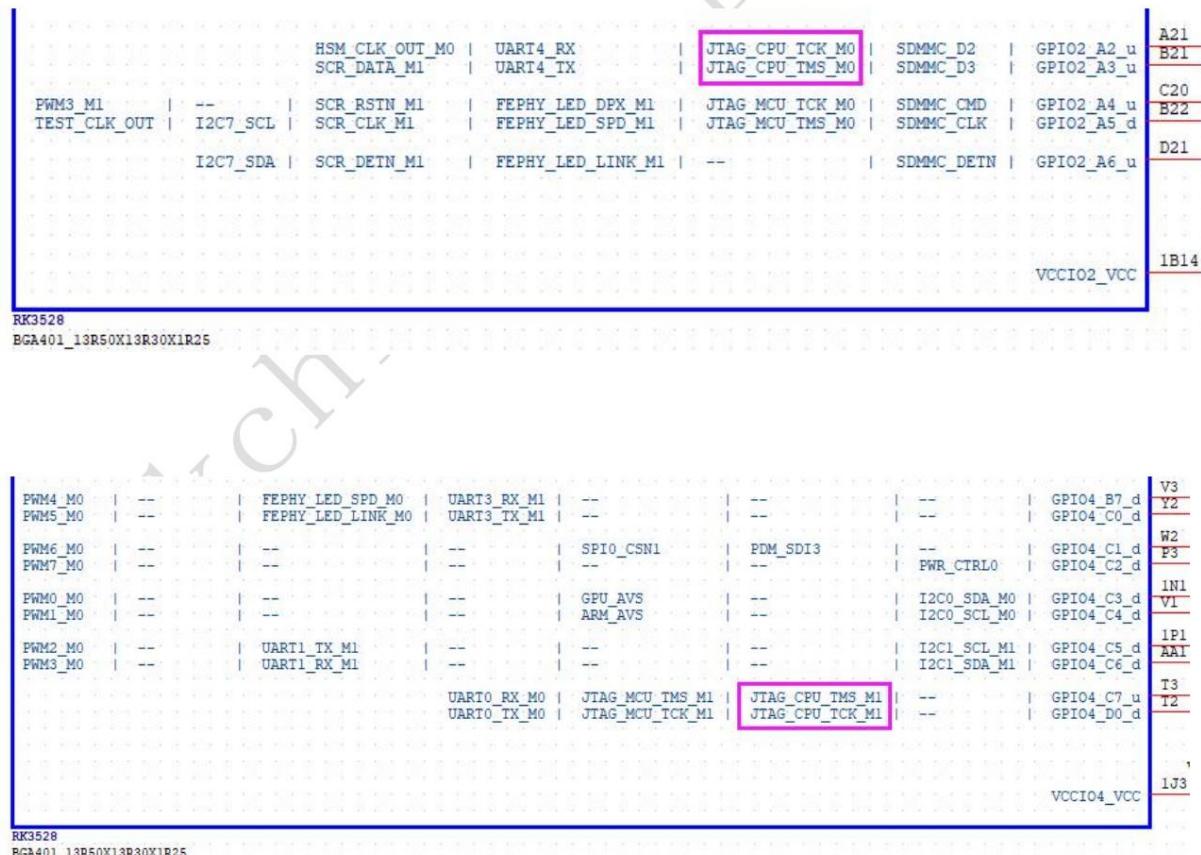


Figure 2-5 RK3528 CPU JTAG pins

The MCU_JTAG module of RK3528 is not open to the public yet and does not require any special processing.

RK3528 UART Debug selects UART0_RX_M0/UART0_TX_M0 by default, and the default baud rate is 1500000bps.

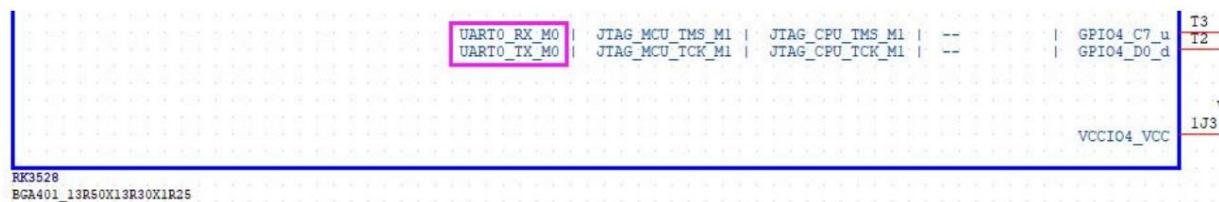


Figure 2-6 RK3528 UART0 M0 pin

The 100 ohm resistor connected in series with UART0_RX_M0/UART0_TX_M0 must not be deleted, and a TVS tube should be added to enhance the anti-static surge capability to prevent damage to the chip pins during the development and debugging process. It is recommended to reserve 2.54mm pins as much as possible. If conditions are unavailable, it is recommended to use 0.7mm. The above test points are convenient for welding.

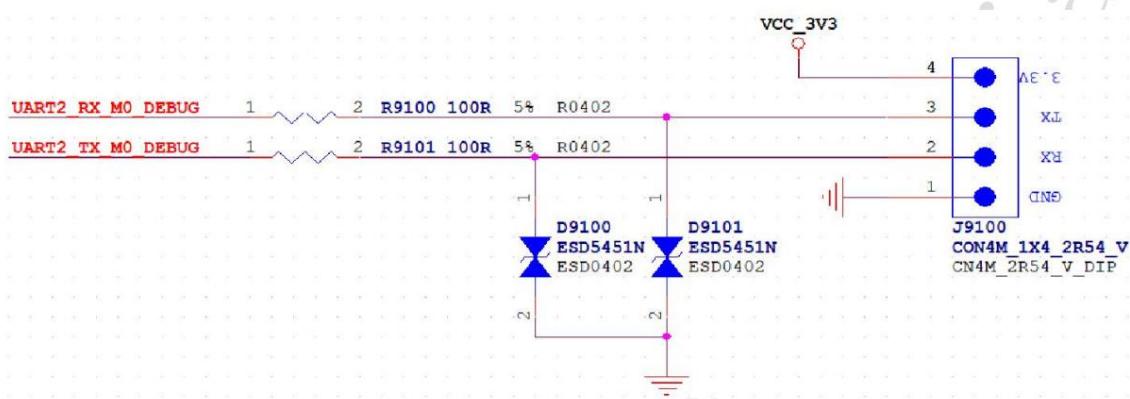


Figure 2-7 RK3528 Debug UART0 connection diagram

2.1.6 DDR Circuit

2.1.6.1 DDR Controller Introduction

The RK3528 DDR controller interface supports the JEDEC SDRAM standard interface. The controller has the following features:

- ÿ Compatible with DDR3/DDR3L/LPDDR3/DDR4/LPDDR4/LPDDR4X standards; ÿ Supports 32-bit data bus width, 2 ranks (chip select), and a maximum total addressable address of 4GB; ÿ Two 16-bit channels form a 32-bit channel, supporting asymmetric designs such as 1GB+2GB combinations;
- ÿ Supports Power Down, Self Refresh and other modes;
- ÿ Programmable output and ODT impedance adjustment with dynamic PVT compensation.

2.1.6.2 Circuit Design Suggestions

The schematics of the RK3528 DDR PHY and each DRAM chip must be consistent with the reference design, including the power decoupling capacitors.

RK3528 can support DDR3/DDR3L, LPDDR3, DDR4 and LPDDR4/LPDDR4X, these DRAMs have different I/O

Signal, select the corresponding signal according to the DRAM type. The RK3528 DDR PHY I/O Map table is as follows:

Table 2-4 RK3528 DDR PHY I/O Map

DDRPHY	DDR4	LPDDR4/LPDDR4X	DDR3	LPDDR3
DDRPHY_A_DQ0	DDR4_DQL6_A	LPDDR4_DQ0_A	DDR3_D4	LPDDR3_D0
DDRPHY_A_DQ1	DDR4_DQL2_A	LPDDR4_DQ1_A	DDR3_D0	LPDDR3_D1
DDRPHY_A_DQ2	DDR4_DQL0_A	LPDDR4_DQ2_A	DDR3_D2	LPDDR3_D2
DDRPHY_A_DQ3	DDR4_DQL1_A	LPDDR4_DQ3_A	DDR3_D1	LPDDR3_D3
DDRPHY_A_DQ4	DDR4_DQL4_A	LPDDR4_DQ4_A	DDR3_D6	LPDDR3_D4
DDRPHY_A_DQ5	DDR4_DQL5_A	LPDDR4_DQ5_A	DDR3_D7	LPDDR3_D5
DDRPHY_A_DQ6	DDR4_DQL7_A	LPDDR4_DQ6_A	DDR3_D5	LPDDR3_D6
DDRPHY_A_DQ7	DDR4_DQL3_A	LPDDR4_DQ7_A	DDR3_D3	LPDDR3_D7
DDRPHY_A_DM0	DDR4_DML_A	LPDDR4_DM0_A	DDR3_DM0	LPDDR3_DM0
DDRPHY_A_DQS0	DDR4_DQSL_P_A	LPDDR4_DQS0P_A	DDR3_DQS0P	LPDDR3_DQS0P
DDRPHY_A_DQSB0	DDR4_DQSL_N_A	LPDDR4_DQS0N_A	DDR3_DQS0N	LPDDR3_DQS0N
DDRPHY_A_DQ8	DDR4_DQU1_A	LPDDR4_DQ8_A	DDR3_D12	LPDDR3_D19
DDRPHY_A_DQ9	DDR4_DQU5_A	LPDDR4_DQ9_A	DDR3_D14	LPDDR3_D16
DDRPHY_A_DQ10	DDR4_DQU0_A	LPDDR4_DQ10_A	DDR3_D15	LPDDR3_D21
DDRPHY_A_DQ11	DDR4_DQU2_A	LPDDR4_DQ11_A	DDR3_D9	LPDDR3_D17
DDRPHY_A_DQ12	DDR4_DQU7_A	LPDDR4_DQ12_A	DDR3_D10	LPDDR3_D20
DDRPHY_A_DQ13	DDR4_DQU3_A	LPDDR4_DQ13_A	DDR3_D8	LPDDR3_D23
DDRPHY_A_DQ14	DDR4_DQU4_A	LPDDR4_DQ14_A	DDR3_D13	LPDDR3_D22
DDRPHY_A_DQ15	DDR4_DQU6_A	LPDDR4_DQ15_A	DDR3_D11	LPDDR3_D18
DDRPHY_A_DM1	DDR4_DMU_A	LPDDR4_DM1_A	DDR3_DM1	LPDDR3_DM2
DDRPHY_A_DQS1	DDR4_DQSU_P_A	LPDDR4_DQS1P_A	DDR3_DQS1P	LPDDR3_DQS2P
DDRPHY_A_DQSB1	DDR4_DQSU_N_A	LPDDR4_DQS1N_A	DDR3_DQS1N	LPDDR3_DQS2N
DDRPHY_B_DQ0	DDR4_DQU4_B	LPDDR4_DQ0_B	DDR3_D29	LPDDR3_D14
DDRPHY_B_DQ1	DDR4_DQU0_B	LPDDR4_DQ1_B	DDR3_D31	LPDDR3_D12
DDRPHY_B_DQ2	DDR4_DQU1_B	LPDDR4_DQ2_B	DDR3_D28	LPDDR3_D13
DDRPHY_B_DQ3	DDR4_DQU5_B	LPDDR4_DQ3_B	DDR3_D30	LPDDR3_D8
DDRPHY_B_DQ4	DDR4_DQU7_B	LPDDR4_DQ4_B	DDR3_D26	LPDDR3_D9
DDRPHY_B_DQ5	DDR4_DQU3_B	LPDDR4_DQ5_B	DDR3_D24	LPDDR3_D15
DDRPHY_B_DQ6	DDR4_DQU6_B	LPDDR4_DQ6_B	DDR3_D27	LPDDR3_D10
DDRPHY_B_DQ7	DDR4_DQU2_B	LPDDR4_DQ7_B	DDR3_D25	LPDDR3_D11
DDRPHY_B_DM0	DDR4_DMU_B	LPDDR4_DM0_B	DDR3_DM3	LPDDR3_DM1
DDRPHY_B_DQS0	DDR4_DQSU_P_B	LPDDR4_DQS0P_B	DDR3_DQS3P	LPDDR3_DQS1P
DDRPHY_B_DQSB0	DDR4_DQSU_N_B	LPDDR4_DQS0N_B	DDR3_DQS3N	LPDDR3_DQS1N
DDRPHY_B_DQ8	DDR4_DQL1_B	LPDDR4_DQ8_B	DDR3_D17	LPDDR3_D27
DDRPHY_B_DQ9	DDR4_DQL3_B	LPDDR4_DQ9_B	DDR3_D19	LPDDR3_D26
DDRPHY_B_DQ10	DDR4_DQL4_B	LPDDR4_DQ10_B	DDR3_D18	LPDDR3_D30

DDRPHY	DDR4	LPDDR4/LPDDR4X	DDR3	LPDDR3
DDRPHY_B_DQ11	DDR4_DQL6_B	LPDDR4_DQ11_B	DDR3_D22	LPDDR3_D31
DDRPHY_B_DQ12	DDR4_DQL0_B	LPDDR4_DQ12_B	DDR3_D16	LPDDR3_D28
DDRPHY_B_DQ13	DDR4_DQL2_B	LPDDR4_DQ13_B	DDR3_D20	LPDDR3_D24
DDRPHY_B_DQ14	DDR4_DQL7_B	LPDDR4_DQ14_B	DDR3_D21	LPDDR3_D25
DDRPHY_B_DQ15	DDR4_DQL5_B	LPDDR4_DQ15_B	DDR3_D23	LPDDR3_D29
DDRPHY_B_DM1	DDR4_DML_B	LPDDR4_DM1_B	DDR3_DM2	LPDDR3_DM3
DDRPHY_B_DQS1	DDR4_DQSL_P_B	LPDDR4_DQS1P_B	DDR3_DQS2P	LPDDR3_DQS3P
DDRPHY_B_DQSB1	DDR4_DQSL_N_B	LPDDR4_DQS1N_B	DDR3_DQS2N	LPDDR3_DQS3N
DDRPHY_A0	DDR4_A0	LPDDR4_ODT1_CA_B	DDR3_A9	LPDDR3_ODT2
DDRPHY_A1	DDR4_A1	LPDDR4_CKE1_A	DDR3_A14	—
DDRPHY_A2	DDR4_A2	LPDDR4_ODT0_CA_B	DDR3_A13	LPDDR3_ODT3
DDRPHY_A3	DDR4_A3	LPDDR4_CKE0_A	DDR3_A1	—
DDRPHY_A4	DDR4_A4	LPDDR4_A0_B	DDR3_A2	LPDDR3_A5
DDRPHY_A5	DDR4_A5	LPDDR4_A1_A	DDR3_A4	—
DDRPHY_A6	DDR4_A6	LPDDR4_CS1N_B	DDR3_A3	LPDDR3_CSN2
DDRPHY_A7	DDR4_A7	LPDDR4_A4_A	DDR3_A6	—
DDRPHY_A8	DDR4_A8	LPDDR4_A4_B	DDR3_A5	LPDDR3_A6
DDRPHY_A9	DDR4_A9	LPDDR4_CLKP_A	DDR3_A11	LPDDR3_A2
DDRPHY_A10	DDR4_A10	LPDDR4_A1_B	DDR3_A0	—
DDRPHY_A11	DDR4_A11	LPDDR4_A5_B	DDR3_A7	LPDDR3_A7
DDRPHY_A12	DDR4_A12	LPDDR4_A2_A	DDR3_A10	LPDDR3_A4
DDRPHY_A13	DDR4_A13	LPDDR4_CLKN_A	DDR3_A8	LPDDR3_A3
DDRPHY_A14	DDR4_WEN/A14	LPDDR4_CS0N_B	DDR3_ODT0	LPDDR3_CSN3
DDRPHY_A15	DDR4_CASN/A15	LPDDR4_A3_A	DDR3_BA1	LPDDR3_A0
DDRPHY_A16	DDR4_RASN/A16	LPDDR4_A0_A	DDR3_CKE0	—
DDRPHY_ACTN	DDR4_ACTN	LPDDR4_A2_B	DDR3_CSN0	LPDDR3_A9
DDRPHY_BA0	DDR4_BA0	LPDDR4_CKE0_B	DDR3_BA2	LPDDR3_CKE0
DDRPHY_BA1	DDR4_BA1	LPDDR4_A5_A	DDR3_A12	LPDDR3_A1
DDRPHY_BG0	DDR4_BG0	LPDDR4_A3_B	DDR3_BA0	LPDDR3_A8
DDRPHY_BG1	DDR4_BG1	—	DDR33_A15	—
DDRPHY_CKE	DDR4_CKE	LPDDR4_CKE1_B	DDR3_RASN	—
DDRPHY_CK	DDR4_CLKP	LPDDR4_CLKP_B	DDR3_CLKP	LPDDR3_CLKP
DDRPHY_CKB	DDR4_CLKN	LPDDR4_CLKN_B	DDR3_CLKN	LPDDR3_CLKN
DDRPHY_CSB0	DDR4_CSN0	LPDDR4_CS1N_A	DDR3_CASN	LPDDR3_CSN1
DDRPHY_CSB1	DDR4_CSN1	LPDDR4_CS0N_A	DDR3_CSN1	LPDDR3_CSN0
DDRPHY_ODT0	DDR4_ODT0	LPDDR4_ODT1_CA_A DDR3_WEN	LPDDR3_ODT0	LPDDR3_ODT0
DDRPHY_ODT1	DDR4_ODT1	LPDDR4_ODT0_CA_A DDR33_ODT1	LPDDR3_ODT1	LPDDR3_ODT1
DDRPHY_RESETN	DDR4_RESETN	LPDDR4_RESETN	DDR3_RESETN -----	LPDDR3_RESETN -----

ÿ DDR3/DDR3L: Supports swapping

of entire groups between bytes; supports swapping of DQ within a byte; CA order cannot be swapped and must be allocated according to the reference diagram; If you want to use a template with a total bit width of 16 bits or a template that supports a total bit width of 16 bits/32 bits, you must use the template provided by RK; no difference is

allowed. ÿ LPDDR3: The

D0-D7 on the chip side must be connected one-to-one with the LPDDR3_D0-D7 on the master, as well as the corresponding relationship between the associated DQS and DM.

Adjustment is not

supported. Whole-group swapping is supported

between other bytes. DQ swapping is supported

within other bytes. CA order cannot be swapped and must be allocated

according to the reference

diagram. ÿ For DDR4: Whole-group swapping is supported between bytes. DQ swapping is supported within a byte. CA order cannot be swapped and must be

allocated according to the reference diagram. If you want to use a template with a total bit width of 16 bits or a template that supports 16-bit/32-bit total bit width compatibility, you must use the template provided by RK. Differences are not allowed.

ÿ For LPDDR4/LPDDR4x: The DQ and CA

sequences cannot be swapped and must be assigned according to the reference diagram.

Connection method of DDR_RZQ (PIN 1C3) pin of RK3528 DDR PHY:

When using DDR3/DDR3L/DDR4/LPDDR3 chips, the DDR_RZQ pin must be connected to ground through a 120ohm 1% resistor. When

using LPDDR4/LPDDR4x chips, the DDR_RZQ pin must be connected to DDRPHY_VDDQ power supply (ie VCC_DDR) through a 120ohm 1% resistor.

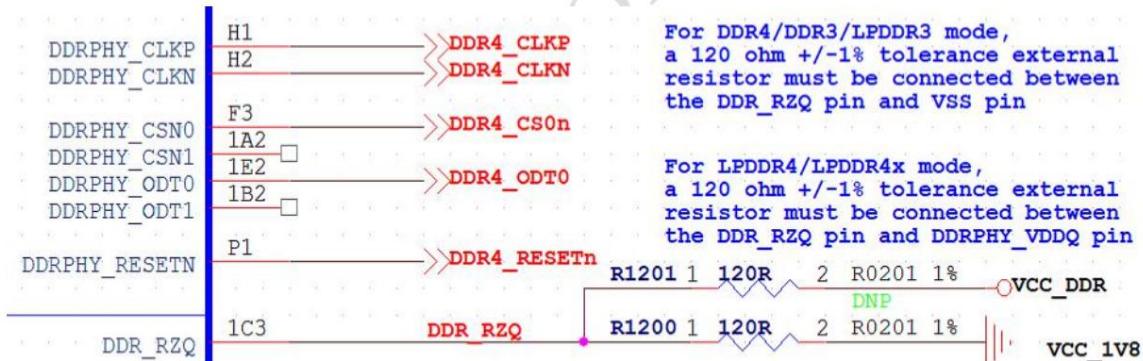


Figure 2-8 RK3528 DDR_RZQ pin

2.1.6.3 DDR Particle Peripheral Circuit Design

ÿ The ZQ pin of DDR3/DDR3L/DDR4/LPDDR3 chips must be connected to ground through a 240ohm 1%

resistor. ÿ The ZQ pin of LPDDR4 chips must be connected to the VCC_DDR power supply through a

240ohm 1% resistor. ÿ The ZQ pin of LPDDR4x chips must be connected to the VCC0V6_DDR power supply

through a 240ohm 1% resistor. ÿ A 1nF capacitor is recommended for the RESET pin of the DDR chip to

improve ESD immunity. ÿ The DDR4 16-bit chip template supports DDP (Dual-Die Package) chips. The default parameters are configured for SDP

(Single-Die Package) chips. If DDP chips are required, please ensure that the following parameters are updated simultaneously:

ÿ DDR4 M9 pin connect to DDR_BG1 net of RK3528

ÿ DDR4 T7 pin connect to GND

ÿ DDR4 E9 pin connect to GND by 240ohm 1% resistor

2.1.6.4 DDR Topology and Matching Design

ÿ DDR3/DDR3L/DDR4 4 16-bit 2CS, 4-layer PCB design. DQ adopts T topology (one drive two), CA adopts

Use Fly-by + T hybrid topology (one drive four)

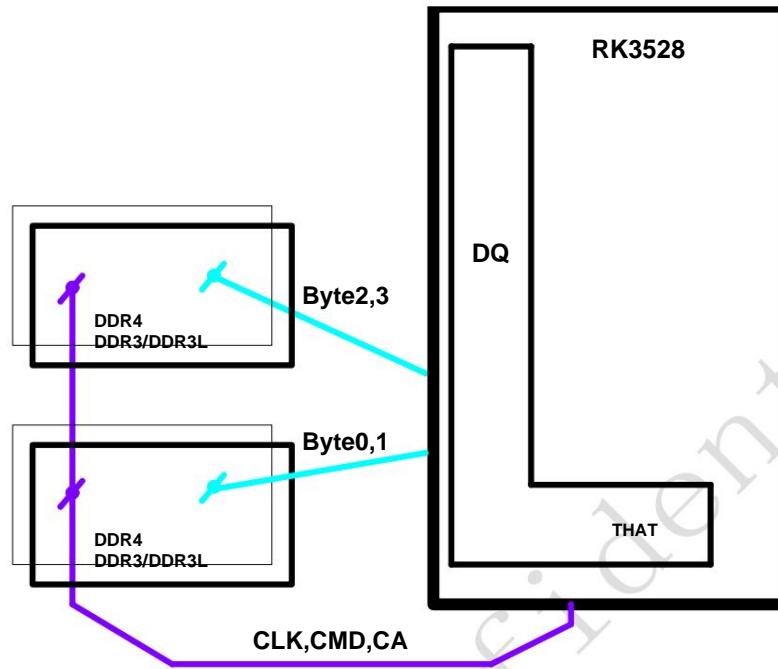


Figure 2-9 2CS 4-chip DDR3/DDR4 Fly-by + T hybrid topology

Clock matching method: Placing an RC circuit at the end of the trace (see the figure below) can improve signal quality and reduce EMI.

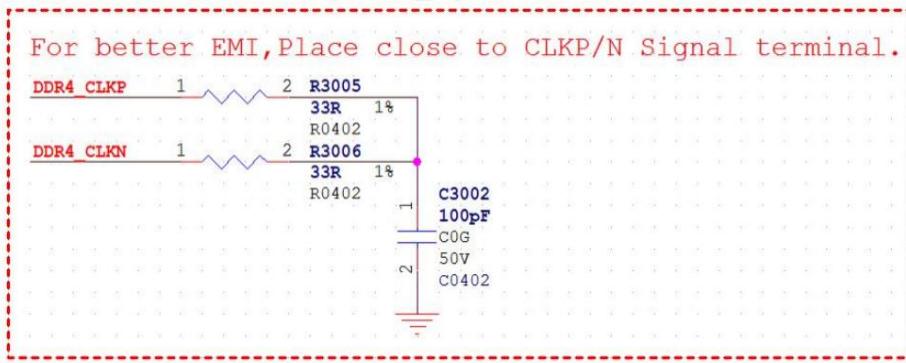


Figure 2-10 2CS 4-chip DDR3/DDR4 Fly-by + T topology CLKP/CLKN termination

ÿ DDR3/DDR3L/DDR4 2 16-bit 1CS, 4-layer PCB design. Topology 1: DQ uses point-to-point connection (one Drive one), CA uses Fly-by topology (one drive two)

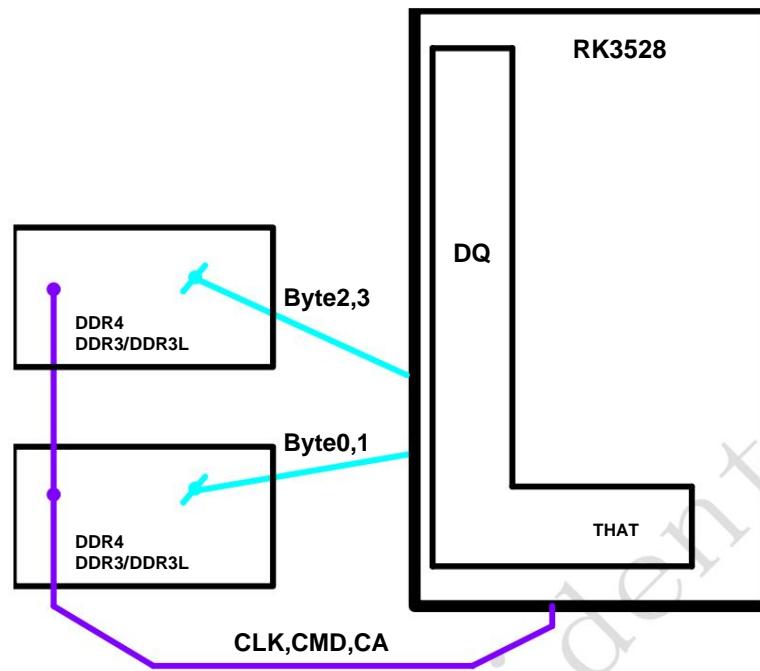


Figure 2-11 1CS 2-chip DDR3/DDR3L/DDR4 Fly-b topology

Clock matching method: Placing an RC circuit at the end of the trace (see the figure below) can improve signal quality and reduce EMI.

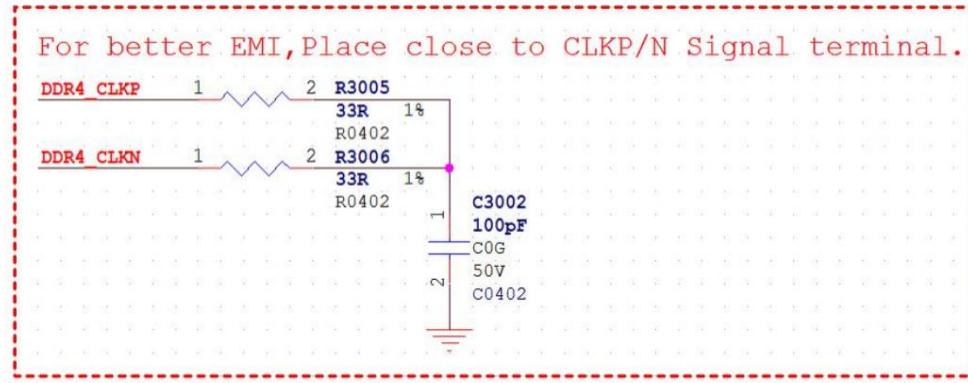


Figure 2-12 1CS 2-chip DDR3/DDR4 Fly-b topology CLKP/CLKN termination

When LPDDR3 is used with one 32-bit chip, DQ and CA adopt a point-to-point topology.

When LPDDR4 is used with one 32-bit chip, DQ and CA adopt a point-to-point topology.

When LPDDR4x is used with one 32-bit chip, DQ and CA adopt a point-to-point topology.

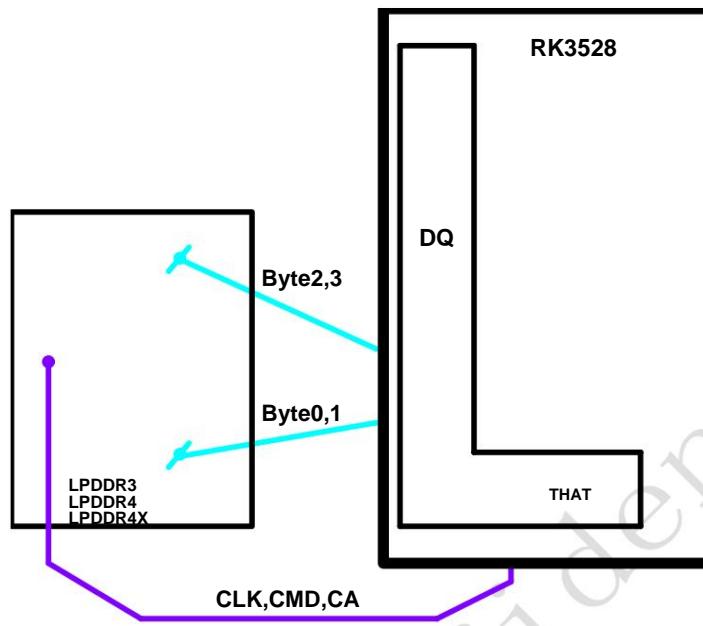


Figure 2-15 1-chip LPDDR3/LPDDR4/LPDDR4X point-to-point topology

Matching method: LPDDR4 chip DQ, CLK, CMD, CA all support ODT, and all point-to-point connections are sufficient. Matching

method: LPDDR4x chip DQ, CLK, CMD, CA all support ODT, and all point-to-point connections are sufficient.

LPDDR3 clock matching method: Placing an RC circuit at the end of the trace (see the figure below) can improve signal quality and reduce EMI.

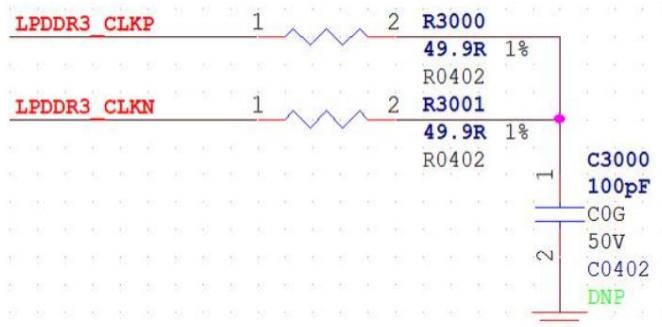


Figure 2-16 1-chip LPDDR3/LPDDR4/LPDDR4X point-to-point topology CLKP/CLKN termination

2.1.6.5 DDR Power Supply Design and Power-On Sequence Requirements

The RK3528 DDR PHY power supply is summarized as follows:

RK3528 DDR PHY has two power supplies, DDRPHY_VDDQ and DDRPHY_VDDQL. When DDR3 chips: DDRPHY_VDDQ

for 1.5V, DDRPHY_VDDQL for 1.5V. When DDR3L chips: DDRPHY_VDDQ for 1.35V, DDRPHY_VDDQL for 1.35V.

LPDDR3 chips: DDRPHY_VDDQ for 1.2V, DDRPHY_VDDQL for 1.2V (to improve compatibility, the actual supply voltage is 1.2V).

1.25V

When DDR4 chips: DDRPHY_VDDQ is 1.2V, DDRPHY_VDDQL is 1.2V

ÿ LPDDR4 particles: DDRPHY_VDDQ supply 1.1V, DDRPHY_VDDQL supply 1.1V ÿ LPDDR4x particles: DDRPHY_VDDQ supply

1.1V, DDRPHY_VDDQL supply 0.6V Power supply circuit points: ÿ VCC_DDR uses an independent BUCK TMI3112H for power supply. Be sure to modify

the FB voltage divider resistor value according to the actual DRAM particles used so that the VCC_DDR output voltage matches the particles.

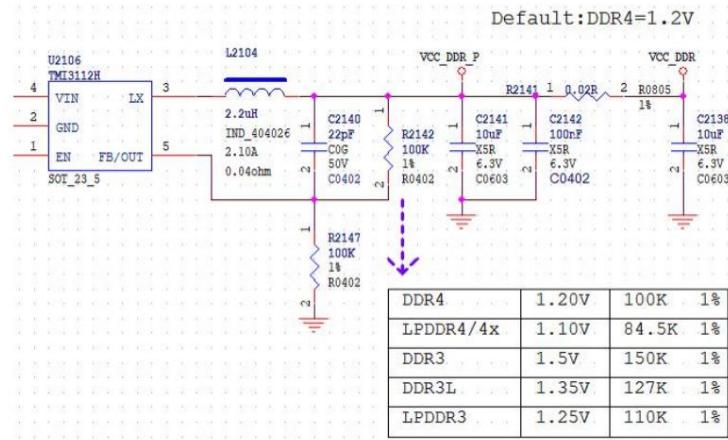


Figure 2-17 VCC_DDR FB parameter adjustment

When designing RK3528, please note that LPDDR4 and LPDDR4X chips must be used with corresponding circuits based on the actual materials.

ÿ When mounting LPDDR4 chips, only the R3004 resistor shown in the figure below needs to be mounted, and R3012 is not required.

ÿ When mounting LPDDR4x chips, only the R3012 resistor shown in the figure below needs to be mounted, and R3004 is not required.

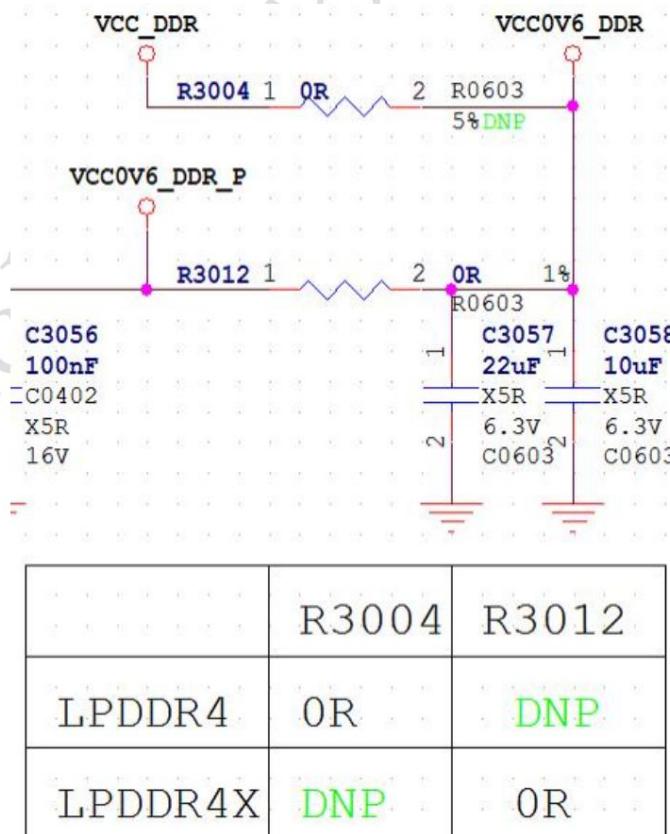


Figure 2-18 LPDDR4/LPDDR4x compatible design power supply selection

For the power-on timing requirements of various DRAM types, please refer to the JEDEC standards.

ÿ The power-on sequence of DDR3/DDR3L SDRAM is shown in the figure below:

1. Apply power (RESET# is recommended to be maintained below $0.2 \times VDD$; all other inputs may be undefined). RESET# needs to be maintained for minimum 200 us with stable power. CKE is pulled “Low” anytime before RESET# being de-asserted (min. time 10 ns). The power voltage ramp time between 300 mv to VDD_{min} must be no greater than 200 ms; and during the ramp, $VDD > VDDQ$ and $(VDD - VDDQ) < 0.3$ volts.
 - VDD and $VDDQ$ are driven from a single power converter output, AND
 - The voltage levels on all pins other than VDD , $VDDQ$, VSS , $VSSQ$ must be less than or equal to $VDDQ$ and VDD on one side and must be larger than or equal to $VSSQ$ and VSS on the other side. In addition, VTT is limited to 0.95 V max once power ramp is finished, AND
 - $Vref$ tracks $VDDQ/2$.

OR

- Apply VDD without any slope reversal before or at the same time as $VDDQ$.
- Apply $VDDQ$ without any slope reversal before or at the same time as VTT & $Vref$.
- The voltage levels on all pins other than VDD , $VDDQ$, VSS , $VSSQ$ must be less than or equal to $VDDQ$ and VDD on one side and must be larger than or equal to $VSSQ$ and VSS on the other side.

Figure 2-19 DDR3 SDRAM power-on sequence

ÿ The power-on sequence of LPDDR3 SDRAM is shown in the figure below:

After...	Applicable Conditions
Ta is reached	V_{DD1} must be greater than V_{DD2} —200mV
	V_{DD1} and V_{DD2} must be greater than V_{DDCA} —200mV
	V_{DD1} and V_{DD2} must be greater than V_{DDQ} —200mV
	V_{Ref} must always be less than all other supply voltages

Figure 2-20 LPDDR3 SDRAM power-on sequence

ÿ The power-on sequence of DDR4 SDRAM is shown in the figure below:

1. Apply power (RESET_n is recommended to be maintained below $0.2 \times VDD$; all other inputs may be undefined). RESET_n needs to be maintained for minimum 200us with stable power. CKE is pulled “ Low” anytime before RESET_n being de-asserted (min. time 10ns) . The power voltage ramp time between 300mV to V_{DD} min must be no greater than 200ms; and during the ramp, $V_{DD} \geq V_{DDQ}$ and $(V_{DD}-V_{DDQ}) < 0.3$ volts. VPP must ramp at the same time or earlier than VDD and VPP must be equal to or higher than VDD at all times.
 - V_{DD} and V_{DDQ} are driven from a single power converter output, AND
 - The voltage levels on all pins other than V_{DD} , V_{DDQ} , V_{SS} , V_{SSQ} must be less than or equal to V_{DDQ} and V_{DD} on one side and must be larger than or equal to V_{SSQ} and V_{SS} on the other side. In addition, V_{TT} is limited to TBDV max once power ramp is finished, AND
 - $VrefCA$ tracks TBD.
 - or
 - Apply V_{DD} without any slope reversal before or at the same time as V_{DDQ}
 - Apply V_{DDQ} without any slope reversal before or at the same time as V_{TT} & $VrefCA$.
 - Apply VPP without any slope reversal before or at the same time as VDD .
 - The voltage levels on all pins other than V_{DD} , V_{DDQ} , V_{SS} , V_{SSQ} must be less than or equal to V_{DDQ} and V_{DD} on one side and must be larger than or equal to V_{SSQ} and V_{SS} on the other side.

Figure 2-21 DDR4 SDRAM power-on sequence

ÿ The power-on sequence of LPDDR4/4x SDRAM is shown in the figure below:

1. While applying power (after Ta), RESET_n is recommended to be LOW ($\leq 0.2 \times V_{DD2}$) and all other inputs must be between VILmin and VIHmax. The device outputs remain at High-Z while RESET_n is held LOW. Power supply voltage ramp requirements are provided in Table 5. V_{DD1} must ramp at the same time or earlier than V_{DD2} . V_{DD2} must ramp at the same time or earlier than V_{DDQ} .

Table 5 — Voltage Ramp Conditions

After	Applicable Conditions
Ta is reached	V_{DD1} must be greater than V_{DD2}
	V_{DD2} must be greater than $V_{DDQ} - 200$ mV

NOTE 1 Ta is the point when any power supply first reaches 300 mV.

NOTE 2 Voltage ramp conditions in Table 5 apply between Ta and power-off (controlled or uncontrolled).

NOTE 3 Tb is the point at which all supply and reference voltages are within their defined ranges.

NOTE 4 Power ramp duration tINIT0 (Tb-Ta) must not exceed 20ms.

NOTE 5 The voltage difference between any of V_{SS} and V_{SSQ} pins must not exceed 100 mV.

Figure 2-22 LPDDR4/4x SDRAM power-on sequence

2.1.6.6 DDR Supported Models

For the RK3528 DDR particle support list, please refer to Rockchip Electronics' "Rockchip_Support_List_DDR" document (please contact our FAE

(Ask for it at the window).

2.1.7 eMMC Circuit

2.1.7.1 eMMC Controller Introduction

The RK3528 eMMC controller has the following features: ÿ

Compatible with 5.1, 5.0, 4.51, and 4.41 specifications; ÿ Supports three data bus widths: 1bit, 4bit, and 8bit; ÿ Supports HS400 mode, and is backward compatible with HS200, DDR50 and other modes; ÿ Supports CMD Queue.

2.1.7.2 eMMC Circuit Design Recommendations

The RK3528 eMMC interface and FSPI Flash interface are multiplexed. When designing the eMMC interface, please refer to the reference schematic for the eMMC signal connection method.

Contains decoupling capacitors for each power supply.

When using eMMC, the boot code is placed in the eMMC.

2.1.7.3 eMMC Topology and Matching Design

eMMC connection diagram:

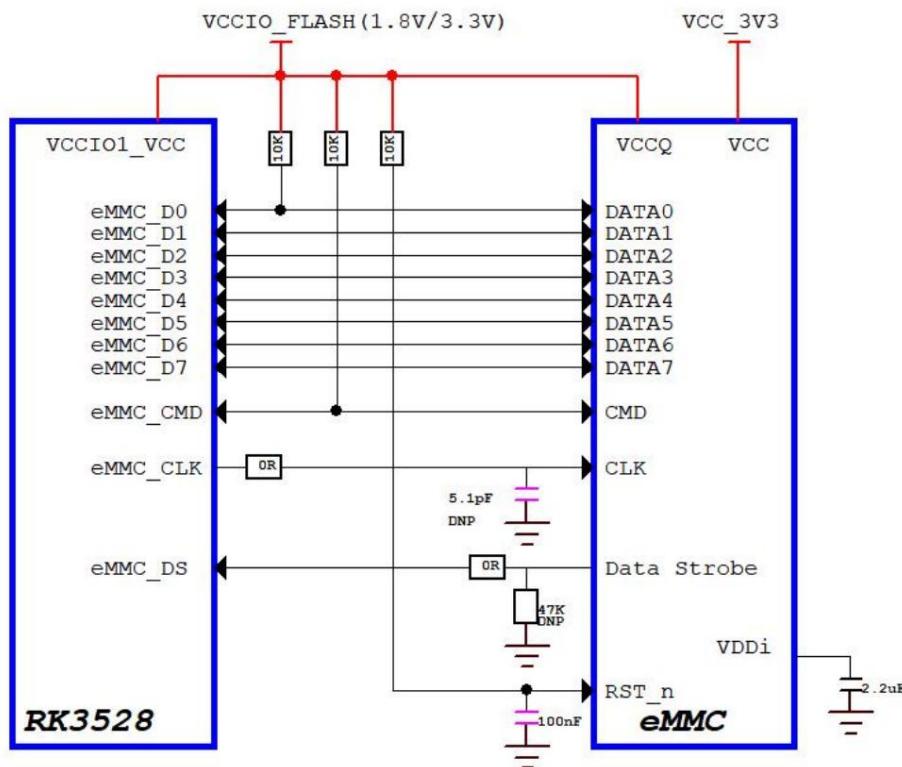


Figure 2-23 eMMC connection diagram

The following table shows the recommended pull-up and pull-down and matching designs for the eMMC interface.

Table 2-5 RK3528 eMMC interface design

Signal	Pull up and down inside the chip	Connection method	Description (chip side)
eMMC_D[7:0] pull-up		Direct connection, D0 needs to be connected to a pull-up resistor. The recommended value is 10K ohm, other Data Pull-up resistor inside the RK3528 chip	eMMC data sending/receiving
eMMC_CLK	drop down	Connect a 22ohm resistor in series with the RK3528	eMMC clock transmission
eMMC_CMD	Pull-up	Direct connection, external pull-up resistor is required, resistance value is recommended Recommended 10K ohm	eMMC command send/receive
eMMC_DATA_ Strobe	drop down	Connect a 0ohm resistor in series with the eMMC terminal and Reserve 47K ohm pull-down resistor	eMMC data and command reception reference Strobe

2.1.7.4 eMMC Power-On Sequence Requirements

The eMMC interface of the RK3528 chip belongs to the VCCIO1_VCC power domain (supports 1.8V or 3.3V), has only one set of power supply, and no timing

Require.

eMMC chips have two power supplies. Please refer to the JEDEC standard for the power-on sequence:

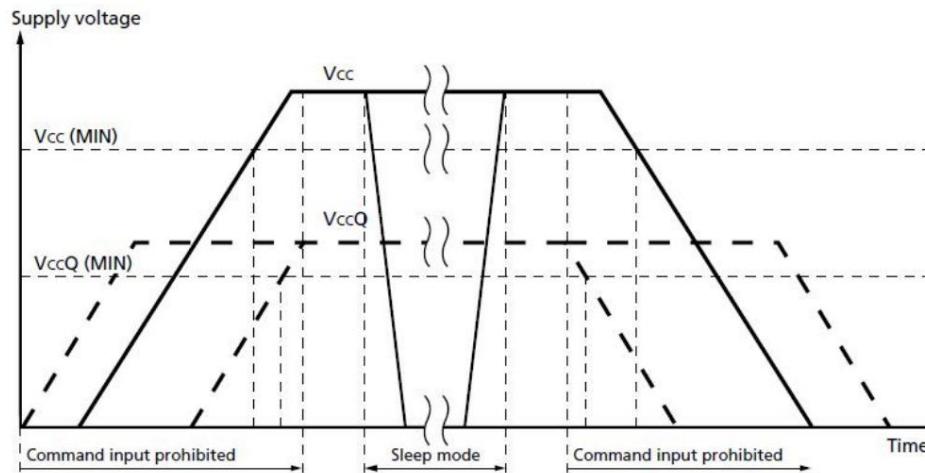


Figure 2-24 eMMC chip power-on and power-off timing

2.1.7.5 List of eMMC-supported models

For the RK3528 eMMC particle support list, please refer to Rockchip Electronics' "RKeMMCSupportList" document (please contact our FAE window (Request)).

2.1.8 FSPI Flash Circuit

2.1.8.1 Introduction to the FSPI Flash (Boot Support) Interface

FSPI is a flexible serial interface controller. There is one FSPI controller in the RK3528 chip, which can be used to connect FSPI devices.

The RK3528 FSPI controller has the following features:

- ÿ Support serial NOR Flash and serial Nand Flash;
- ÿ Support SDR mode;
- ÿ Supports 1-wire, 2-wire and 4-wire modes.



Notice:

RK3528 FSPI

Interface for connecting **Boot** or **SPI Flash/Memory**

It is not recommended to use the device for other functions. **SPI** Peripherals!

2.1.8.2 FSPI Flash Circuit Design Recommendations

The RK3528 FSPI Flash interface and EMMC interface are multiplexed, with the power domain being VCCIO1_VCC (supporting 1.8V or 3.3V).

When designing the FSPI Flash interface, please follow the reference schematic for FSPI Flash signal connections, including the power decoupling capacitors for each channel.

When using FSPI Flash, the boot code is placed in FSPI Flash.

2.1.8.3 FSPI Flash Topology and Matching Design

FSPI Flash connection diagram:

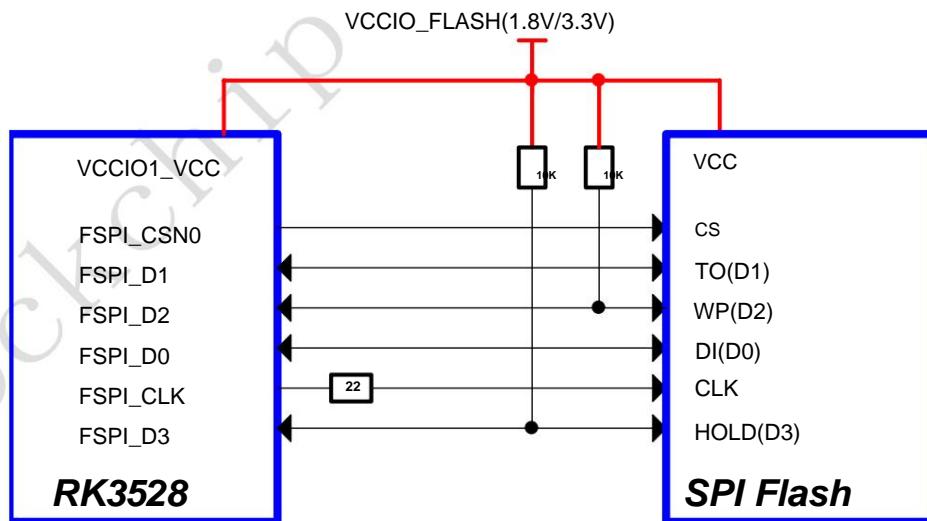


Figure 2-25 FSPI Flash connection diagram

The pull-up and pull-down and matching design recommendations for the FSPI interface are shown in the following table:

Table 2-6 RK3528 FSPI interface design

Signal	Pull up and down inside the chip	Connection method	Description (chip side)
FSPI_D[3:0]	D2 pull-up	Direct connection; D2, D3 need to reserve pull-up resistors externally.	FSPI data transmission/reception
	D0/D1/D3 pull-up	The recommended reserved resistance value is 10K ohm	
FSPI0_CLK	drop down	Connect a 22ohm resistor in series with the RK3528	FSPI clock transmission
FSPI0_CS_N0/CS_N1 pull-up		Direct connection	FSPI chip select signal

2.1.8.4 FSPI power-on timing requirements

The RK3528 chip FSPI Flash interface has only one set of power supply and no timing requirements.

SPI Flash has only one power supply, which must be the same as the power domain power supply corresponding to the selected FSPI interface.

2.1.8.5 SPI Flash Supported Models

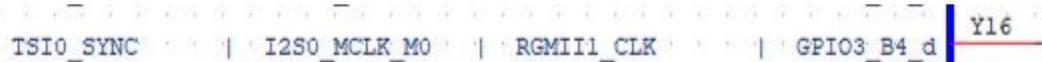
For the list of RK3528 SPI Flash particles supported, please refer to Rockchip Electronics' RK_SpiNor_and_SLC_Nand_SupportList document (please contact our FAE window to obtain it).

2.1.9 GPIO Circuit

2.1.9.1 GPIO Pin Name Description

For example, the functions TSI0_SYNC, I2S0_MCLK_M0 and RGMII1_CLK are multiplexed on GPIO3_B4.

You can choose one of the functions to use.



- ÿ Except for boot-related GPIO, the rest of the IO reset defaults to input;
- ÿ GPIOx_xx_u where _u indicates that the default state of this IO reset is internal pull-up;
- ÿ GPIOx_xx_d, where _d indicates that the default state of this IO reset is internal pull-down;
- ÿ GPIOx_xx_z where _z indicates that the default state of this IO reset is high impedance;
- ÿ The suffix of each function name is _M0 or M1 or _M2, which means the same function is multiplexed on different IOs. Only one of them can be selected at a time.

For example, when selecting the UART2 function, you must select the combination of UART2_TX_M0 and UART2_RX_M0.

The combination of UART2_TX_M0 and UART2_RX_M1 has the same constraints for all functions with different IOMUX.

2.1.9.2 GPIO drive capability

In RK3528, GPIO provides multiple levels of adjustable drive strength, which are Level 0-5 for most and Level 0-3 for some GPIOs.

For details, please refer to the RK3528_PinOut document. In addition, the initial default drive strength varies depending on the type of GPIO.

Please refer to the chip TRM for configuration modification, or refer to "SupportDriveStrength" in Table 5 of the "RK3528_PinOut" document.

and Default IO DriveStrength columns.

2.1.9.3 GPIO Power Supply

In RK3528, there are two types of GPIO: one that only supports 3.3V and the other that supports 1.8V/3.3V.

The power pins of the GPIO power domain are described as follows:

Table 2-7 RK3528 GPIO power pin description

Power Domain	GPIO Type	Pin Name	describe
PRIVATE LIMITED	3.3V	PMUIO_VCC3V3	3.3V Only IO supply for this GPIO domain (group).
VCCIO0_VCC(n=0-4) 1.8V/3.3V		VCCIO0_VCC	1.8V or 3.3V IO supply for this GPIO domain (group).

PMUIO is a fixed-level power domain and cannot be configured.

VCCIO0_VCC (n=0-4) power domain RK3528 chip can automatically identify the voltage of the hardware configuration, without the need for software to power the hardware.

pressure to configure.

For example, if the VCCIO0 power domain is configured to 1.8V, VCCIO0_VCC=1.8V; if it is configured to 3.3V, VCCIO0_VCC=3.3V.

Notes:

ÿ In addition, please note that the IO level of the power domain must be consistent with the IO level of the connected peripheral chip/device;

ÿ Each power domain power supply pin must be placed near at least one 100nF decoupling capacitor. For detailed design, see the reference schematic diagram. Do not delete it at will.

remove;

ÿ If all IOs in a power domain are not used, the power supply of this power domain can be unpowered and the pin can be left floating.

2.2 Power Supply Design

2.2.1 Introduction to RK3528 Power Supply

2.2.1.1 RK3528 chip power requirements

Table 2-8 RK3528 chip power requirements

Module	Power pin	describe
PLL	PMU_PLL_AVDD0V9ÿPMU_PLL_AVDD1V8	System PLL, DDR PLL power supply
PMU_DVDD	PMU_LOGIC_DVDD	PMU logic power supply
DDR PLL	DDR_PLL_AVDD1V8	DDR PHY PLL power supply
DDR VDDQ	DDR_VDDQ	DDR IO power supply (except ck\cke\reset Power supply)
DDR VDDQL	DDR_VDDQL	LPDDR4/4X_CKE &RESET source
CPU_DVDD	CPU_DVDD	A53_0ÿA53_1ÿA53_2ÿA53_3 power supply
GPU_DVDD	GPU_DVDD	GPU power supply
LOGIC_DVDD	LOGIC_DVDD	Logic power supply
IT	VCCIO0_VCCÿVCCIO2_VCCÿ VCCIO3_VCCÿVCCIO4_VCC	Power supply for each GPIO
IT	PMUIO_VCC3V3	PMUIO power supply



Module	Power pin	describe
IT	VCCIO1_VCC	EMMCIO power supply
USB2.0 PHY	USB20_DVDD0V9�USB20_AVDD1V8 USB20_AVDD3V3	USB2.0 HOST ȳ USB2.0 OTG PHY power
PCIe2.0/U3 Combo PHY	PCIE20_USB30_AVDD0V9�PCIE20_USB30_AVDD1V8	PCIe20/U3 Combo PHY Power Supply
SARADC	SARADC_AVDD1V8	Power supply for SAR ADC and TSADC
OTP	OTP_VCC1V8	OTP Power Supply
HDMI TX PHY	HDMI_TX_DVDD0V9�HDMI_TX0_AVDD1V8	HDMI 2.0 PHY power supply
ACODEC PHY	ACODEC_AVDD1V8	ACODEC PHY Power Supply
VDAC PHY	VDAC_AVDD1V8	VDAC PHY power supply
FEPHY PHY	FEPHY_AVDD0V9�FEPHY_AVDD1V8�FEPHY_AVDD3V3 FEPHY PHY ȳ	

2.2.1.2 RK3528 chip power-on timing requirements

In theory, the low voltage of the same module should be powered on first and the high voltage should be powered on later; the same modules with the same voltage should be powered on together, and there is no timing requirement between different modules.

After the last voltage is stable after power-on, RESETn must be released for at least 10ms.

The typical power-on sequence recommended by the reference diagram is as follows:

Digital power supply:

PMU_PLL_AVDD0V9� PMU_LOGIC_DVDD� LOGIC_DVDD ȳ
PMU_PLL_AVDD1V8�CPU_DVDD/GPU_DVDD
ȳ SARADC:
LOGIC_DVDD ȳ SARADC_AVDD1V8
ȳ OTPȳ
LOGIC_DVDD ȳ OTP_VCC1V8
ȳ USB PHYȳ
LOGIC_DVDD /USB20_DVDD0V9 ȳ USB20_AVDD1V8 ȳ USB20_AVDD3V3
ȳ PCIe20/U3 Combo PHYȳ
PCIE20_USB30_AVDD0V9� PCIE20_USB30_AVDD1V8
ȳ HDMI PHYȳ
LOGIC_DVDD/ HDMI_TX_DVDD0V9ȳ HDMI_TX0_AVDD1V8
ȳ DDR PHYȳ
LOGIC_DVDD ȳ DDR_PLL_AVDD1V8ȳ DDR_VDDQL/DDR_VDDQ
ȳ FEPHY PHYȳ
FEPHY_AVDD0V9 ȳ FEPHY_AVDD1V8ȳ FEPHY_AVDD3V3
ȳ VDACȳ
LOGIC_DVDD ȳ VDAC_AVDD1V8

According to the power network names assigned in the reference schematic, the overall recommended power-on sequence is as follows:

PMU_PLL_AVDD0V9�LOGIC_DVDDȳUSB20_DVDD0V9�PCIE20_USB30_AVDD0V9ȳ
HDMI_TX_DVDD0V9ȳFEPHY_AVDD0V9ȳCPU_DVDDȳGPU_DVDD
ȳ PMU_PLL_AVDD1V8ȳDDR_PLL_AVDD1V8ȳSARADC_AVDD1V8ȳOTP_VCC1V8ȳ

USB20_AVDD1V8 ў PCIE20_USB30_AVDD1V8 ў HDMI_TX0_AVDD1V8 ў FEPHY_AVDD1V8 ў

VDAC_AVDD1V8 ў ACODEC_AVDD1V8

ў FEPHY_AVDD3V3 ў USB20_AVDD3V3 ў PMUIO_VCC3V3

ў VCC_DDR ў DDR_VDDQ/DDR_VDDQL ў RESETn

Note: In actual application, the power supply of VCC_1V8 is VCC_3V3. The risk is controllable because VCC_1V8 is higher than VCC_3V3.

Reach system operating demand levels earlier.

2.2.1.3 RK3528 chip power-off timing requirements

During the power-off process, RESETn must be pulled low first, and then all power supplies are powered off.

2.2.2 Power Supply Design Recommendations

2.2.2.1 Power-on and standby circuit solutions

The power supply status of each module when RK3528 is powered on for the first time is as follows:

Table 2-9 Power supply requirements for each module when RK3528 is powered on for the first time

Module	Power pin	Power supply requirements for the first time
PLL	PMU_PLL_AVDD0V9 ў PMU_PLL_AVDD1V8	Power supply required
PMU_DVDD	PMU_LOGIC_DVDD	Power supply required
DDR PLL	DDR_PLL_AVDD1V8	Power supply required
DDR_VDDQ	DDR_VDDQ	Power supply required
DDR_VDDQL	DDR_VDDQL	Power supply required
CPU_DVDD	CPU_DVDD	No power supply required
GPU_DVDD	GPU_DVDD	No power supply required
LOGIC_DVDD	LOGIC_DVDD	Power supply required
IT	VCCIO0_VCC ў VCCIO2_VCC ў VCCIO3_VCC ў VCCIO4_VCC	No power supply required
IT	PMUIO_VCC3V3	Power supply required
IT	VCCIO1_VCC	Power supply required
USB2.0 PHY	USB20_DVDD0V9 ў USB20_AVDD1V8 ў USB20_AVDD3V3	Power supply required
PCIe2.0/U3 Combo PHY	PCIE20_USB30_AVDD0V9 ў PCIE20_USB30_AVDD1V8	Power supply required
SARADC	SARADC_AVDD1V8	Power supply required
OTP	OTP_VCC1V8	Power supply required
HDMI TX PHY	HDMI_TX_DVDD0V9 ў HDMI_TX0_AVDD1V8	No power supply required
Acodec PHY	ACODEC_AVDD1V8	No power supply required
VDAC PHY	VDAC_AVDD1V8	No power supply required
FEPHY PHY	FEPHY_AVDD0V9 ў FEPHY_AVDD1V8 ў FEPHY_AVDD3V3	No power supply required

2.2.2.2 PLL Power Supply

The RK3528 chip PLL is distributed in two parts, as follows:

Table 2-10 RK3528 internal PLL introduction

Module	power supply	Standby mode
Inside the DDR&PMU unit	PMU_PLL_AVDD0V9 and PMU_PLL_AVDD1V8 cannot be powered off.	
DDR PHY PLL	DDR_PLL_AVDD1V8	Do not turn off the power

ŷ PMU_PLL_AVDD0V9: Peak current 10mA

ŷ PMU_PLL_AVDD1V8: Peak current 10mA

DDR_PLL_AVDD1V8: Peak current 5mA

It is recommended to use LDO power supply:

ŷ 0.9V AC requirement ŷ<20mVŷ

ŷ 1.8V AC requirement ŷ<50mV

A stable PLL power supply helps improve chip working stability, and the decoupling capacitors should be placed close to the pins. For specific capacitor quantity and capacity, refer to

Schematic diagram, please do not adjust it at will.

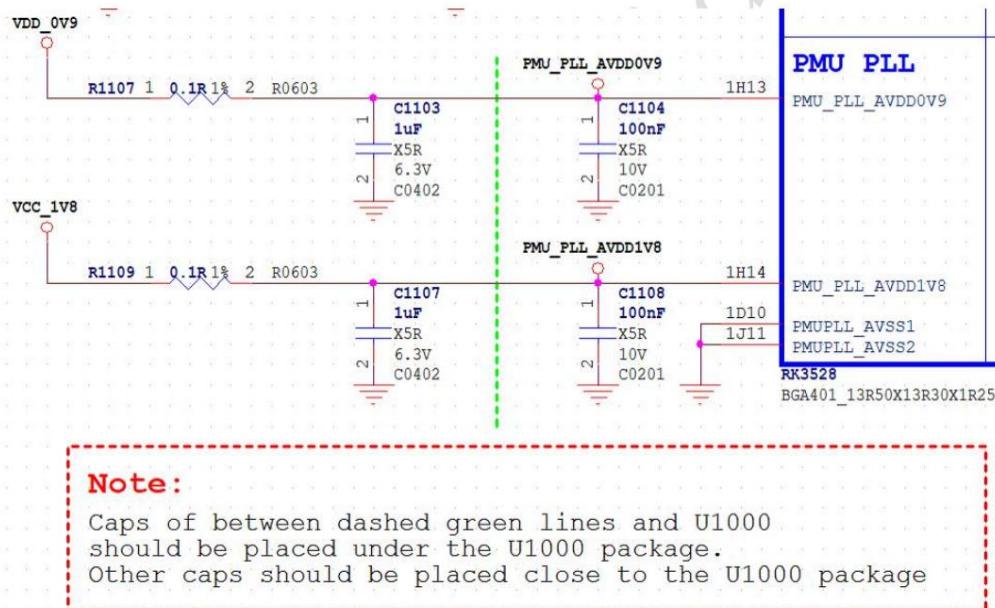


Figure 2-26 RK3528 chip PLL power pin

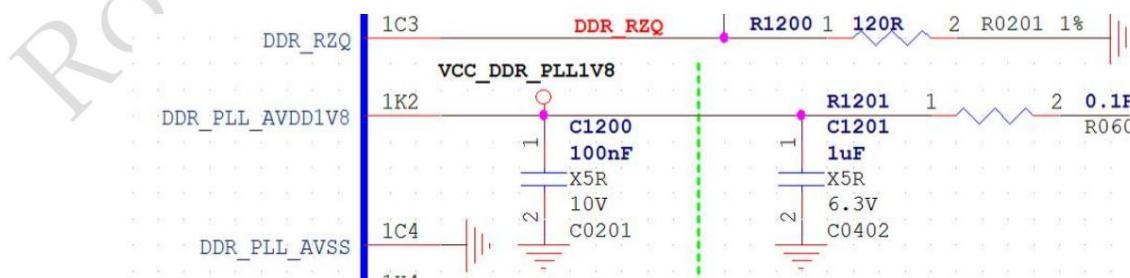


Figure 2-27 RK3528 chip DDR PHY PLL power pin

2.2.2.3 PMU LOGIC_DVDD Power Supply

The PMU_LOGIC_DVDD power supply of RK3528 supplies power to the LOGIC of the internal PMU unit. The peak current is 50mA. Please do not delete it.

Decoupling capacitors in the RK3528 chip reference design schematic.

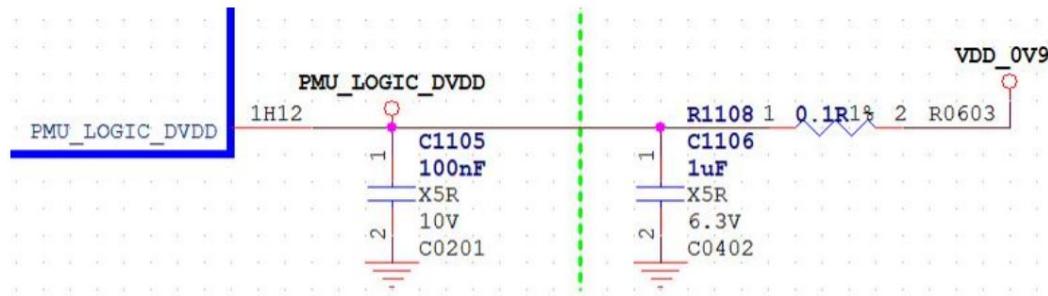


Figure 2-28 RK3528 chip PMU_LOGIC_DVDD power pin

2.2.2.4 CPU_DVDD Power Supply

The CPU_DVDD power supply of RK3528 is used to power the CORE1–CORE4 units of A53. It uses a DC/DC power supply and supports dynamic frequency and voltage regulation. The default supply voltage is 0.9V. The peak current can reach more than 1.5A. Please do not delete the RK3528 chip reference design principle.

The decoupling capacitors in the figure.

The main requirements for DC/DC BUCK are as follows:

- ÿ Output current is greater than 1.5A with a 30% margin;
- ÿ Output voltage accuracy requirement is $\pm 1.5\%$; ÿ Buck transient response requirement: $I_{load} = \text{Buck Max current} * 10\% - \text{Buck Max current} * 80\%$ jump, slope 1A/us, ripple

The wave is required to be within $\pm 5\%$;

If you are sensitive to the power consumption of the entire machine, you also need to consider the efficiency issue.

During layout, place the capacitors between the green line and the chip on the back of the RK3528 chip. The total capacitance of the CPU_DVDD power supply is

It needs to be greater than 30uF to ensure that the power ripple is within $\pm 5\%$ and avoid excessive power ripple under heavy load conditions.

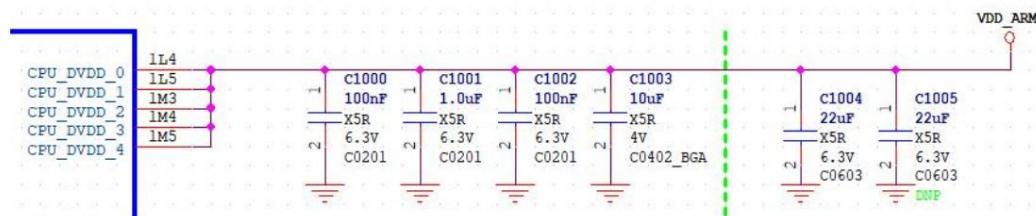


Figure 2-29 RK3528 chip CPU_DVDD power pin

2.2.2.5 LOGIC_DVDD Power Supply

The RK3528's LOGIC_DVDD power supply provides power to the internal logic unit. It uses an independent DC/DC power supply, supports dynamic frequency and voltage modulation, and defaults to a fixed voltage supply. Peak current can reach over 1.5A. Do not delete the decoupling capacitors in the RK3528 chip reference design schematic.

The main requirements for DC/DC bucks are as follows: Output

- current must be greater than or equal to 1.5A with a 30% margin; Output voltage accuracy must be within $\pm 1.5\%$;

ŷ Buck transient response requirements: $I_{load} = \text{BUCK Max current} * 10\% - \text{BUCK Max current} * 80\% \text{ jump, slope } 1A/\mu s, \text{ ripple}$

The wave is required to be within $\pm 5\%$:

If you are sensitive to the power consumption of the entire machine, you also need to consider the efficiency issue.

During layout, place the capacitors between the green line and the chip on the back of the RK3528 chip. The total capacitance of the LOGIC_DVDD power supply must be greater than 30uF to avoid excessive power ripple under heavy load conditions.

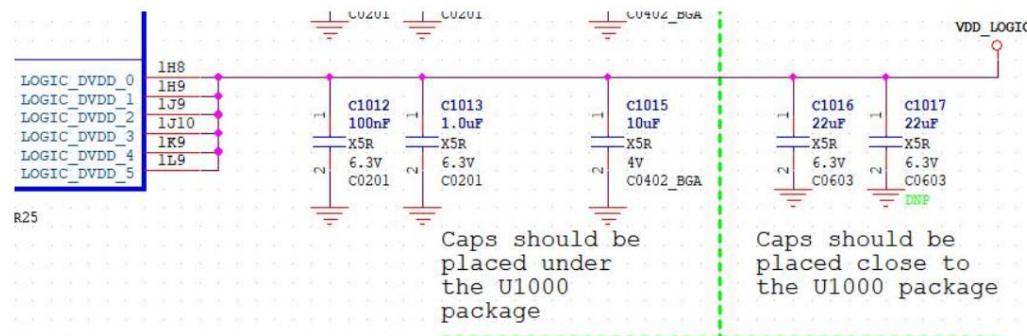


Figure 2-30 LOGIC_DVDD power supply capacitor

2.2.2.6 GPU_DVDD Power Supply

The GPU_DVDD power supply of RK3528 supplies power to the internal GPU unit. It uses an independent DC/DC power supply and supports dynamic frequency modulation.

Voltage regulation function, the default fixed voltage power supply. Do not delete the decoupling capacitor in the RK3528 chip reference design schematic.

In actual product design, GPU_DVDD and LOGIC_DVDD can be combined for power supply. The main requirements for the

DC/DC BUCK are as follows: ŷ Output current greater than or equal

to 0.5A with a 30% margin; ŷ Output voltage accuracy must be within $\pm 1.5\%$; ŷ BUCK transient

response requirements: $I_{load} = \text{BUCK Max current} * 10\% - \text{BUCK Max current} * 80\% \text{ jump, slope } 1A/\mu s, \text{ ripple}$

The wave is required to be within $\pm 5\%$:

If you are sensitive to the power consumption of the entire machine, you also need to consider the efficiency issue.

During layout, place the capacitors from the green line to the chip position on the back of the RK3528 chip. The total capacitance of the GPU_DVDD power supply is

It needs to be greater than 10uF to ensure that the power ripple is within $\pm 5\%$ and avoid excessive power ripple under heavy load conditions.

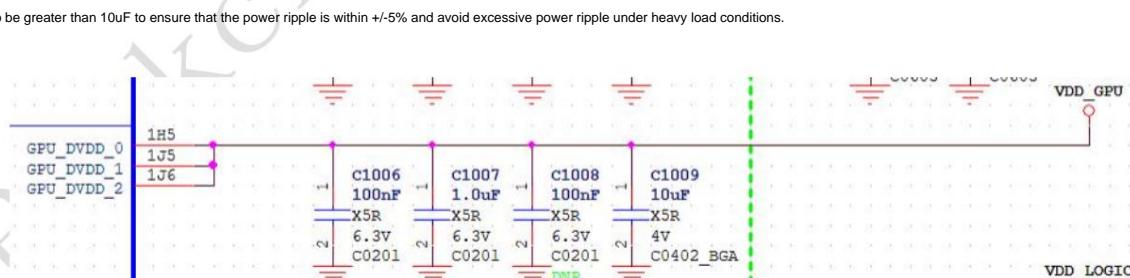


Figure 2-31 RK3528 chip GPU_DVDD power pin

2.2.2.7 DDR_VDDQ/DDR_VDDQL Power Supply

The DDR PHY interface of the RK3528 chip supports DDR3/DDR3L/DDR4/LPDDR4/LPDDR4x level standards.

The PHY has two power supplies, DDRPHY_VDDQ and DDRPHY_VDDQL. For power supply information, see 2.1.6.5 DDR Power Supply Design and Power-On Sequence Requirements. When designing a product, ensure that the chip usage meets the design requirements.

Similarly, a DC/DC power supply is used. Different chips have different peak currents. Please select according to the actual chip and evaluate the peak current. When using a single LPDDR3, a single LPDDR4, a single LPDDR4x, or two 16-bit DDR3/3L chips, or two 16-bit DDR4 chips, a 1A DC/DC can be used. For more than two DDR3 or DDR4 chips, a DC/DC of 2A or more is recommended. In addition, do not delete the decoupling capacitors in the RK3528 chip reference design schematic.

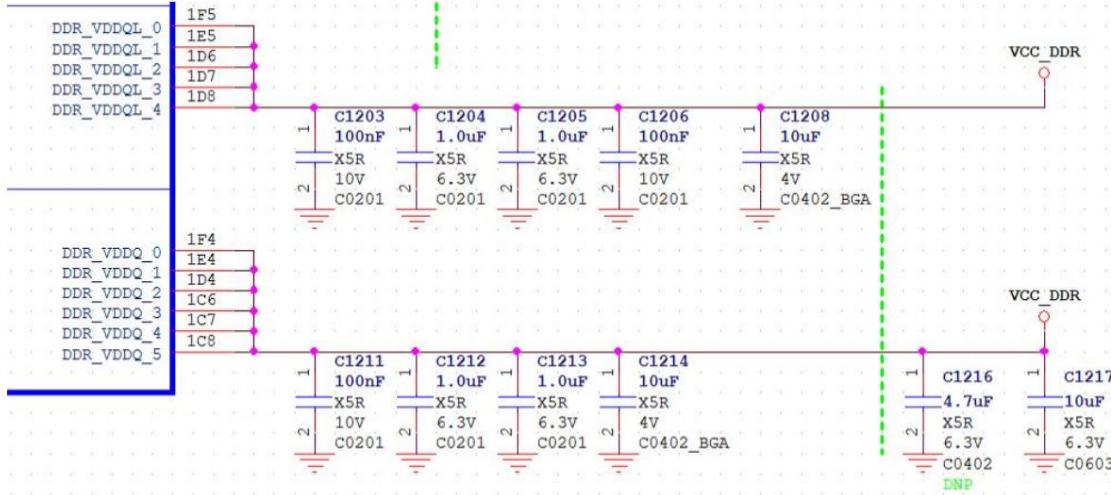


Figure 2-32 DDR power pins of the RK3528 chip in DDR3/DDR3L/DDR4/LPDDR3/LPDDR4 mode

When designing the layout, place the filter capacitor within the green dotted line in the figure below on the back of the RK3528 chip to ensure that the power ripple is within 80mV and avoid large power ripple caused by heavy load.

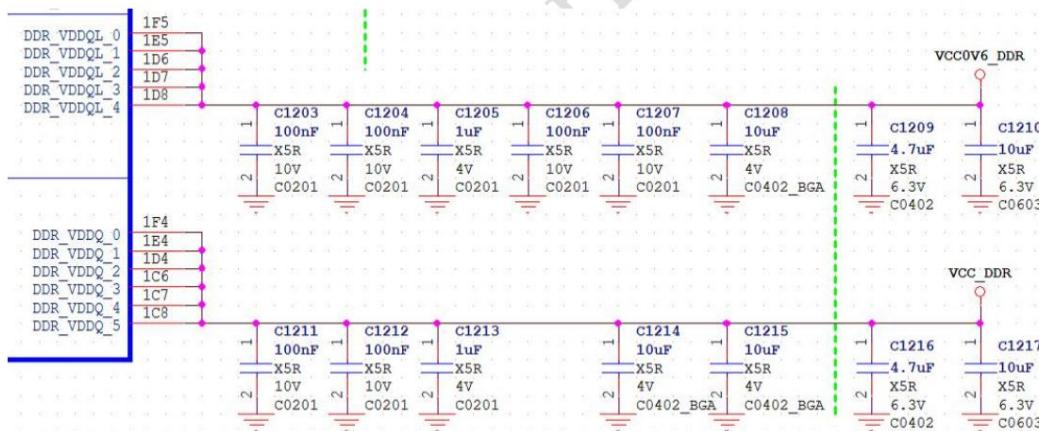


Figure 2-33 Power filter capacitors for the RK3528 chip in LPDDR4/4x mode

2.2.2.8 USB2.0 PHY Power Supply

RK3528 has two USB2.0 interfaces. For detailed connection methods, please refer to **2.3.4 Introduction to USB2.0/USB Circuit Unit**.

USB20_DVDD0V9, USB20_AVDD1V8, USB20_AVDD3V3 power is provided to USB20_HOST1_DP/M,

USB20_OTG0_DP/M PHY power supply, do not delete the decoupling capacitors in the RK3528 chip reference design schematic.

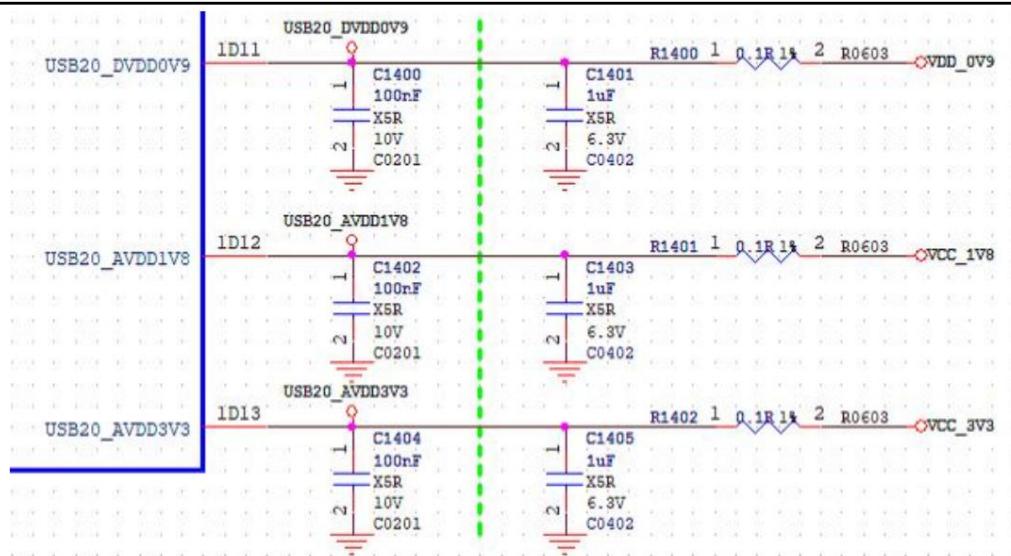


Figure 2-34 RK3528 USB2.0 PHY power pin

USB20_DVDD0V9: Peak current 5mA

USB20_AVDD1V8: Peak current 30mA

USB20_AVDD3V3: Peak current 10mA

It is recommended to use LDO power supply:

0.9V AC requirement <25mV

1.8V AC requirement: <50mV; 3.3V AC

requirement: <200mV A stable power supply helps

improve chip operating stability, and decoupling capacitors should be placed close to the pins. For the specific number and capacity of capacitors, refer to the principle

Since the **RK3528** chip

firmware must be downloaded from the **USB20_OTG0_DP/M interface**, the first time it is powered on, **USB20_DVDD0V9**, **USB20_AVDD1V8** and **USB20_AVDD3V3** must be powered.

2.2.2.9 PCIE2.0/USB3.0 Combo PHY Power Supply

RK3528 has one PCIE2.0/USB3.0 Combo PHY interface:

PCIE20_USB30_AVDD0V9, **PCIE20_USB30_AVDD1V8** power is for PCIE2.0/USB3.0 Combo PHY

For power supply, please do not delete the decoupling capacitors in the RK3528 chip reference design schematic.

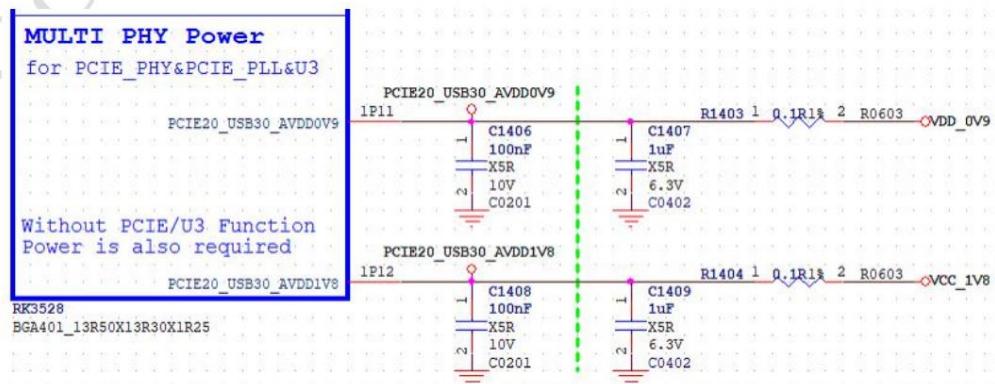


Figure 2-35 RK3528 PCIE2.0/USB3.0 Combo PHY power pin

PCIE20_USB30_AVDD0V9: Peak current 50mA
PCIE20_USB30_AVDD1V8: Peak

current 20mA It is recommended to use LDO power supply:

0.9V AC requirement <20mV

1.8V AC requirement: <50mV A stable power supply

helps improve chip operating stability, and the decoupling capacitors should be placed close to the pins. For the specific number and capacity of capacitors, refer to the principle

When this function is not used,

due to the need for power supply of the internal PLL module of RK3528 , there is an internal logic relationship, so PCIE2.0/USB3.0

The PHY port must also be powered.

2.2.2.10 ACODEC & VDAC PHY Power Supply

RK3528 has one integrated Acodec PHY interface and one VDAC PHY interface.

ACOCEC_AVDD1V8 and VDAC_AVDD1V8 are powered by ACODEC&VDAC PHY, please do not delete the RK3528 chip

Refer to the decoupling capacitors in the design schematic. As shown in the figure below, the capacitor layout on the left side of the green dotted line needs to be close to the chip pins.

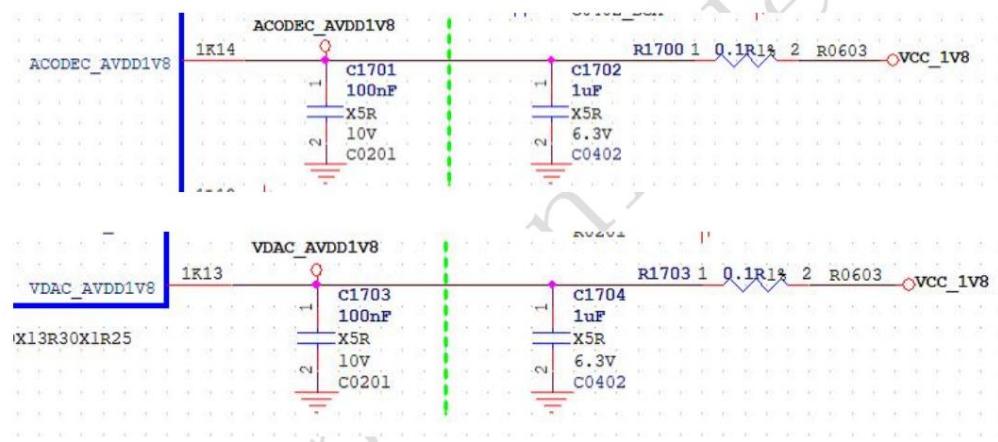


Figure 2-36 RK3528 ACODEC&VDAC PHY power pins

ACOCEC_AVDD1V8: Peak current 5mA
VDAC_AVDD1V8: Peak

current 5mA It is recommended to use LDO power supply:

1.8V AC requirement: <50mV A stable power supply

helps improve chip operating stability, and decoupling capacitors should be placed close to the pins. Refer to the schematic diagram for the specific number and capacity of capacitors. Do not adjust them arbitrarily.

If the ACODEC & VDAC functions are not used, ACOCEC_AVDD1V8 and VDAC_AVDD1V8 do not need to be powered. It is recommended to leave them floating.

2.2.2.11 FEPHY Power Supply

RK3528 has one FEPHY interface. The three power supplies FEPHY_AVDD0V9, FEPHY_AVDD1V8, and FEPHY_AVDD3V3 are used to power FEPHY. Please do not delete the decoupling capacitors in the RK3528 chip reference design schematic.

The layout needs to be close to the chip pins.

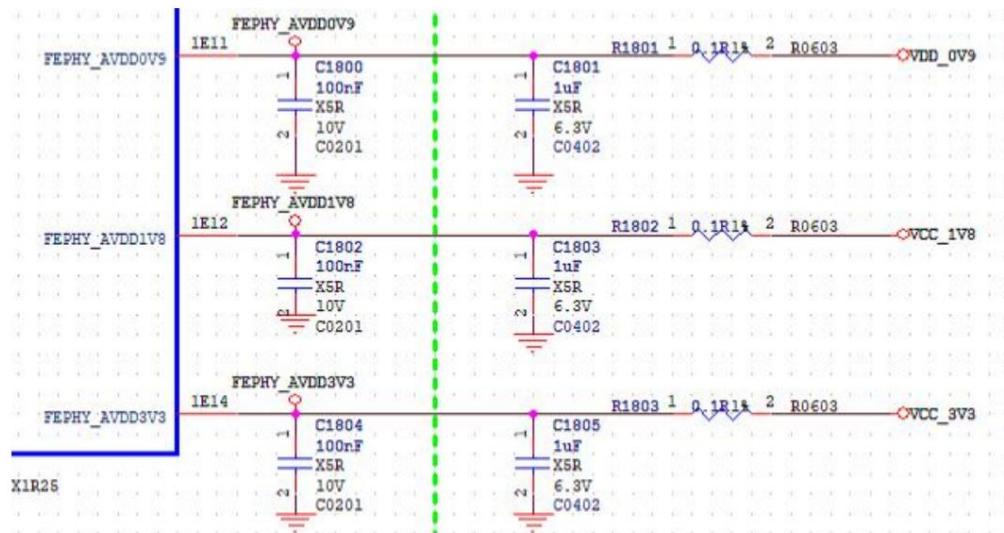


Figure 2-37 RK3528 FEPHY power pins

ÿ FEPHY_AVDD0V9: Peak current 5mA
ÿ FEPHY_AVDD1V8:

Peak current 30mA
ÿ FEPHY_AVDD3V3: Peak current 10mA It

is recommended to use LDO power supply:

ÿ 0.9V AC requirement <20mV

ÿ 1.8V AC requirement: <50mV
ÿ 3.3V AC

requirement: <200mV A stable power supply helps

improve chip operating stability, and decoupling capacitors should be placed close to the pins. For the specific number and capacity of capacitors, refer to the principle

Please do not adjust the picture at will.

If the FEPHY function is not used, then FEPHY_AVDD0V9, FEPHY_AVDD1V8 and FEPHY_AVDD3V3 can be used.

No power supply, it is recommended to leave it floating.

2.2.2.12 HDMI Power

RK3528 has one HDMI PHY interface and supports HDMI2.0 4K/60fps.

HDMI_TX_DVDD0V9 and HDMI_TX_AVDD1V8 power supplies are used to power the HDMI PHY. Please do not delete the decoupling capacitors in the RK3528 chip reference design schematic.

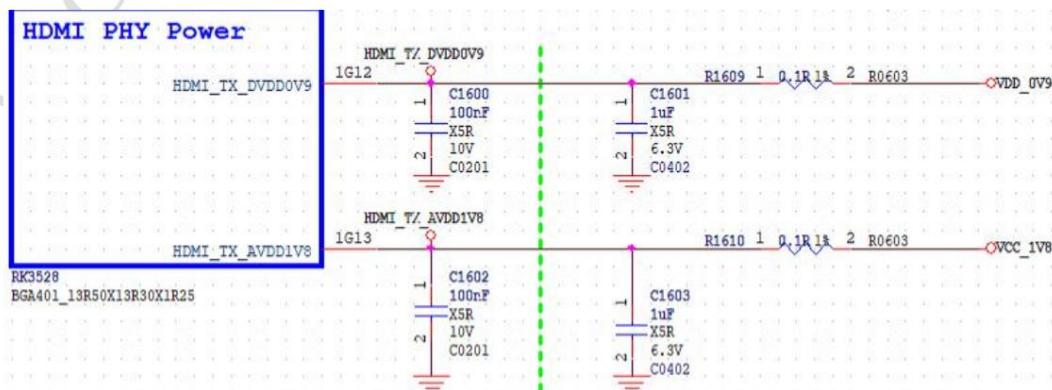


Figure 2-38 RK3528 HDMI2.0 PHY power pin

ÿ HDMI_TX_DVDD0V9: Peak current is 10mA
ÿ HDMI_TX_AVDD1V8: Peak

current is 20mA It is recommended to use LDO power supply:

ÿ 0.9V AC requirement $<20mV$

ÿ 1.8V AC requirement: $<50mV$ A stable power supply

helps improve chip operating stability, and the decoupling capacitors should be placed close to the pins. For the specific number and capacity of capacitors, refer to the principle

Please do not adjust the picture at will.

If the HDMI function is not used, HDMI_TX_DVDD0V9 and HDMI_TX_AVDD1V8 can be powered off. It is recommended to leave them suspended.

Empty processing.

2.2.2.13 SARADC/OTP Power Supply

RK3528 has 1 SARADC with 4 inputs. SARADC_AVDD1V8 is used to power SARADC and TSADC.

Delete the decoupling capacitor in the RK3528 chip reference design schematic.

ÿ SARADC_AVDD1V8: Peak current: 1.5mA It is recommended to use

LDO power supply:

ÿ PSRR@1KHz should be greater than 65dB

ÿ 1.8V AC requirement $<50mV$

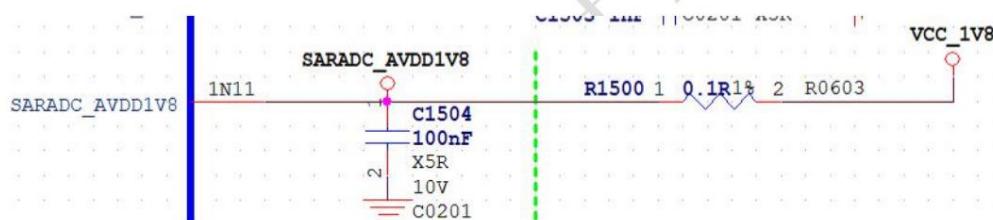


Figure 2-39 RK3528 SARADC power pin

RK3528 has one OTP. OTP_VCC1V8 is used to power the OTP. Do not delete the capacitor in the RK3528 chip reference design schematic. ÿ OTP_VCC1V8: Peak

current 60mA. LDO or DC/DC can be used to power the

OTP.

A stable power supply helps improve chip operating stability, and decoupling capacitors should be placed close to the pins. For the specific number and capacity of capacitors, refer to the schematic diagram and do not adjust them at will.

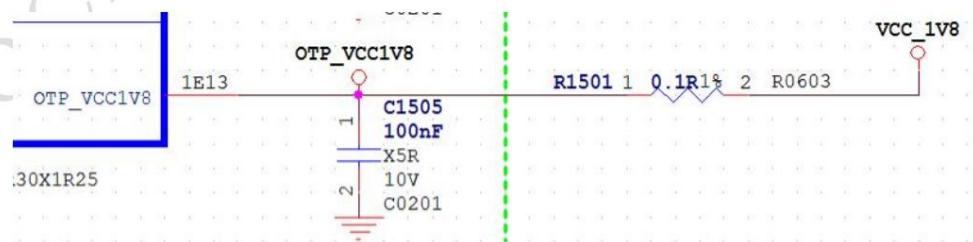


Figure 2- 40 RK3528 OTP power pin

2.2.3 Introduction to RK3528 Discrete Power Supply Solution

2.2.3.1 RK3528+ Discrete Power Supply Power Tree

Discrete power supply solution, GPU_DVDD and LOGIC_DVDD are combined into one power supply in product design, thus saving one DC/DC circuit and reducing cost.

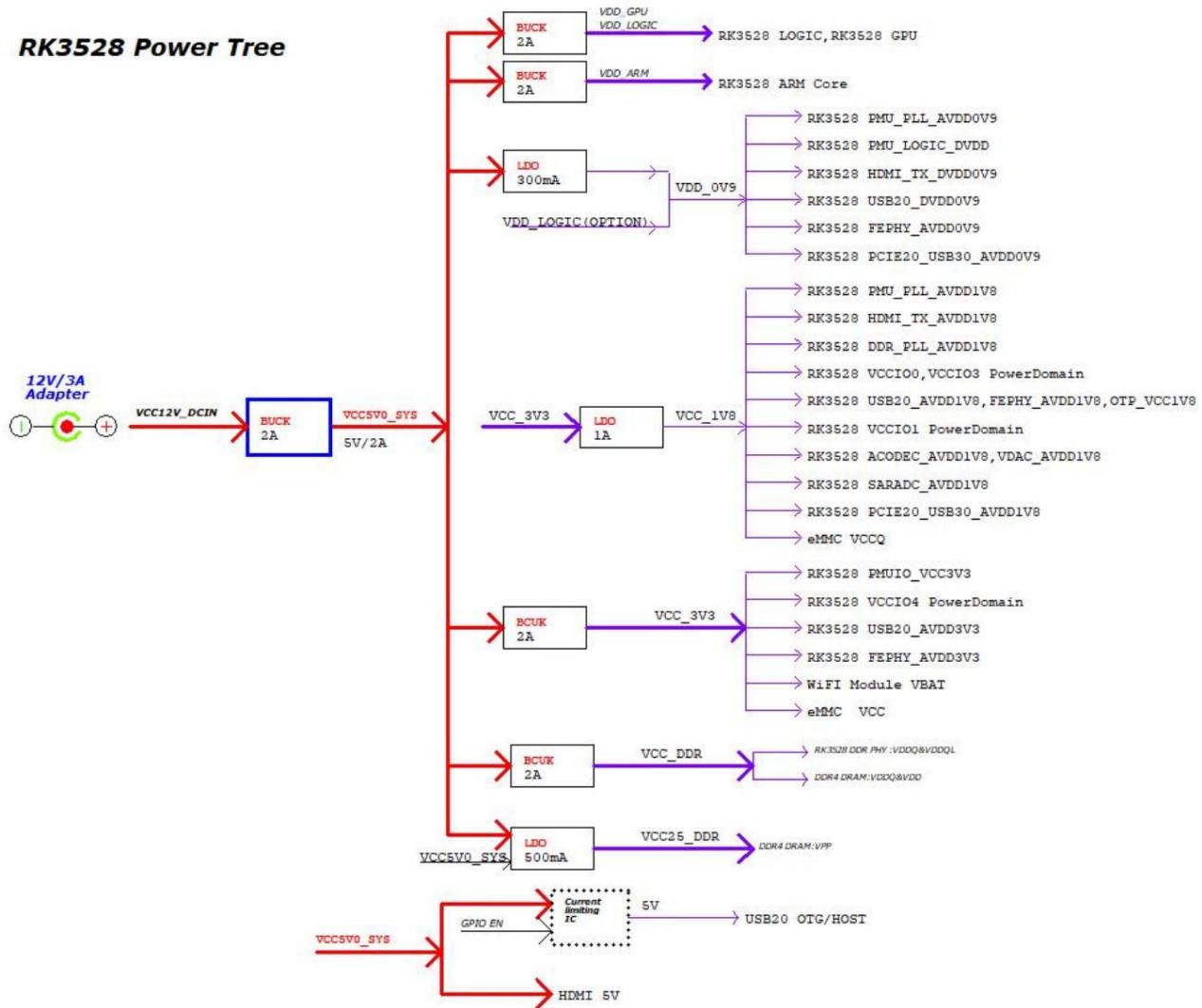


Figure 2-41 RK3528 discrete power supply architecture

2.2.3.2 Discrete Power Supply Power-On Sequence

RK3528 uses a discrete power supply. The DCIN_12V input is converted to 5.2V through DC/DC, and then passes through the DC/DC and LDO output systems.

The various voltages required by the system, all power supplies are powered by default when they are turned on.

Power Supply	EXT BUCK&LDO	Supply Limit	Power Name	Time Slot	Default Voltage	Default ON/OFF	Sleep ON/OFF	Peak Current	Sleep Current
VCC5V0_SYS	BUCK1	2.0A	VDD_LOGIC VDD_GPU	Slot:1	0.9V	ON	ON	TBD	TBD
VCC5V0_SYS	BUCK2	2.0A	VDD_ARM	Slot:1	0.95V	ON	ON	TBD	TBD
VCC5V0_SYS	LDO1	0.3A	VDD_0V9	Slot:1	0.9V	ON	ON	TBD	TBD
VCC_3V3	LDO2	1.0A	VCC_1V8	Slot:2	1.8V	ON	ON	TBD	TBD
VCC5V0_SYS	BUCK3	2.0A	VCC_3V3	Slot:2	3.3V	ON	ON	TBD	TBD
VCC5V0_SYS	BUCK4	2.0A	VCC_DDR	Slot:2	ADJ $FB=0.6V$	ON	ON	TBD	TBD
VCC12V_DCIN	BUCK5	3.0A	VCC5V0_SYS	Slot:0	5.2V	ON	ON	TBD	TBD

Figure 2-42 RK3528 discrete power supply power-on timing chart

Power Sequence

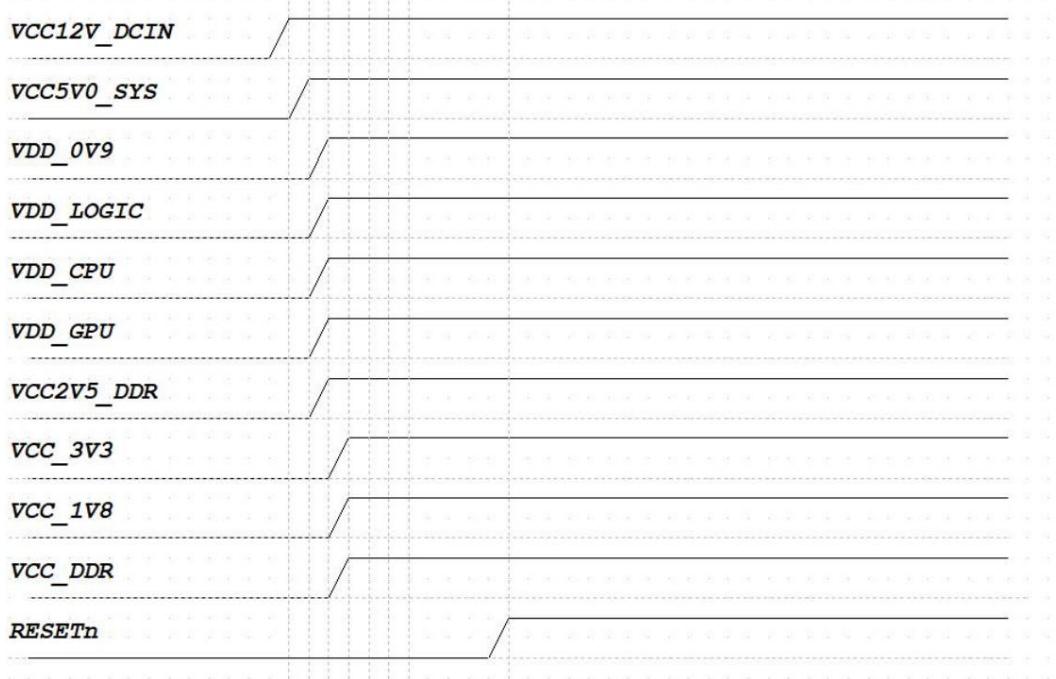


Figure 2-43 RK3528 discrete power supply power-on timing diagram

2.2.3.3 Core module peak current meter

The following data is the peak current of each core module, for evaluation of power supply solutions and PCB layout, for reference only.

Note: You cannot simply add up all the peak currents to calculate the SOC. To evaluate the cooling solution, please calculate the average working current based on the actual scenario.

Current conduction.

Table 2-11 RK3528 Peak Current Meter

RK3528 core module current limit

Environment: Chip TSADC temperature 100°C;

Heat dissipation: bare board, no heat sink;

Test method: After the development board is stable, run and record for 15 minutes;

Operational scenarios: The test results of different modules under their respective extreme scenarios are for reference only;

Note: The following data is the test data on the internal R&D board, which is for design reference only and does not represent the final capability of the chip.

It is highly relevant to international application scenarios. If you need in-depth optimization, you can discuss it with technical support personnel.

	Power network	Voltage (V)	Peak current mA	Peak power (mW)
Core Module	VDD_CPU	1.025	1.40	1.44
	VDD_LOGIC	0.9	1.00	0.90
	VDD_GPU	0.855	1.00	0.86
	VCC_DDR	1.2	0.90	1.09

illustrate:

1. Table data DDR particle type DDR4, VCC_DDR includes DDR_VDDQ and DDR_VDDQL.
2. Test the peak current of VDD_LOGIC and VDD_GPU independent power supplies.

2.3 Functional Interface Design Guidelines

2.3.1 SDMMC/SDIO

RK3528 integrates one SDMMC controller and two SDIO controllers, both of which support SDIO3.0 protocol and MMC V4.51

SDIO0 and SDIO1 can support up to 200MHz, while SDMMC only supports up to 150MHz.

2.3.1.1 SDMMC Interface

The SDMMC interface is multiplexed in the VCCIO2 power domain;

Support System Boot, with SD card function assigned by default;

SDMMC and JTAG functions are multiplexed together. By default, the function is selected through the SDMMC_DET state. For details, please refer to

Section 2.1.5 Description;

VCCIO2 power supply, requires external 3.3V or 1.8V power supply;

When connecting an SD card: If only SD2.0 mode is supported: 3.3V power can be directly supplied; if SD2.0 mode is supported, SD3.0 is compatible.

Mode: The default power supply is 3.3V. After negotiating with the SD card to run SD3.0 mode, the power supply voltage needs to be switched to 1.8V.

This is achieved by adjusting the FB voltage divider resistor parameters of the DC/DC.

When connected to an SDIO device: supply 1.8V or 3.3V according to the peripheral device and the actual operating mode;

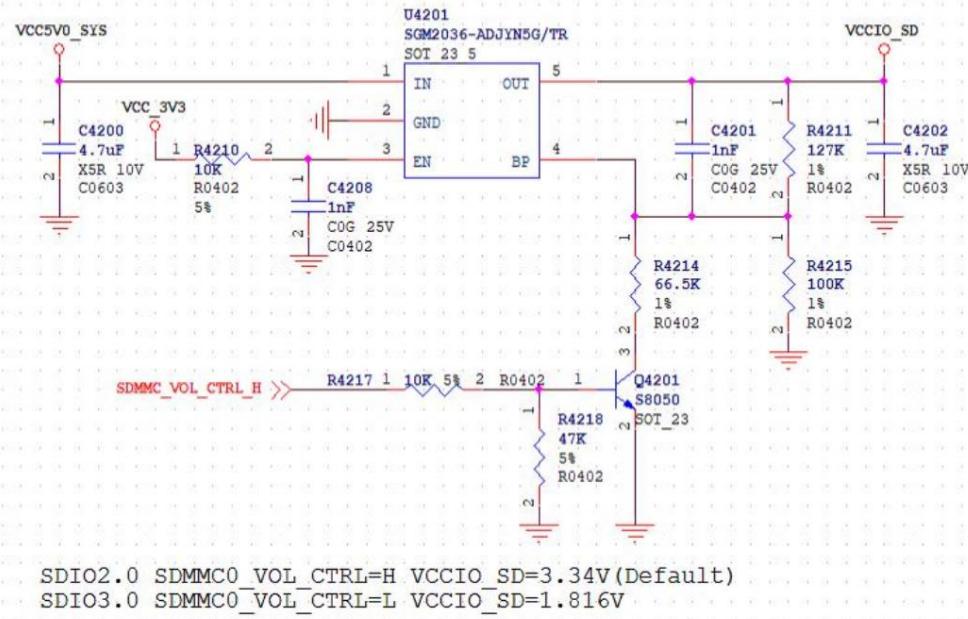


Figure 2-44 RK3528 SD card 1.8V/3.3V power switching FB parameters

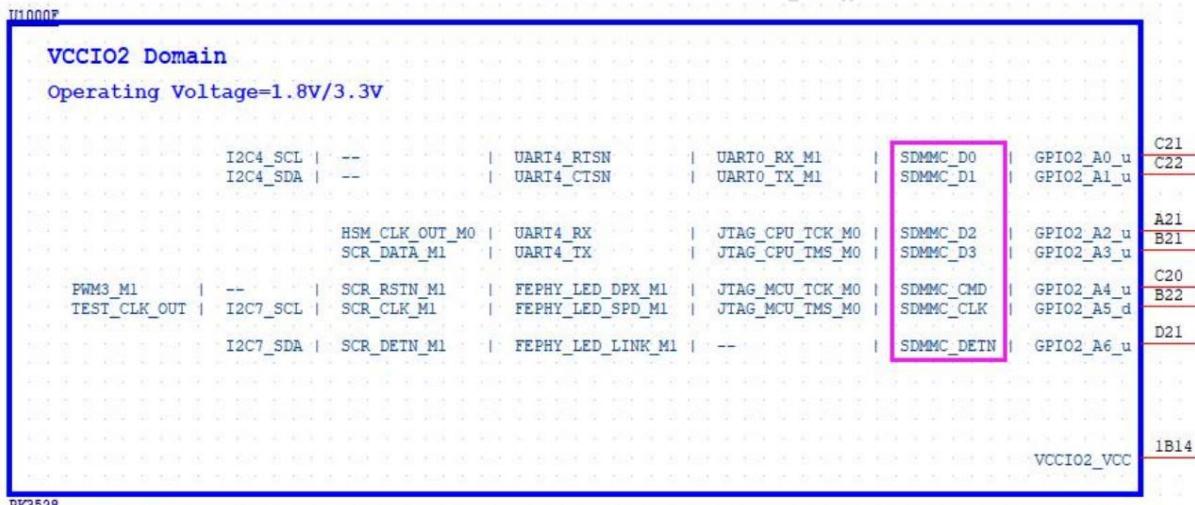


Figure 2-45 RK3528 SDMMC interface pins

When using a connector to connect a board to a board, it is recommended to connect a resistor with a certain resistance (between 22ohm and 100ohm, depending on the specific resistance).

When connected to an SD card, please pay

attention to the following issues:

1) The VDD pin of the SD card is 3.3V, so the decoupling capacitor must not be removed and should be placed close to the card holder during layout.

2) SDMMC_D[3:0], SDMMC_CMD, and SDMMC_CLK must be connected in series with a 22ohm resistor, and SDMMC_DET must be connected in series with a 22ohm resistor.

100 ohm resistor;

3) ESD devices need to be placed at the SD card position for SDMMC_D[3:0], SDMMC_CMD, SDMMC_CLK, and SDMMC_DET signals. SD3.0

mode must be supported, and the junction capacitance of the ESD device must be less than 1pF. If only SD2.0 mode is required, the

junction capacitance of the ESD device can be relaxed to 9pF.

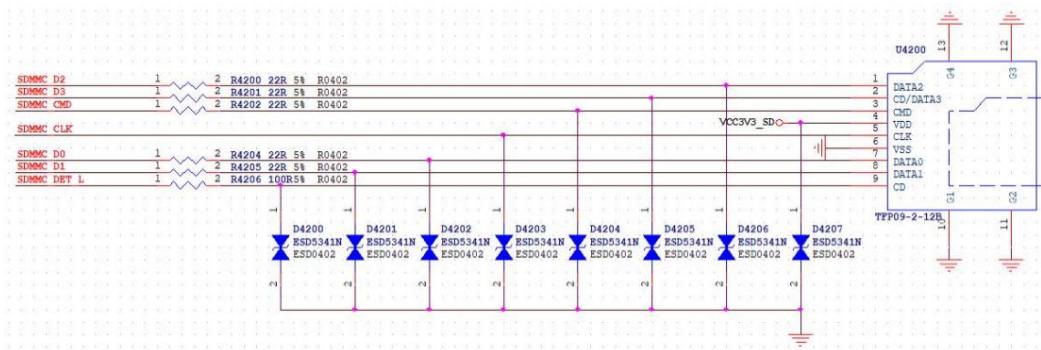


Figure 2-46 SD Card interface circuit

4) The pull-up and matching design recommendations for the SDMMC interface are shown in the table below:

Table 2-12 SDMMC0 interface design

Signal	Internal pull-up and pull-down	Connection method	Description (chip side)
SDMMC0_D[3:0]	Pull-up	Connect a 22ohm resistor in series Use the corresponding IO internal pull-up resistor	SD data sending/receiving
SDMMC0_CLK	drop down	Connect a 22ohm resistor in series	SD clock transmission
SDMMC0_CMD	Pull-up	Connect a 22ohm resistor in series Use the corresponding IO internal pull-up resistor	SD command send/receive
SDMMC0_DET	Pull-up	Connect a 100ohm resistor in series Use the corresponding IO internal pull-up resistor	SD card insertion detection

2.3.1.2 SDIO interface

ŷ The SDIO interface has two SDIO0 and SDIO1, which are in the VCCIO0 power domain and the VCCIO3 power domain respectively.

The design of the scale is 20 signals, including UART, I2S, GPIO related control signals, to meet the needs of SDIO WIFI peripherals

All signals.

ŷ System Boot is not supported;

ŷ VCCIO0 and VCCIO3 power supply is 1.8V or 3.3V. Select the corresponding voltage according to the peripherals.

The IO remains consistent.

U1000D

VCCIO0 Domain**Operating Voltage=1.8V/3.3V**

I2C3_SCL_M0	SCR_DETN_M0	PCIE_CLKREQN_M1	SDIO0_D0	GPIO1_A0_d	AB2
I2C3_SDA_M0	SCR_DATA_M0	PCIE_WAKEN_M1	SDIO0_D1	GPIO1_A1_d	Y3
PWM0_M1	UART5_RX_M0	SCR_CLK_M0	PCIE_PERSTN_M1	SDIO0_D2	GPIO1_A2_d
PWM1_M1	UART5_TX_M0	SCR_RSTN_M0	--	SDIO0_D3	GPIO1_A3_d
PWM4_M1	--	HSM_CLK_OUT_M1	--	SDIO0_CMD	GPIO1_A4_d
UART5_RTSN_M0	I2C2_SCL_M1	--	SDIO0_CLK	GPIO1_A5_d	AB3
UART5_CTSN_M0	I2C2_SDA_M1	--	SDIO0_DETN	GPIO1_A6_d	AA3
PWM2_M1	--	--	--	SDIO0_PWRREN	GPIO1_A7_d
UART7_CTSN_M1	--	--	UART2_RX_M1	GPIO1_B0_d	AA2
UART7_RTSN_M1	--	--	UART2_TX_M1	GPIO1_B1_d	1R7
UART7_TX_M1	I2C5_SCL_M0	--	UART2_RTSN_M1	GPIO1_B2_d	1P7
UART7_RX_M1	I2C5_SDA_M0	--	UART2_CTSN_M1	GPIO1_B3_d	1R6
PWM7_M1	--	--	I2S0_MCLK_M1	GPIO1_B4_d	1P4
PWM6_M1	--	SPDIF_TX_M1	I2S0_SCLK_M1	GPIO1_B5_d	1P6
			SPI1_CLK	I2S0_LRCK_M1	GPIO1_B6_d
			SPI1_MOSI	I2S0_SD1_M1	GPIO1_B7_d
			SPI1_MISO	I2S0_SDO_M1	GPIO1_C0_d
			SPI1_CSNO	--	GPIO1_C1_u
			SPI1_CSNI	--	GPIO1_C2_d
			CLK_32K_OUT_M1	GPIO1_C3_d	Y5
					1N6
					VCCIO0_VCC

RK3528

BGA401_13R50X13R30X1R25

Figure 2-47 RK3528 SDIO0 interface function pins

U1000G

VCCIO3 Domain**Operating Voltage=1.8V/3.3V**

TS10_D7	UART2_RX_M0	RGMII1_TXD1	GPIO3_A0_d	AA19
TS10_D6	UART2_TX_M0	RGMII1_RXD0	GPIO3_A1_d	Y18
TS10_D5	UART2_RTSN_M0	RGMII1_RXD1	GPIO3_A2_d	Y17
TS10_D4	UART2_CTSN_M0	RGMII1_RXD0	GPIO3_A3_d	AA18
UART6_CTSN	--	SDIO1_CLK	RGMII1_TXCLK	GPIO3_A4_d
UART6_RTSN	--	SDIO1_CMD	RGMII1_RXCLK	GPIO3_A5_d
PCIE_CLKREQN_M0	--	TS11_VALID	SDIO1_D0	GPIO3_A6_d
PCIE_WAKEN_M0	--	TS11_SYNC	SDIO1_D1	GPIO3_A7_d
PCIE_PERSTN_M0	--	UART7_CTSN_M0	SDIO1_D2	GPIO3_B0_d
		UART7_RTSN_M0	SDIO1_D3	GPIO3_B1_d
UART7_TX_M0	I2C6_SCL_M0	TS10_CLKIN	SDIO1_PWRREN	GPIO3_B2_d
UART7_RX_M0	I2C6_SDA_M0	TS10_VALID	SDIO1_DETN	GPIO3_B3_d
TS10_SYNC	I2S0_MCLK_M0	--	--	GPIO3_B4_d
TS10_D1	I2S0_SCLK_M0	ETH_CLK_25M_OUT	GPIO3_B5_d	AB17
TS10_D2	I2S0_LRCK_M0	RGMII1_MDC	GPIO3_B6_d	AA17
TS10_D3	I2S0_SD1_M0	RGMII1_MDIO	GPIO3_B7_d	AA16
TS10_FAIL	I2S0_SDO_M0	RGMII1_TXEN	GPIO3_C0_d	AB16
PWM6_M2	--	UART6_TX_M1	I2C3_SCL_M1	GPIO3_C1_d
PWM5_M1	SPDIF_TX_M2	UART6_RX_M1	I2C3_SDA_M1	REF_CLK_OUT_M1
			CLK_32K_OUT_M0	RGMII1_RXDV_CRS
				GPIO3_C2_d
				GPIO3_C3_d
				IM13
				VCCIO3_VCC

RK3528
BGA401_13R50X13R30X1R25

Figure 2-48 RK3528 SDIO1 interface function pins

ÿ The pull-up and matching design recommendations for the SDIO interface are shown in the table:

Table 2-13 SDIO interface design

Signal	Internal pull-up and pull-down	Connection method	Description (chip side)
SDIO0/1_D[3:0] pull-down		Connect a 22ohm resistor in series, which can be deleted if the trace is short. Use the corresponding IO internal pull-up resistor	SD data sending/receiving
SDIO0/1_CLK pull-down		Connect a 22ohm resistor in series	SD clock transmission
SDIO0/1_CMD pull-down		Connect a 22ohm resistor in series, which can be deleted if the trace is short. Use the corresponding IO internal pull-up resistor	SD command send/receive

When using a connector to connect a board to a board, it is recommended to connect a resistor with a certain resistance (between 22ohm and 100ohm, depending on the specific resistance).

Test is subject to the requirements) and TVS devices should be reserved.

2.3.1.3 Notes when connecting SDIO to WIFI

- ÿ Please ensure that the IO level of the module is consistent with the IO level of the CPU, otherwise level matching is required;
- ÿ Please select the crystal load capacitance according to the CL capacitance value of the actual crystal used, and control the frequency tolerance at room temperature within 10ppm;
- ÿ The antenna reserves a γ -type circuit for antenna matching adjustment;
- ÿ Confirm the connection direction of PCM and UART interface, such as IN and OUT, TXD and RXD;
- ÿ If you need to use a module with a 32.768k clock input, you need to pay attention to the clock amplitude.
- ÿ WIFI is compatible with multiple modes. When mounting the chip, you must select the module according to the actual module and do not mount it randomly.

2.3.2 SARADC Circuit

RK3528 integrates a SARADC controller with a resolution of 10 bits, a speed of 1MS/s, and an input voltage range of 0-1.8V.

Can provide 4 SARADC inputs.

SARADC_IN0 is dedicated to the setting of SYSTEM BOOT startup sequence and cannot be used for other functions.

The value obtained in this way is used to determine which interface to boot from. The settings are as follows: (Rup/Rdown represent pull-up and pull-down resistors)

TABLE

Item	Rup	Rdown	ADC	BOOT MODE
LEVEL1	DNP	100K	0	USB (Maskrom mode)
LEVEL2	100K	12K	114	
LEVEL3	100K	27K	228	FSPI--USB
LEVEL4	100K	51K	342	
LEVEL5	100K	82K	456	
LEVEL6	100K	120K	570	EMMC--USB
LEVEL7	100K	200K	683	EMMC--SD Card--USB
LEVEL8	100K	330K	796	SD Card--USB
LEVEL9	100K	820K	910	
LEVEL10	100K	DNP	1023	FSPI--EMMC--SD Card--USB

If Rup=DNP, Rdown=100K; RK3528 device is connected to the USB cable, then powered on, the system can directly enter Maskrom.

SARADC_IN1 is used as the key input sample and multiplexed as the Recovery mode key (cannot be modified).

SARADC_IN1 is pulled up to VCC_1V8 through a 10Kohm pull-up resistor. The default is high level (1.8V).

If the system has already been burned with firmware, power on and enter the system directly. If the Recovery mode button is pressed during system startup, that is, SARADC_IN1 is kept at a low level (0V), the RK3528 enters the Loader burn mode. When the PC recognizes the USB device, release the button to restore SARADC_IN1 to a high level (1.8V), and then the firmware burn can be performed. Therefore, if the product does not have a button, SARADC_IN1 will be in an unstable state when it is left floating, which may affect the startup. Therefore, the 10Kohm pull-up resistor of SARADC_IN1 must be retained and cannot be deleted to ensure the default normal startup judgment. For the convenience of development, it is recommended to reserve a button or test point for SARADC_IN1.

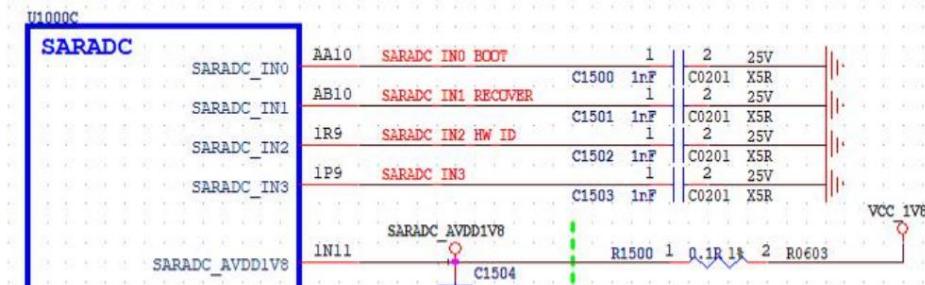


Figure 2-49 SARADC INx Interface

RK3528 SARADC design points:

- ÿ The decoupling capacitor of SARADC_AVDD1V8 power supply must not be deleted. When laying out, it must be placed close to the RK3528 pin.
- ÿ If SARADC_IN[3:0] is used, a 1nF capacitor must be added near the pin to eliminate jitter. ÿ When used for key acquisition, ESD protection must be done near the key, and the 0 key value must be connected in series with a 100ohm resistor to enhance anti-static surge protection. capability (if there is only one key, the ESD must be close to the key, first passing through the ESD \rightarrow 100ohm resistor \rightarrow 1nF \rightarrow chip pin).

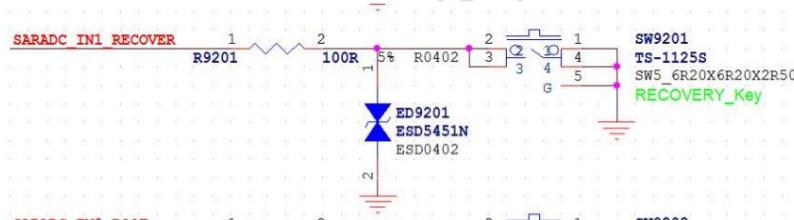


Figure 2-50 RK3528 SARADC single-button circuit

2.3.3 OTP Circuit

RK3528 has 8Kbit internal space and high 1Kbit address non-safe space for programming. Supports programming, reading and idle modes.

In these modes, the OTP_VCC1V8 pin must be powered.

The decoupling capacitor of the OTP_VCC1V8 power supply must not be deleted and should be placed close to the RK3528 pin during layout.

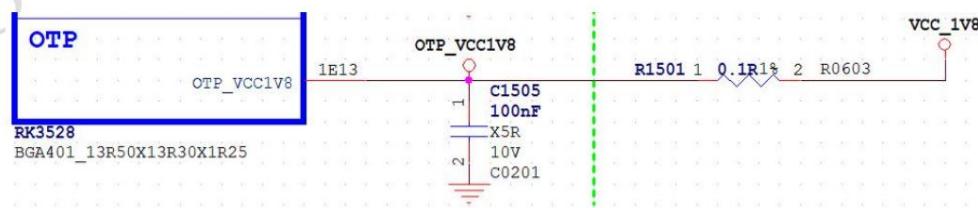


Figure 2-51 RK3528 OTP power pin

2.3.4 PCIE2.0/USB Circuit

The RK3528 chip has a built-in USB3.0 OTG0 controller, a USB2.0 HOST1 controller, and a PCIE2.0 controller.

There are 2 USB2.0 PHYs and one PCIE2.0/USB3 Combo PHY.

The internal multiplexing relationship between these

controllers and PHY is as follows: ȳ The USB2.0 HOST1 controller and USB2.0 PHY are combined, and the external interface is USB2.0 HOST1. ȳ The USB3.0 OTG0 controller can be combined with USB2.0 PHY, and the external interface is USB2.0 OTG0. ȳ The USB3.0 OTG0 controller can be combined with PCIE2.0/USB3 Combo PHY and USB2.0 PHY, and the external interface is USB3.0 OTG0.

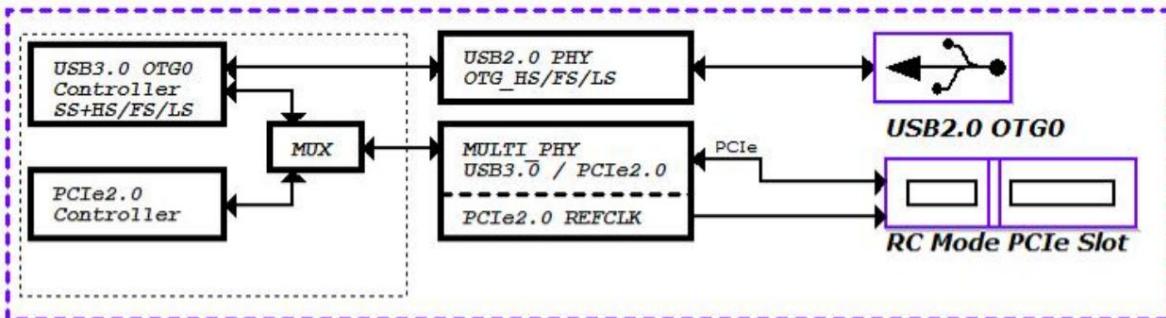
ȳ PCIE2.0 controller and PCIE2.0/USB3 Combo PHY combination, the external interface is RC Mode PCIe Slot.

In summary: There are 2 ways of combination:

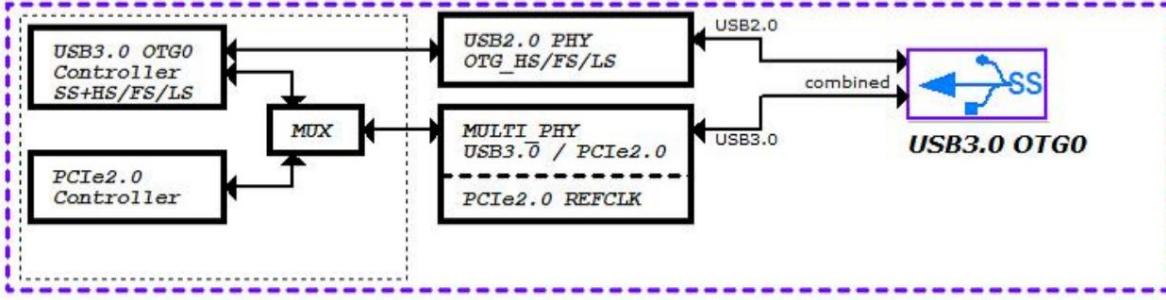
ȳ 1 x USB2.0 HOST1 + 1 x USB2.0 OTG0 + PCIE2.0

ȳ 1 x USB2.0 HOST1 + 1 x USB3.0 OTG0

Case1: USB2.0 OTG0 + PCIE2.0 x1 Lane



Case2: USB3.0 OTG0



USB2.0 HOST1

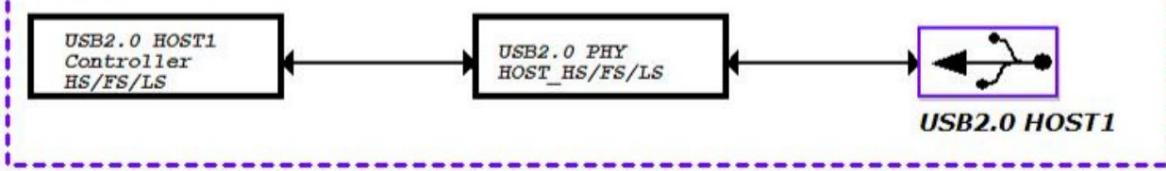


Figure 2-52 Internal multiplexing relationship between PCIE/USB PHY and PCIE/USB Controller

The USB2.0 OTG0 controller supports HS/FS/LS. The signal names are shown in the red box in the figure below. Currently, only this interface of RK3528 supports Fireware Download. Please be sure to reserve this interface in your application.

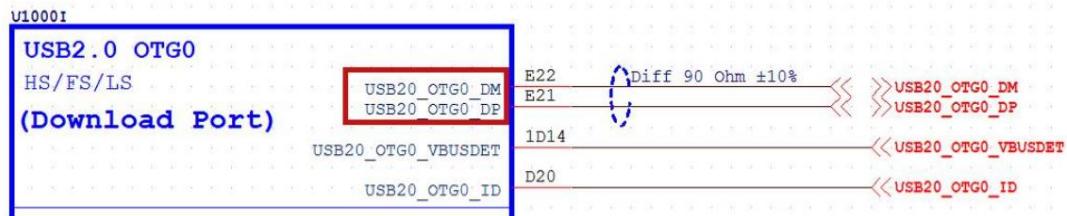


Figure 2-53 USB2.0 OTG0 pins



Notice

only `USB2.0_OTG_DM/USB2.0_OTG_DP`support *Download Firmware*

If the product does not use this interface, it must be used during debugging and production.

Reserve this interface. Note: `USB20_OTG0_VBUSDET`

Must be connected too!

The USB2.0 HOST1 controller uses the USB2.0 HOST1 PHY. The signals in the box below constitute the USB2.0 HOST1 interface.

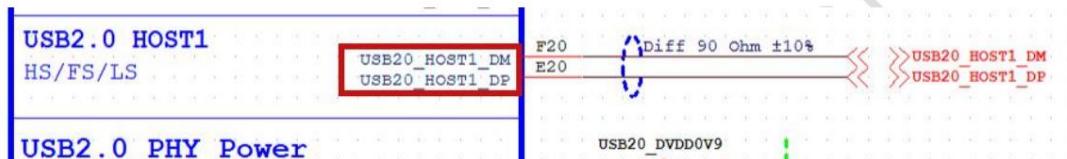


Figure 2-54 USB2.0 HOST1 pins

USB3.0 OTG0 controller, using PCIE2.0/USB3 Combo PHY and USB2.0 PHY, the signals in the box below constitute USB3.0 OTG0 interface.

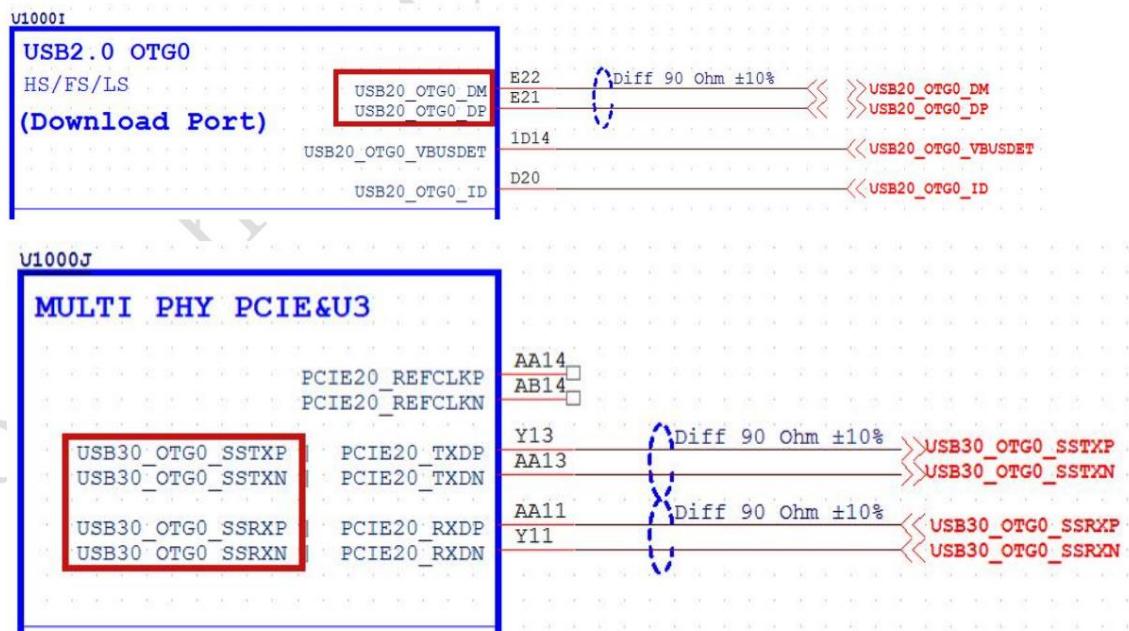


Figure 2-55 USB30 OTG0 pins

The combination of PCIE2.0 controller and PCIE2.0/USB3 Combo PHY, the signals in the box below constitute the RC Mode PCIe Slot.

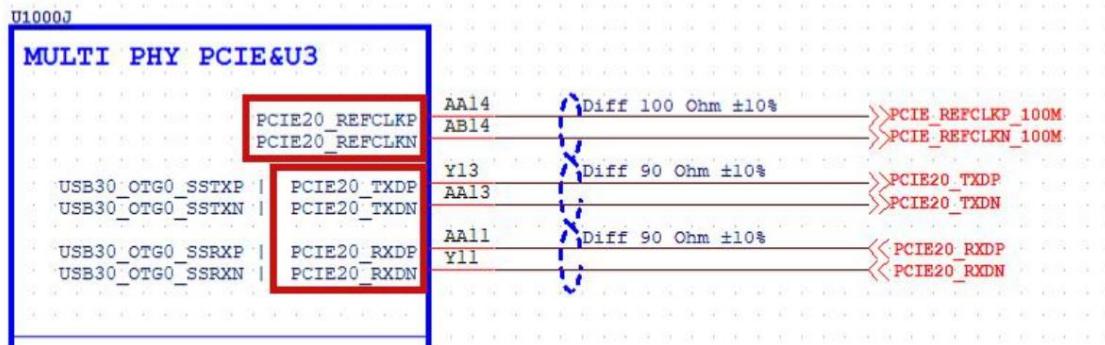


Figure 2-56 PCIe 2.0 pins

Please note the following when designing USB2.0/USB3.0:

- ÿ USB2.0_OTG_DM/USB2.0_OTG0_DP is the system firmware burning port. If the product does not use this interface, this interface must be reserved during the debugging and production process, otherwise debugging and production firmware burning will not be possible;
- ÿ USB20_OTG0_ID has a 200Kohm resistor inside that pulls it up to USB20_AVDD1V8; ÿ USB20_OTG0_VBUSDET is the OTG and Device mode detection pin, high for DEVICE device, 2.7-3.3V, TYP: 3.0V, it is recommended to place a 100nF capacitor on the pin.

The OTG mode can be set to the following three modes:

ÿ OTG mode: automatically switches to device mode or HOST mode according to the ID pin status, ID high is device, ID low is HOST,

When in device mode, it will also check whether the VBUSDET pin is high (greater than 2.3V). If it is high, it will pull up DP and start enumeration;

ÿ Device mode: When set to this mode, no ID pin is needed. You only need to check whether the VBUSDET pin is high (greater than 2.3V).

If it is high, DP will be pulled high to start enumeration;

ÿ HOST mode: When set to this mode, you do not need to care about the ID and VBUSDET status. (If the product only needs HOST

Mode, but since only USB2.0_OTG_DM/USB2.0_OTG0_DP is the system firmware burning port, this port is needed in both debugging and production processes.

When burning and adb debugging, it needs to be set to device mode, so the USB20_OTG0_VBUSDET signal must also be connected).

Before uboot starts, the default mode is device mode. After entering uboot, you can configure these three modes according to actual needs.

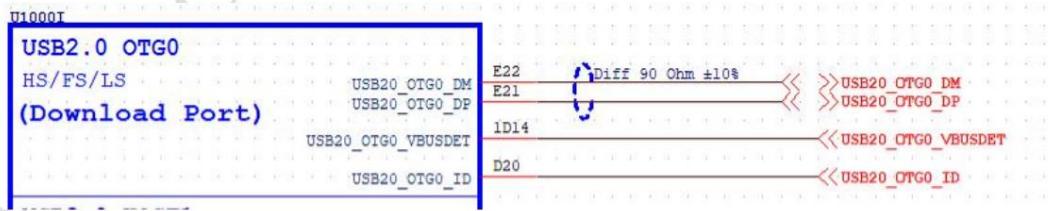


Figure 2-57 RK3528 USB20_OTG0 circuit

If using Micro USB2.0 interface, you need to use 5V on the USB connector to identify whether there are other devices connected or connected to other devices.

The device needs to adopt the following circuit:

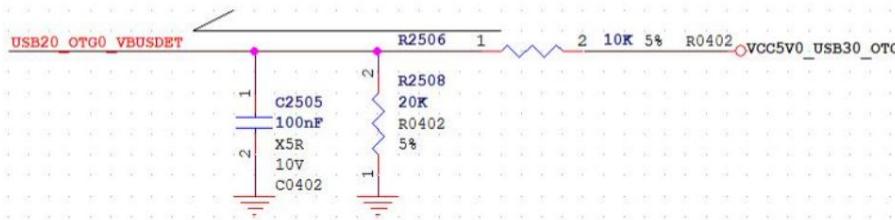


Figure 2-58 USB20_OTG0_VBUSDET detection circuit

- ÿ To improve USB performance, the decoupling capacitors for each PHY power supply must not be removed and should be placed close to the pins during layout.
- ÿ To enhance anti-static and surge capabilities, ESD devices must be reserved for the signals. The ESD parasitic capacitance of USB2.0 signals must not exceed 3pF. In addition, a 2.2ohm resistor must be connected in series with the DP/DM of the USB2.0 signal to enhance anti-static surge capabilities. This resistor must not be removed. See the figure below, which shows USB2.0_OTG_DM/DP as an example. Other USB2.0 interfaces require the same treatment.

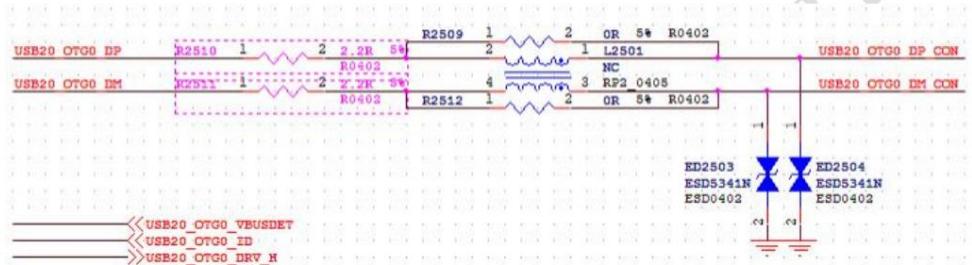


Figure 2-59 USB2.0 signal connected in series with a 2.2ohm resistor circuit

- ÿ To suppress electromagnetic radiation, you can consider reserving common mode choke on the signal line.

Choose to use resistors or common-mode inductors based on actual conditions. See the figure below, taking USB2.0_OTG_DM/DP as an example. Other USB2.0 interfaces require the same treatment.

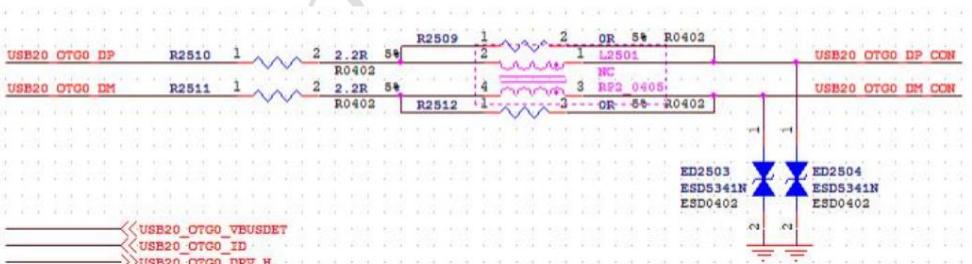


Figure 2-60 USB2.0 signal string common mode inductor circuit

If the USB20_OTG0_ID signal is used, ESD devices must be reserved for the signal to enhance the anti-static and surge capabilities, and the 100ohm resistor, do not delete, see the figure below:

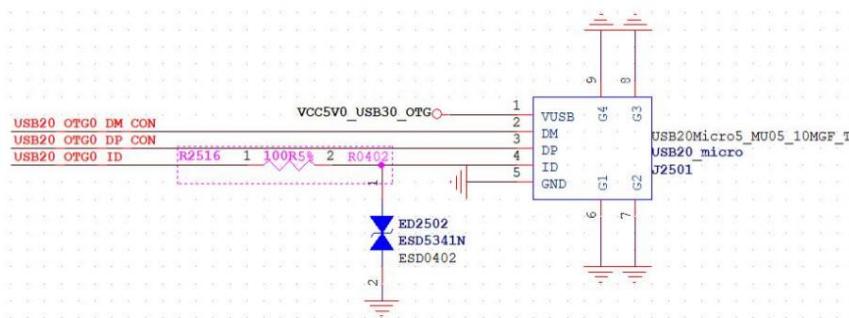


Figure 2-61 USB20_OTG0_ID pin circuit

When the HOST function is used, it is recommended to add a current limiting switch to the 5V power supply. The current limiting size can be adjusted according to application needs. The current limiting switch is controlled by 3.3V GPIO. It is recommended to add 22uF and 100nF or more capacitor filtering to the 5V power supply; if the USB port may be connected to a mobile hard disk, it is recommended to increase the filtering capacitor to more than 100uF.

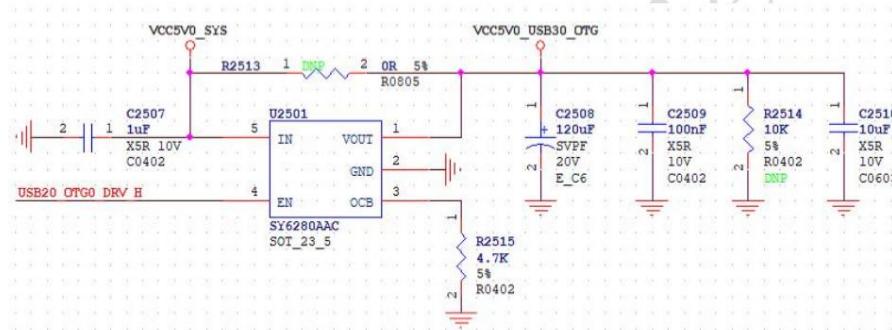


Figure 2-62 USB 5V current limiting circuit

The USB3.0 protocol requires adding a 100nF AC coupling capacitor on the SSTXP/N line. The AC coupling capacitor is recommended to use a 0201 package, which is lower. The ESR and ESL can also reduce the impedance variation on the line.

All signals of the USB socket must be equipped with ESD devices and placed close to the USB connector during layout.

Signal, ESD parasitic capacitance shall not exceed 0.3pF.

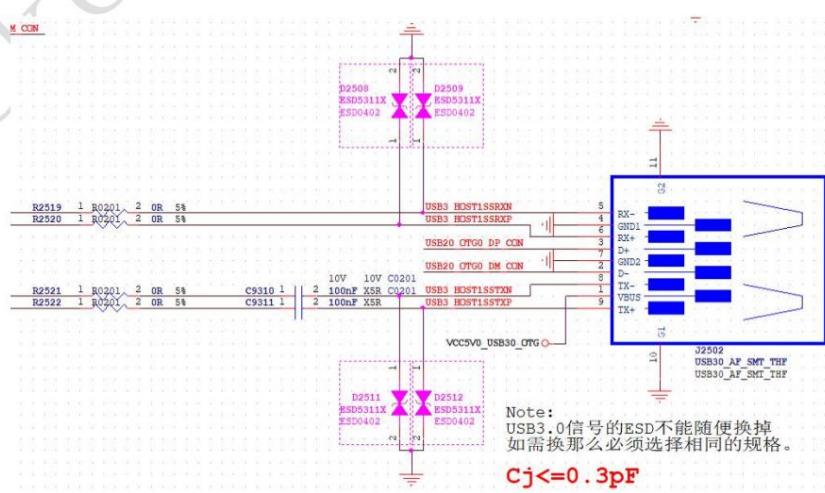


Figure 2-63 USB socket ESD circuit

The recommended USB2.0/USB3.0 interface matching design is shown in the following table:

Table 2-14 RK3528 USB2.0/USB3.0 interface design

Signal	Connection method	illustrate
USB20_OTG0_DP/DM	Connect a 2.2ohm resistor in series	USB HS/FS/LS mode data input/output
USB30_OTG0_SSTXN/SSTXP connected in series with a 100nF capacitor (0201 package recommended)		USB SS mode data output
Connect a 0ohm resistor in series with USB30_OTG0_SSRXN/SSRXP		USB SS mode data input
USB20_OTG0_ID	Connect a 100ohm resistor in series (pull-up is required externally, and the pull-up power supply needs to be To be connected to the same power supply as USB20_AVDD_1V8)	USB OTG ID identification, required for Micro-USB interface To use
USB20_OTG0_VBUSDET	Resistor voltage divider detection	USB OTG insertion detection
USB20_HOST1_DP/DM	Connect a 2.2ohm resistor in series	USB HS/FS/LS mode data input/output

2.3.5 Video input interface circuit

2.3.5.1 TSI interface

RK3528 supports two groups of TSI inputs. The TSI interfaces are distributed on the VCCIO3 power domain. In actual product design, it is necessary to

The IO level must be consistent with it, otherwise it will cause communication abnormality or malfunction.

The signal in the box below is the TSI input signal:

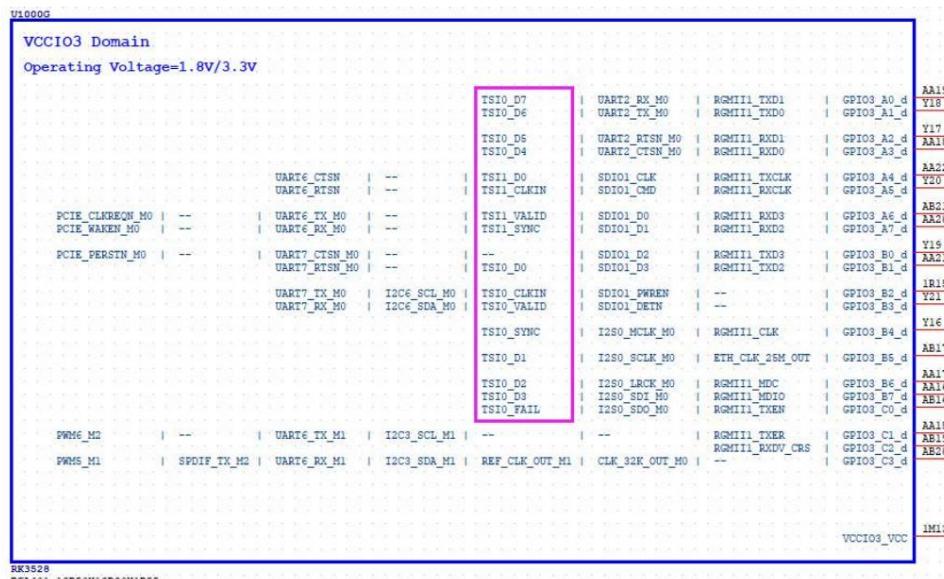


Figure 2-64 RK3528 TSI function pins

The TSI interface supports 2-channel TSI stream serial input, a maximum of 96 hardware PID filters, and DVB-CSA/AES/DES descrambling algorithms.

One string and one parallel and two strings, two mode signal selections are as follows:

Mode	Parallel+Serial	Serial+Serial
TSIO_D0	TSIO_D0	TSIO_D0
TSIO_D1	TSIO_D1	Leave floating
TSIO_D2	TSIO_D2	Leave floating
TSIO_D3	TSIO_D3	Leave floating
TSIO_D4	TSIO_D4	Leave floating
TSIO_D5	TSIO_D5	Leave floating
TSIO_D6	TSIO_D6	Leave floating
TSIO_D7	TSIO_D7	Leave floating
TSIO_CLKIN	TSIO_CLKIN	TSIO_CLKIN
TSIO_VALID	TSIO_VALID	TSIO_VALID
TSIO_SYNC	TSIO_SYNC	TSIO_SYNC
TSIO_FAIL	TSIO_FAIL or Leave floating	TSIO_FAIL or Leave floating
TSII_D0	TSII_D0	TSII_D0
TSII_CLKIN	TSII_CLKIN	TSII_CLKIN
TSII_VALID	TSII_VALID	TSII_VALID
TSII_SYNC	TSII_SYNC	TSII_SYNC

Figure 2-65 RK3528 TSI two modes

The pull-up and matching design recommendations for the TSI interface are shown in the table:

Table 2-15 RK3528 CIF interface design

Signal	Internal pull-up and pull-down	Connection method	Description (chip side)
TSI0_D[7:0]	drop down	Connect a 22ohm resistor in series, close to the device end	TSI Data Input
TSI0_CLKIN	drop down	Connect a 22ohm resistor in series, close to the device end	TSI clock input
TSI0_VALID	drop down	Connect a 22ohm resistor in series, close to the device end	TSI packet valid flag input
TSI0_SYNC	drop down	Connect a 22ohm resistor in series, close to the device end	TSI packet transmission start mark input
TSI0_FAIL	drop down	Connect a 22ohm resistor in series, close to the chip end	TSI data error flag input
TSI1_D0	drop down	Connect a 22ohm resistor in series, close to the device end	TSI Data Input
TSI1_CLKIN	drop down	Connect a 22ohm resistor in series, close to the device end	TSI clock input
TSI1_SELECT	drop down	Connect a 22ohm resistor in series, close to the device end	TSI packet valid flag input
TSI1_SYNC	drop down	Connect a 22ohm resistor in series, close to the device end	TSI packet transmission start mark input

When using a connector to connect a board to a board, it is recommended to connect a resistor with a certain resistance (between 22ohm and 100ohm, depending on the specific resistance).

and reserve ESD devices.

2.3.6 Video output interface circuit

The VOP controller of the RK3528 chip has 2 Port outputs and supports HDMI/CVBS video interface output.

VOP and video interface output path diagram:

RK3528 VIDEO INTERFACE DIAGRAM

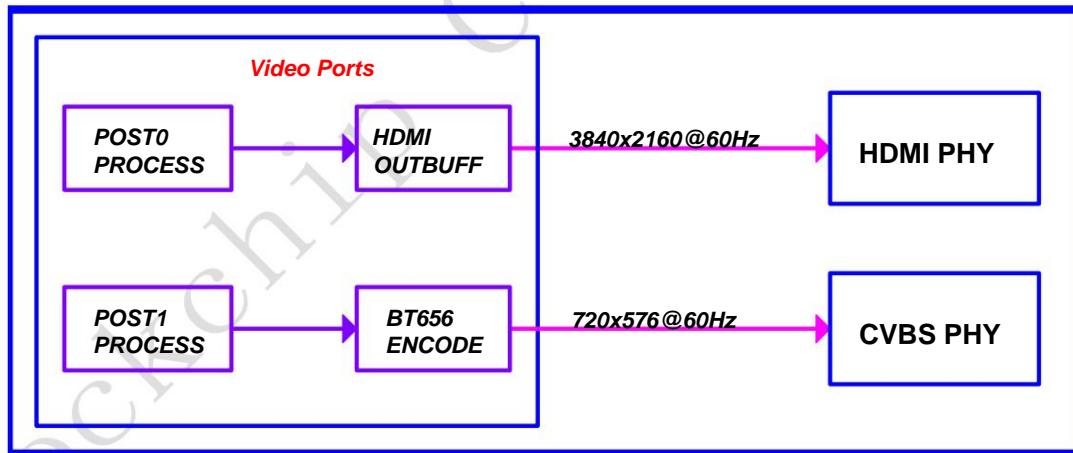


Figure 2-66 RK3528 VOP and video interface output path diagram

2.3.6.1 HDMI interface

RK3528 has 1 HDMI PHY interface, supports HDMI2.0 TX mode: maximum resolution supports 4K@60Hz, supports RGB/YCbCr444/YCbCr420 (Up to 10bit) format.

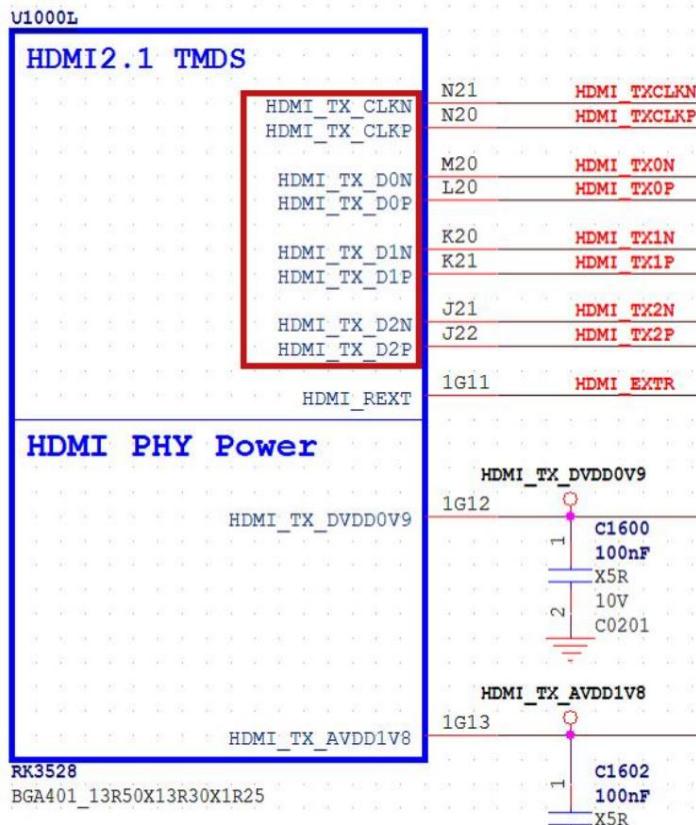


Figure 2-67 RK3528 HDMI PHY pins

HDMI_RXTR is the external reference resistor pin of HDMI PHY. It is connected to a 1kohm resistor with a precision of 1% to ground. The resistor must not be changed. value, and place it close to the RK3528 chip pins during layout.



Figure 2-68 RK3528 HDMI_RXTR pin

HDMI_TX_HPD is multiplexed to the GPIO of the PMUIO power domain, and the level supports 5V voltage.

HDMI_TX_SCL/SDA is multiplexed to the GPIO of the PMUIO power domain, and the level supports 5V voltage.

HDMI_TX_CEC is multiplexed to the GPIO of the PMUIO power domain, with a voltage level of 3.3V.

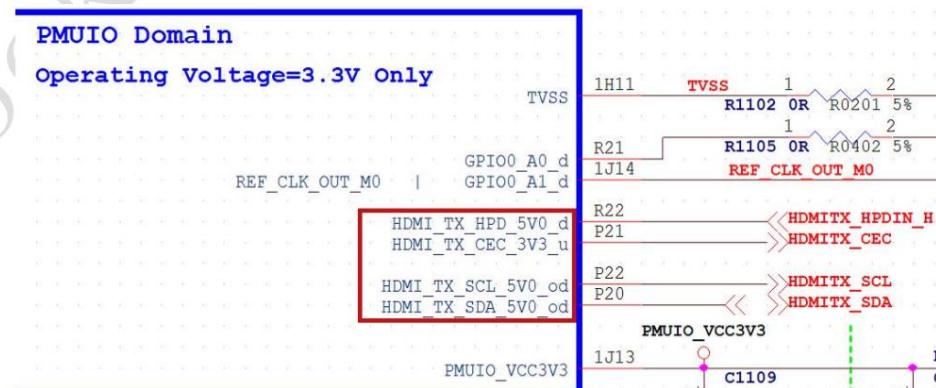


Figure 2-69 RK3528 HDMI_TX_HPD/SCL/SDA/CEC function pins

The HPD signal needs to be connected in series with a 1Kohm resistor at the HDMI connector end to enhance the anti-static surge capability, and a 100Kohm resistor to ground is reserved.

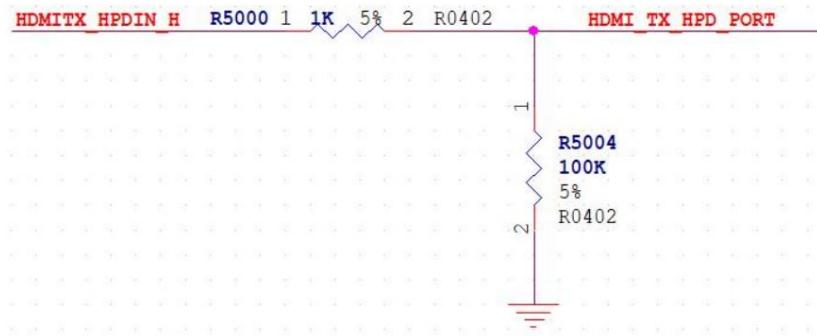


Figure 2-70 RK3528 HDMI_TX_HPD circuit

The CEC protocol specifies a 3.3V level and requires that a 3.3V voltage be applied to the CEC pin through a 27K resistor. Leakage current is not allowed to exceed 1.8uA. RK3528 has a 27K pull-up resistor inside.

Test ID 7-15: CEC Line Degradation

Reference	Requirement
[HDMI: Table 4-40] CEC line Electrical Specifications for all Configurations	A device with power removed (from the CEC circuitry) shall not degrade communication between other CEC devices (e.g. the line shall not be pulled down by the powered off device). Maximum CEC line leakage current must be $\leq 1.8\mu A$

Figure 2-71 HDMI CEC protocol requirements

The D5000 diode must not be removed, as it is used to prevent the Sink terminal from leaking to VCC5V0_SYS.

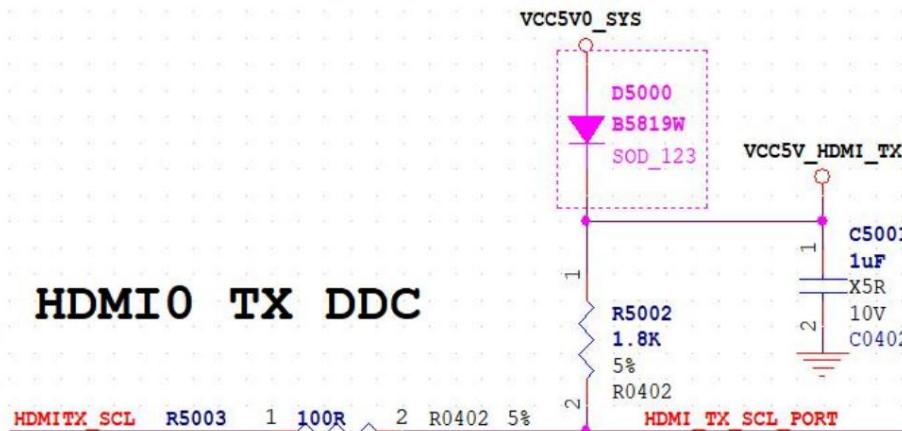


Figure 2-72 HDMI 5V power supply

The voltage of Pin18 of HDMI socket should be kept between 4.8-5.3V, and 1uF decoupling capacitor should be placed on the pin. It should not be deleted.

Placed near the HDMI connector pins.

To enhance the anti-static capability, ESD devices must be reserved for the signal. The ESD parasitic capacitance of the HDMI2.1 TMDS signal must not exceed 0.4pF.

It is recommended that the ESD parasitic capacitance of other signals should not exceed 1pF.

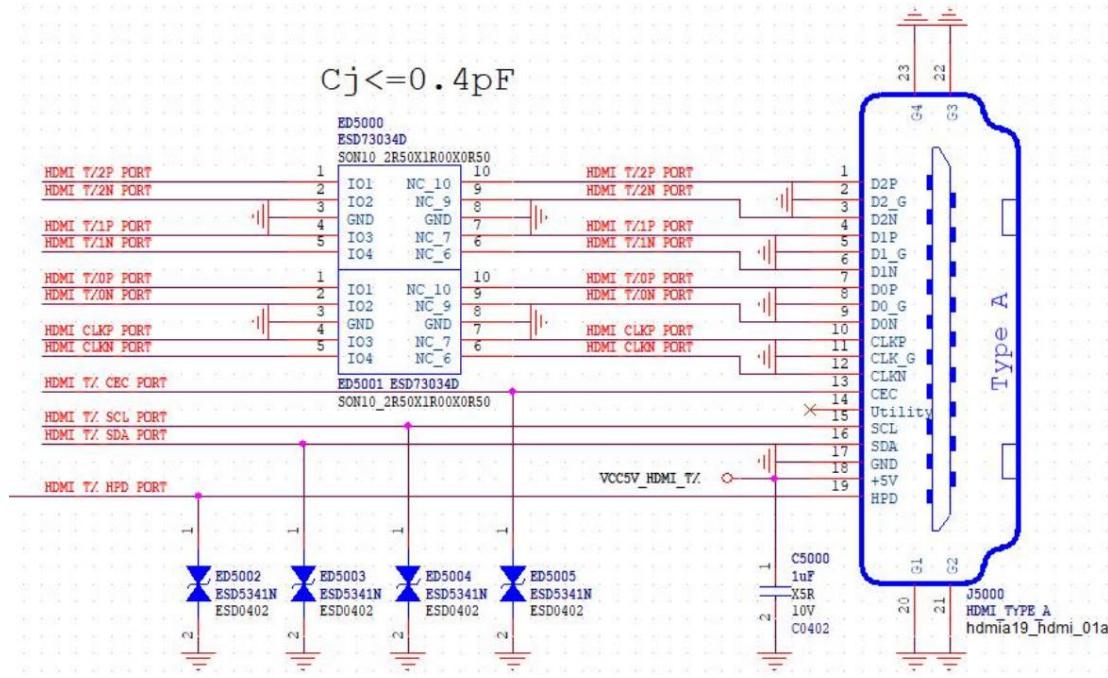


Figure 2-73 HDMI TX connector ESD circuit

The analog part of the RK3528 HDMI interface is designed according to HDMI2.1, and the Data edge is too fast. If you want to test TMDS, you need to

The edge slew rate is required, so this indicator may fail. It has no effect on the function, but if it has passed HDMI certification and EMI testing,

It is recommended to reserve the following circuit: Data P/N connects to ground with a 1pF capacitor and a 4.7R resistor in series. Clk connects to a common-mode inductor in series.

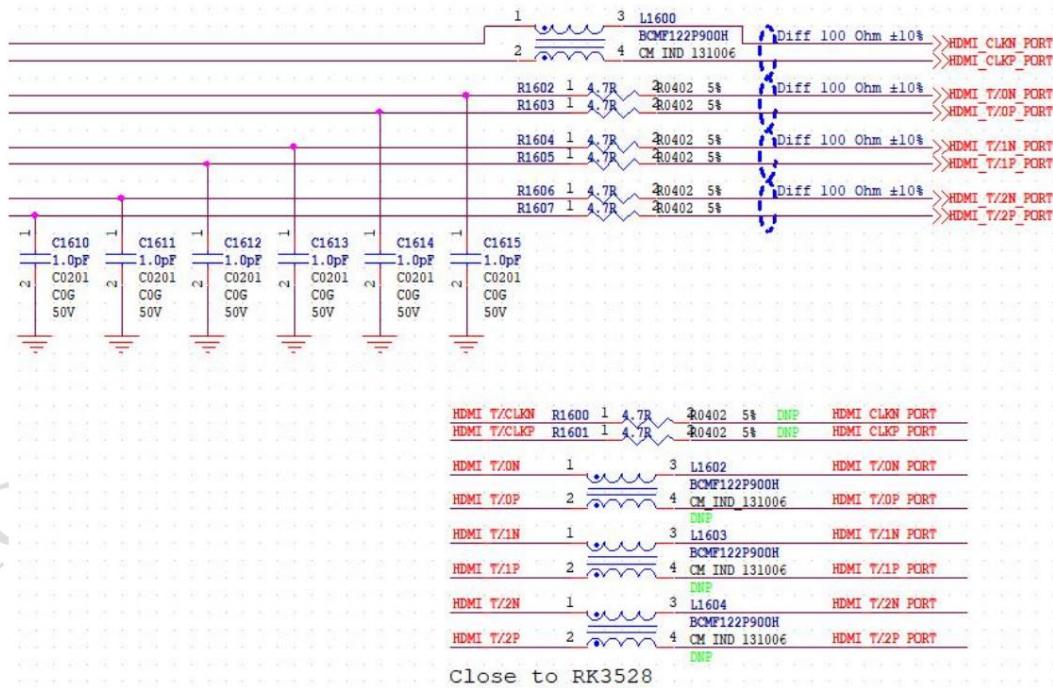


Figure 2-74 HDMI edge too fast reserve circuit

The following table shows the recommended HDMI TX interface matching design.

Table 2-16 RK3528 HDMI TX interface design

Signal	Connection method	illustrate
HDMI_TX_D0P/D0N series with a 2.2ohm resistor		TMDS data Lane 0 output
HDMI_TX_D1P/D1N series with a 2.2ohm resistor		TMDS data Lane 1 output
HDMI_TX_D2P/D2N series with a 2.2ohm resistor		TMDS data Lane 2 output
HDMI_TX_CLKP/CLKN series with a 2.2ohm resistor		TMDS clock output
HDMI_TX_REXT	1kohm 1% resistor to ground	External reference resistor for HDMI_TX PHY
HDMI_TX_HPD	Connect a 1kohm resistor in series	HDMI insertion detection
HDMI_TX_CEC	Connect a 22ohm resistor in series	HDMI CEC signal
HDMI_TX_SCL	Connect a 100ohm resistor in series and pull up a 1.8kohm resistor to VCC5V_HDMI_TX	HDMI DDC Clock
HDMI_TX_SDA	Connect a 100ohm resistor in series and pull up a 1.8kohm resistor to VCC5V_HDMI_TX	HDMI DDC data input and output

2.3.6.2 CVBS Interface

RK3528 supports one CVBS with a maximum output resolution of 720x576@60Hz.

The CVBS_VDAC_IOUTP pin must be connected to ground via a 75ohm 1% resistor and placed close to the RK3528; the VDAC_IOUTN pin must be grounded.

VDAC_IREF is the external reference resistor pin of CVBS PHY. Connect a 1kohm resistor with a precision of 1% to ground. The resistor must not be changed.

value, and place it close to the RK3528 chip pins during layout.

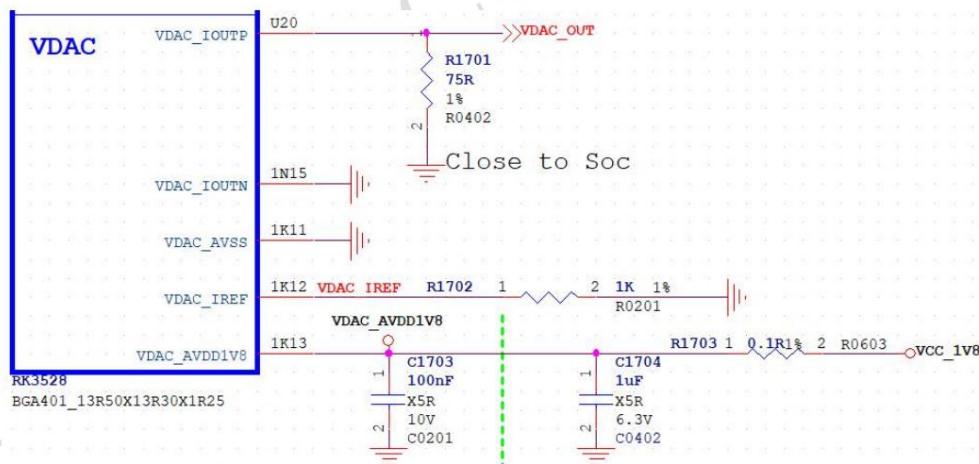


Figure 2-75 RK3528 CVBS PHY pins

The VDAC sampling clock is 27MHz, and the capacitor C5100 and the inductor L5100 form an LC parallel resonant circuit, which is mainly used to prevent CVBS

The 27MHz frequency component of the output signal passes through, and the impedance of the LC parallel resonant circuit is the largest at the local oscillation frequency (as shown in the impedance characteristic curve below).

The local oscillator frequency of the circuit parameter design is around 27MHz. According to the following calculation formula, the local oscillator frequency is 26.5258MHz, which is close to the CVBS sampling frequency.

Clock 27MHz.

$$f = \frac{1}{2 \cdot \sqrt{LC}} = \frac{1}{2 \cdot \sqrt{1.8 \cdot 20 \cdot 10^{-9} F}} = 26.5258 \text{ MHz}$$

Capacitors C5101 and C5102 are used to filter out the high-frequency noise components of the circuit (the bandwidth of the composite video signal is 6MHz).

The oscillator and its filtering circuit make the output waveform smoother and help improve EMI and other problems.

To enhance anti-static capability, ESD devices must be reserved for the signal and placed close to the connector pins.

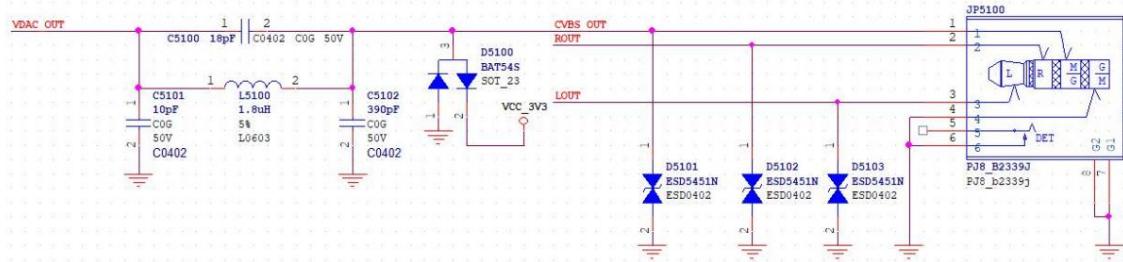


Figure 2-76 RK3528 CVBS circuit

Table 2-12 RK3528 CVBS interface design

Signal and multiplexing are pulled up and down by default	Connection method	Power domain
VDAC_IOUTP	THAT	75ohm 1% resistor to ground
VDAC_IOUTN	THAT	Grounding
VDAC_IREF	THAT	Connect a 1K precision resistor in series to ground

2.3.7 Audio-related circuit design

RK3528 provides a total of 4 groups of I2S interfaces, 1 group of PDM interface, and 1 SPDIF TX interface.

Among them, it provides 2 groups of I2S interfaces, 1 group of PDM interfaces, and 1 SPDIF TX interface. The IO domain multiplexing of these interfaces is as follows:

The power domains they belong to are shown in the following table for users to flexibly allocate and select.

Table 2-17 RK3528 external audio interface and IO multiplexing

External interface	First reuse (M0)	Second reuse (M1)	The third reuse (M2)	Internal power domain
I2S0	VCCIO3	VCCIO0	-	PD_VPU
I2S1	VCCIO4	-	-	PD_RKVENC
PDM	VCCIO4	-	-	PD_RKVENC
SPDIF_TX	VCCIO4 GPIO4_A1	VCCIO0 GPIO1_C3	VCCIO3 GPIO3_C3	PD_RKVENC

The remaining unleadsd audio interfaces are used to match the video input/output interfaces. Their internal allocation correspondence is described in 2.3.7.1 Audio Subsystem.

The internal power domains of these audio interfaces are as follows:

Domain consistency:

ÿ I2S2 belongs to PD_VPU;

ÿ I2S3 belongs to PD_VO;

2.3.7.1 Audio Subsystem Block Diagram

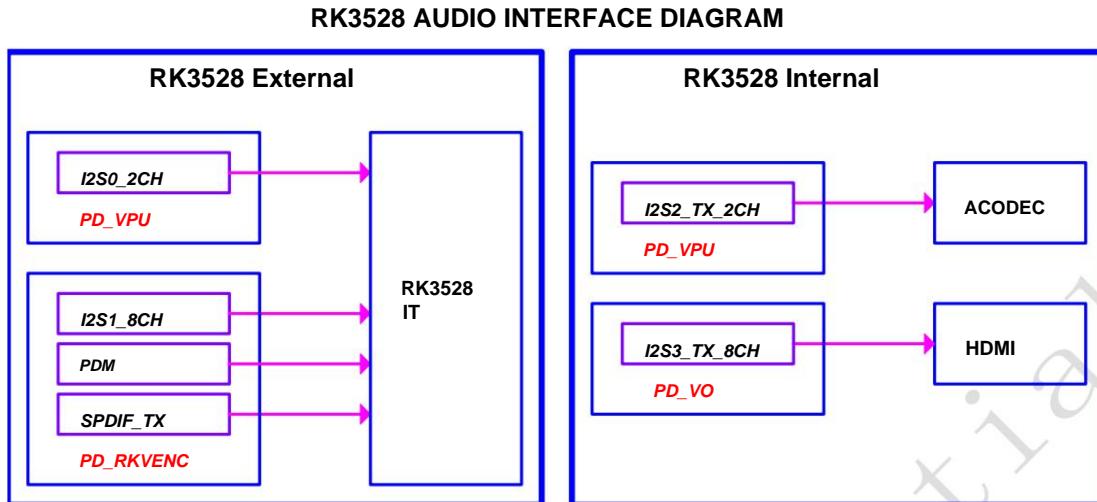


Figure 2-77 RK3528 audio subsystem block diagram

2.3.7.2 I2S Digital Audio Interface

As the most widely used digital audio interface, I2S can be used for communication with peripherals such as audio ADC, audio DAC, audio Codec, and DSP.

Integrated audio input and output support is also provided for the video input/output interfaces.

Both I2S interfaces of RK3528 support master-slave mode, bit width from 16 to 32 bits, and sampling rate up to 192kHz.

Please refer to the TRM document for detailed description of the format and timing.

2.3.7.2.1 I2S0 Digital Audio Interface

The I2S0 interface contains independent 2-channel output and 2-channel input. For output data SDO and input data SDI, a set of references are used.

Bit/frame clock SCLK/LRCK.

The I2S0 interface supports master-slave working mode and is software configurable. It supports 3 I2S formats (normal, left-aligned, right-aligned); supports 4 PCM formats (early, late1, late2, late3).

This group of I2S pins is multiplexed in two different power domains, I2S0_M0 is multiplexed in VCCIO3, I2S0_M1 is multiplexed in VCCIO0, and the two All signals can be led out in a complete group. The two multiplexing locations cannot be used at the same time, and only one group can be used at a time. level to match the corresponding IO power domain.

The recommended pull-up and pull-down and matching designs for the I2S0 interface are shown in the table.

Table 2-18 RK3528 I2S0 interface signal description

Signal	Default pull-up and pull-down	Connection method	Description (chip side)
I2S0_MCLK_M0	drop down	Connect a 22ohm resistor in series	I2S system clock output
I2S0_SCLK_M0	drop down	Connect a 22ohm resistor in series	I2S Continuous Serial Clock, Bit Clock
I2S0_LRCK_M0	drop down	Connect a 22ohm resistor in series	I2S frame clock for channel selection
I2S0_SDIN_M0	drop down	Direct connection	I2S serial data input
I2S0_SDO_M0	drop down	Direct connection	I2S serial data output
I2S0_MCLK_M1	drop down	Connect a 22ohm resistor in series	I2S system clock output
I2S0_SCLK_M1	drop down	Connect a 22ohm resistor in series	I2S Continuous Serial Clock, Bit Clock
I2S0_LRCK_M1	drop down	Connect a 22ohm resistor in series	I2S frame clock for channel selection

Signal	Default pull-up and pull-down	Connection method	Description (chip side)
I2S0_SDI_M1	drop down	Direct connection	I2S serial data input
I2S0_SDO_M1 ý To	drop down	Direct connection	I2S serial data output

To improve the performance of the I2S interface, the decoupling capacitor corresponding to the VCCIO power domain must not be deleted and should be placed close to the pin during layout;

When using a connector to connect a board to a board, it is recommended that a resistor with a certain resistance value (between 22ohm and 100ohm) be connected in series with the clock/control/signal.

The specific time is subject to whether it can meet the SI test) and TVS devices are reserved.

2.3.7.2.2 I2S1 Digital Audio Interface

The I2S1 interface contains 8 independent channels of output and 8 independent channels of input. For output data SDOx and input data SDIx, both refer to the same

Group bit/frame clock SCLK/LRCK.

The I2S1 interface supports master-slave working mode and is software configurable. It supports 3 I2S formats (normal, left-aligned, right-aligned); supports 4 PCM formats (early, late1, late2, late3).

This group of I2S pins are not reused and are all on the power domain VCCIO4. You need to check the IO level of the I2S peripheral to match the corresponding IO

Power domains are powered.

The pull-up and pull-down and matching design recommendations for the I2S1 interface are shown in the table:

Table 2-19 RK3528 I2S1 interface signal description

Signal	Default pull-up and pull-down	Connection method	Description (chip side)
I2S1_MCLK	drop down	Connect a 22ohm resistor in series	I2S system clock output
I2S1_SCLK	drop down	Connect a 22ohm resistor in series	I2S Continuous Serial Clock, Bit Clock
I2S1_LRCK	drop down	Connect a 22ohm resistor in series	I2S frame clock for channel selection
I2S1_SDO0	drop down	Direct connection	I2S serial data 0 output
I2S1_SDO1	drop down	Direct connection	I2S serial data 1 output
I2S1_SDO2	drop down	Direct connection	I2S serial data 2 output
I2S1_SDO3	drop down	Direct connection	I2S serial data 3 output
I2S1_SDIO	drop down	Direct connection	I2S serial data 0 input
I2S1_SDII	drop down	Direct connection	I2S serial data 1 input
I2S1_SDII	drop down	Direct connection	I2S serial data 2 input
I2S1_SDIII	drop down	Direct connection	I2S serial data 3 input

To improve I2S interface performance, the decoupling capacitors corresponding to the VCCIO power domain must not be removed and should be placed close to the pins during layout.

When using a connector to connect a board to a board, it is recommended that a resistor with a certain resistance value (between 22ohm and 100ohm) be connected in series with the clock/control/signal.

The specific time is subject to whether it can meet the SI test) and TVS devices are reserved.

2.3.7.3 PDM digital audio interface

RK3528 provides one set of PDM interfaces, which can be led out.

PDM works in master receive mode (RK3528 provides PDM clock and receives data) and supports 8-channel input

input capability, bit width from 16 to 24 bits, and sampling rate up to 192kHz.

The PDM interface is usually used to connect a digital microphone or to record the analog microphone through the analog audio ADC of the PDM interface.

The following figure shows the data format of the PDM interface. PDM_DATA consists of Data(R) and Data(L). PDM is a 1-bit sampling interface.

Data(L) and Data(R) are sampled on the rising and falling edges of CLK, that is, each PDM_SDIx data line can transmit two channels of audio data.

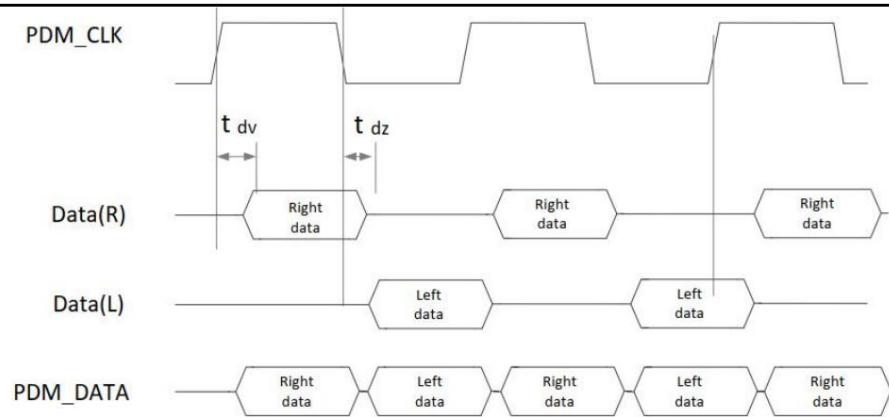


Figure 2-78 RK3528 PDM interface data format

The corresponding relationship between common sampling rates and PDM_CLK is shown in the following table, which can be used as a reference during hardware commissioning:

Table 2-20 RK3528 PDM_CLK frequency and sampling rate comparison table

PDM_CLK frequency	Sampling rate
3.072MHz	12kHz, 24kHz, 48kHz, 96kHz, 192kHz
2.8224MHz	11.025kHz, 22.05kHz, 44.1kHz, 88.2kHz, 176.4kHz
2.048MHz	8kHz, 16kHz, 32kHz, 64kHz, 128kHz

The PDM pins are not multiplexed and are all on the power domain VCCIO4. You need to check the IO level of the PDM peripherals to match the corresponding IO voltage.

Power supply from the source domain.

The pull-up and pull-down and matching design recommendations for the PDM interface are shown in the table. To improve the impact of PCB traces on the clock, two co-source and co-phase

PDM clocks, PDM_CLK0 and PDM_CLK1, can be allocated according to layout routing requirements to avoid single CLK routing.

The impact of branches.

Table 2-21 RK3528 PDM interface signal description

Signal	Default pull-up and pull-down	Connection method	Description (chip side)
PDM_CLK0	drop down	Connect a 22ohm resistor in series	PDM Clock 0
PDM_CLK1	drop down	Connect a 22ohm resistor in series	PDM Clock 1
PDM_SDIO	drop down	Direct connection	PDM data input 0
PDM_SD11	drop down	Direct connection	PDM data input 1
PDM_SD12	drop down	Direct connection	PDM Data Input 2
PDM_SD13	drop down	Direct connection	PDM Data Input 3

To improve PDM interface performance, decoupling capacitors corresponding to the VCCIO power domain must not be removed and should be placed close to the pins during layout.

When using a connector to connect a board to a board, it is recommended that a resistor with a certain resistance value (between 22ohm and 100ohm) be connected in series with the clock/control/signal.

The specific time is subject to whether it can meet the SI test and TVS devices are reserved.

2.3.7.4 SPDIF TX digital audio interface

RK3528 provides one set of SPDIF_TX interface. The SPDIF_TX pin is multiplexed in three different power domains. SPDIF_TX_M0 is multiplexed.

On VCCIO4, GPIO4_A1; SPDIF_TX_M1 is multiplexed on VCCIO0, GPIO1_C3; SPDIF_TX_M2 is multiplexed on VCCIO3,

GPIO3_C3. The IO level of the SPDIF_TX peripheral needs to be checked to match the corresponding IO power domain.

The pull-up and matching design recommendations for the SPDIF interface are shown in the table:

Table 2-22 RK3528 SPDIF_TX interface signal description

Signal and multiplexing	Default pull-up and pull-down	Connection method	Power domain
SPDIF_TX_M0	drop down	Connect a 22ohm resistor in series	VCCIO4
SPDIF_TX_M1	drop down	Connect a 22ohm resistor in series	VCCIO0
SPDIF_TX_M2	drop down	Connect a 22ohm resistor in series	VCCIO3

To improve the performance of the SPDIF interface, the decoupling capacitors corresponding to the VCCIO power domain must not be removed and should be placed close to the pins during layout.

When using a connector to connect a board to a board, it is recommended that a resistor with a certain resistance value (between 22ohm and 100ohm) be connected in series with the clock/control/signal.

The specific time is subject to whether it can meet the SI test) and TVS devices are reserved.

2.3.7.5 ACODEC Audio Interface

RK3528 supports one pair of LINEOUT_L/R stereo output.

ACODEC_VCM is the common mode voltage pin of ACODEC PHY, connect an external 4.7uF capacitor to ground, and do not change the resistor value.

Place it close to the RK3528 chip pins.

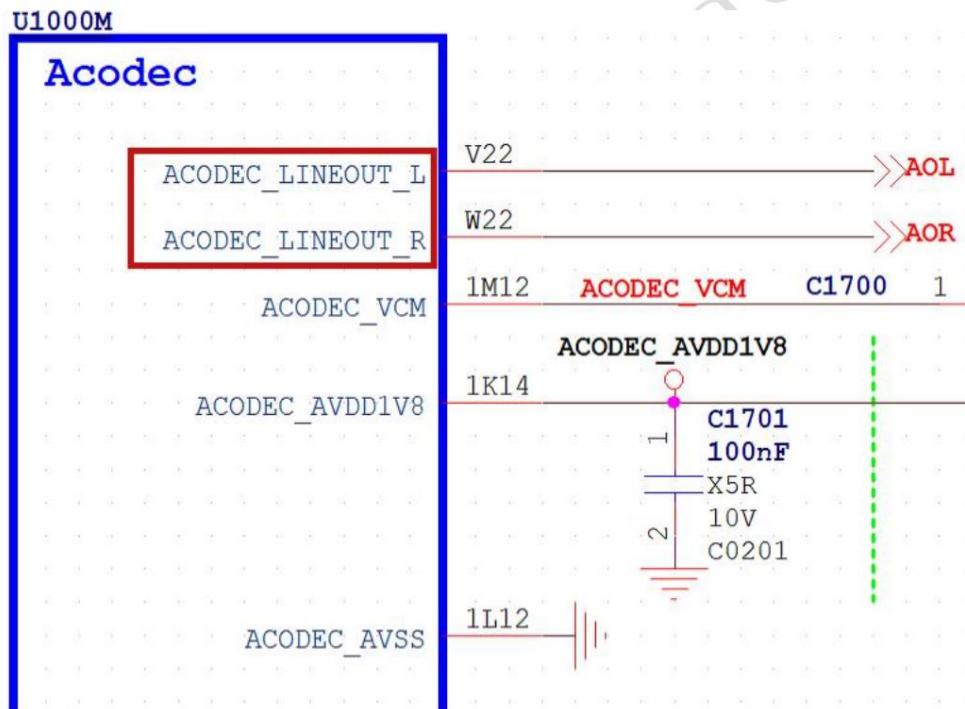


Figure 2-78 RK3528 ACODEC PHY pins

When driving dual stereo sound, ACODEC LINEOUT_L/R output needs to be connected in series with a 4.7uF capacitor and placed close to the amplifier. The maximum output voltage

About 1.56Vpp (552mVrms). In order to meet the output 2Vrms indicator, the power amplifier needs to be amplified by about 4 times. The specific circuit diagram is based on

ACODEC LINEOUT_L/R needs to be routed differentially with GND. See Section 3.3.14 for details.

2-Vrms Audio Line Driver

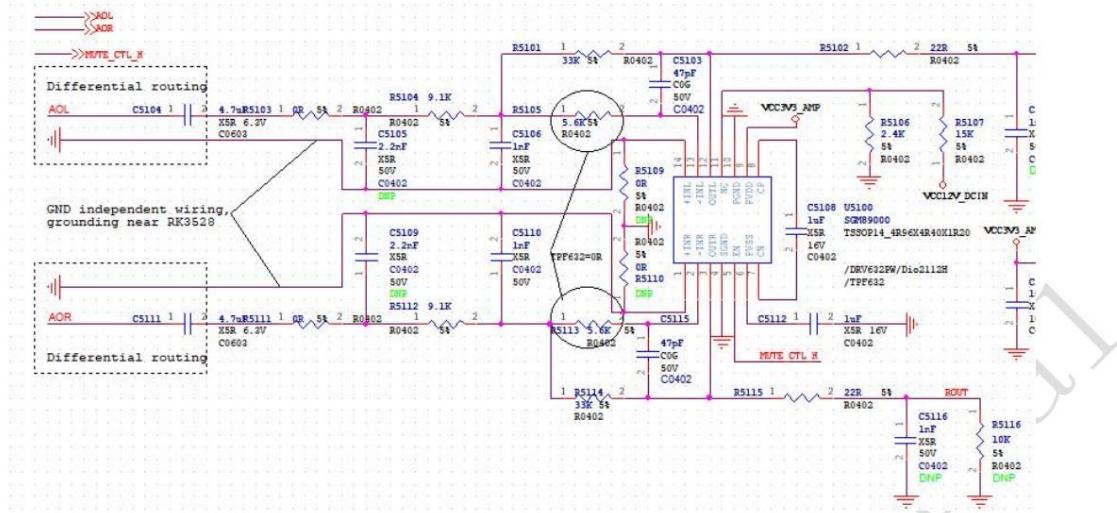


Figure 2-79 RK3528 AUDIO circuit diagram

Currently on the market, there are two structures of 3.5mm four-section audio headphone jacks, the national standard (OMTP) and the American standard (CTIA). The signal connection requires

Please refer to the corresponding specifications of the headphone socket. The diagram in this article defaults to the national standard four-section headphone connection method, as shown below.

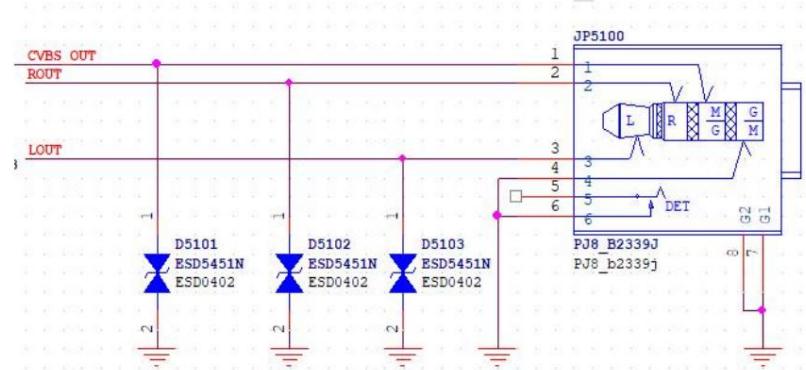


Figure 2-80 BK3528 AUDIO interface

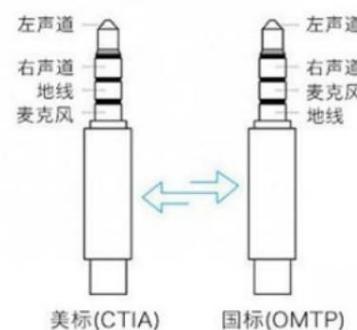


Figure 2-81 3.5mm headphone jack difference

When driving the speaker, LINEOUT L/R can be connected to one of them, or both signals can be connected in series with capacitors and then connected to the same input of the amplifier.

Input (the amplification factor will be doubled), the amplification factor of the power amplifier is set according to the power amplifier selection and needs, and the circuit is shown in the figure below.

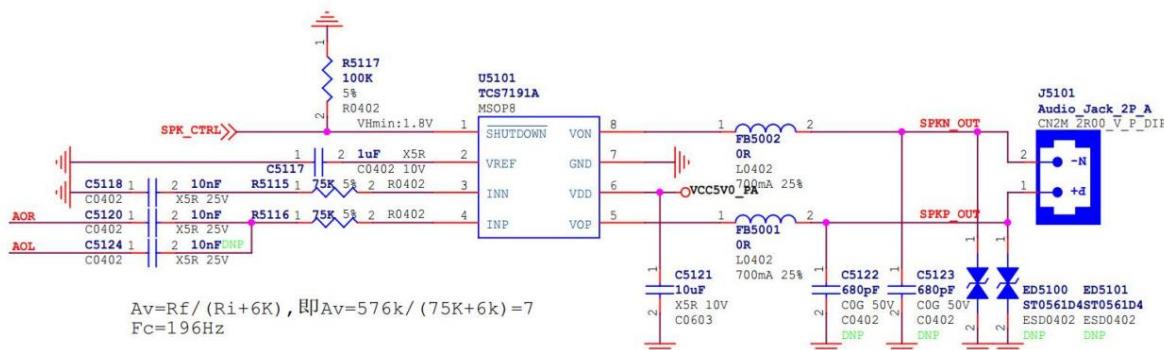


Figure 2-82 RK3528 ACODEC output driver speaker

Table 2-12 RK3528 ACODEC interface design

Signal and multiplexing are pulled up and down by default	Connection method	Power domain
ACODEC_LINEOUT_L	THAT	Connect a 4.7uF capacitor in series LINEOUT output
ACODEC_LINEOUT_R	THAT	Connect a 4.7uF capacitor in series LINEOUT output
ACODEC_VCM	THAT	Connect a 4.7uF capacitor to ground ACODEC internal reference

2.3.7.6 Audio Peripheral Design Reference

This section provides design suggestions for common audio scenarios for your reference.

2.3.7.6.1 Sound playback equipment, headphones, and speakers

For speaker playback requirements, the default implementation uses the ACODEC DAC inside the RK3528 to achieve analog output, and then uses the audio

The power amplifier realizes power amplification to drive the speaker, as shown in the figure below.

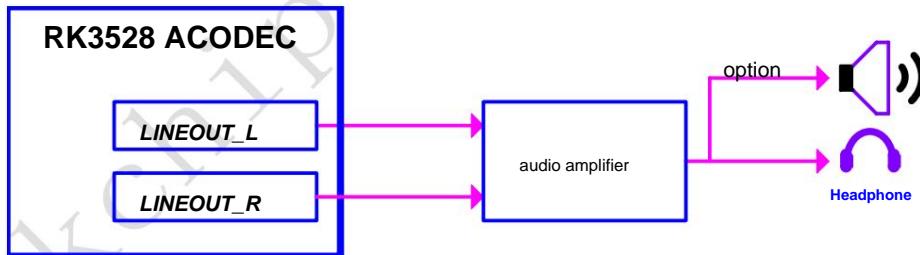


Figure 2-83 RK3528 ACODEC output diagram

In addition, RK3528 can also connect to the audio DAC to achieve analog output through I2S signal, and then achieve power amplification and drive through the audio amplifier.

Move the speaker, as shown below.

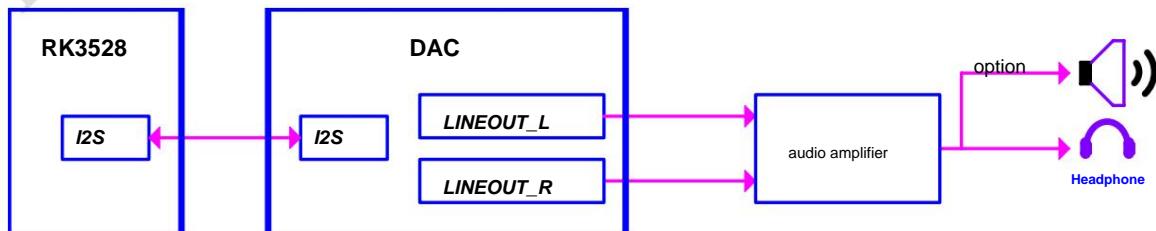


Figure 2-84 RK3528 I2S output diagram

2.3.7.6.2 Recording equipment and microphones

For recording needs, you can use the PDM interface to connect a PDM microphone, or use the ADC of the I2S/PDM interface to connect an external analog MIC to achieve.

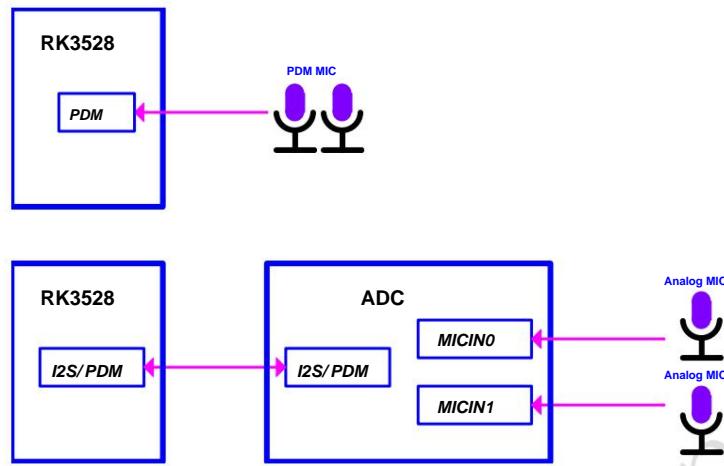


Figure 2-85 MIC input circuit diagram

In addition, you can also use the Codec with integrated ADC and DAC to implement related functions, as shown in the figure below.

For design references of functions such as phone and Bluetooth calling, please contact RK at this stage to obtain:

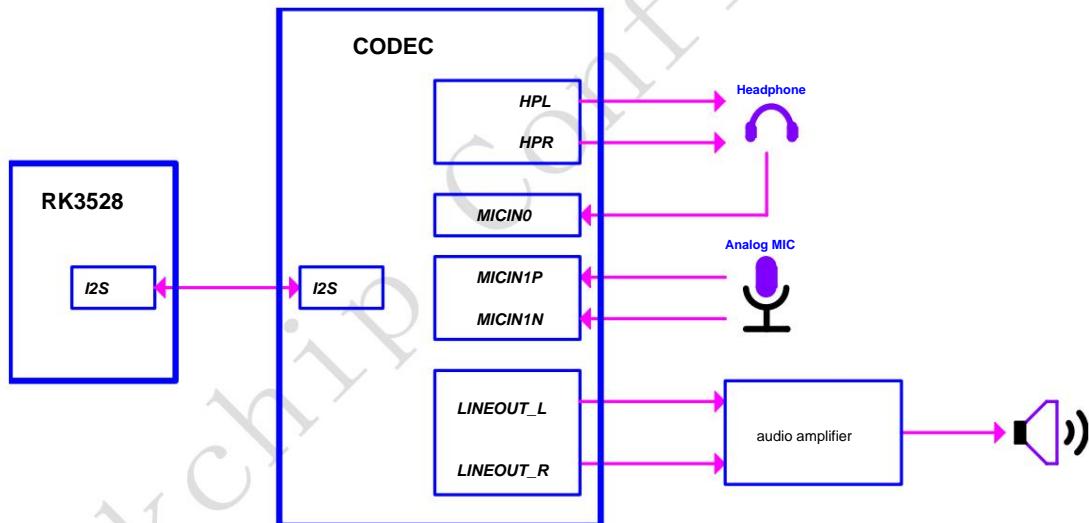


Figure 2-86 RK3528 external CODEC audio solution diagram

2.3.8 Ethernet interface circuit

The RK3528 chip integrates 1 GMAC controller, 1 EMAC controller and FEPHY.

2.3.8.1 FEPHY Interface

The FEPHY integrated inside the RK3528 can be connected to the transformer and RJ45 interface through the MDI signal.

FEPHY_REXT is the external reference resistor pin of FEPHY. It is connected to a 6.04kohm resistor with a precision of 1% to ground. The resistor value must not be changed. It should be placed close to the RK3528 chip pin during layout.

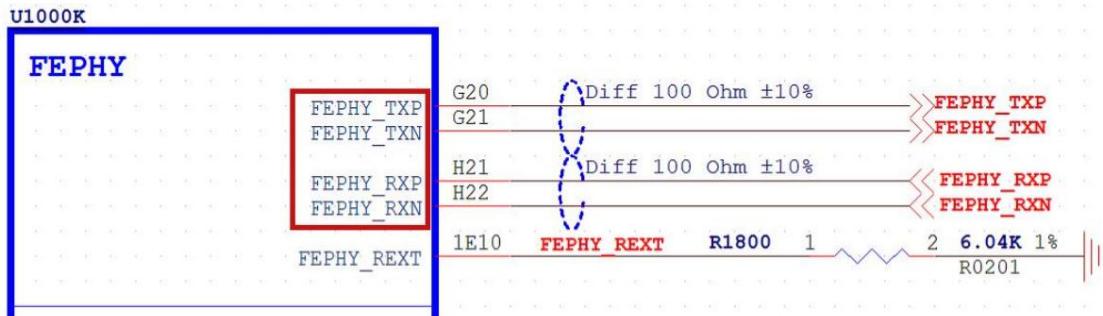


Figure 2-87 RK3528 built-in FEPHY circuit diagram

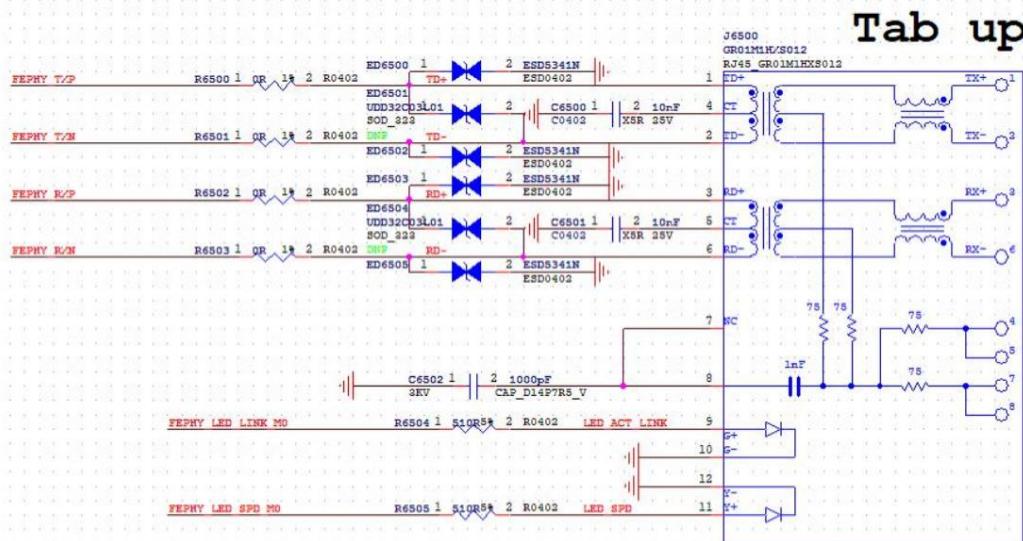


Figure 2-88 RK3528 RJ45 interface

Table 2-11 RK3528 FEPHY interface design

Signal	Internal pull-up and pull-down	Connection method	Description (chip side)
FEPHY_RXP/_RXN	THAT	Connect directly with 0ohm resistor in series	Data receiving differential pair signal
FEPHY_TXP/TXN	THAT	Connect directly with 0ohm resistor in series	Data transmission differential pair signal
FEPHY_EXTR	THAT	Connect 6.04K precision resistor in series to ground	Reference resistor

Design points:

ÿ The 0ohm resistor connected in series with the differential signal cannot be omitted and needs to be reserved.

ÿ The REXT resistor is placed close to the chip.

2.3.8.2 RGMII Interface Circuit

The GMAC controller supports the following features:

ÿ RGMII interface supporting 10/100/1000 Mbps data transmission rate;

ÿ RMII interface supporting 10/100 Mbps data transfer rate.

The RGMII/RMII interface of the GMAC operates in the VCCIO3 power domain.

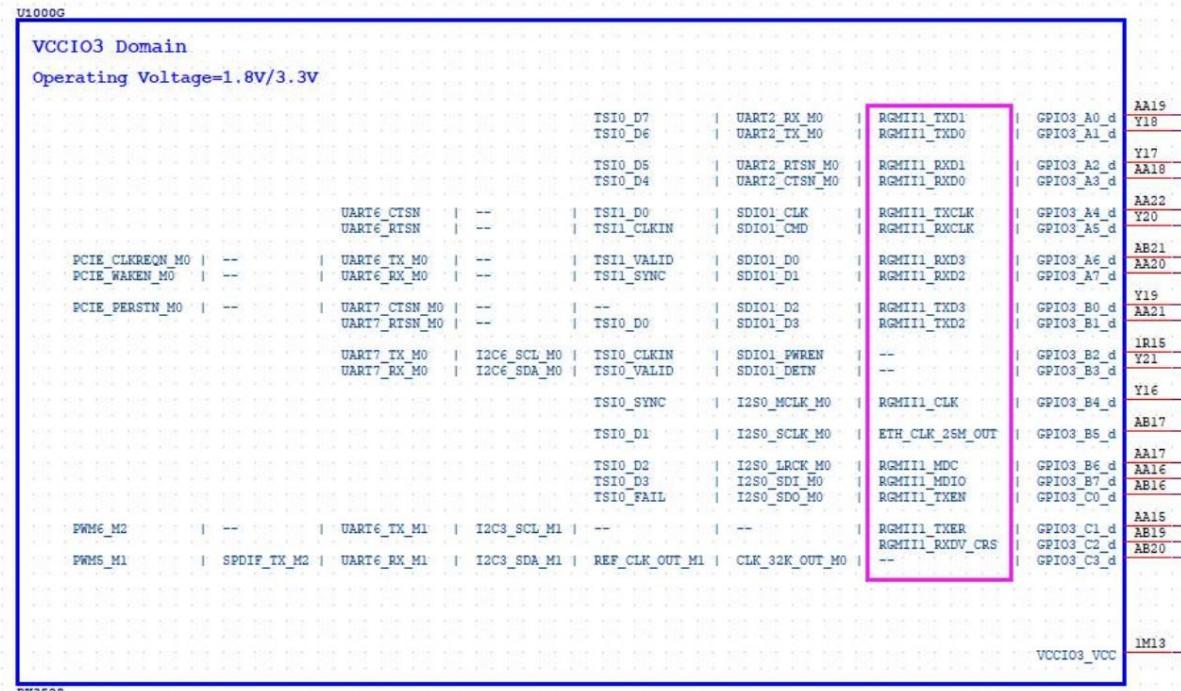


Figure 2-89 RK3528 GMAC0 functional pins

Please note the following when designing the RGMII/RMII interface:

þ GMAC can support 1.8V or 3.3V level, which is determined by VCCIO3_VCC (Pin 1M13). Pin 1M13 is connected to 1.8V power supply.

It is 1.8V level, Pin 1M13 is connected to 3.3V power supply, which is 3.3V level;

þ If possible, it is recommended that RGMII/RMII use 1.8V level to obtain better signal quality;

To improve the performance of the RGMII/RMII interface, the decoupling capacitor of the VCCIO3 power supply must not be removed and should be placed close to the pin during layout.

þ ETH_REFCLKO_25M requires a 0 ohm resistor to be reserved in series at the RK3528 end to improve signal quality according to actual conditions;

þ TXD0-TXD3, RXCLK, RXDV need to reserve a 0 ohm resistor in series at the RK3528 end, which can be increased according to actual conditions.

Signal quality;

þ RXD0-RXD3, RXCLK, RXDV need to be connected in series with a 22 ohm resistor at the PHY end to improve signal quality;

þ The pull-up and matching design recommendations for the RGMII/RMII interface are as shown in the table:

Table 2- 23 RK3528 RGMII/RMII interface design

Signal	IO Type (Chip side)	Connection method	RGMII interface	Signal Description	RMII interface	Signal Description
GMAC1_TXD[3~0]	Output	Reserve a 0ohm resistor in series, close to RK3528 side	RGMIIx_TXD[3~0]	Data transmission	RMIIx_TXD[1~0]	Data transmission
GMAC1_RXCLK output		Reserve a 0ohm resistor in series, close to RK3528 side	RGMIIx_RXCLK	Data sending reference time bell	-	-
GMAC1_RXEN output		Reserve a 0ohm resistor in series, close to RK3528 side	RGMIIx_RXEN	Data transmission enable (up rising edge) and data transmission Error (falling edge)	RMIIx_RXEN	Data sending use Signal
GMAC1_RXD[3~0]	enter	Connect 22ohm resistor in series Resistance, close to the PHY end	RGMIIx_RXD[3~0]	Data Reception	RMIIx_RXD[1~0]	Data Reception
GMAC1_RXCLK input		Connect 22ohm resistor in series Resistance, close to the PHY end	RGMIIx_RXCLK	Data reception reference time bell	-	-

GMAC1_RXDV input		Connect a 22ohm resistor in series, close to the PHY end	RGMIIx_RXDV	Data reception valid (rising edge) and reception error (falling edge)	RMIIx_RXDV_CRS	Data reception valid and carrier sense
GMAC1_MCLKI NOTE	Input/Output	Output mode: Reserved 0ohm resistor in series, close to RK3528 end Input mode: Reserved 22ohm resistor in series, close to PHY end	RGMIIx_MCLKIN_125M	PHY sends 125MHz to MAC, optional	RMII_MCLKIN_50M or RMII_MCLKOUT_50M	RMII data transmission and data reception reference clock
ETH_REFCLKO_25M	Output	Reserved 0ohm resistor in series, close to RK3528 end Reserved	ETHx_REFCLKO_25M	RK3528 provides 25MHz clock replacement PHY Crystal	ETHx_REFCLKO_25M	RK3528 provides 25MHz clock replaces PHY crystal
GMAC1_MDC Output		0ohm resistor in series, close to RK3528 end External pull-up	RGMIIx_MDC	manages the data clock.		
GMAC1_MDIO	Input/Output	1.5K-1.8Kohm resistor When the board-to-board	RGMIIx_MDIO	Manage data import/export	RMIIx_MDIO	Manage data import/export

connection is realized through the connector, it is recommended to connect a resistor with a certain resistance value (between 22ohm-100ohm, the specific resistance should be able to meet the requirements) so that the SI test shall prevail), and TVS devices shall be reserved;

⑤ RGMII connection diagram 1 (taking RK631 as an example), please see the reference diagram for the specific circuit (GEPHY working clock uses an external 25MHz Crystals):

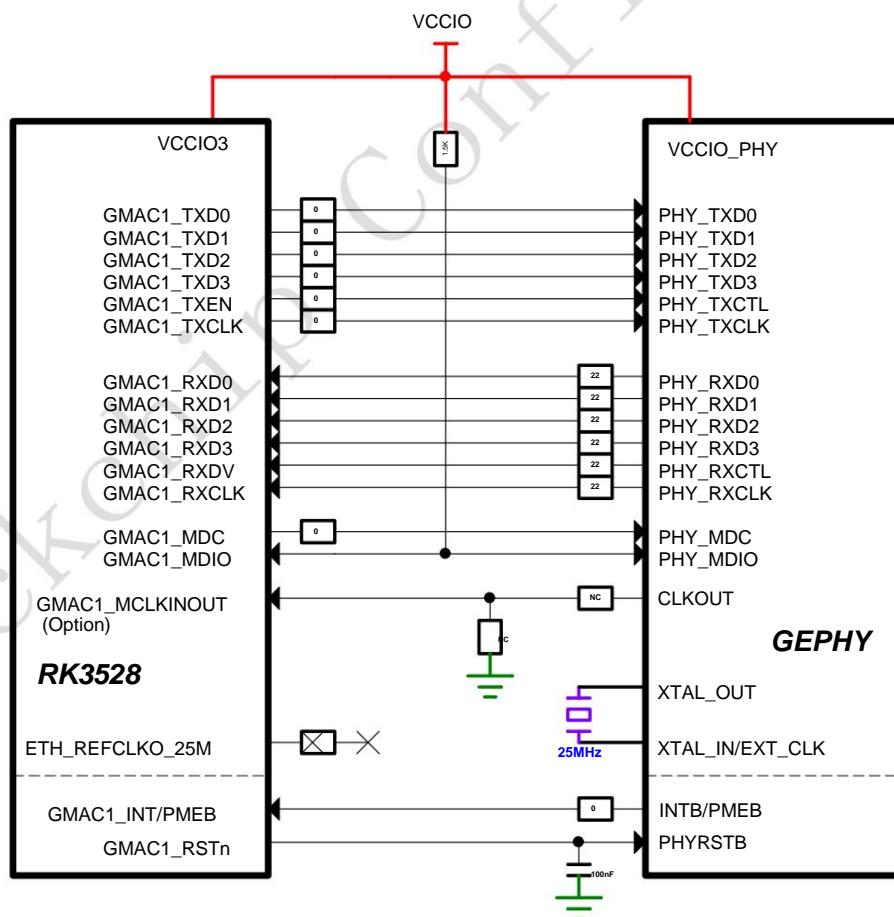


Figure 2-90 RGMII connection diagram 1

⑥ RGMII connection diagram 2 (taking RK631 as an example), for the specific circuit, please see the reference diagram (GEPHY working clock uses RK3528 to provide 25MHz provided):

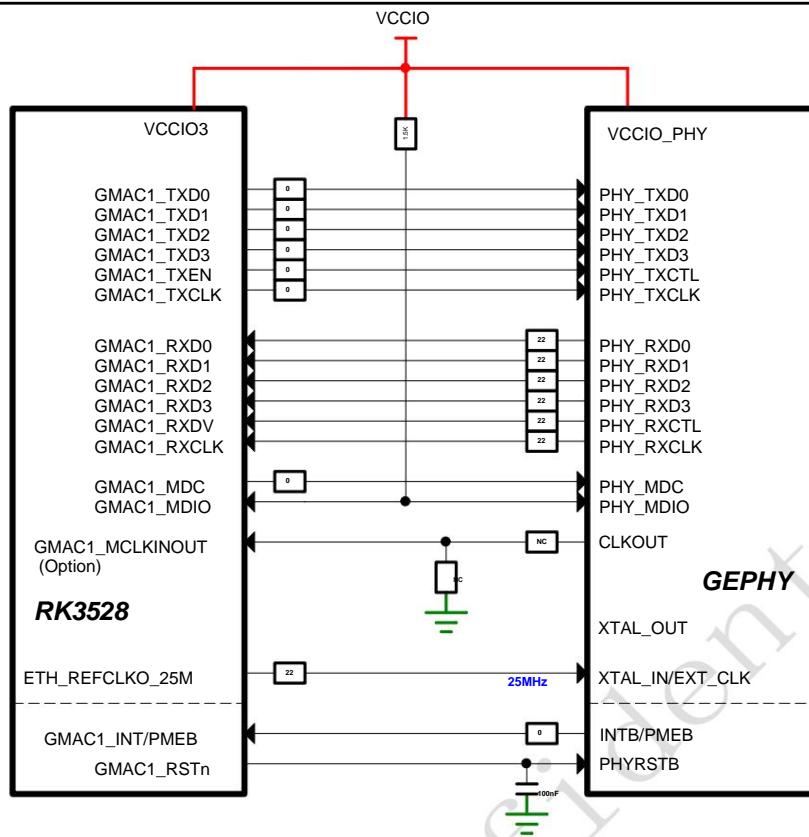


Figure 2-91 RGMII connection diagram 2

RMII connection diagram 1 (taking RTL8201F as an example), please see the reference diagram for the specific circuit (GMAC1_MCLKINOUT uses output mode, that is, when the FEPHY working clock is also the reference clock of the RMII interface. Some FEPHYS do not support this mode, so please note):

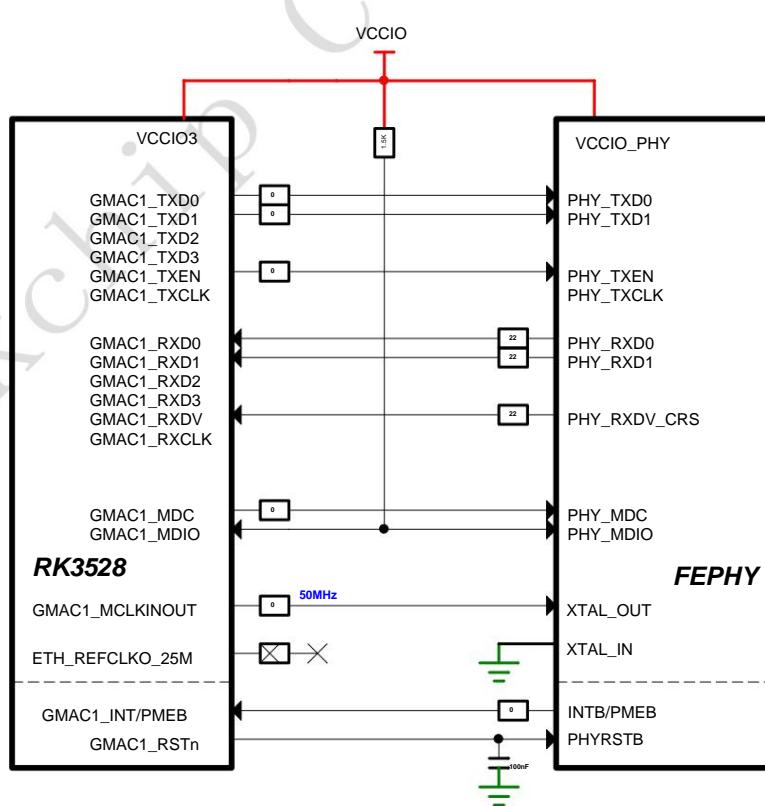


Figure 2-92 RMII connection diagram 1

RMII connection diagram 2 , please see the reference diagram for the specific circuit (FEPHY working clock uses 25MHz crystal,

GMAC1_MCLKINOUT uses output mode. When used as the reference clock for the RMII interface, the TXCLK of FEPHY needs to be configured as input mode):

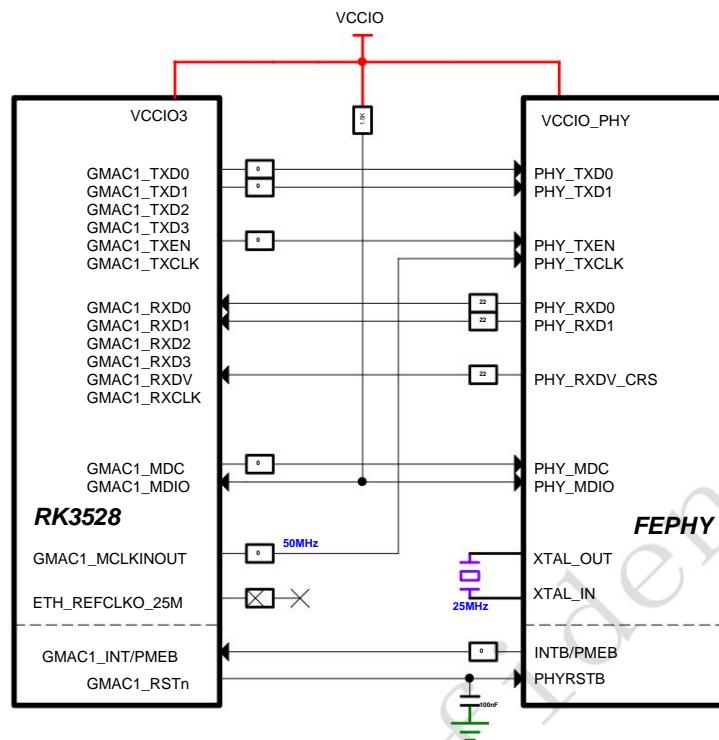


Figure 2-93 RMII connection diagram 2

ÿ RMII connection diagram 3 (taking RTL8201F as an example), please see the reference diagram for the specific circuit (use the 25MHz provided by RK3528 instead of FEPHY crystal, GMAC1_MCLKINOUT uses output mode. When used as the reference clock for the RMII interface, FEPHY's TXCLK needs to be configured as input mode):

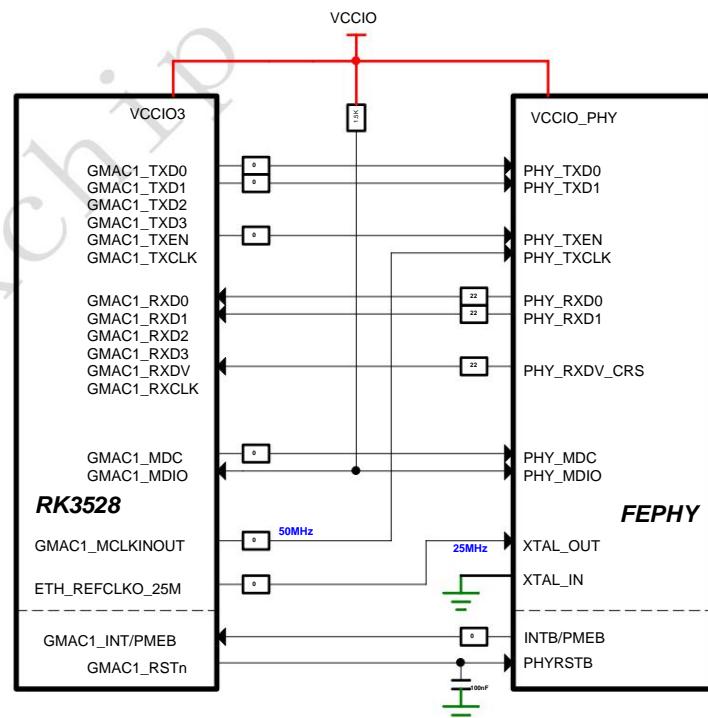


Figure 2-94 RMII connection diagram 3

ÿ RMII connection diagram 4, please see the reference diagram for the specific circuit (FEPHY working clock uses an external 25MHz crystal,

GMAC1_MCLKINOUT uses input mode, the reference clock of the RMII interface is provided by FEPHY, and the TXCLK of FEPHY needs to be configured as output mode):

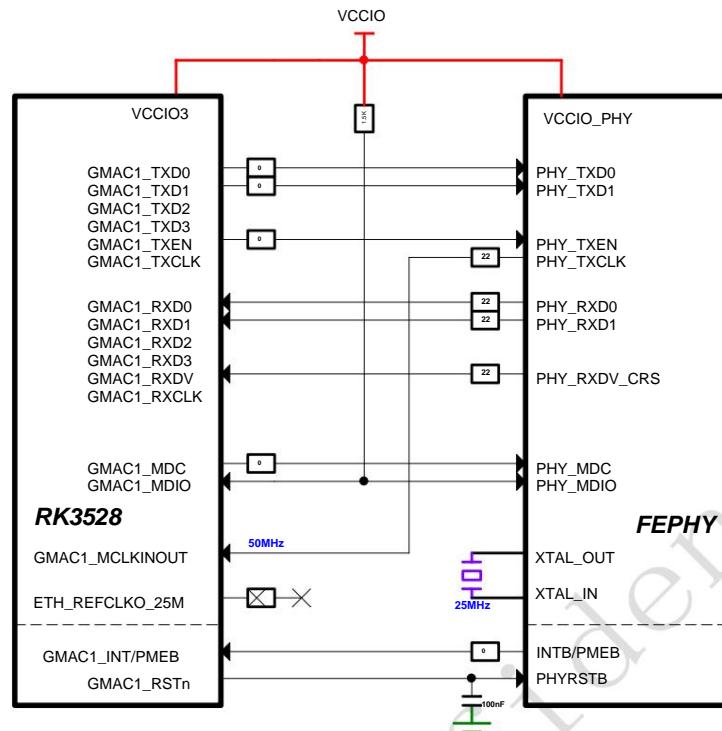


Figure 2-95 RMII connection diagram 4

RMII connection diagram 5 (taking RTL8201F as an example), please see the reference diagram for the specific circuit (use the 25MHz provided by RK3528 instead of FEPHY crystal, GMAC1_MCLKINOUT uses input mode, the reference clock of the RMII interface is provided by FEPHY, and FEPHY's TXCLK needs to be configured as output mode):

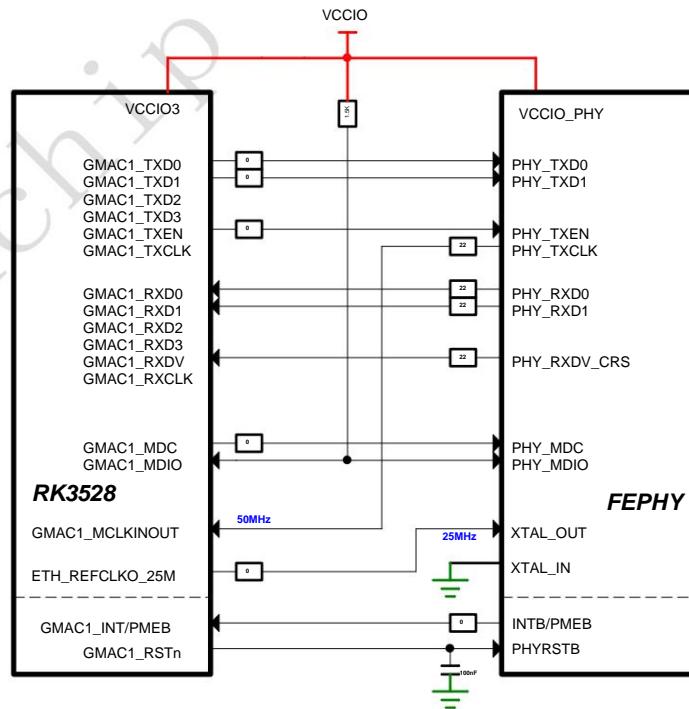


Figure 2-96 RMII connection diagram 5

In RGMII mode, the TX/RX clock path inside the RK3528 chip integrates delayline and supports adjustment; the reference diagram defaults to

The configuration is: the timing between TXCLK and data is controlled by MAC, and the timing between RXCLK and data is controlled by PHY (for example, when using RK631, RXCLK has 2nS delay enabled by default. Other PHYs should pay attention to this configuration);

ÿ The reset signal of Ethernet PHY needs to be controlled by GPIO. The GPIO level must match the PHY IO level. A 100nF capacitor must be added close to the PHY pin to enhance anti-static capability. Note: The reset pin of RK631 only supports 3.3V level.

ÿ INTB/PMEB of RK631 is open drain output, external pull-up resistor must be added; ÿ When PHY uses an external crystal, the crystal capacitor should be selected according to the load capacitance value of the actual crystal used, and the frequency deviation should be controlled within +/-20ppm Within;

ÿ The external resistor of RSET pin of RK631 is 2.49K ohm with 1% accuracy, which cannot be modified at will; ÿ MDIO must be connected with an external pull-up resistor, 1.5-1.8Kohm is recommended, and the pull-up power supply must be consistent with the IO power supply; ÿ The connection of the center tap of the transformer of RK631 must be connected according to the reference diagram. If you change to other Ethernet PHY, the center tap of the transformer

For the connection of the tap, it is recommended to refer to the reference design of each Ethernet PHY manufacturer, because different PHY manufacturers have different connection Way;

ÿ It is recommended to use a high-voltage safety capacitor for the 1000pF isolation capacitor, with a sufficiently large electrical gap to ensure safety against lightning strikes. ÿ It is recommended to use a 0805 or larger package for the 75 ohm resistor on the high-voltage side of the network transformer. ÿ Lightning protection tubes need to be added to achieve a lightning protection level of 4KV or above. Ordinary isolation transformers can only meet the 2KV level requirement. ÿ If there is a requirement for lightning differential testing, TVS tubes need to be added between the MDI differential pairs. ÿ Be sure to confirm that the RJ45 package is consistent with the schematic diagram. The RJ45 has Tab down and Tab up, and the signal order is exactly the opposite.

If using RK631, it is recommended to use Tab down, the MDI order is in order;

ÿ The initial hardware configuration of PHY must match the actual requirements.

2.3.9 UART interface circuit

The RK3528 chip has 8 UART controllers and supports the following functions:

Each contains two 64-byte FIFOs for data reception and transmission; Supports 115.2Kbps, 460.8Kbps, 921.6Kbps, 1.5Mbps, 3Mbps, and 4Mbps; Supports programmable baud rates and non-integer clock dividers; Supports interrupt-based or DMA-based modes; Supports 5-8 bit width transmission. Considering the flexibility of different product applications, the eight

UARTs are multiplexed in several different power domains, with the suffixes _M0/_M1 to distinguish different multiplexing locations. _M0/_M1 cannot be used simultaneously, and only one group can be selected when assigning. For example, if UART0_M0 is selected, it cannot be selected.

UART0_M1

RK3528 UART interface distribution:

Table 2- 24 RK3528 UART interface distribution

UART Number	Reuse	Multiplexing power domains
UART0	M0, M1	M0_VCCIO0 M1_VCCIO1
UART1	M0, M1	M0_VCCIO4 M1_VCCIO4

UART Number	Reuse	Multiplexing power domains
UART2	M0, M1	M0>VCCIO3 M1>VCCIO0
UART3	M0, M1	M0>VCCIO4 M1>VCCIO4
UART4	-	VCCIO2
UART5	M0, M1	M0>VCCIO0 M1>VCCIO1
UART6	M0, M1	M0>VCCIO3 M1>VCCIO3
UART7	M1 M2	M0>VCCIO3 M1>VCCIO0

Table 2-25 RK3528 UART flow control interface distribution

UART Number	Reuse	Multiplexing power domains
UART0_RTSN	-	-
UART0_CTSN	-	-
UART1_RTSN	-	VCCIO4
UART1_CTSN	-	
UART2_RTSN	M0, M1	M0>VCCIO3 M1>VCCIO0
UART2_CTSN	-	
UART3_RTSN	-	VCCIO4
UART3_CTSN	-	
UART4_RTSN	-	VCCIO2
UART4_CTSN	-	
UART5_RTSN	M0, M1	M0>VCCIO0 M1>VCCIO1
UART5_CTSN	-	
UART6_RTSN	-	VCCIO3
UART6_CTSN	-	
UART7_RTSN	M0, M1	M0>VCCIO3 M1>VCCIO0
UART7_CTSN	-	

UART0 M0 is the Debug UART of RK3528 by default.

Adjust the power supply of the corresponding power domain according to the IO level of the UART peripheral and they must be consistent.

The recommended UART interface matching design is shown in the table below:

Table 2- 26 RK3528 UART interface design

Signal	Connection method	Description (chip side)
UARTx_RX	Direct connection	UART data input
UARTx_TX	Direct connection	UART data output
UARTx_CTSn	Direct connection	UART clear to send signal
UARTx_RTSn	Direct connection	UART request to send signal

When using a connector to connect a board to a board, it is recommended to connect a resistor with a certain resistance (between 22ohm and 100ohm, depending on the specific resistance).

Test is subject to the requirements) and TVS devices should be reserved.

2.3.10 SPI Interface Circuit

In addition to the FSPI controller, the RK3528 chip also has two general SPI controllers that support the following functions:

- ÿ Supports both master and slave modes;
- ÿ Support 4, 8, and 16-bit serial data transmission;
- ÿ Supports full-duplex and half-duplex mode transmission.

2 SPIs are not multiplexed. RK3528 SPI interface distribution:

Table 2- 27 RK3528 SPI interface distribution

SPI number	Reuse	Multiplexing power domains
SPI0	-	VCCIO4
SPI1	-	VCCIO0

Adjust the power supply of the corresponding power domain according to the IO level of the SPI peripheral and they must be consistent.

The SPI interface matching design recommendations are shown in the table:

Table 2- 28 RK3528 SPI interface design

Signal	Connection method	Description (chip side)
SPIx_CLK	Direct connection	SPI clock
SPIx_MOSI	Direct connection	SPI data output (Master)
SPIx_MISO	Direct connection	SPI data input (Master)
SPIx_CS0	Direct connection	SPI Chip Select 0
SPIx_CS1	Direct connection	SPI chip select 1

When using a connector to connect a board to a board, it is recommended to connect a resistor with a certain resistance (between 22ohm and 100ohm, depending on the specific resistance).

Test is subject to the requirements) and TVS devices should be reserved.

2.3.11 I2C Interface Circuit

The RK3528 chip has 8 I2C controllers and supports the following functions:

- ÿ Support I2C bus master mode;
- ÿ Support software programmable clock frequency and transmission rate up to 400Kbit/s;
- ÿ Supports 7-bit and 10-bit addressing modes.

Considering the flexibility of different product applications, 8 I2Cs are reused in several different power domains, and the suffixes _M0/_M1 are used to distinguish different reuse bits.

_M0/_M1 cannot be used at the same time. Only one of them can be selected during allocation. For example, if I2C1_M0 is selected, I2C1_M1 cannot be selected.

The distribution of RK3528 I2C interfaces is shown in the following table:

Table 2- 29 RK3528 I2C interface distribution

I2C Numbering	Reuse	Multiplexing power domains
I2C0	M0, M1	M0_VCCIO4
		M1_VCCIO4
I2C1	M0, M1	M0_VCCIO4
		M1_VCCIO4
I2C2	M1	M1_VCCIO0
I2C3	M0, M1	M0_VCCIO0
		M1_VCCIO3
I2C4	-	VCCIO2
I2C5	M0, M1	M0_VCCIO0
		M1_VCCIO1
I2C6	M0, M1	M0_VCCIO3
		M1_VCCIO1
I2C7	-	VCCIO2
HDMI_TX_I2C	-	PMUIO0

HDMI_TX_SCL/HDMI_TX_SDA is the I2C/DDC bus of HDMI TX, which is a dedicated bus.

Adjust the power supply of the corresponding power domain according to the IO level of the I2C peripheral and they must be consistent.

I2C signals SCL and SDA require external pull-up resistors. Depending on the bus load, select resistors of different resistance values. 2.2kohm is recommended.

Pull-up resistor.

The addresses of the devices on the I2C bus should not conflict, and the pull-up power supply must be consistent with the power supply.

The recommended I2C interface matching design is shown in the table below:

Table 2- 30 RK3528 I2C interface design

Signal	Connection method	Description (chip side)
I2Cx_SCL	Direct connection	I2C clock
I2Cx_SDA	Direct connection	I2C data output/input

When using a connector to connect a board to a board, it is recommended to connect a resistor with a certain resistance (between 220ohm and 100ohm, depending on the specific resistance).

Test is subject to the requirements) and TVS devices should be reserved.

2.3.12 PWM Interface Circuit

The RK3528 chip integrates two independent PWM controllers, each with four channels, for a maximum of eight PWM channels.

The following features are supported:

- ÿ Support capture mode;
- ÿ Support continuous mode or one-time mode;
- ÿ PWM3 and PWM7 support IR input function;

Each channel has two clock input options, one is a fixed frequency from the crystal oscillator, and the other is a frequency divided from the PLL bus.

Configurable.

Considering the flexibility of different product applications, the 8 PWMs are multiplexed in several different power domains, and the suffixes _M0/_M1/_M2 are used to distinguish different

Reuse location.

The distribution of RK3528 PWM interfaces is shown in the following table:

Table 2-31 RK3528 PWM interface distribution

PWM number	Reuse	Multiplexing power domains
PWM0	M0, M1	M0>VCCIO4 M1>VCCIO0
PWM1	M0, M1	M0>VCCIO4 M1>VCCIO0
PWM2	M0, M1	M0>VCCIO4 M1>VCCIO0
PWM3	M0, M1	M0>VCCIO4 M1>VCCIO2
PWM4	M0, M1	M0>VCCIO4 M1>VCCIO0
PWM5	M0, M1	M0>VCCIO4 M1>VCCIO3
PWM6	M0 M1 M2	M0>VCCIO4 M1>VCCIO0 M2>VCCIO3
PWM7	M0, M1	M0>VCCIO4 M1>VCCIO0

ÿ According to the IO level of the PWM peripheral, adjust the power supply of the corresponding power domain and keep it consistent;

ÿ When using a connector to connect a board to a board, it is recommended to connect a resistor with a certain resistance (between 22ohm and 100ohm, depending on the specific resistance).

SI test shall prevail), and TVS devices shall be reserved;

ÿ When the infrared receiver signal is input, please pay attention to the following:

ÿ Select PWM3/PWM7 as the infrared receiver input;

ÿ The power supply of the infrared receiver requires a 22-100ohm resistor and a capacitor of 10uF or more for RC filtering;

ÿ The infrared receiver uses 38KHz by default. If you change to other frequencies, the software needs to be adjusted accordingly.

ÿ The output level of the infrared receiver must match the IO level of RK3528;

ÿ It is recommended to connect a 22 ohm resistor and a 1nF capacitor to the infrared receiver output pin, and then connect it to RK3528 to enhance the anti-static surge capability.

force;

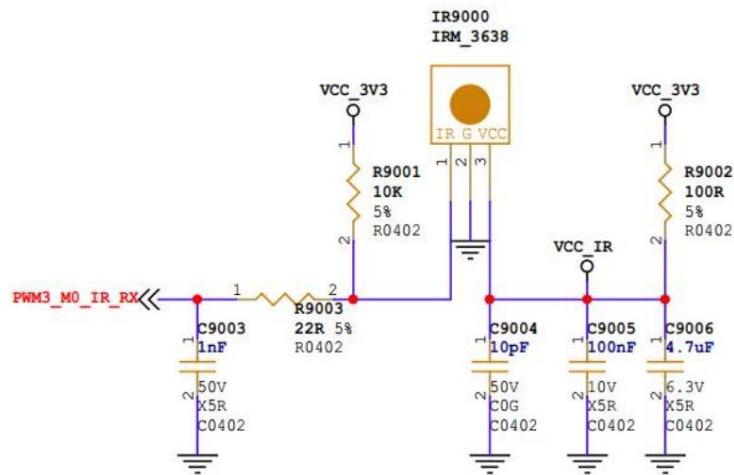


Figure 2-97 Infrared receiver circuit

When arranging the infrared receiver, it should be kept away from the wireless module antenna, such as the WIFI antenna, to avoid affecting the infrared when transmitting wireless data.

Signal reception:

The infrared receiver should be placed away from direct light from the LED light source on the board to prevent the LED flickering frequency from affecting infrared reception;

It is recommended that the IR signal be ground-enclosed throughout the entire process. If ground-enclosed processing is not possible, it is recommended that the distance between it and other signals be ≥ 2 times the line width.

2.3.13 RK3528 Unused Module Pin Processing

Please refer to the document "RK3528_Methods for Processing Unused Pins_V10".

3 PCB Design Recommendations

3.1 PCB stackup design

To minimize reflections during high-speed signal transmission, impedance matching must be maintained at the signal source, receiver, and transmission line. The specific impedance of a single-ended signal line depends on its trace width and position relative to the reference plane. The trace width and spacing between differential pairs required for specific impedances are determined by the selected PCB stackup. Because minimum trace width and spacing are determined by PCB type and cost constraints, the selected PCB stackup must meet all impedance requirements, including those on inner and outer layers, and for both single-ended and differential traces.

Layer definition design principles:

The layer adjacent to the main chip is the ground plane, providing a reference plane for device wiring; All signal layers are as close to the ground plane as possible; Avoid two signal layers being directly adjacent to each other; The main power supply is as close to its corresponding layer as possible; In principle, a symmetrical structure design should be adopted. The meaning of symmetry includes: dielectric layer thickness and type, copper foil thickness, pattern distribution type (large copper foil layer, circuit layer) symmetry.

PCB layer definition recommendation: When setting up specific PCB layers, you should flexibly follow the above principles and determine the appropriate layers based on actual needs.

When arranging layers, avoid mechanically following the established layout. The following are common layer layout recommendations for reference. When setting up layers, if there are adjacent routing layers, increase the spacing between them to reduce crosstalk. For cross-segment routing, ensure that critical signals have a relatively complete reference ground plane or provide necessary bridging measures.

RK3528 currently uses a 4-layer through-hole PCB stackup. The following stackup structure is used as an example to provide customers with guidance on stackup structure selection and evaluation.

If you choose another type of stackup structure, please recalculate the impedance according to the specifications given by the PCB manufacturer.

3.1.1 4-layer PTH board stackup

In the 4-layer PTH board stackup design, the reference plane of the top layer signal L1 is L2, and the reference plane of the bottom layer signal L4 is L3.

It is TOP-Gnd-Power-Bottom, and it is recommended to use 1oz for all.

The figure below shows the reference stackup and characteristic impedance line width for a 1.6mm thick board.

Layer No.	sig/pln	Copper thk. before process (oz)	Construction	Finished thikness (um)	Finished thikness (mil)	Tolerance	Dk (1GHz)
S/M							
1	TOP	1	PP 1080X1(RC68%)	18 35 81	0.71 1.38 3.19	+/-10 +/-10 +/-14	3.5 4.2
2	GND	1	Core	35 1300	1.38 51.18	+/-10 +/-30	4.5
3	POWER	1	PP 1080X1(RC68%)	81	3.19	+/-14	4.2
4	BOTTOM	1		35 18	1.38 0.71	+/-10 +/-10	3.5
S/M				总计：	1638	64.49	

Figure 3-1 6-layer PTH board stackup

层数	阻抗属性	线宽 mil	线距 mil	伴随地间距 mil	伴随地宽度 mil	铜厚(成品) OZ	要求阻抗 Ohm	参考层	计算值 Ohm	备注
L1/L4	特性	5				1	50	L2/L3	49.94	计算值 带绿油 55.28
L1/L4	差分	3.8	6			1	100	L2/L3	100.23	
L1/L4	差分	4	4			1	90	L2/L3	90.66	
L1/L4	差分	23		5	20	1	50	L3/L2	50.35	挖掉相邻层

Figure 3-2 6-layer PTH board impedance line reference value

3.1.2 RK3528 Fan-Out Design

þ Ball fan-out design of the outer three circles

The signal of the second circle can be routed out from the middle of the two balls with a 4mil line width.

It is recommended to set up a grid and route the wires from the middle of the two balls. Since part of the balls in the first circle are removed, 4 wires can be routed. The signal of the third circle is

Run a 4mil line between the two balls in the second circle, and then run the line out through the area where the ball positions are dug out in the first circle.

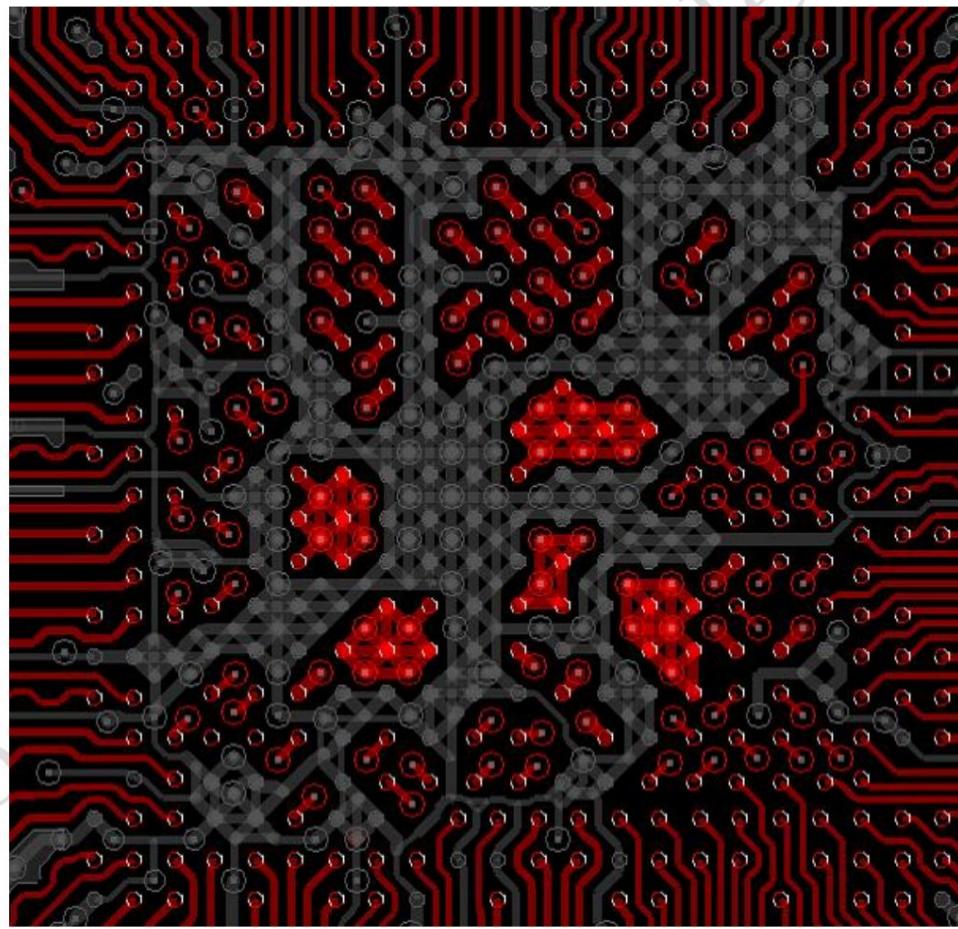


Figure 3-3 RK3528 fan-out diagram 1

Inner circle ball fan-out design

If the first, second, and third circle signals are all used, then starting from the fourth circle, you need to change layers to inner layers. Be sure to change the layer vias according to the rules and

It is recommended to place 2-4 rows of layer-changing vias at intervals, leaving one row empty without placing layer-changing vias, and leaving as large a channel as possible for the ground plane and the power plane.

As shown in the figure below, the ground plane has copper cladding, with multiple channels connected to the outside ground, which is beneficial to SI/PI and heat dissipation.

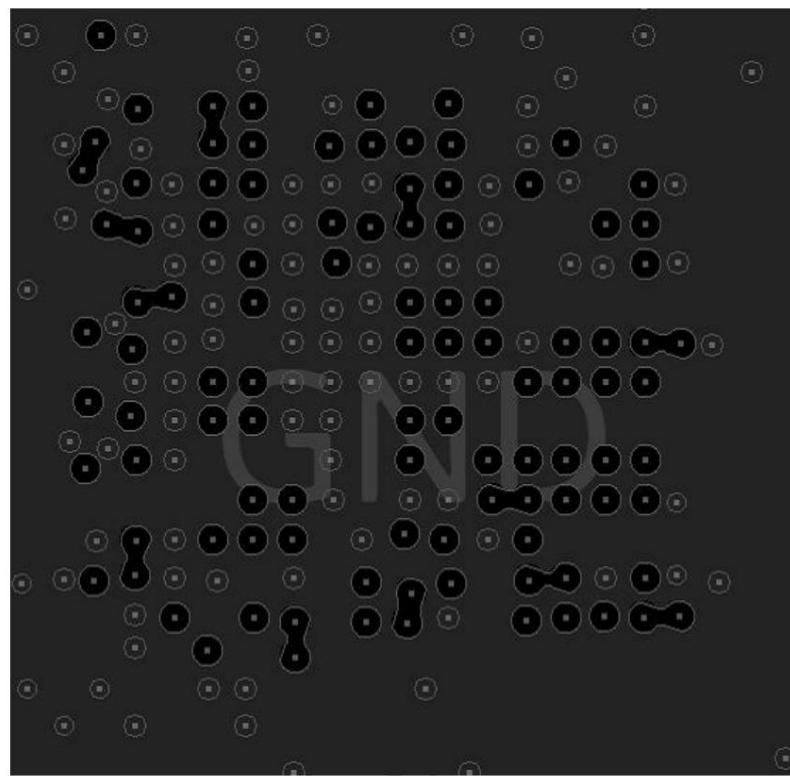


Figure 3-4 RK3528 fan-out diagram 2

As shown in the figure below, the copper coverage of the power layer is regular. The vias are placed in a regular manner to make the various power supplies have as large a copper coverage channel as possible, effectively improving the power supply.

Electricity quality.

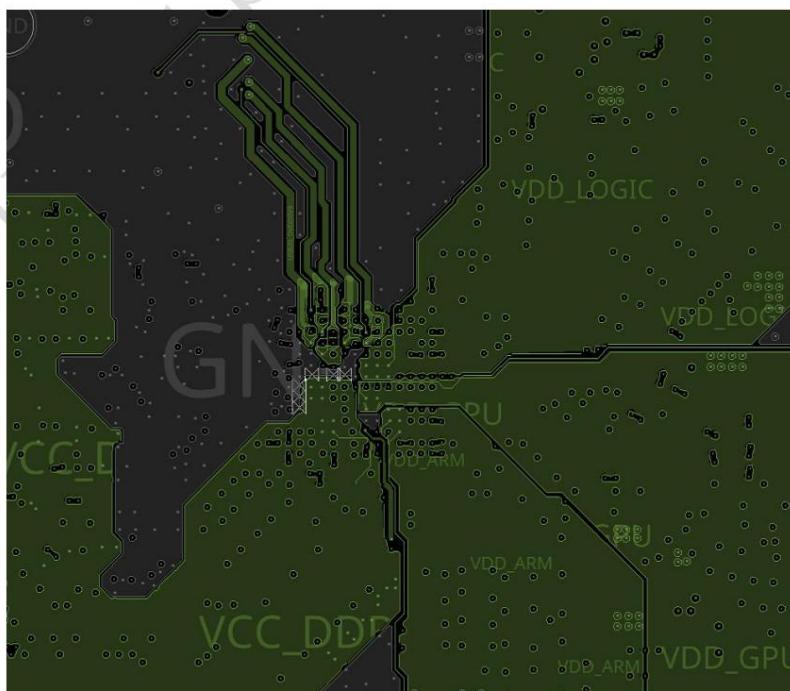


Figure 3-5 RK3528 fan-out diagram 3

As shown in the figure below, the bottom layer routing (the inner layer routing is similar), the layer-changing via is set according to the grid and placed in the middle of the ball.

The fan-out is 3.5mil wide.

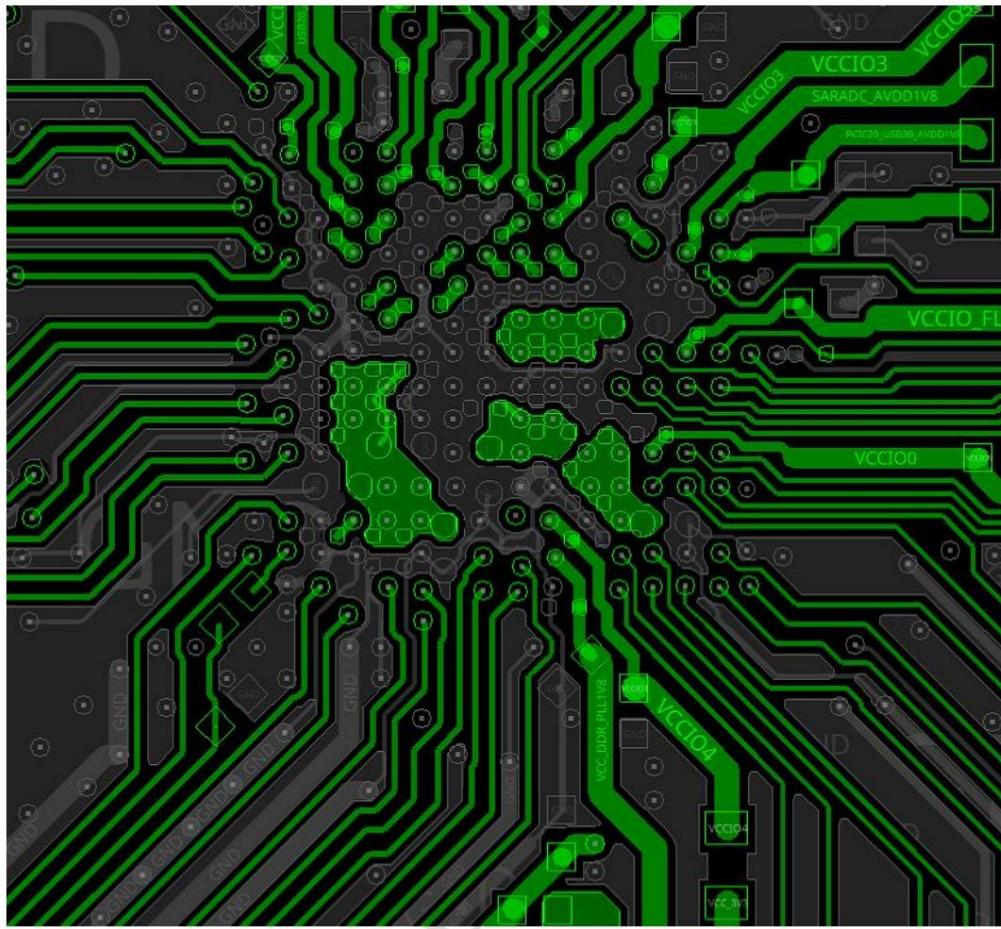


Figure 3-6 RK3528 fan-out diagram 4

3.2 General Wiring Recommendations

(1) The trace length should include vias and packages.

(2) The intra-differential pair delay difference refers to the delay difference between the two traces of the same differential signal pair; while the inter-differential pair delay difference refers to the delay difference between the two traces of different differential signals.

The signal spacing refers to the air spacing.

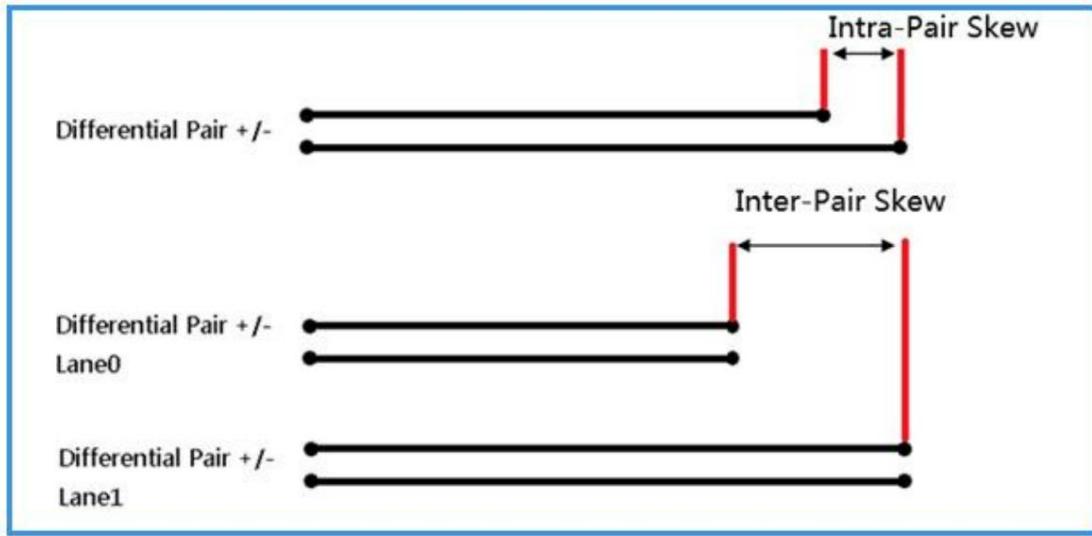


Figure 3-7 Diagram of differential pair delay difference

(3) High-speed signal routing should reference the GND plane, and the GND reference plane should be complete and continuous. The following designs should be avoided.

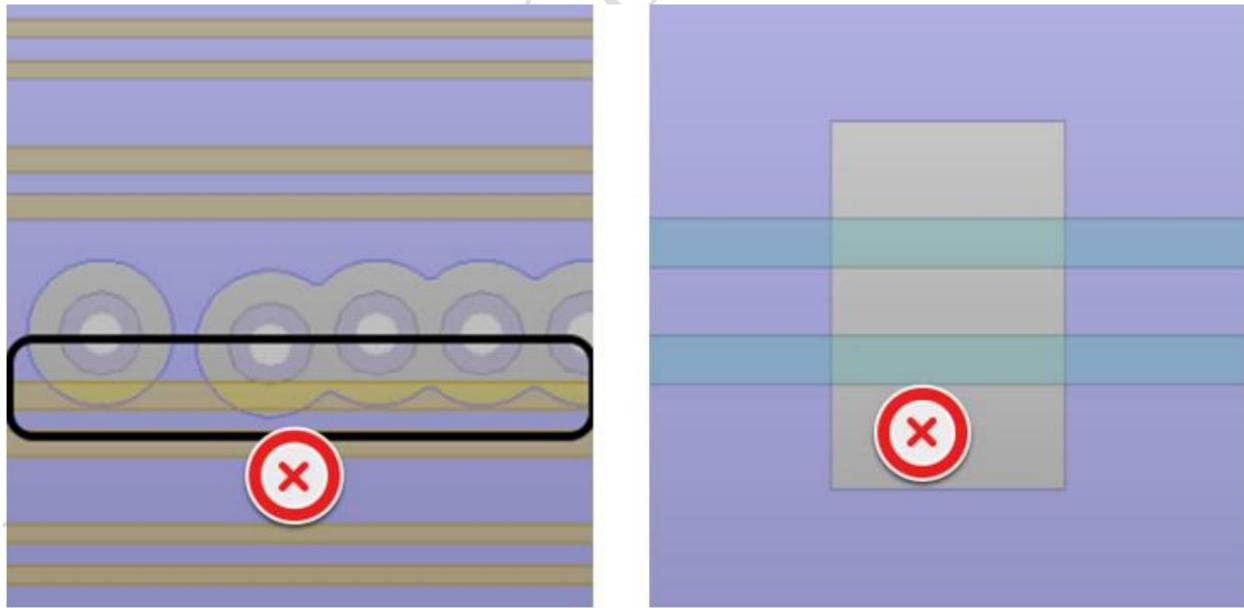


Figure 3-8 Schematic diagram of incomplete reference plane

(4) Since the solder pads of the surface mount device will cause the impedance to decrease, in order to reduce the impact of the impedance mutation, it is recommended to press the solder pad directly below the surface mount pad.

The common surface mount components include capacitors, ESD, common mode suppression inductors, connectors, etc.

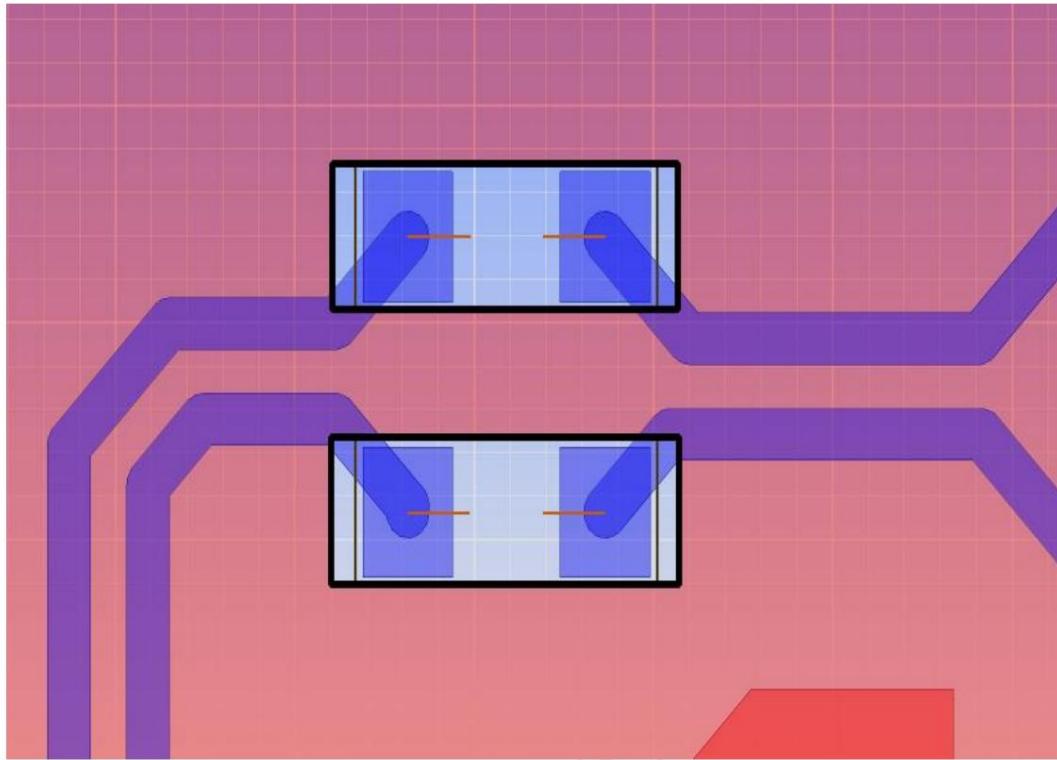


Figure 3-9 Schematic diagram of reference layer hollowing

(5) It is recommended that the routing distance from the ground copper sheet on the same layer be at least 3 times the line width.

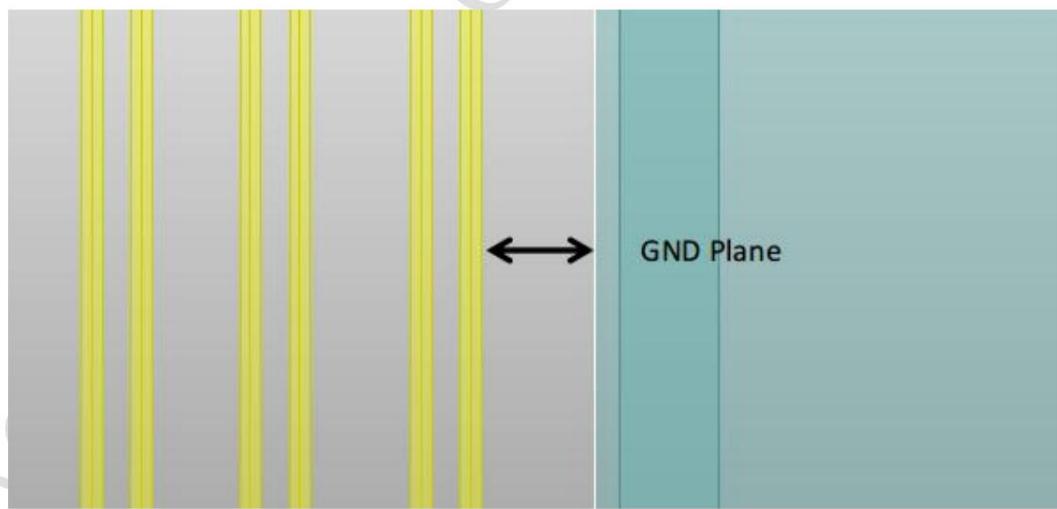


Figure 3-10 Schematic diagram of the distance between the trace and the ground copper foil on the same layer

(6) Avoid the via stub effect, especially when the stub length exceeds 12mil. It is recommended to evaluate the via stub effect on signal integrity through simulation.

impact.

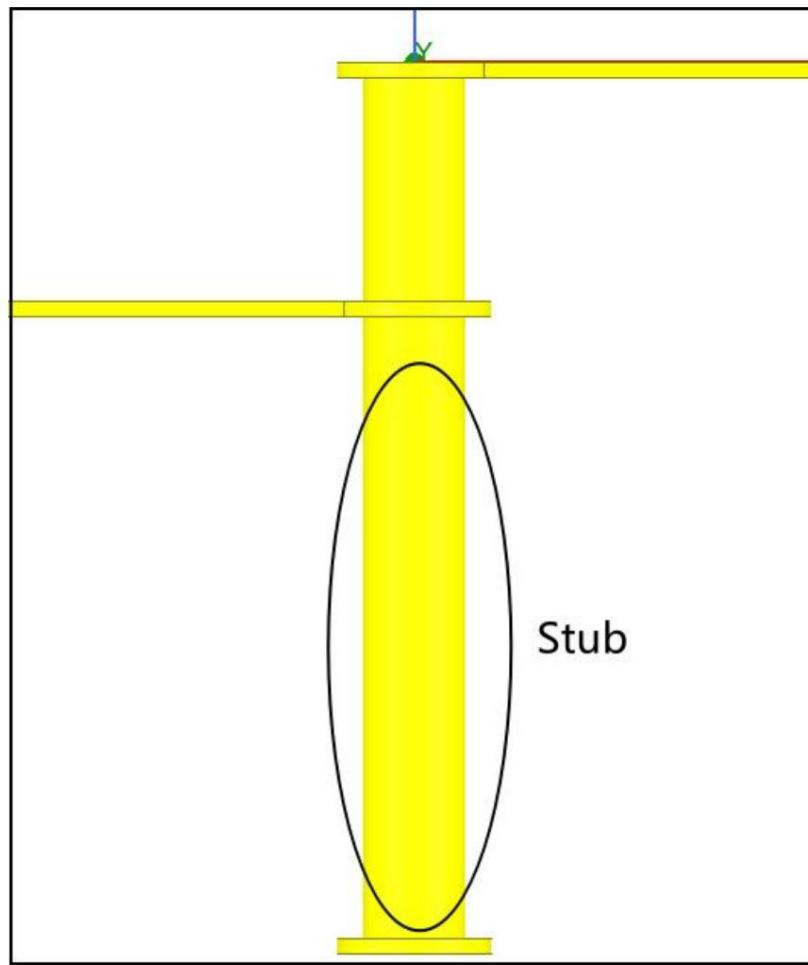


Figure 3-11 Schematic diagram of via tail pile

(7) Avoid high-speed signal cross-zone. It is recommended that high-speed signals be at least 40 mils away from the edge of the reference plane.

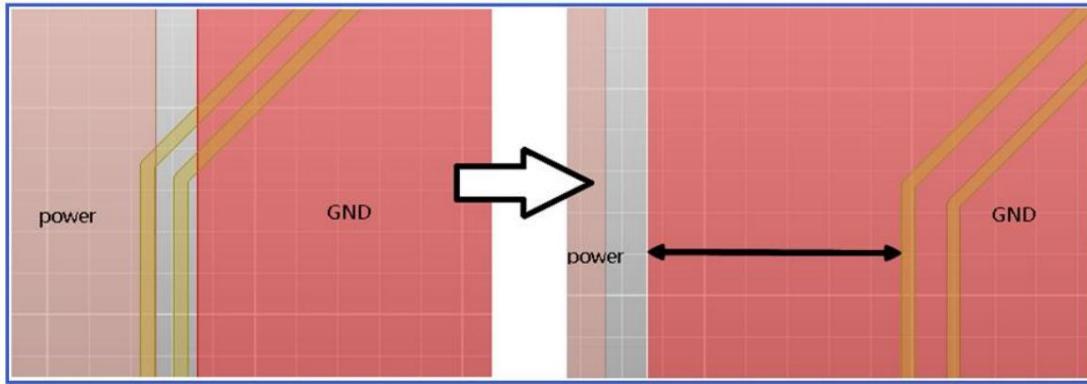


Figure 3-12 Cross-region diagram

(8) It is recommended not to place test points on high-speed signals.

(9) When routing, try to minimize corners. It is recommended to use 135 degrees instead of 90 degrees.

(10) Place the coupling capacitor as close to the connector as possible.

(11) The series resistor should be placed close to the sending device, such as the series resistor on the eMMC clock signal, which is recommended to be placed close to the CPU side.

(within 400 mil).

(12) It is recommended to drill a ground through hole on each ground pad of the IC (such as eMMC particles, FLASH particles, etc.).

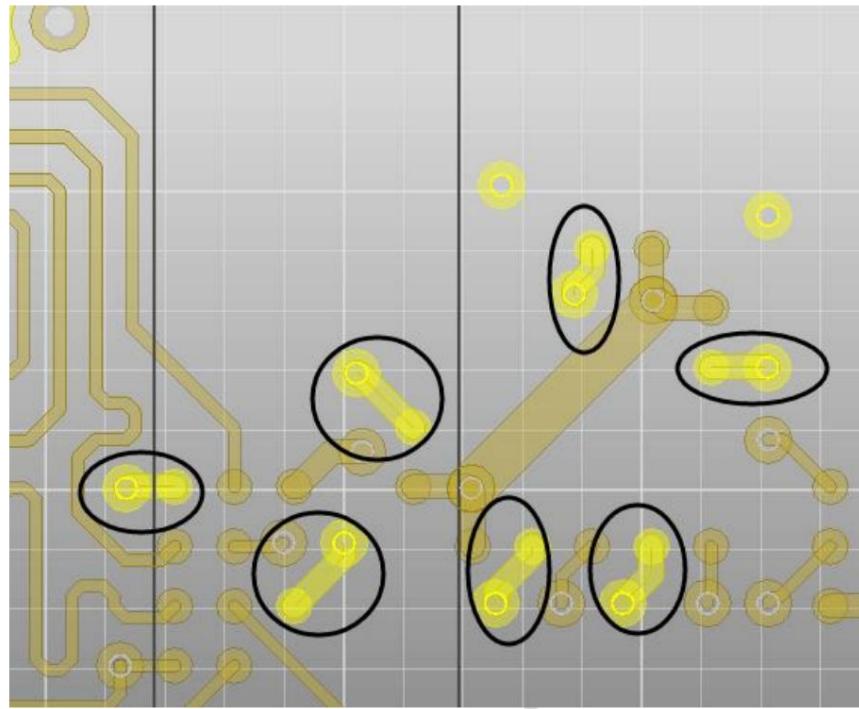


Figure 3-13 Schematic diagram of ground via

(13) Avoid placing circuits around clock devices (such as crystals, crystal oscillators, clock generators, clock distributors), switching power supplies, magnetic devices, etc.

Wire.

(14) Remove all non-functional pads.

(15) It is recommended that a ground through hole be drilled for each ground pad of the ESD device, and the through hole should be as close to the pad as possible.

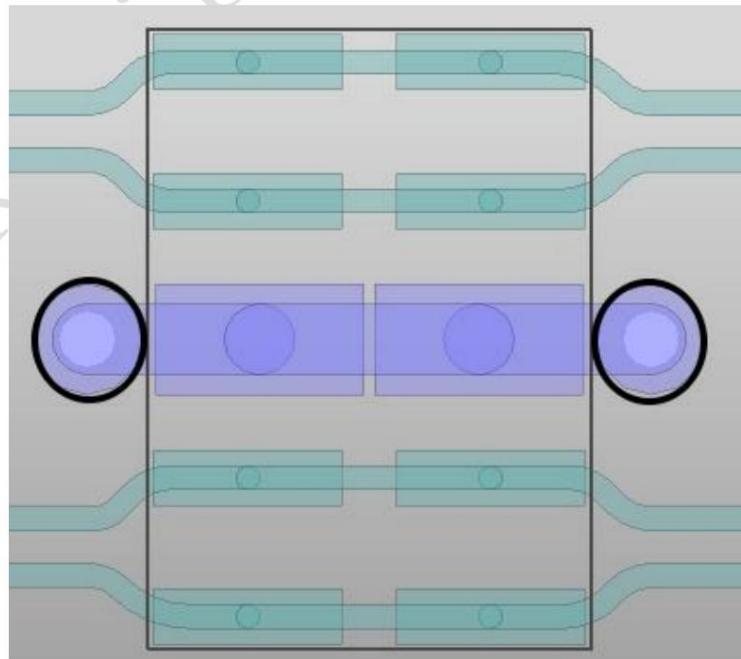


Figure 3-14 Schematic diagram of ESD device ground via

(16) Differential signals require equal length within the pair, that is, the delay difference between P and N should be as small as possible. Therefore, when there is a delay between the differential lines P and N

When there is a delay difference, compensate for it by winding the wires nearby. Pay special attention to the winding dimensions, which should meet the requirements shown in the figure below to reduce the impact of impedance changes.

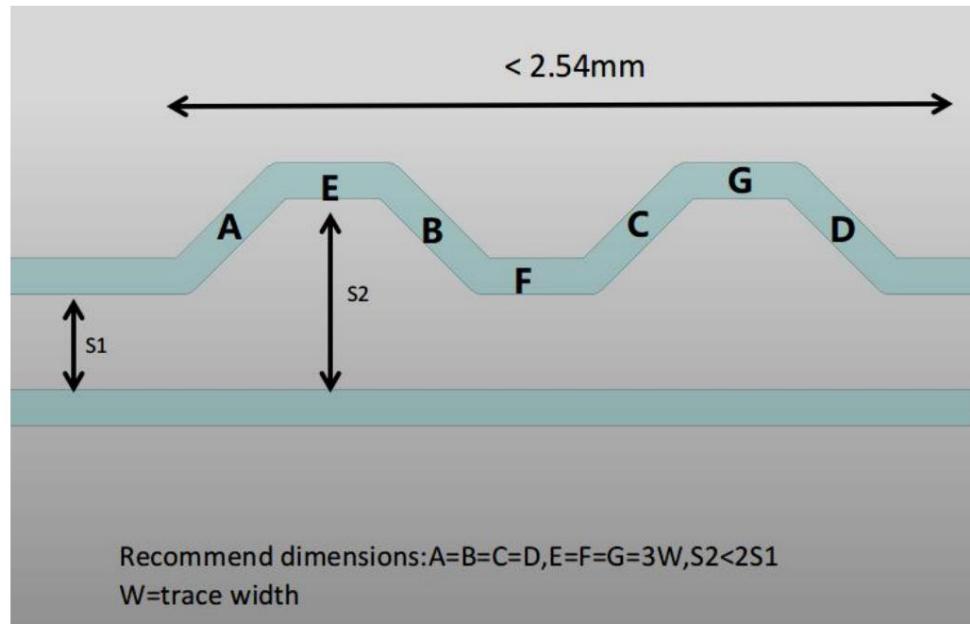


Figure 3-15 Winding compensation diagram

(17) If there is unequal length (within 300 mils) within the differential line pair, make winding compensation as soon as possible.

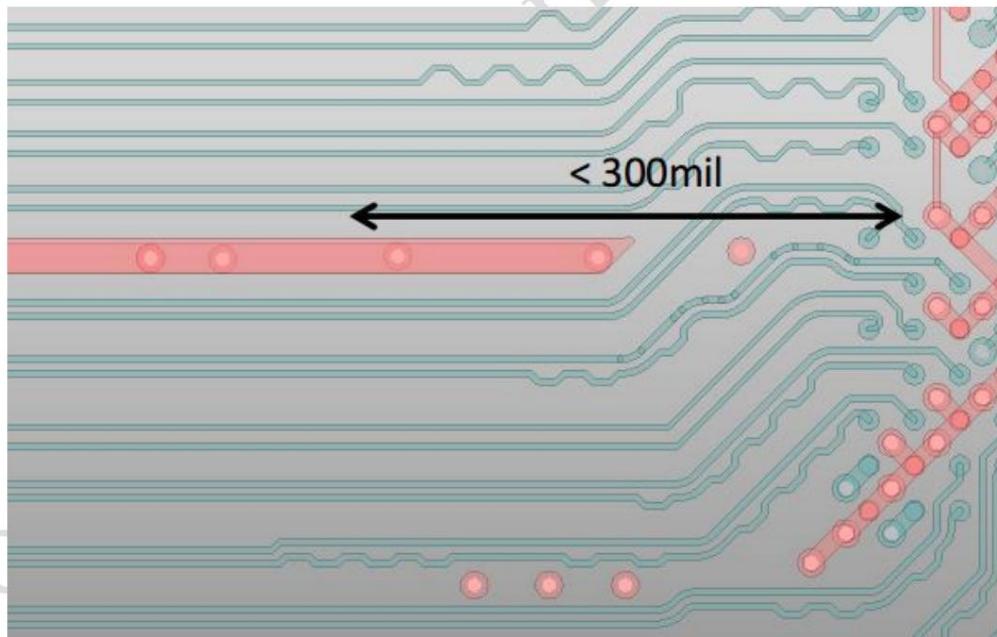


Figure 3-16 Diagram of winding compensation within a differential pair

(18) When the routing layer is changed and the reference layer before and after the layer change is the ground plane, a companion via needs to be placed next to the signal via to ensure the return flow.

Path continuity. For differential signals, signal vias and return vias should be placed symmetrically; for single-ended signals, it is recommended to place them next to the signal vias.

Place a return via to reduce crosstalk between vias.

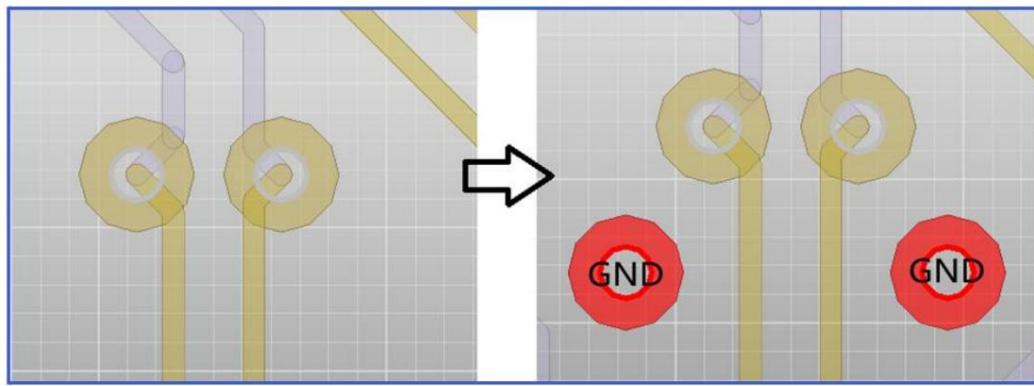


Figure 3-17 Schematic diagram of differential layer-switching vias

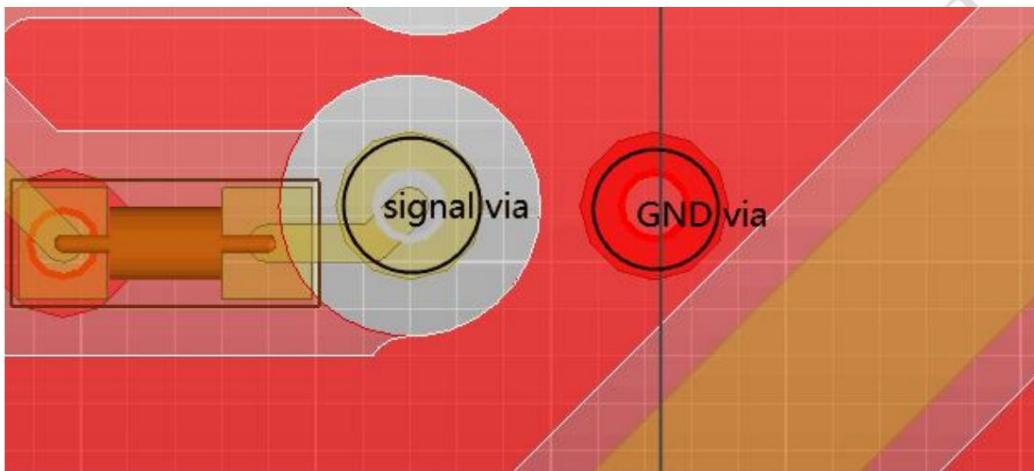


Figure 3-18 Schematic diagram of single-ended signal layer-changing via

(19) Differential corresponding symmetrical routing.

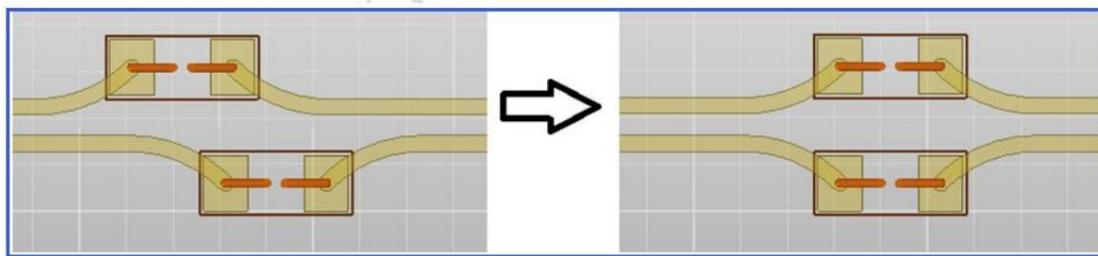


Figure 3-19 Symmetrical wiring diagram

ROCK

(20) It is recommended to drill at least one ground through hole on each ground pad of the high-speed connector, preferably two ground through holes, and the through holes should be as close as possible.

Solder pad.

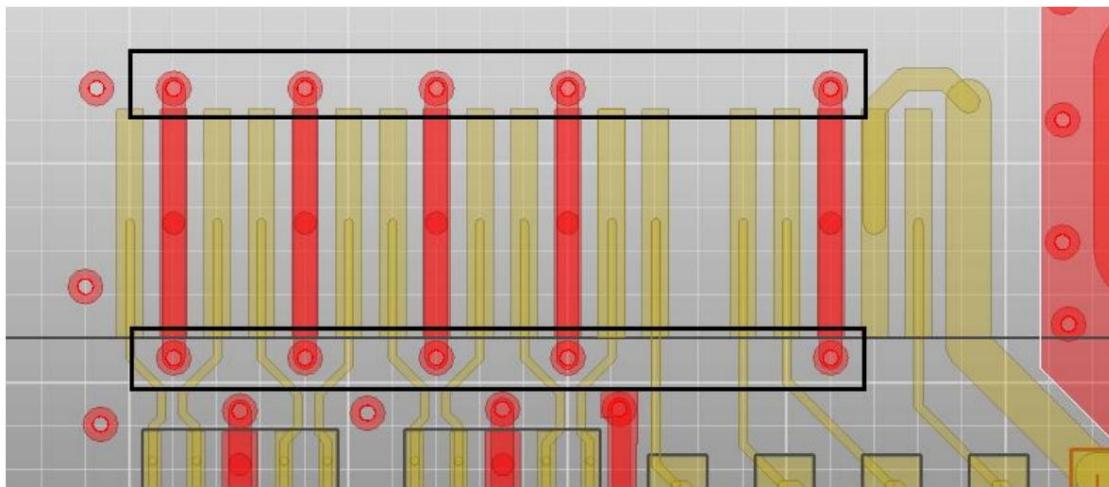


Figure 3-20 Schematic diagram of connector pad through hole

(21) When laying copper at the connector position, be careful not to let the ground copper cover exceed the ground pad.

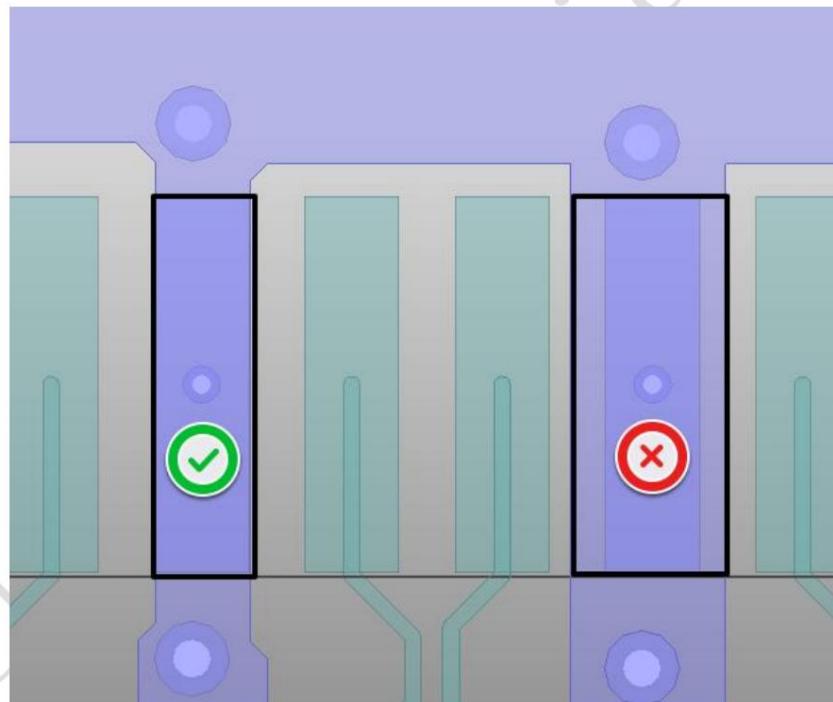


Figure 3-21 Schematic diagram of copper pad

(22) The distance between the connector's ground copper foil and the signal PAD must be at least 3 times the line width.

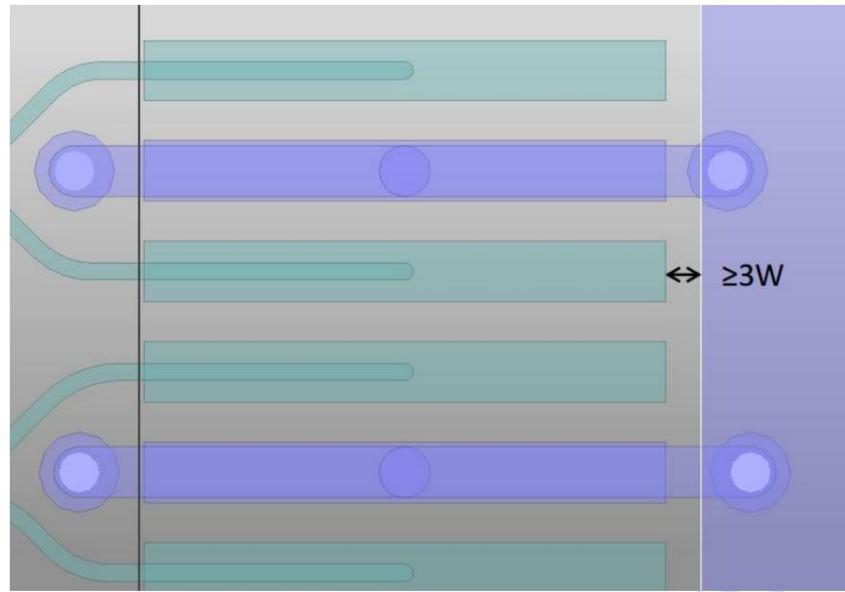


Figure 3-22 Schematic diagram of the connector ground copper

(23) It is recommended to use serpentine winding as shown in the figure below to reduce the crosstalk caused by winding.

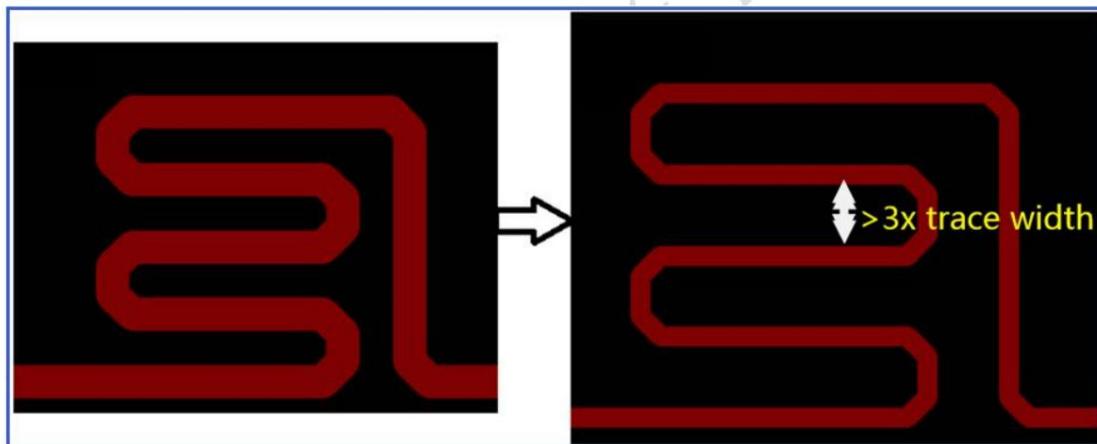


Figure 3-23 Schematic diagram of serpentine winding

(24) The length of the residual pile should be minimized. It is recommended that the residual pile length be zero.

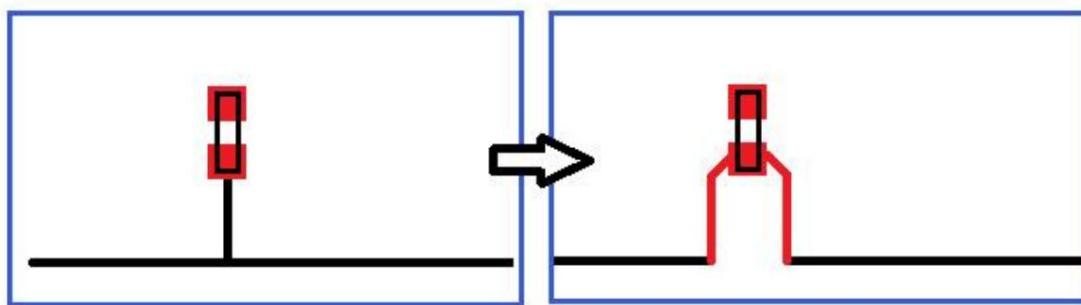


Figure 3-24 Schematic diagram of wiring piles

(25) When the reference plane of the routing crosses the power layer, it is recommended to add ground capacitors on the two power layers to improve the return path.

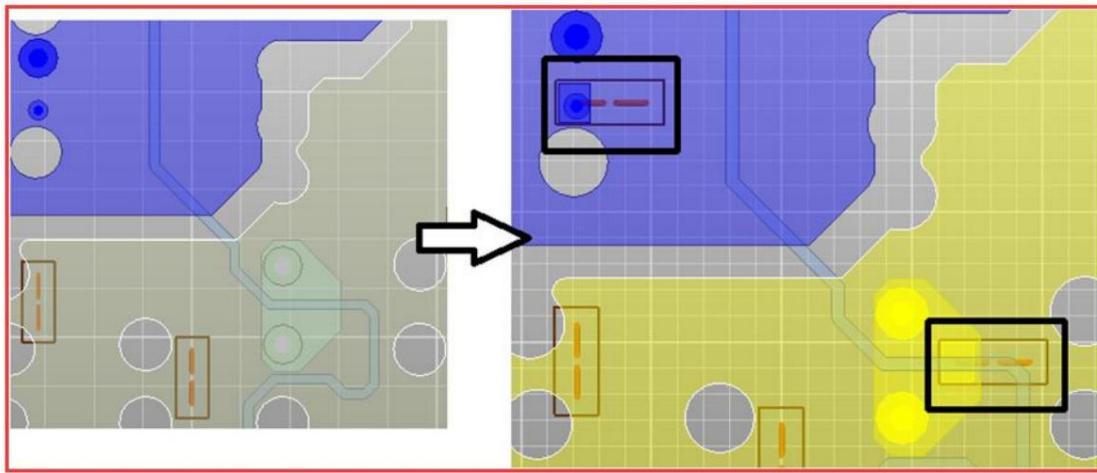


Figure 3-25 Schematic diagram of cross-power plane

(26) It is recommended that in the RK3528 BGA area, there should be one ground via for every 1.4 ground pads, and the ground vias should be connected to the ground pads.

Connect all ground planes together.

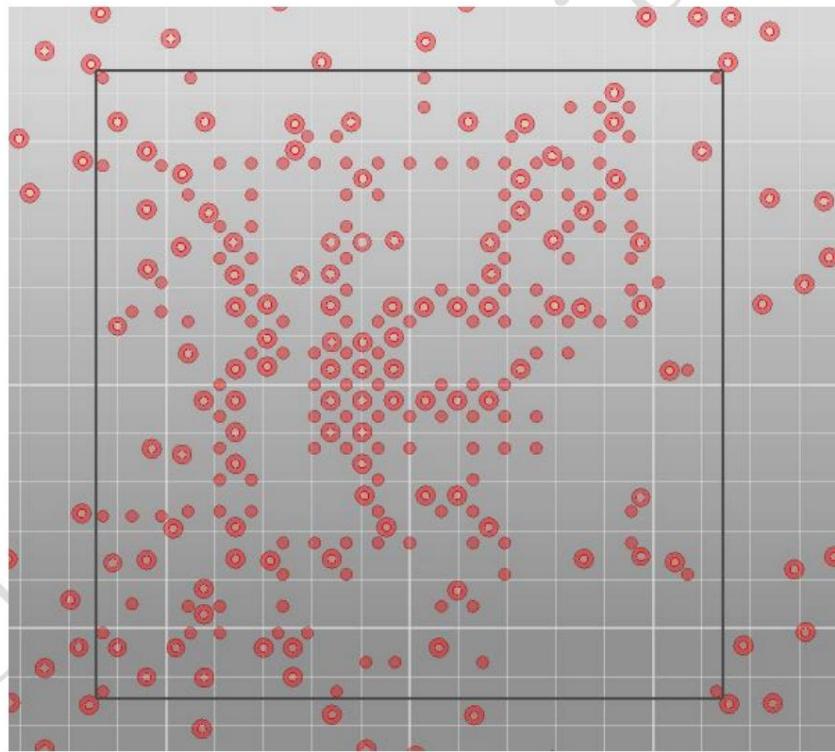


Figure 3-26 Schematic diagram of the number of GND vias at BGA

3.3 Interface PCB Design Recommendations

3.3.1 Clock/Reset Circuit PCB Design

In the PCB design of the clock circuit, please note:

ÿ The crystal circuit layout needs to be given priority. When laying out, it should be placed on the same layer as the chip and as close as possible to avoid drilling holes. The crystal routing

Keep it as short as possible, away from interference sources, and as far away from the edge of the board as possible;

ÿ The crystal and clock signals need to be grounded throughout. At least one GND via should be added every 200-300 mils, and the ground reference plane of the adjacent layer must be intact.

ÿ When laying out the crystal circuit, if it is placed on a different layer from the chip, the crystal routing and traces must be fully grounded to avoid interference. ÿ No traces are allowed on the clock traces XIN and XOUT, as well as in the area below the crystal, to prevent noise from coupling into the clock circuit. ÿ A ground ring can be placed around the top layer below the crystal. The ground ring is connected to the adjacent ground layer through vias to isolate noise. ÿ The second layer below the crystal maintains a complete ground reference plane, avoiding any trace splitting, which helps isolate noise and maintains the crystal output.

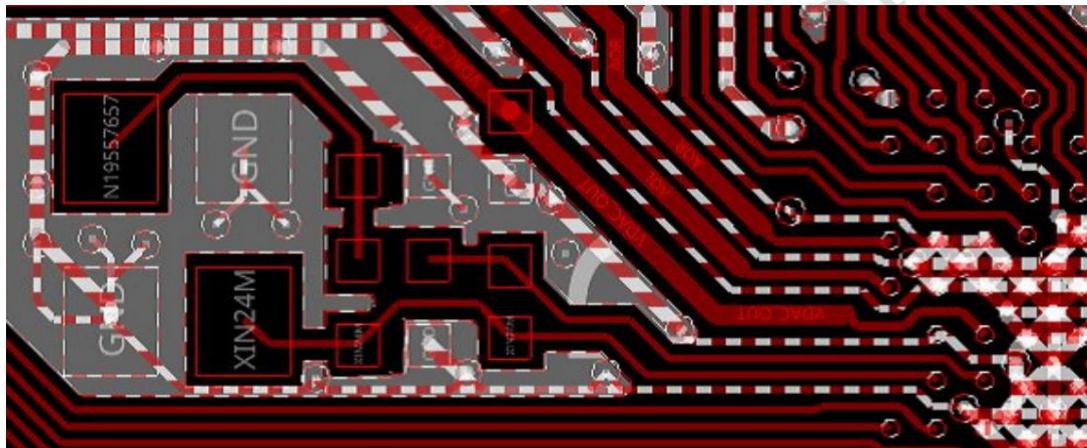


Figure 3-27 RK3528 crystal layout and routing

ÿ PMU_PLL_AVDD0V9, PMU_PLL_AVDD1V8, OSC_1V8 power supply decoupling capacitors must be placed on the chip pins

On the back side, when routing, try to make it pass through the capacitor pad first and then to the chip pin.

In the PCB design of the reset circuit, please note:

ÿ During layout, the RESETn reset signal should be kept away from the board edge and metal connectors to prevent abnormalities caused by ESD from causing reset mode.

Block freeze;

ÿ The RESETn filter capacitor should be placed as close to the chip pin as possible. The signal must pass through the capacitor before entering the chip. Pay attention to the filter capacitor.

The ground pad must have a 0402 ground via. If space permits, it is recommended to have two or more for better grounding.

ÿ The RESETn signal should be kept away from strong interference signals such as DCDC and RF to prevent interference. If the trace is long, it is recommended to wrap it with ground.

And add at least one GND via every 400mil of the ground wire;

ÿ The TVS protection diode of the RESETn button should be placed as close to the button as possible. The signal topology is: button ÿ TVS ÿ 100 ohm ÿ

Capacity (close to CPU) ÿCPU;

ÿ When ESD occurs, the ESD current must first be attenuated by the TVS device.

3.3.2 Power Circuit PCB Design

RK3528 uses a split power supply solution. From the perspective of power quality, the overall layout requires the BUCK to be as close to the RK3528 as possible. (When considering heat dissipation design, it needs to be placed appropriately, not too close nor too far away. A spacing of 20mm-50mm is recommended. Try not to place it at the edge of the board, as this is not conducive to heat dissipation.) When placing it, the routing (copper cover) from the BUCK output to the RK3528 needs to be smooth and avoid any crossing.

3.3.2.1 DC-DC PCB Design for Discrete Power Supplies

The input capacitor C_{IN} and the output capacitor C_{OUT} are placed between the V_{IN} pin, V_{OUT} pin and the GND of the DC/DC. Try to reduce the loop area between V_{IN} , V_{OUT} and the GND of the DC/DC. This can reduce the EMI amplitude of the power supply and greatly improve the stability of the DCDC circuit.

Below:

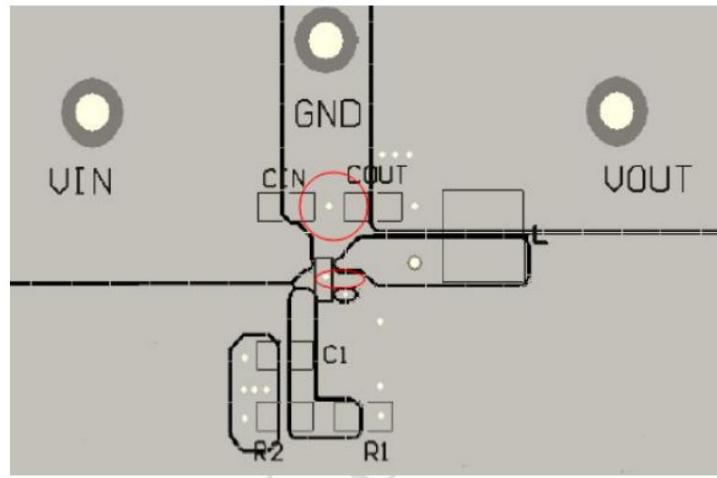


Figure 3-28 Discrete power supply DC/DC layout and routing

For the input capacitor C_{IN} , output capacitor C_{OUT} and DC/DC GND, try to make as many vias as possible. It is recommended to use more than 4 0503 vias.

If the V_{IN} and V_{OUT} power supplies change layers, it's recommended to drill more vias, preferably four or more 0503 vias (this is related to current flow, as described below). The inductor should be as close to the DC/DC as possible, with thick and short traces. The resistor ground at the FB terminal should be as far away from interference sources as possible.

3.3.2.2 DC-DC Power Supply Remote Feedback Design

The 100ohm feedback resistor needs to be placed close to the output capacitor, with one end of the resistor connected to the DC-DC output capacitor and the other end connected to the DC-DC The V_{OUT} feedback pin of the RK3528 is also connected to the farthest load in the same power network as the RK3528 power pin. The feedback line should be 4 mil wide and must be routed along with the power copper to avoid interference. The feedback line should be spaced at least 6 mils apart from other signals. For example, see the VDD_ARM power copper and feedback line routing diagram. Other power lines should be handled similarly.

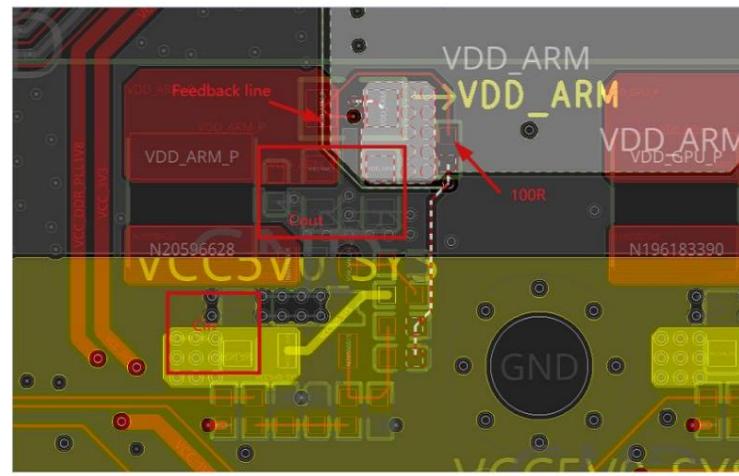


Figure 3-29 RK3528 chip VDD_ARM power remote feedback design

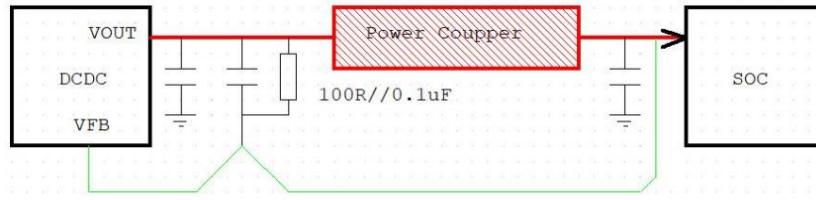


Figure 3-30 DC/DC remote feedback design diagram

3.3.2.3 RK3528 VDD_CPU Power Supply PCB Design

The copper width of VDD_CPU must meet the current requirements of the chip. The copper connected to the chip power pin is wide enough and the path cannot be blocked by vias.

The segmentation is too severe, and the effective line width must be calculated to confirm that the path connected to each power PIN of the CPU is sufficient.

When the VDD_CPU power supply is changed in the peripheral layer, it is necessary to make as many power vias as possible to reduce the voltage drop caused by

the layer change vias; it is recommended that each decoupling capacitor GND pin has \geq one GND via, and each power pin has \geq one power via.

For capacitors in 0805 packages, it is recommended to have two vias for each pin. The vias should be placed close to the pins, otherwise the decoupling effect will be affected.

For the power pin of RK3528 chip VDD_CPU, it is recommended to have \geq 5 power vias, and the top layer should be laid out in a "well" shape with cross connections. The recommended trace width is 10mil.



Figure 3-31 RK3528 chip VDD_CPU power pin routing and vias

The decoupling capacitors near the VDD_CPU power pin of RK3528 on the schematic diagram must be placed on the back of the corresponding power pins.

The capacitor should be as close to RK3528 as possible.

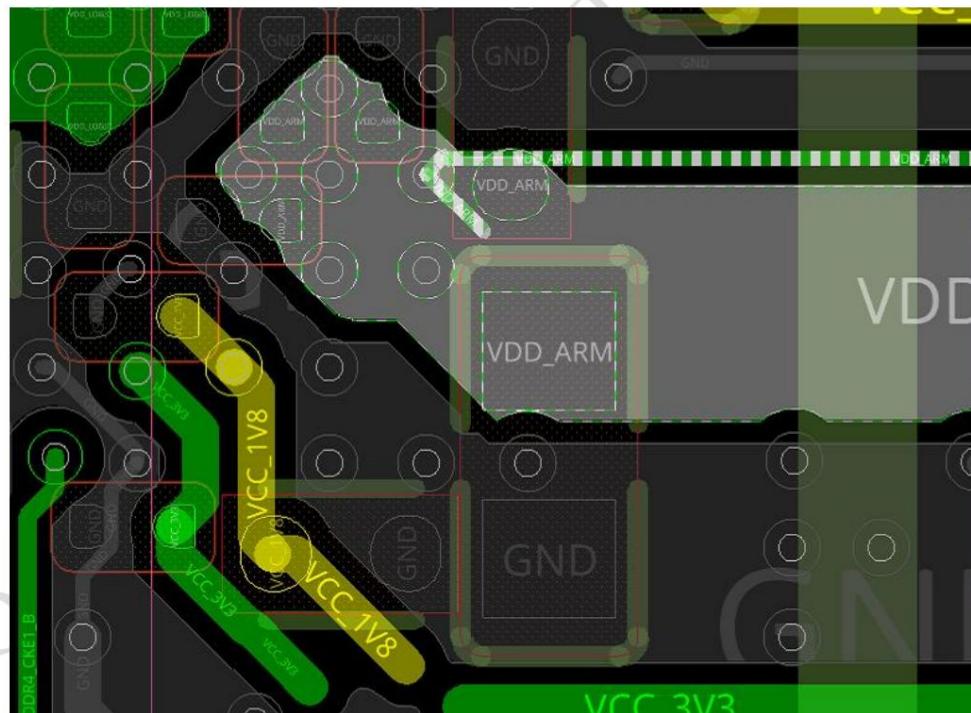


Figure 3-32 Decoupling capacitor placement on the back of the RK3528 chip VDD_CPU power pin

VDD_CPU current is relatively large, the effective overcurrent width needs to be \geq 60mil; the peripheral area width is recommended to be greater than 100mil. A power supply layer is required

The plane and the adjacent GND return plane, and the distance between the two planes is recommended to be less than 5mil. The role of the plane is to reduce the voltage drop on the one hand, and on the other hand

The plane capacitance between the power plane and the adjacent GND plane can effectively reduce the high-frequency PDN. It is recommended to use one ounce of copper for the power copper.

Helps reduce current density.

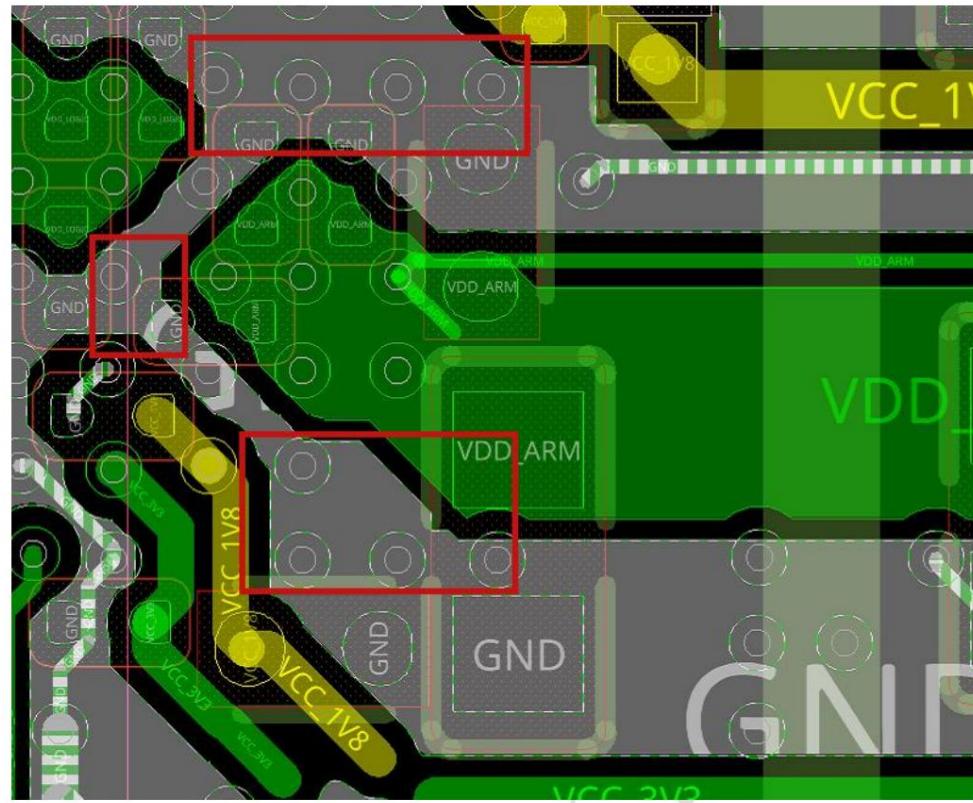


Figure 3-33 BIG power ground via placement diagram

(1) At the DCDC output, the number of 0503 vias on the power supply layer is recommended to be 6.

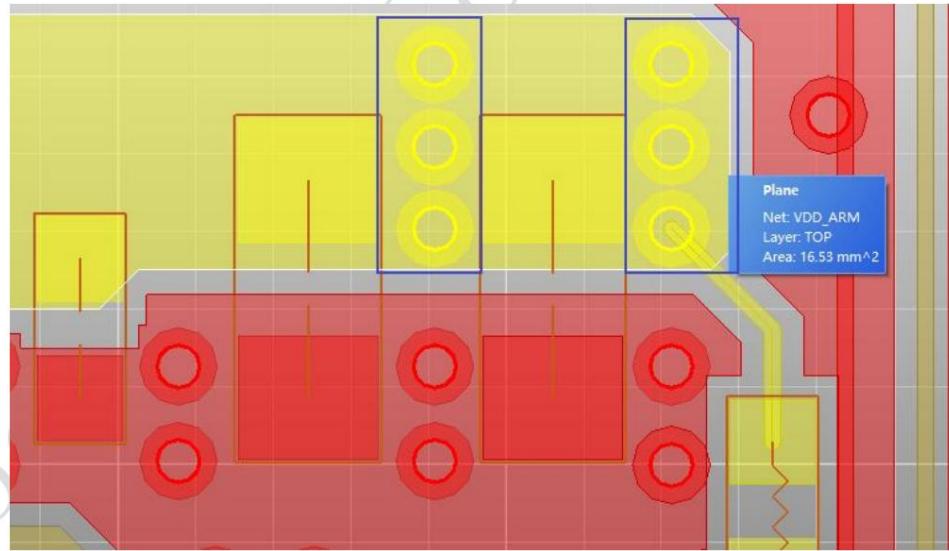


Figure 3-34 Diagram of the number of DCDC layer-changing vias

(2) For the decoupling capacitors at the DCDC, power supply, and GND pads, it is recommended to have two vias for each pad. Removing the capacitors is not recommended.

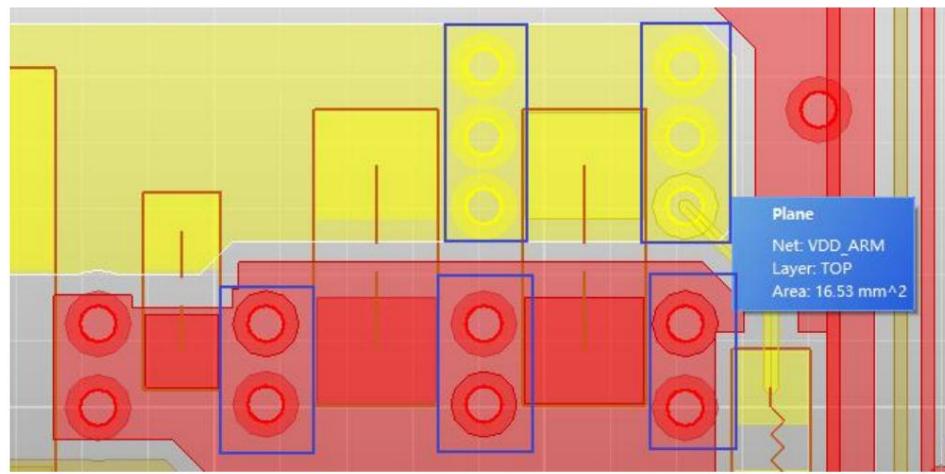


Figure 3-35 Schematic diagram of the number of decoupling capacitor vias

(3) The copper width from the DCDC to the bottom of the 3528 chip is recommended to be $\geq 200\text{mil}$. The DC resistance is recommended to be $\leq 5\text{ milliohms}$.



Figure 3-36 Schematic diagram of copper foil width

(4) The decoupling capacitors near the RK3528 power pins on the schematic diagram must be placed on the back of the corresponding power pins.

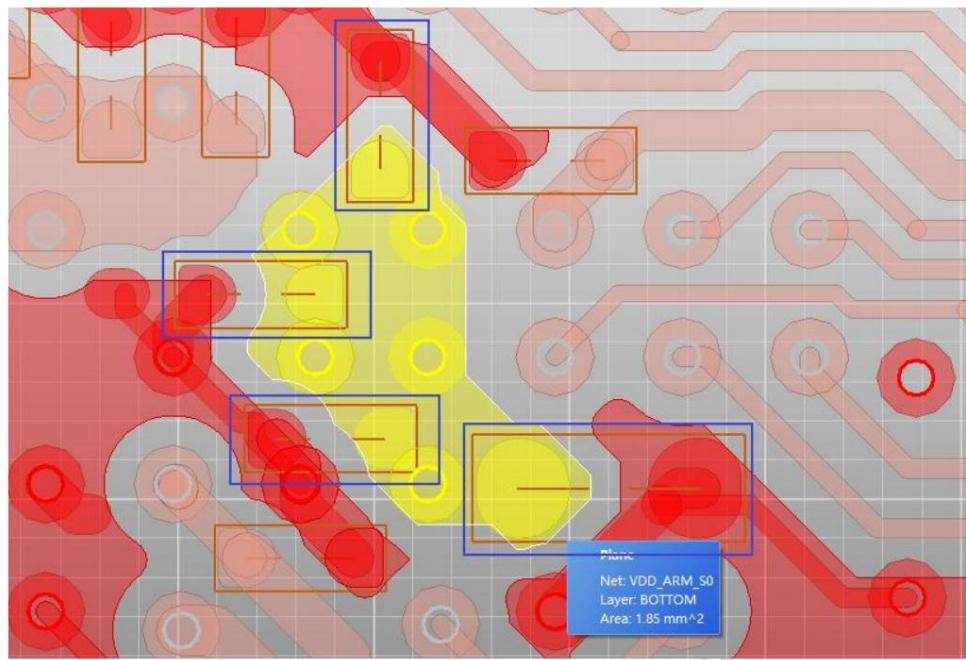


Figure 3-37 Capacitor quantity diagram

(5) The recommended number of power vias for the RK3528 power pins is 5.

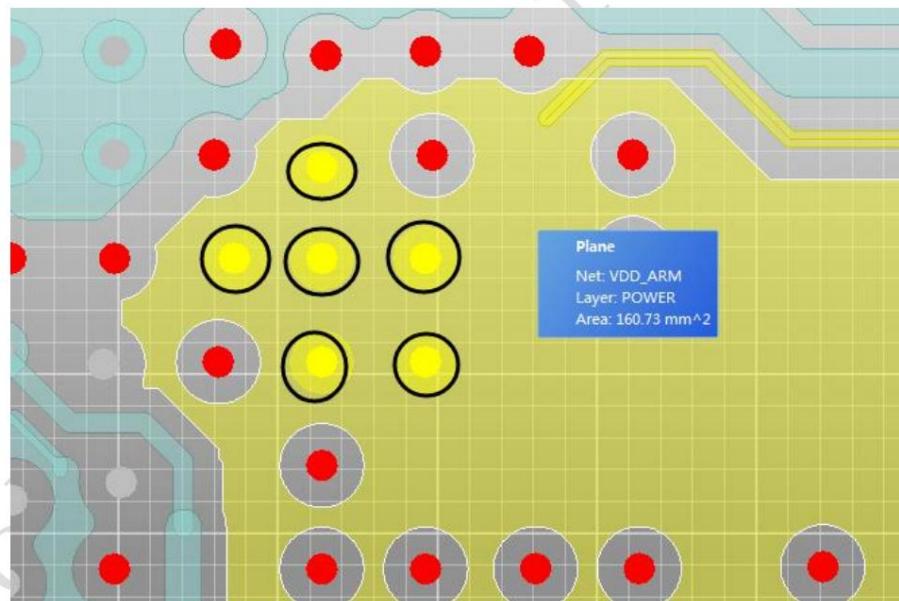


Figure 3-38 Schematic diagram of the number of power vias

(6) The number of GND vias within 40mil of the power pin (the distance between the center of the via) is required to be at least ≥ 4 , and ≥ 5 is recommended.

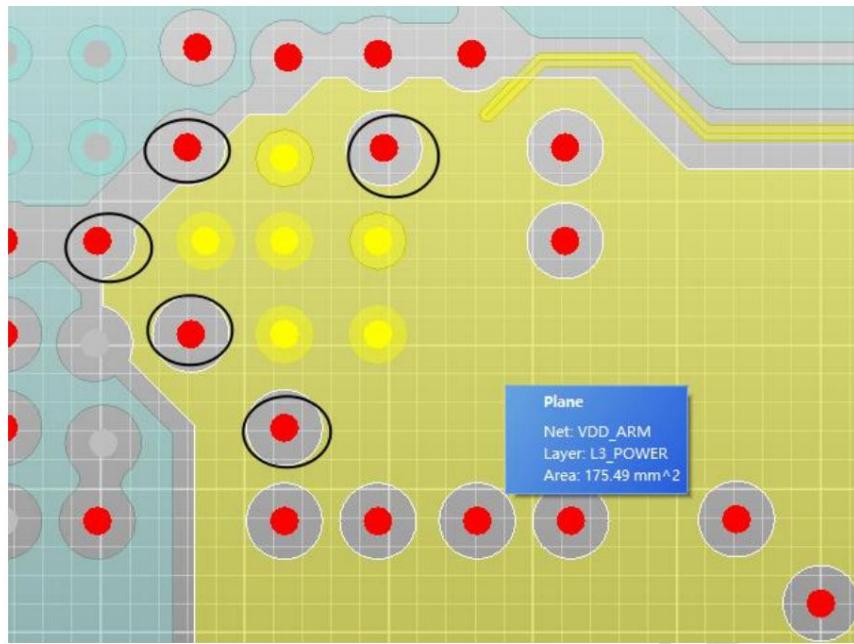


Figure 3-39 Schematic diagram of the number of GND vias within 40mil of the power pin

(7) The effective width of the copper foil under the RK3528 BGA is $\geq 55mil$



Figure 3-40 Schematic diagram of the copper foil under the BGA

(8) The recommended target impedance values for the VDD_ARM power supply PDN are as follows:

Table 3-1 Recommended target impedance values for the VDD_ARM power supply PDN

frequency	Impedance value (unit: ohm)
100Khz~1Mhz	≥ 0.03
1Mhz ~30Mhz	≥ 0.06
30Mhz~100Mhz	≥ 0.17

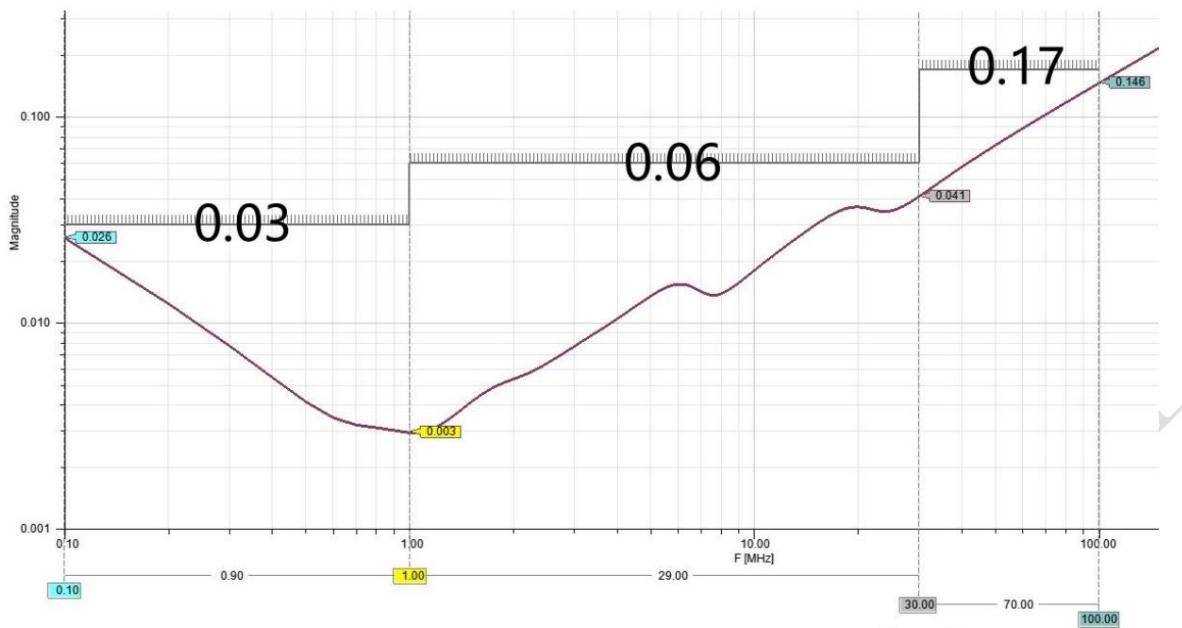


Figure 3-41 VDD_ARM power supply recommended PDN requirements

3.3.2.4 RK3528 VDD_LOGIC&VDD_GPU Power Supply PCB Design

The copper width of VDD_LOGIC must meet the current requirements of the chip. The copper connected to the chip power pin is wide enough and the path cannot be blocked by vias.

The segmentation is too severe, and the effective line width must be calculated to confirm that the path connected to each power PIN of the CPU is sufficient.

When the VDD_LOGIC power supply is changed on the periphery, it is necessary to make as many power vias as possible to reduce the voltage drop caused by the layer change vias; it is recommended that each decoupling capacitor GND pin has \geq one GND via, and each power pin has \geq one power via.

For capacitors in 0805 packages, it is recommended to have two vias for each pin. The vias should be placed close to the pins, otherwise the decoupling effect will be affected.

For the power pin of RK3528 chip VDD_LOGIC, it is recommended to have ≥ 6 power vias, and the top layer should be in a "well" shape with cross connections.

The recommended trace width is 10 mil.

RK3528 VDD_GPU and VDD_LOGIC PCB are combined for power supply.

The VDD_GPU copper width must meet the current requirements of the chip. The copper connected to the chip power pin is wide enough, and the path cannot be too severely divided by vias. The effective line width must be calculated to confirm that the path connected to each power PIN of the CPU is sufficient.

It is recommended that each decoupling capacitor GND pin has \geq one GND via, and each power pin has \geq one power via.

For capacitors in 0805 packages, it is recommended to have two vias for each pin. The vias should be placed close to the pins, otherwise the decoupling effect will be affected.

For the power pin of RK3528 chip VDD_GPU, it is recommended to have ≥ 4 power vias, and to use a "well" shape on the top layer for cross connection. The recommended trace width is 10mil.

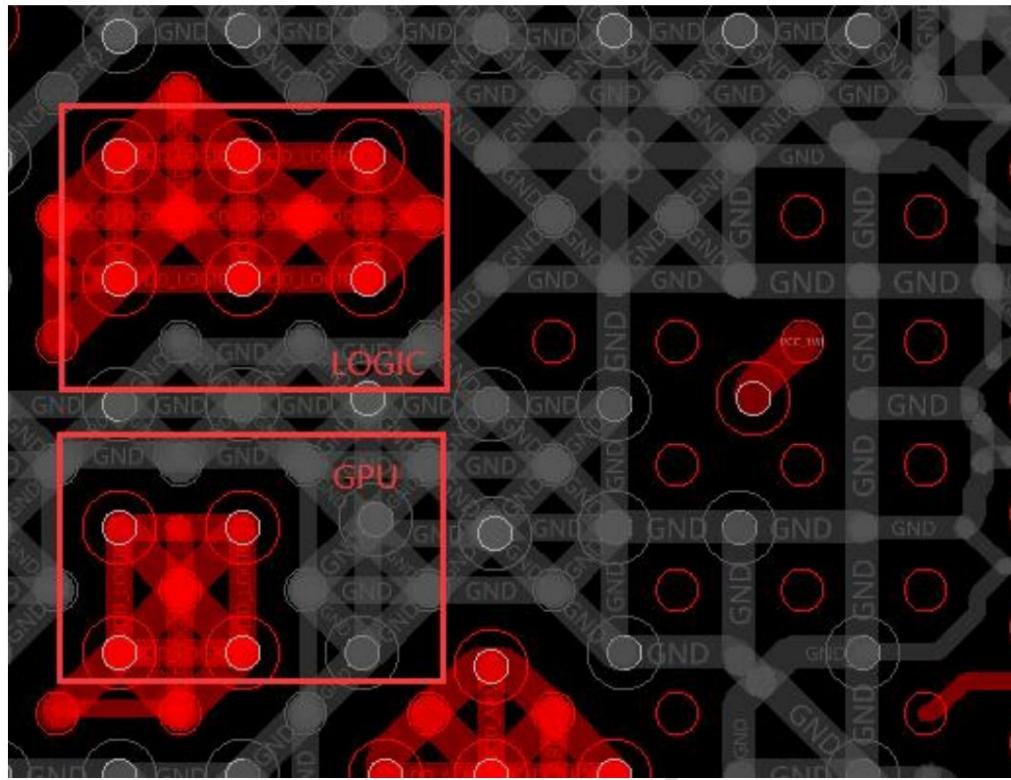


Figure 3-42 RK3528 chip VDD_LOGIC & VDD_GPU power pin routing and vias

The decoupling capacitors near the VDD_LOGIC power pin of RK3528 on the schematic diagram must be placed on the back of the corresponding power pins, and the rest of the decoupling capacitors must be placed on the back of the corresponding power pins.

The coupling capacitor should be as close to RK3528 as possible.

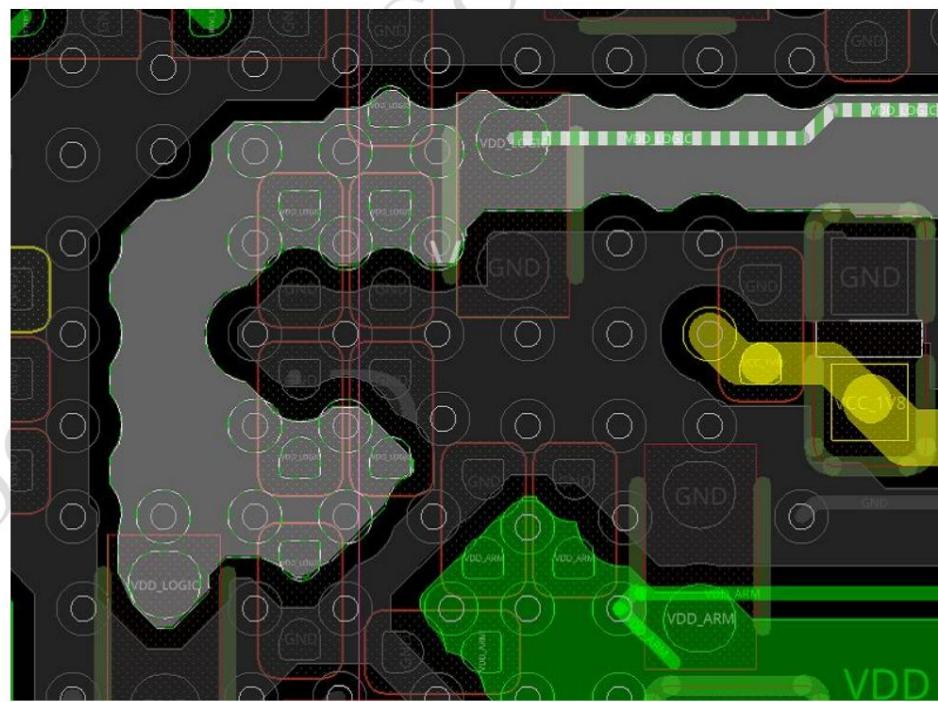


Figure 3-43 Decoupling capacitor placement on the back of the RK3528 chip VDD_LOGIC & VDD_GPU power pins

VDD_LOGIC current is relatively large, the effective overcurrent width needs to be ≥30mil; the peripheral area width is recommended to be greater than 100mil.

The source plane and the adjacent GND return plane are connected, and the distance between the two planes is recommended to be less than 5mil. The plane can reduce the voltage drop and

On the one hand, the plane capacitance between the power plane and the adjacent layer GND plane can effectively reduce the high-frequency PDN. It is recommended to use one ounce of copper for the power copper.

skin, which helps to reduce the current density.

In the CPU area, the number of GND vias within the 40mil range (via center to via center spacing) of the LOGIC power vias is recommended to be ≥12.

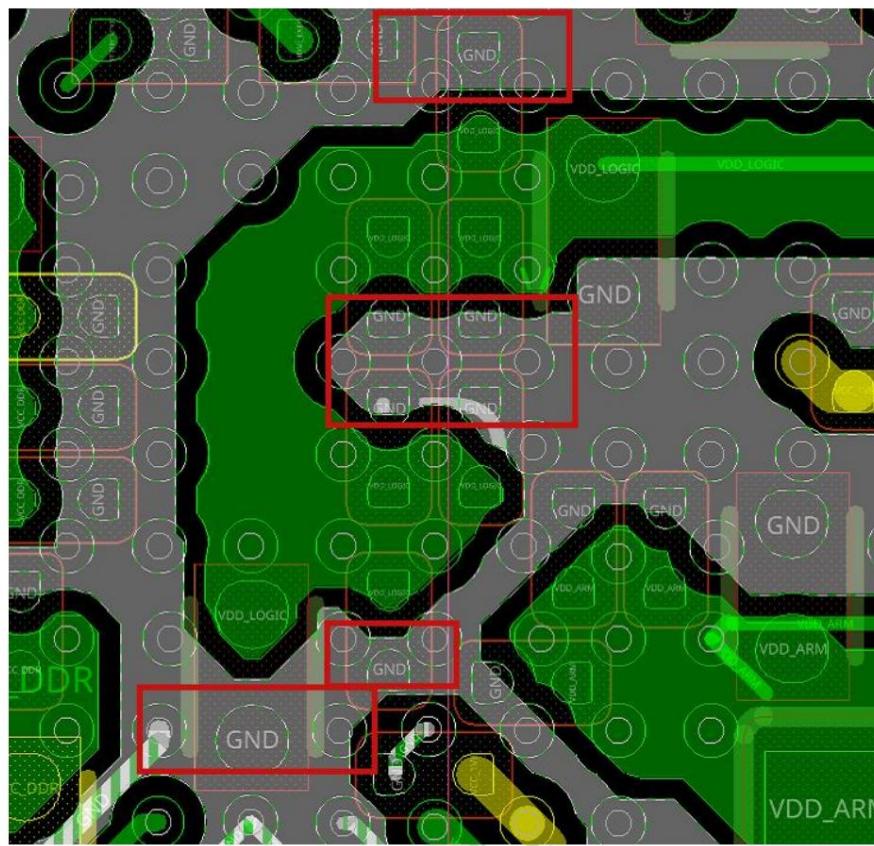


Figure 3-44 RK3528 chip VDD_LOGIC & VDD_GPU power ground via placement diagram

(1) In order to reduce costs, VDD_GPU and VDD_LOGIC power supplies are combined. At the DCDC output, the power supply is switched to 0503.

The recommended number of vias is ≥ 6.

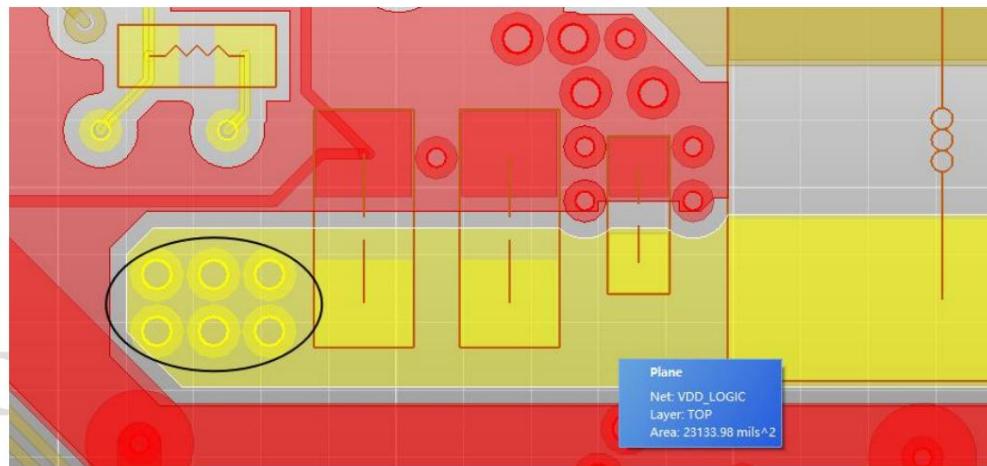


Figure 3-45 Diagram of the number of DCDC layer-changing vias

(2) For the decoupling capacitors at the DCDC, power supply, and GND pads, it is recommended to have two vias for each pad. Removing the capacitors is not recommended.

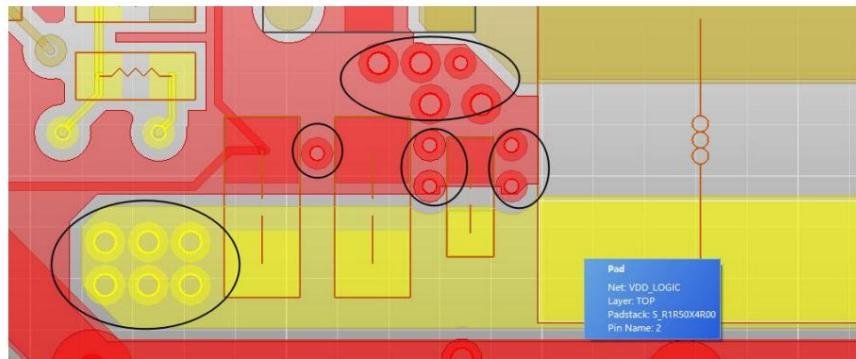


Figure 3-46 Schematic diagram of the number of decoupling capacitor vias

(3) The copper width from the DCDC to the bottom of the 3528 chip is recommended to be $\geq 200\text{mil}$. The DC resistance is recommended to be $\leq 5\text{ milliohms}$.



Figure 3-47 Schematic diagram of copper width

(4) The decoupling capacitors near the RK3528 power pins on the schematic diagram must be placed on the back of the corresponding power pins.

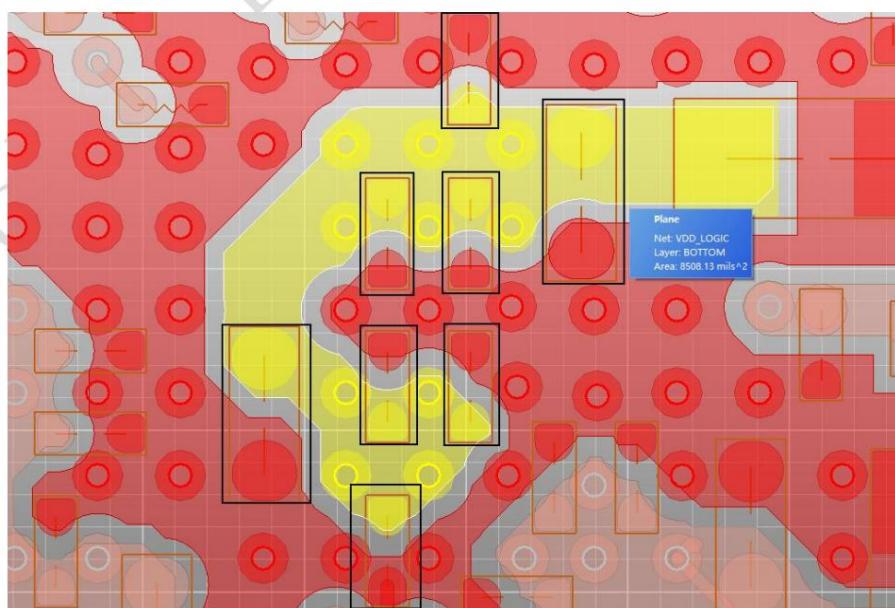


Figure 3-48 Schematic diagram of capacitor quantity

(5) The number of power vias required for the RK3528 power pins must be ≥ 10.

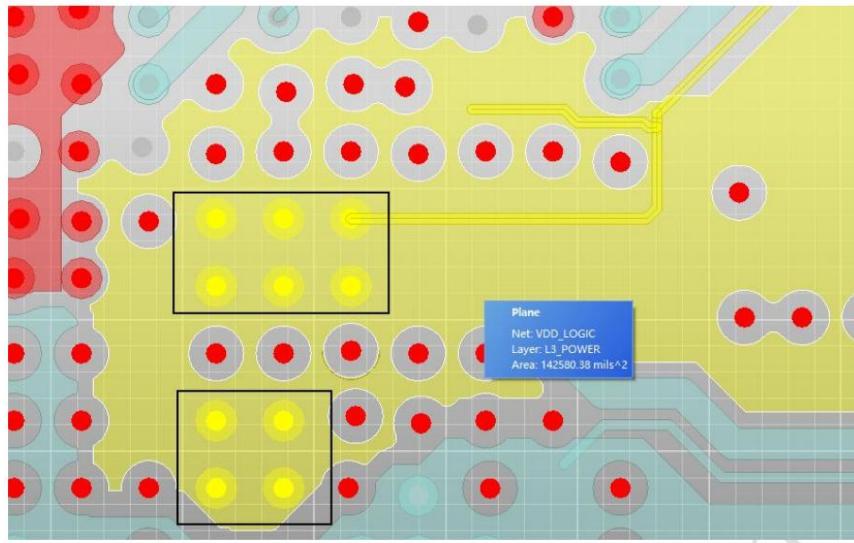


Figure 3-49 Schematic diagram of the number of power vias

(6) The number of GND vias within 40mil of the power pin must be ≥9.

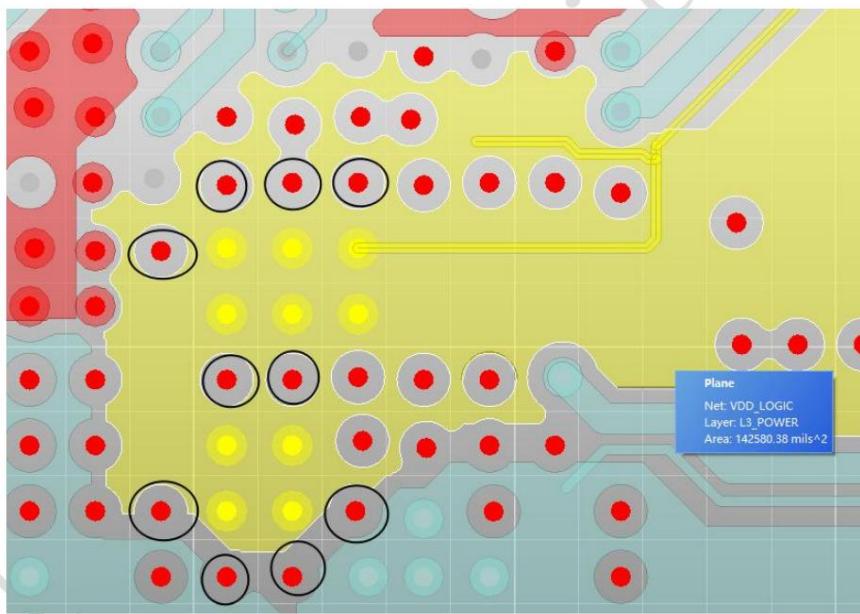


Figure 3-50 Diagram of the number of GND vias within 40mil of the power pin

(7) The effective width of the copper foil under the RK3528 BGA is ≥ 55mil

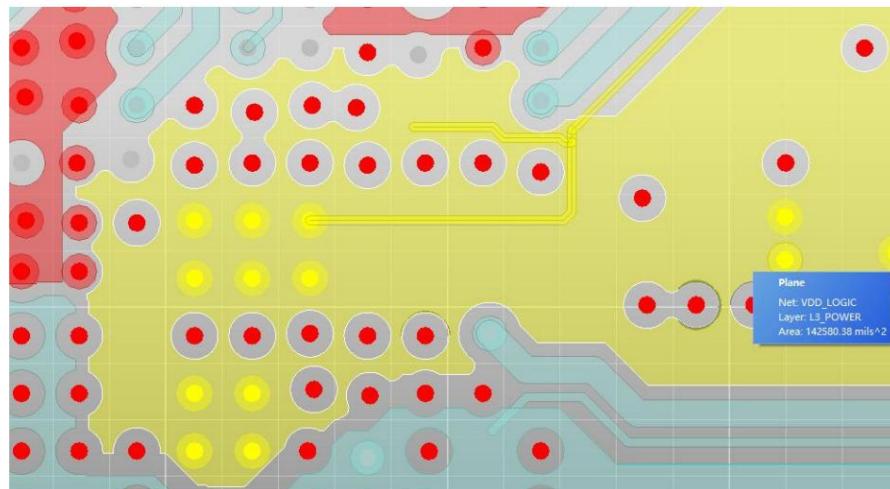


Figure 3-51 Schematic diagram of the copper foil under the BGA

(8) The recommended target impedance values for the combined VDD_GPU and VDD_LOGIC power supply PDN are as follows:

Table 3-2 Recommended target impedance values for the combined VDD_GPU and VDD_LOGIC power supply PDN

frequency	Impedance value (unit: ohm)
100Khz~1Mhz	≤ 0.03
1Mhz ~30Mhz	≤ 0.035
30Mhz~100Mhz	≤ 0.085

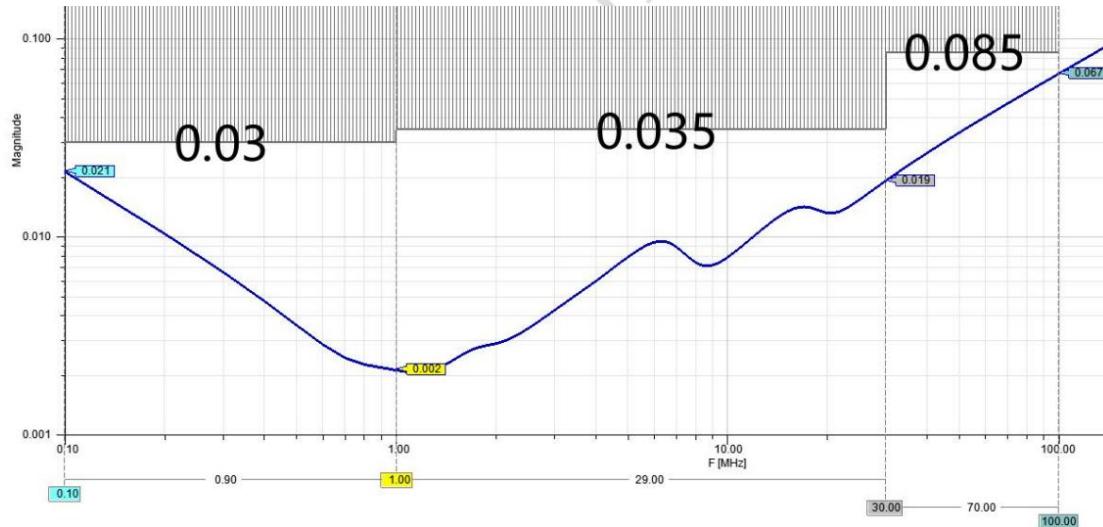


Figure 3-52 Recommended PDN requirements for the combined power supply of VDD_GPU and VDD_LOGIC

3.3.2.5 RK3528 VCC_DDR Power Supply PCB Design

The copper width of VCC_DDR must meet the current requirements of the chip. The copper connected to the chip power pin is wide enough and the path cannot be blocked by vias.

The segmentation is too severe, and the effective line width must be calculated to confirm that the path connected to each power PIN of the CPU is sufficient.

When the VCC_DDR power supply is switched at the periphery, as many power vias as possible should be drilled to reduce the voltage drop caused by the vias during the layer switching.

It is recommended that each decoupling capacitor GND pin has ≥ 1 GND via, and each power pin has ≥ 1 power via.

For capacitors in 0805 packages, it is recommended to have two vias for each pin. The vias should be placed close to the pins, otherwise the decoupling effect will be affected.

For the power pins of RK3528 chip VCC_DDR, it is recommended to have ≥ 8 power vias, and to have a "well" shape on the top layer, cross-connected, and build

The recommended trace width is 10mil.

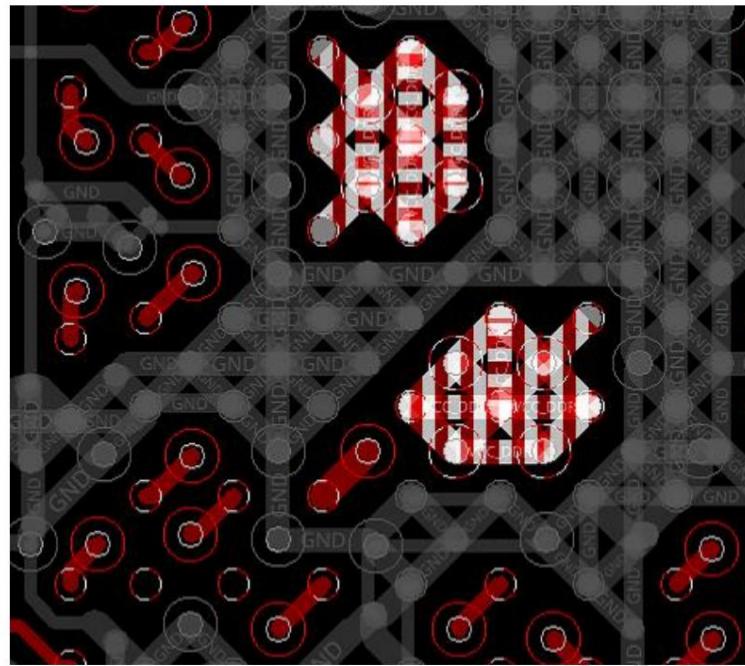


Figure 3-53 RK3528 chip VCC_DDR power pin routing and vias

The decoupling capacitors near the VCC_DDR power pin of RK3528 on the schematic diagram must be placed on the back of the corresponding power pins.

The capacitor should be as close to RK3528 as possible.

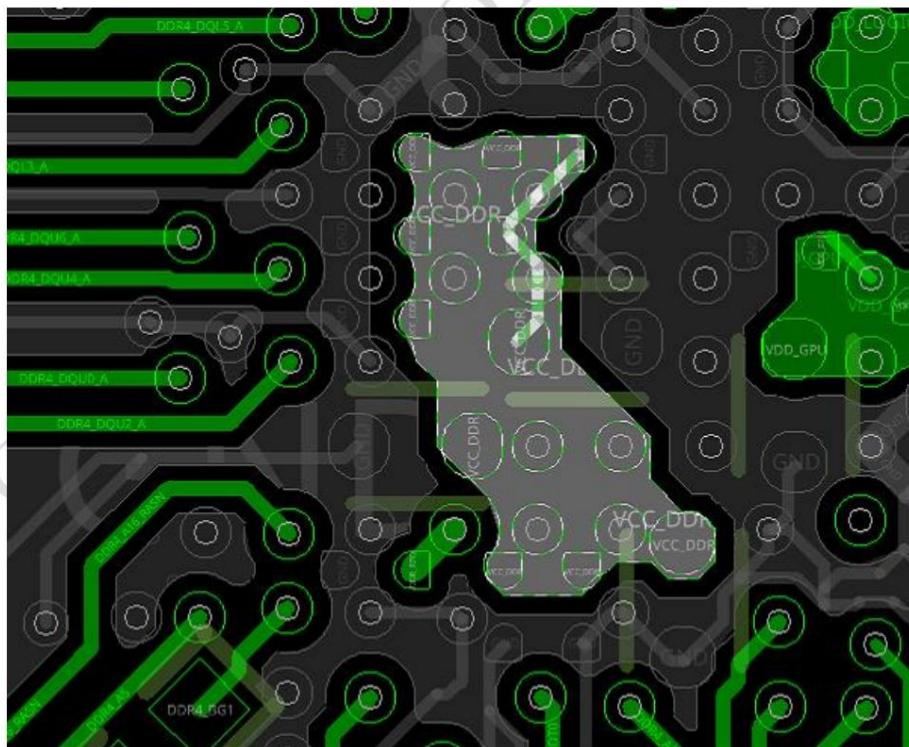


Figure 3-54 Decoupling capacitor placement on the back of the RK3528 chip VCC_DDR power pin

VCC_DDR current is relatively large, the effective overcurrent width needs to be ≥30mil; the peripheral area width is recommended to be greater than 100mil. A power supply layer is required

The plane and the adjacent GND return plane, and the distance between the two planes is recommended to be less than 5mil. The role of the plane is to reduce the voltage drop on the one hand, and on the other hand

The plane capacitance between the power plane and the adjacent GND plane can effectively reduce the high-frequency PDN. It is recommended to use one ounce of copper for the power copper.

Helps reduce current density.

In the CPU area, the recommended number of GND vias within the 50-mil range (via center-to-via center spacing) of the VCC_DDR power vias is ≥12.

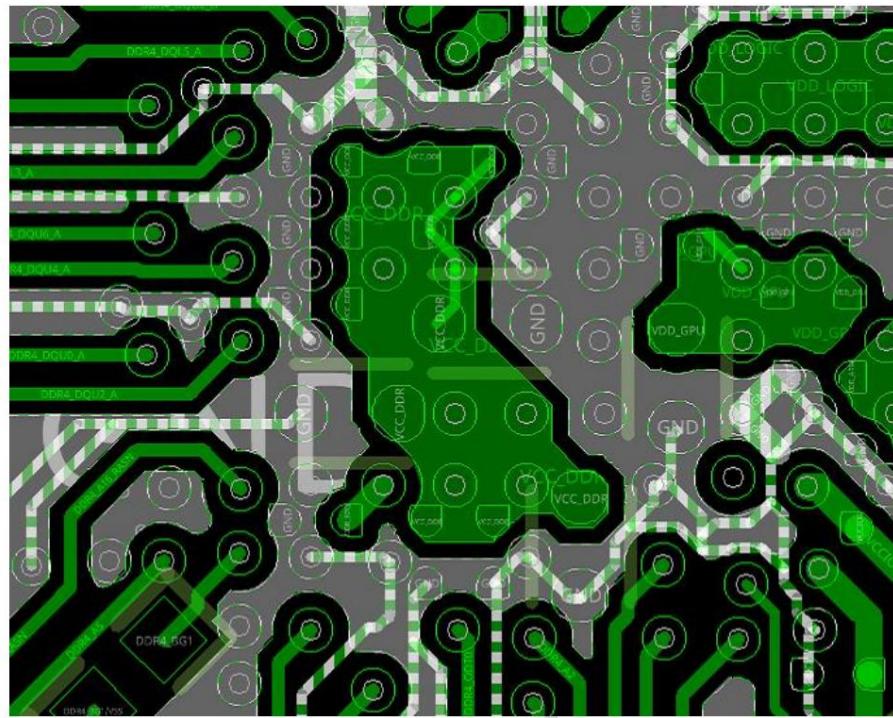


Figure 3-55 VCC_DDR power ground via placement diagram

(1) At the DCDC output, the number of 0503 vias on the power supply layer is recommended to be ≥6.

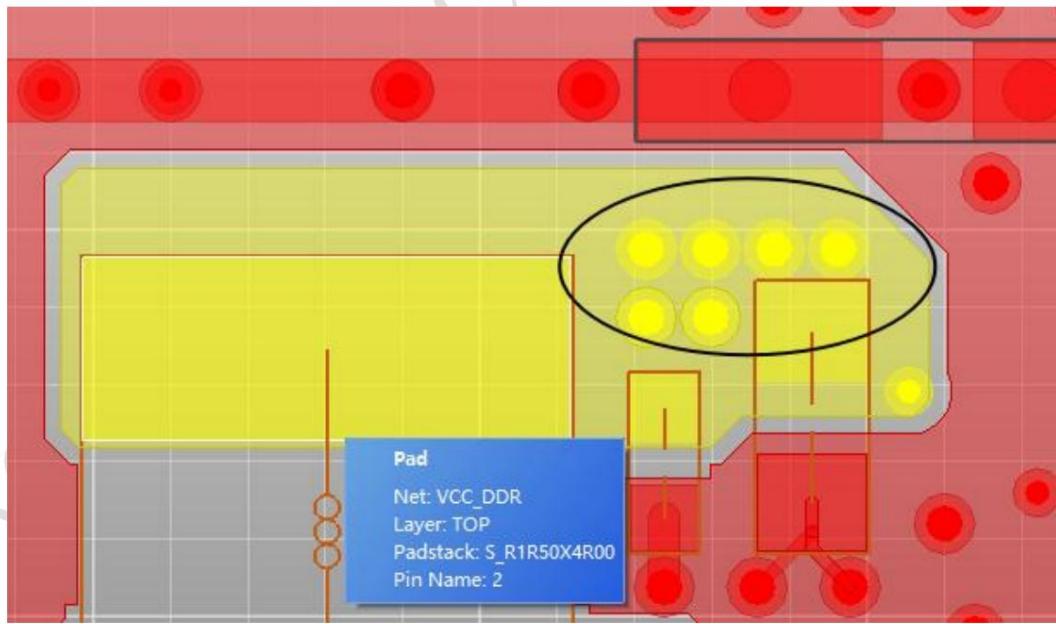


Figure 3-56 Diagram of the number of DCDC layer-changing vias

(2) For the decoupling capacitors at the DCDC, power supply, and GND pads, it is recommended to have two vias for each pad. Removing the capacitors is not recommended.

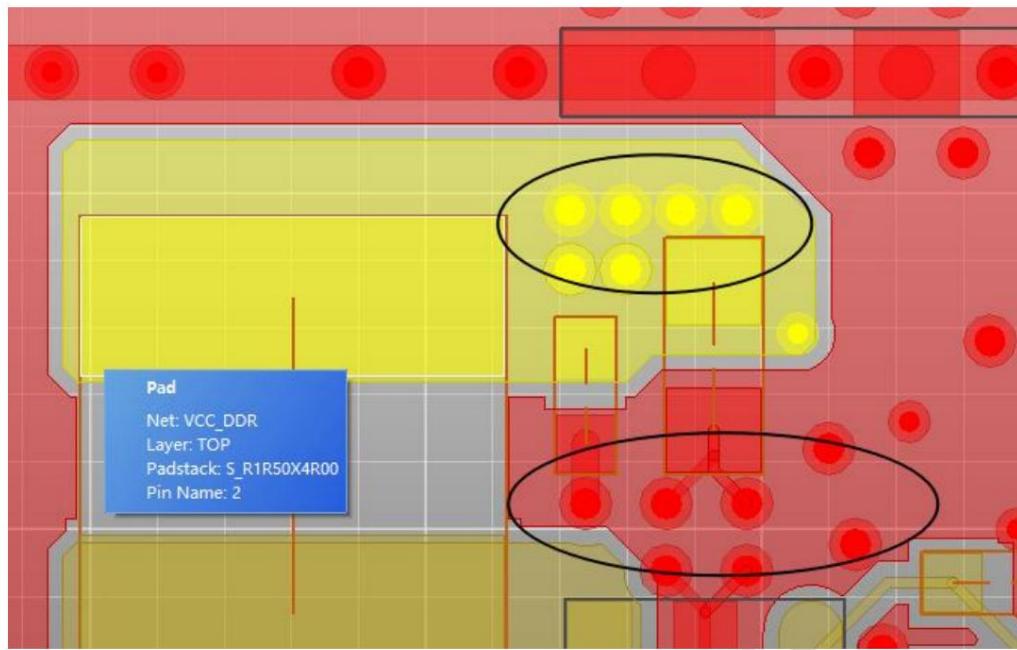


Figure 3-57 Schematic diagram of the number of decoupling capacitor vias

(3) For the number of power vias corresponding to the DDR chip power pins, it is recommended to directly copy our template and not to modify it.

As follows: one power pin \geq 0.9 power vias.

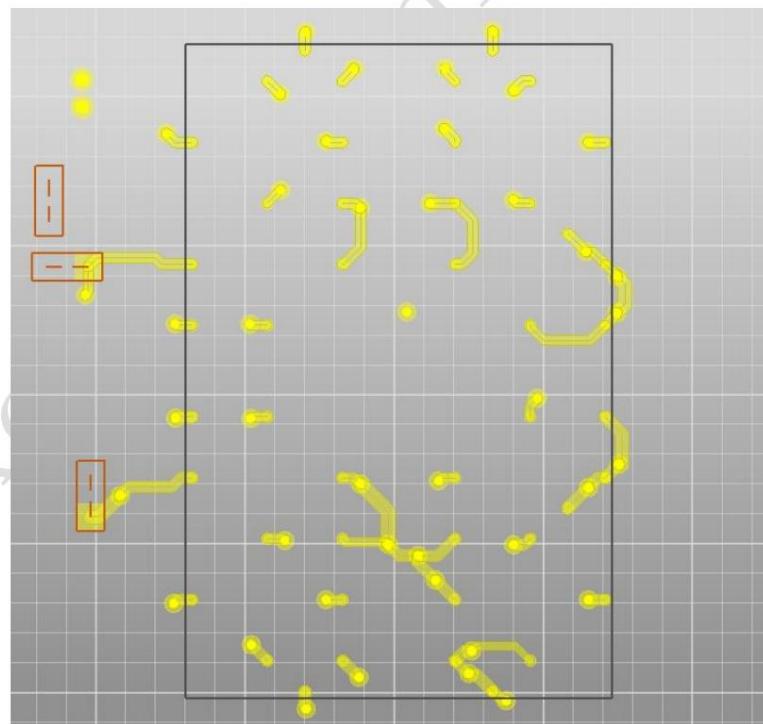


Figure 3-58 Schematic diagram of the number of vias corresponding to the DDR power pins

(4) The decoupling capacitors near the RK3528 power pins on the schematic diagram must be placed on the back of the corresponding power pins.

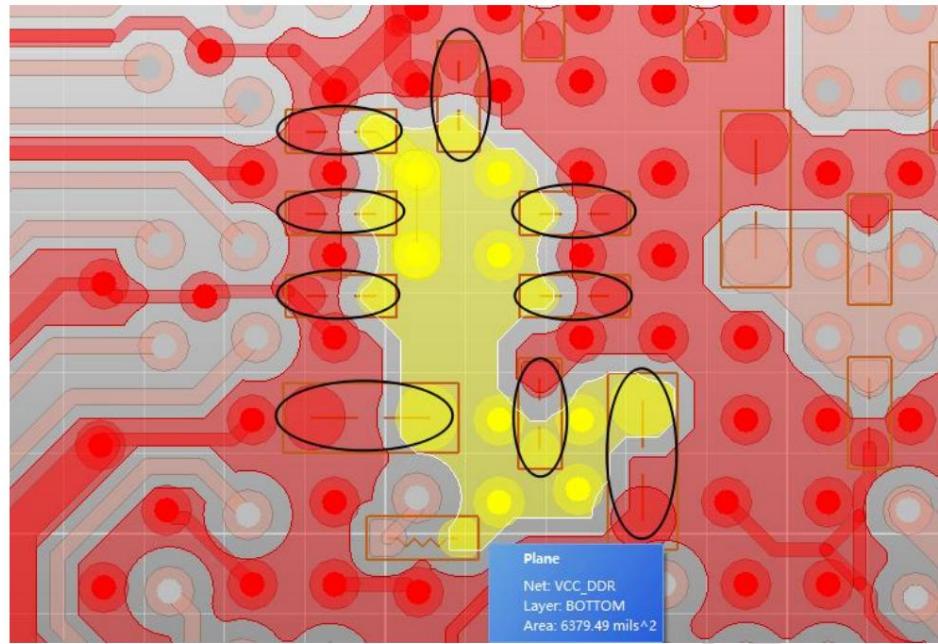


Figure 3-59 Schematic diagram of capacitor quantity

(5) For the number of vias corresponding to the RK3528 power pins, it is recommended to directly copy our template and not modify it. Our design example is as follows:

1.5 power pins > 1 power via.

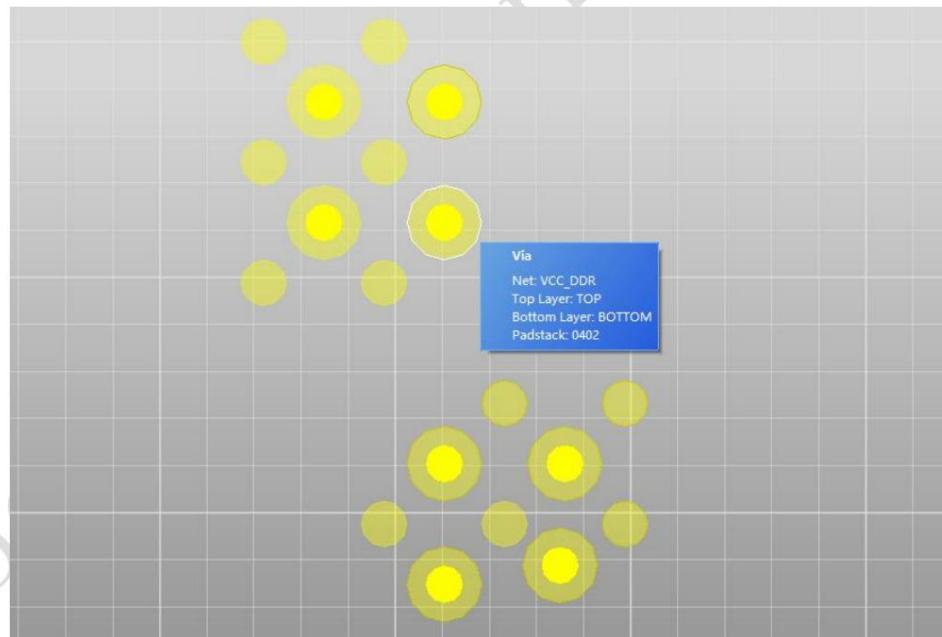


Figure 3-60 Schematic diagram of the number of power vias

(6) The number of GND vias within 40mil of the RK3528 power pin is recommended to be greater than the number of power pins.

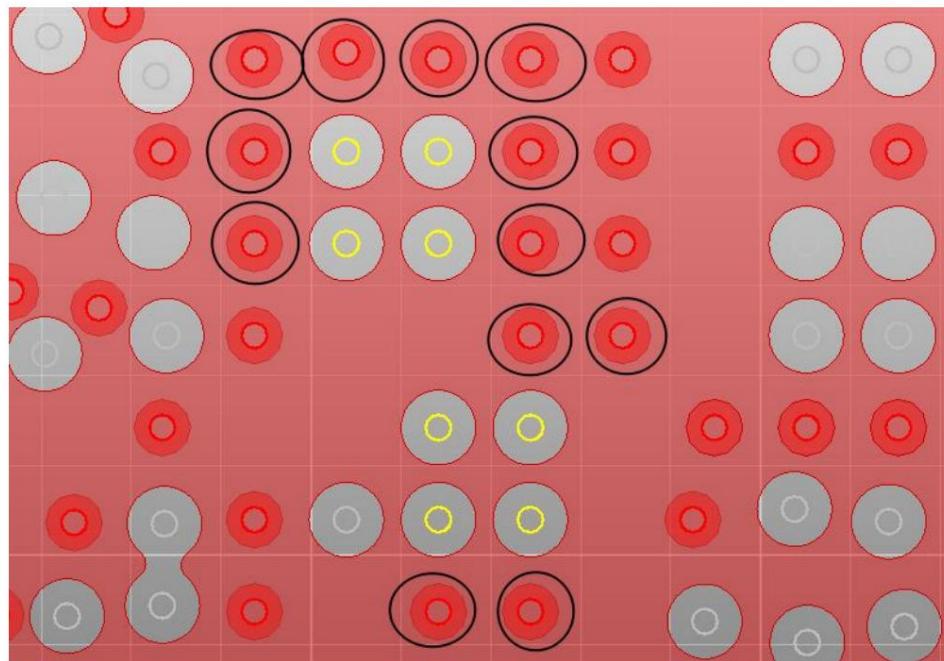


Figure 3-61 Schematic diagram of the number of GND vias within 40mil of the power pin

(7) The effective width of the copper foil under the RK3528 BGA is \geq 40mil



Figure 3-62 Schematic diagram of the copper foil under the BGA

(8) The recommended DC resistance of VCC_DDR is \leq 5 milliohms.

(9) The recommended target impedance values for the RK3528 VCC_DDR power supply PDN are as follows:

Table 3-3 RK3528 VCC_DDR power supply PDN target impedance recommended values

frequency	Impedance value (unit: ohm)
100Khz~1Mhz	≥0.025
1Mhz ~30Mhz	≥0.035
30Mhz~100Mhz	≥0.1

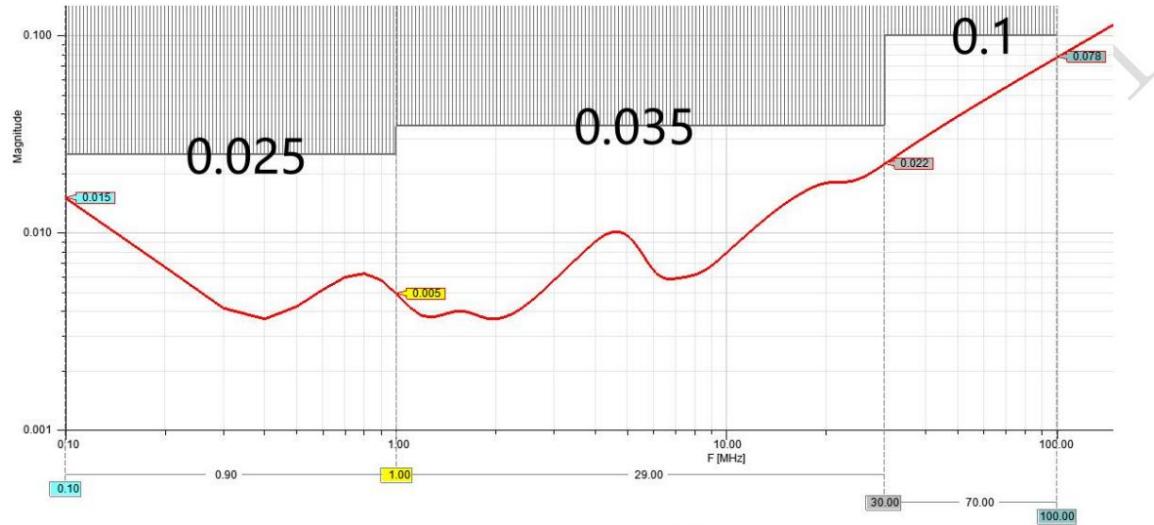


Figure 3-63 RK3528 VCC_DDR power supply recommended PDN requirements

(10) The recommended target impedance values for the DDR chip VCC_DDR power supply PDN are as follows:

Table 3-4 DDR chip VCC_DDR power supply PDN target impedance recommendation value

frequency	Impedance value (unit: ohm)
100Khz~1Mhz	≥0.025
1Mhz ~30Mhz	≥0.03
30Mhz~100Mhz	≥0.06

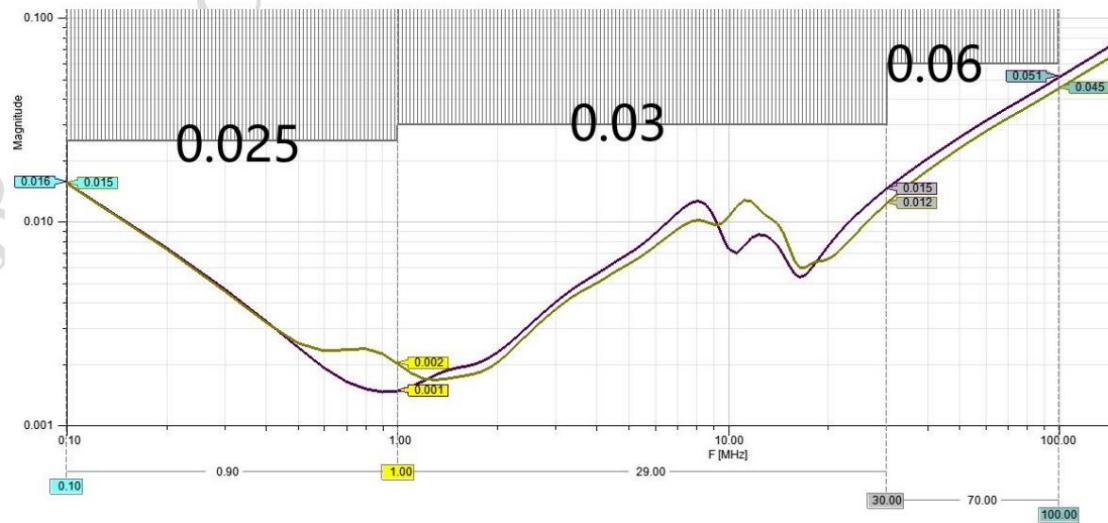


Figure 3-64 DDR chip VCC_DDR power supply recommended PDN requirements

3.3.2.6 RK3528 VCC0V6_DDR Power Supply PCB Design

(1) At the DCDC output, the number of 0503 power supply layer switching vias is recommended to be ≥6.

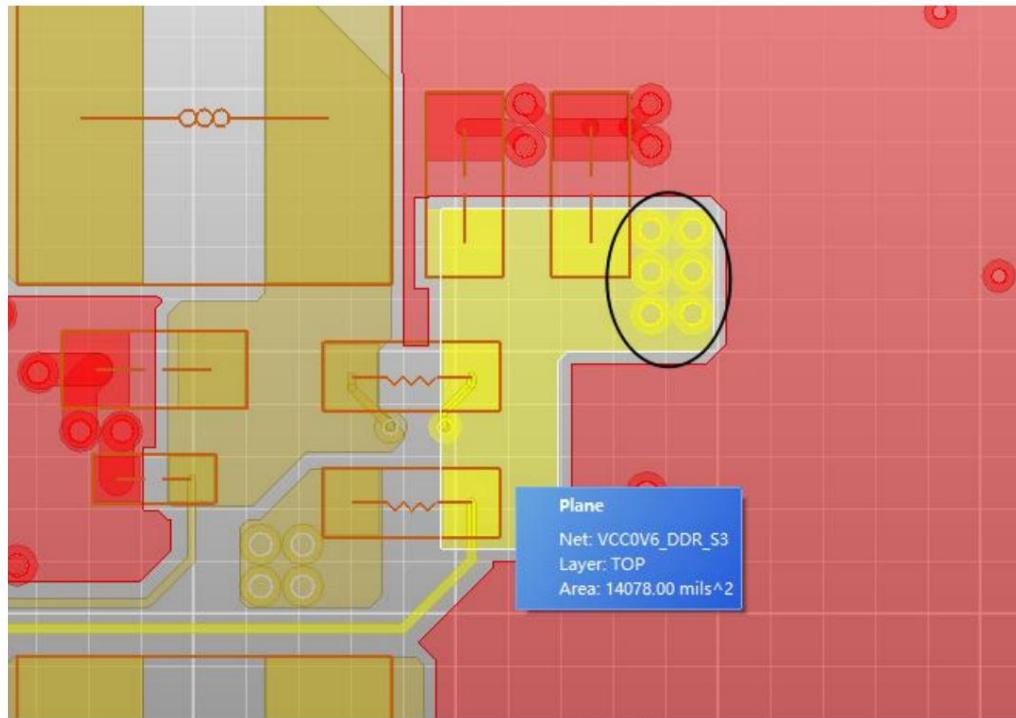


Figure 3-65 Diagram of the number of DCDC layer-changing vias

(2) For the decoupling capacitors at the DCDC, power supply, and GND pads, it is recommended to have two vias for each pad. Removing the capacitors is not recommended.

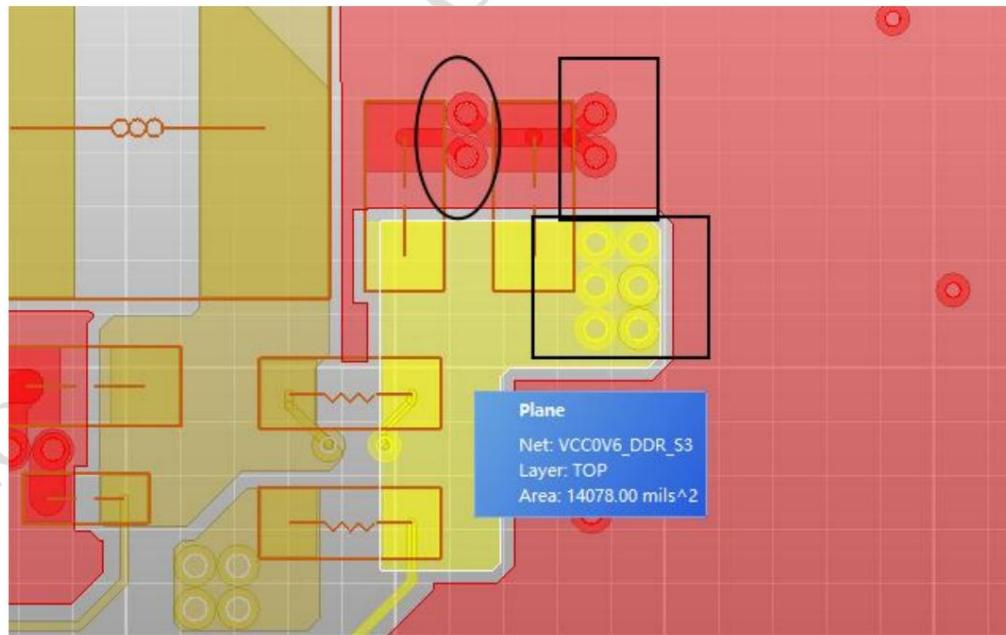


Figure 3-66 Schematic diagram of the number of decoupling capacitor vias

(3) For the number of power vias corresponding to the DDR chip power pins, it is recommended to directly copy our template and not to modify it.

As follows: one power pin ≥ 0.9 power vias.

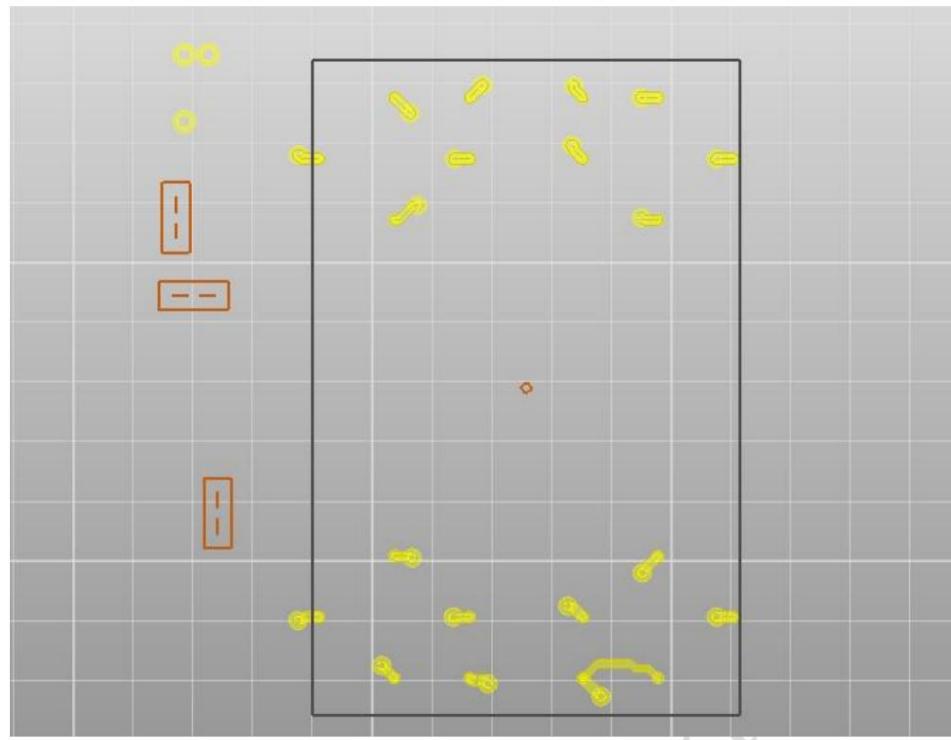


Figure 3-67 Schematic diagram of the number of vias corresponding to the DDR power pins

(4) The decoupling capacitors near the RK3528 power pins on the schematic diagram must be placed on the back of the corresponding power pins.

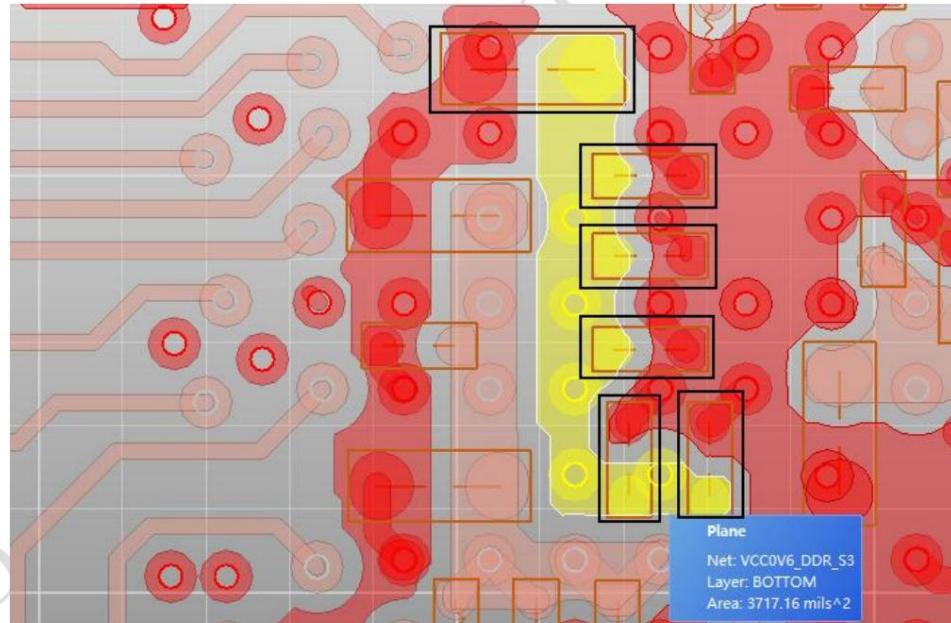


Figure 3-68 Schematic diagram of capacitor quantity

(5) For the number of vias corresponding to the RK3528 power pins, it is recommended to directly copy our template and not modify it. Our design example is as follows:

1.25 power pins \rightarrow 1 power via.

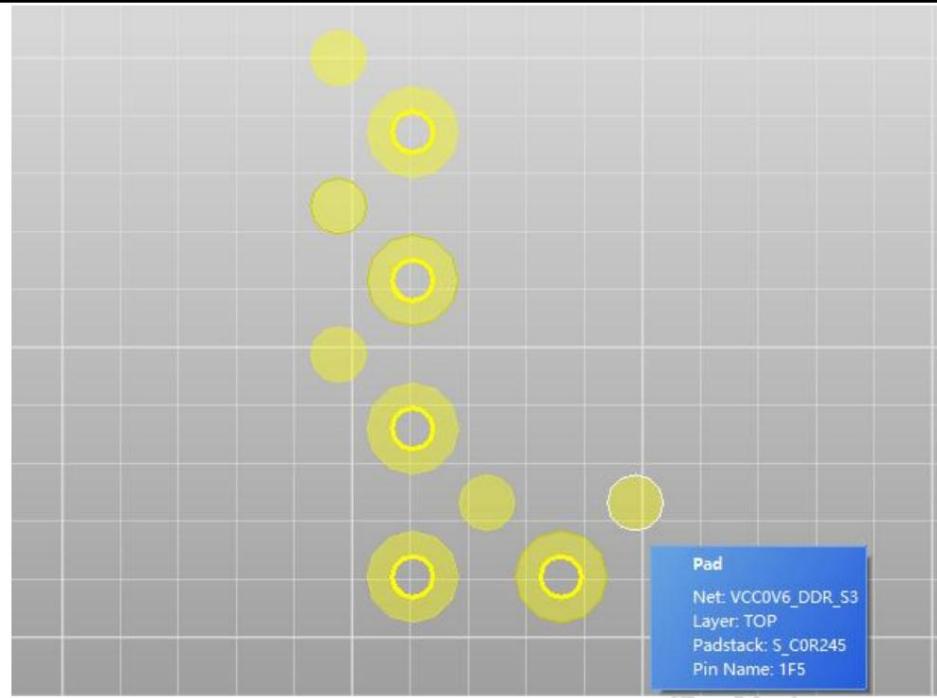


Figure 3-69 Schematic diagram of the number of power vias

(6) The number of GND vias within 40mil of the RK3528 power pin is recommended to be \geq the number of power pins.

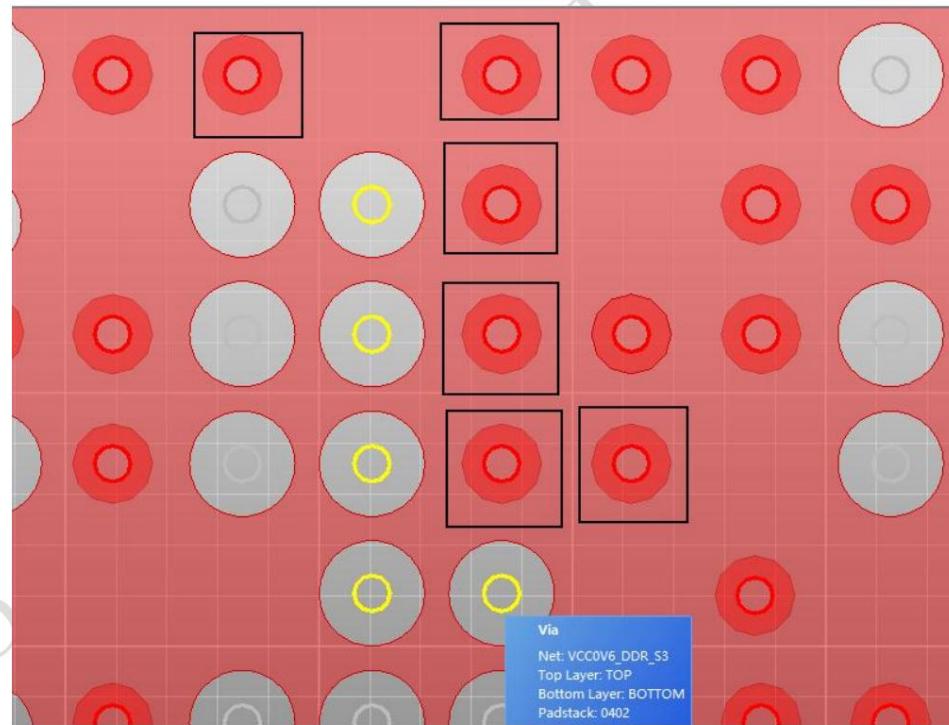


Figure 3-70 Diagram of the number of GND vias within 40mil of the power pin

(7) VCC0V6_DDR power supply DC resistance \leq 15 milliohms

(8) The recommended target impedance values for the RK3528 VCC0V6_DDR power supply PDN are as follows:

Table 3-5 RK3528 VCC0V6_DDR power supply PDN target impedance recommended values

frequency	Impedance value (unit: ohm)
100Khz~1Mhz	≥0.03
1Mhz ~30Mhz	≥0.045
30Mhz~100Mhz	≥0.12

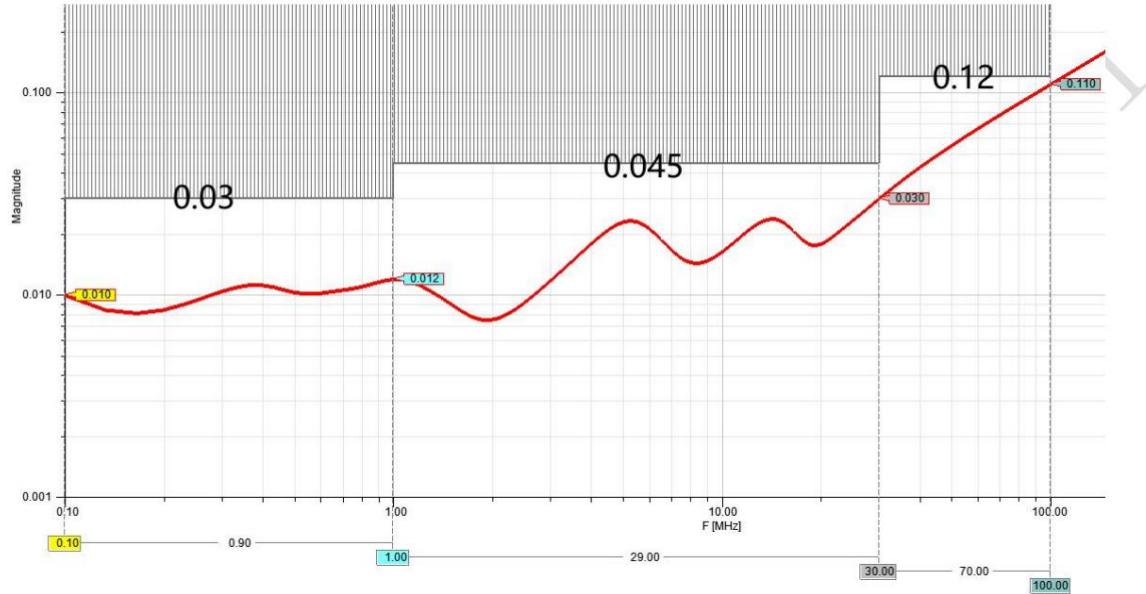


Figure 3-71 RK3528 VCC0V6_DDR power supply recommended PDN requirements

(9) The recommended target impedance values for the DDR chip VCC0V6_DDR power PDN are as follows:

Table 3-6 DDR chip VCC0V6_DDR power PDN target impedance recommendation

frequency	Impedance value (unit: ohm)
100Khz~1Mhz	≥0.025
1Mhz ~30Mhz	≥0.035
30Mhz~100Mhz	≥0.05

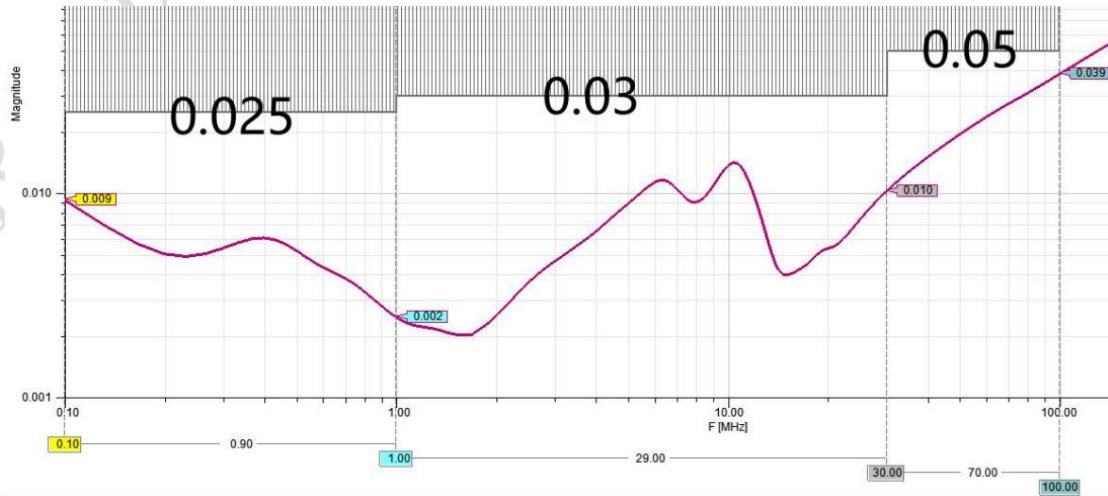


Figure 3-72 DDR chip VCC0V6_DDR power supply recommended PDN requirements

3.3.2.7 RK3528 GND pin PCB design

The GND pin of the RK3528 chip should have at least one via for every two balls, and preferably one via for every 1.5 balls.

It provides better SI and PI conditions and also helps with heat dissipation.

The adjacent layer of the RK3528 chip must be a complete GND plane to ensure that the main reference ground is close to the CPU ball to ensure power integrity and enhance the heat dissipation of the PCB.

The GND balls of the same network under the RK3528 chip are arranged in a "well" shape on the top layer and cross-connected. The recommended trace width is 10 mil.

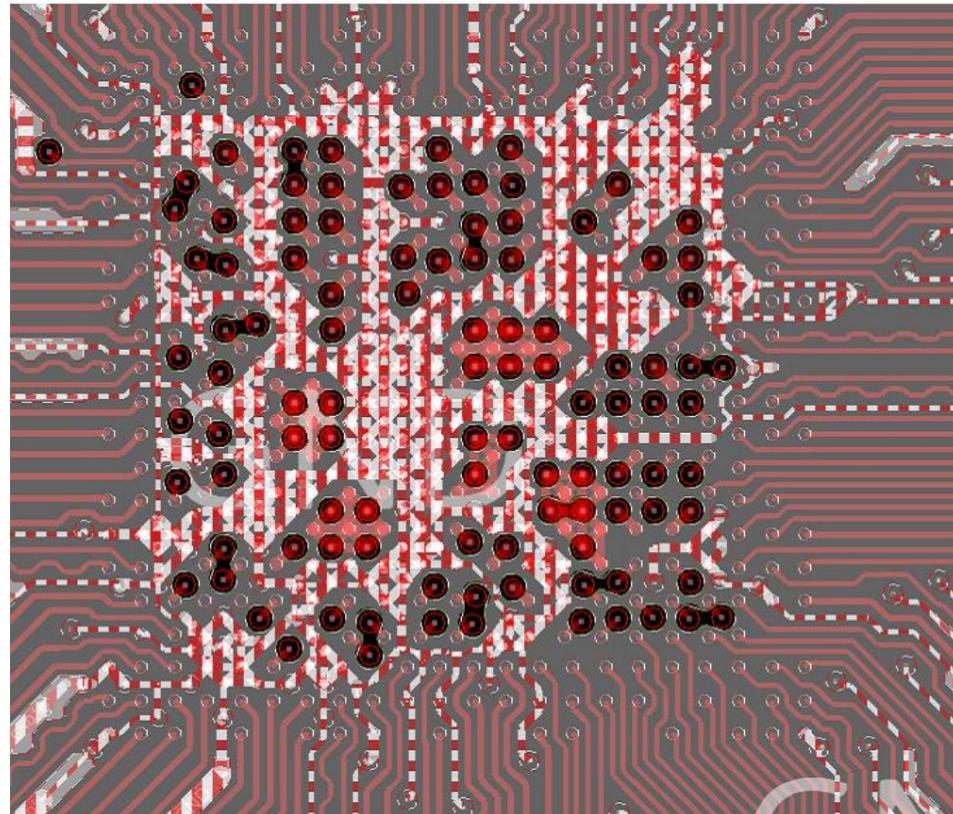


Figure 3-73 RK3528 chip VSS pin routing and vias

During layout, when placing the layer-changing vias for each signal of RK3528, they are required to be placed in the middle of the ball interval and in a regular pattern. As shown in the figure, the copper covering of the GND layer, the ground in the middle of the RK3528 chip has a large area of copper connected to the outer ground copper, which is beneficial to the power supply. Signal integrity, on the other hand it is beneficial to chip heat dissipation.

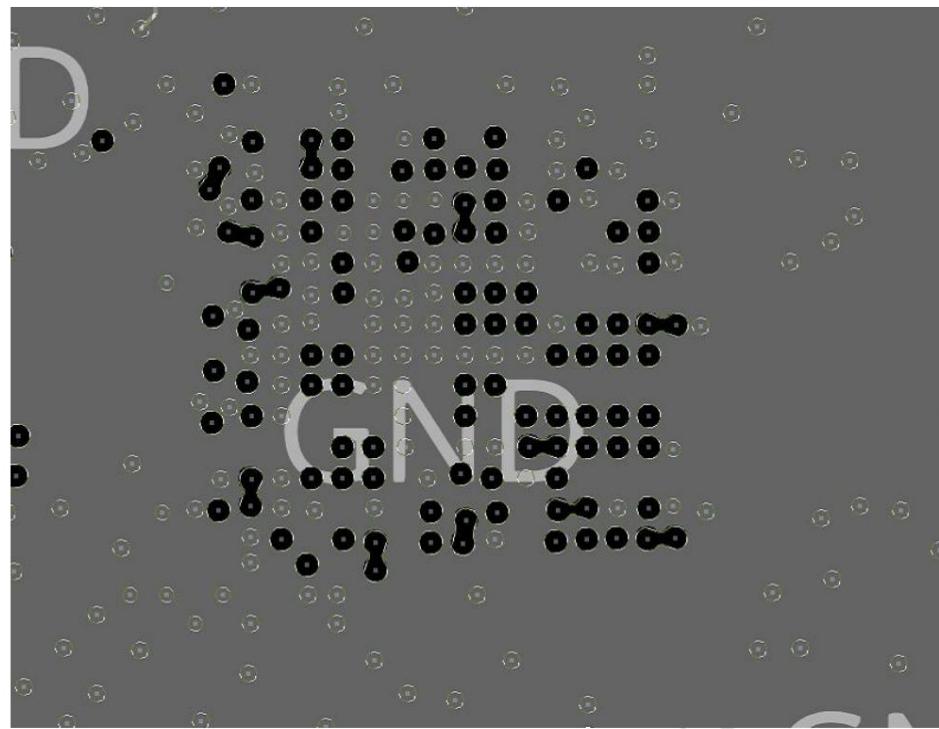


Figure 3-74 RK3528 chip ground copper coverage

3.3.2.8 PCB Design of Other Power Supplies for RK3528

For other power supplies of RK3528, the decoupling capacitor close to RK3528 on the schematic diagram must be placed on the back of the chip pins.

It is recommended to have a corresponding GND via. In the worst case, at least two GND pads should have one GND via to avoid multiple occurrences of the worst case.

Design under certain circumstances.

The power supply of high-speed interface and PLL needs to ensure that the capacitor is close to the power via. The distance between the capacitor with small capacitance, such as 100nF capacitor and the power via is

(The distance from the center of the via to the edge of the capacitor pad) is recommended to be $\leq 12\text{mil}$. The spacing between the 1uF capacitor and the power via is recommended to be $\leq 50\text{mil}$.

It is recommended that the GND pin of the capacitor correspond to a GND via.

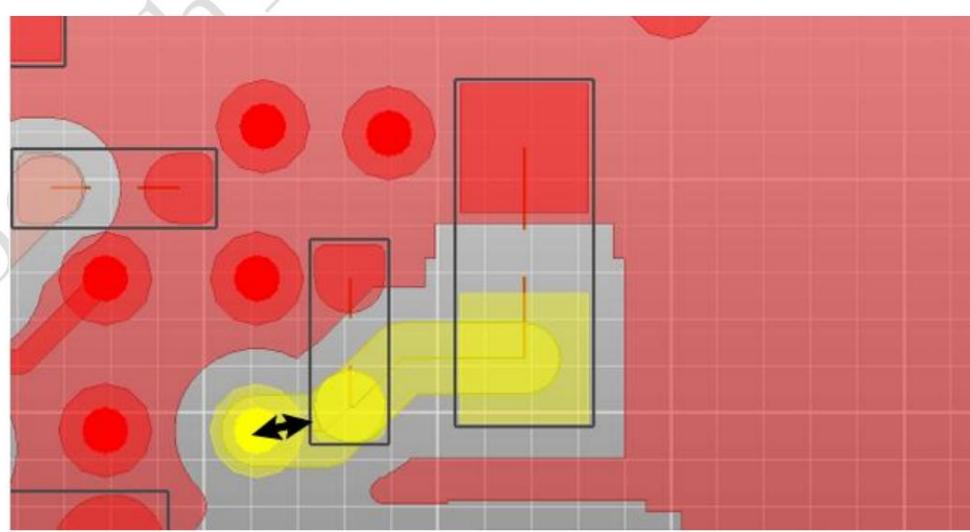


Figure 3-75 Schematic diagram of placing power capacitors close to power vias



Figure 3-76 Schematic diagram of the number of GND vias corresponding to the GND pin of the power capacitor

3.3.3 DRAM Circuit PCB Design

Since the RK3528 DDR interface speed is very high and the PCB design is difficult, it is strongly recommended to use the DDR template and corresponding DDR firmware. DDR template is released after rigorous simulation and test verification. If you design the PCB yourself, please refer to the following PCB

Design suggestion: It is strongly recommended to perform simulation optimization before releasing the board.

DDR interface PCB design is difficult, so we strongly recommend using the DDR template and corresponding DDR firmware we provide. The DDR template is released after rigorous simulation and test verification. If you design the PCB yourself, please refer to the following PCB design suggestions, and simulation optimization is recommended.

Then release the board.

(1) The number of GND pins and corresponding GND vias in the RK3528 DDR area should be strictly followed according to the template design. GND pins should not be deleted.

Vias, for example.

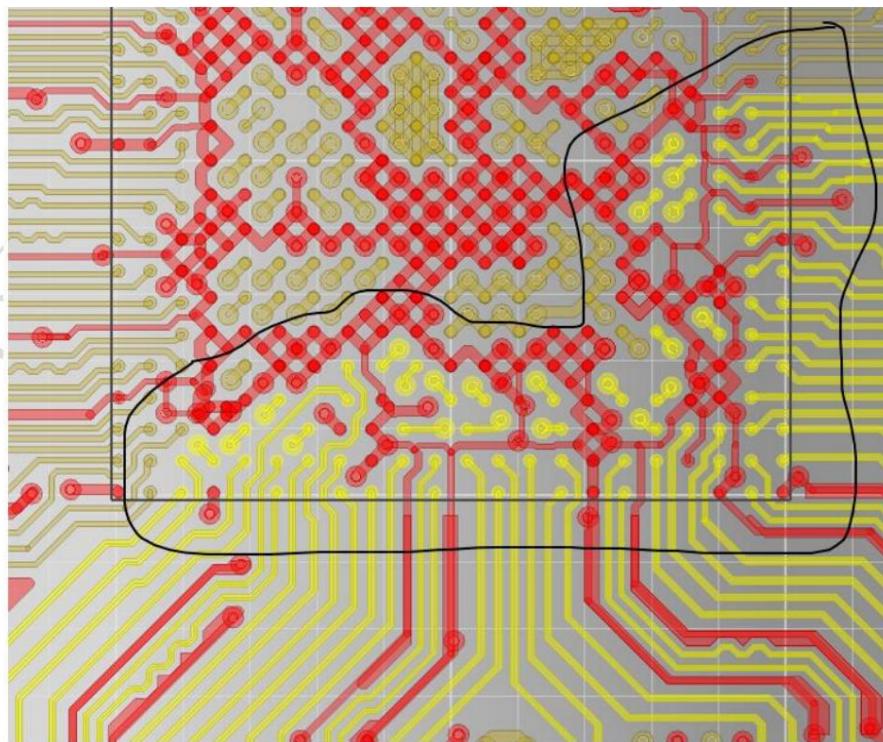


Figure 3-77 Template GND via design

(2) To ensure the quality of DQ and DQS signals, it is recommended to select the GND plane as the reference plane. The following figure shows a 4-layer PCB with the chip on

On the first layer, when designing the template, our company will make the DQ and DQS signals of the fourth layer refer to the GND plane of the third layer instead of the third layer.

At the same time, it is recommended to wrap the DQ and DQS signals on the fourth layer with a ground connection. You can wrap one DQ with a ground connection, or two DQs with a ground connection.

It is recommended to add a GND via every 500mil or less of the ground line. And the signal layer change via should be within 25mil (the distance between the via center and the via center).

GND return vias need to be added.

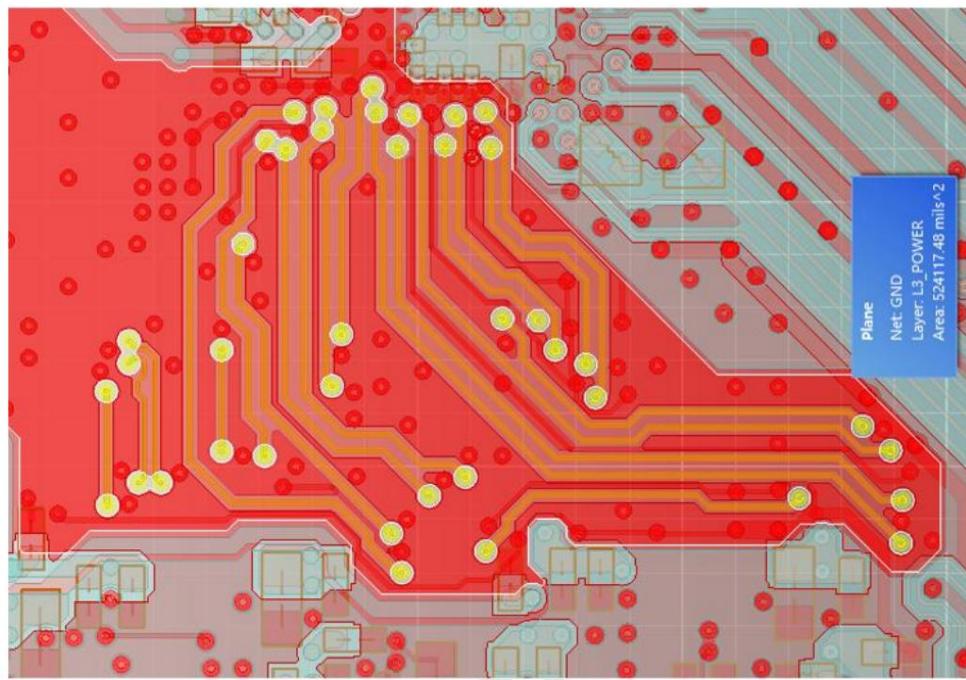


Figure 3-78 Schematic diagram of the fourth layer's DQ and DQS signal reference GND plane

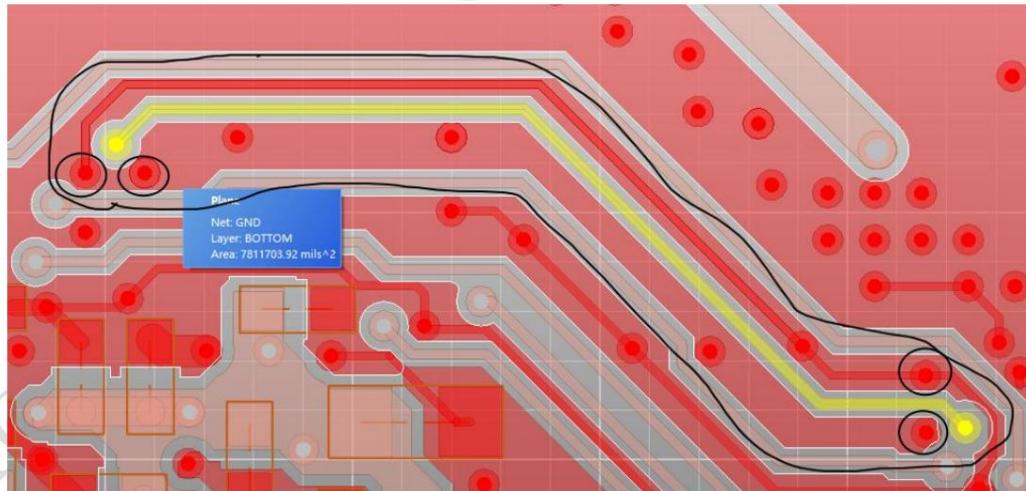


Figure 3-79 Schematic diagram of a DQ ground connection

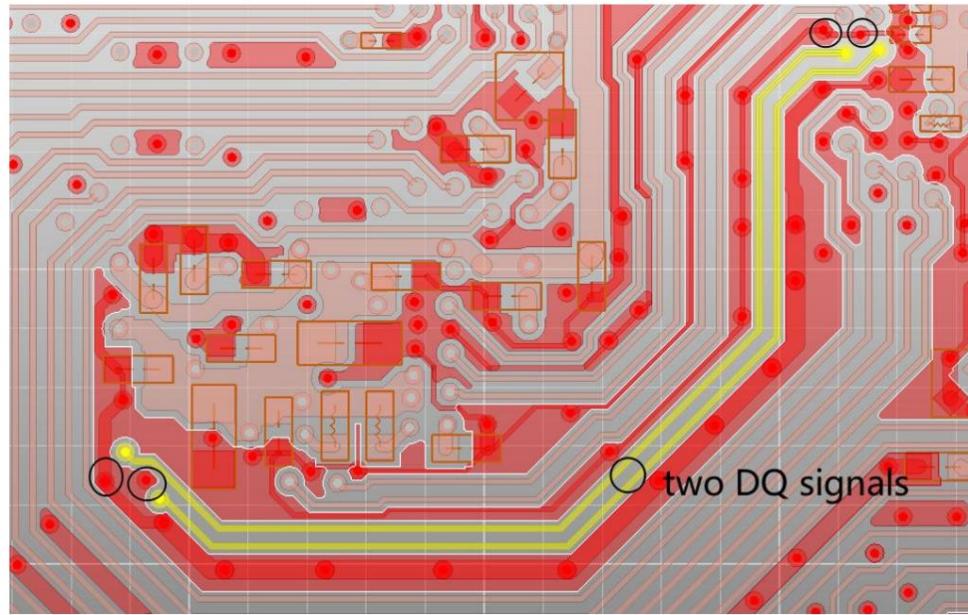


Figure 3-80 Schematic diagram of two DQ grounding

(3) The closer the trace is to the edge of the reference layer, the worse the signal return will be. The distance between the trace and the edge of the reference layer is recommended to be $\geq 12\text{mil}$.

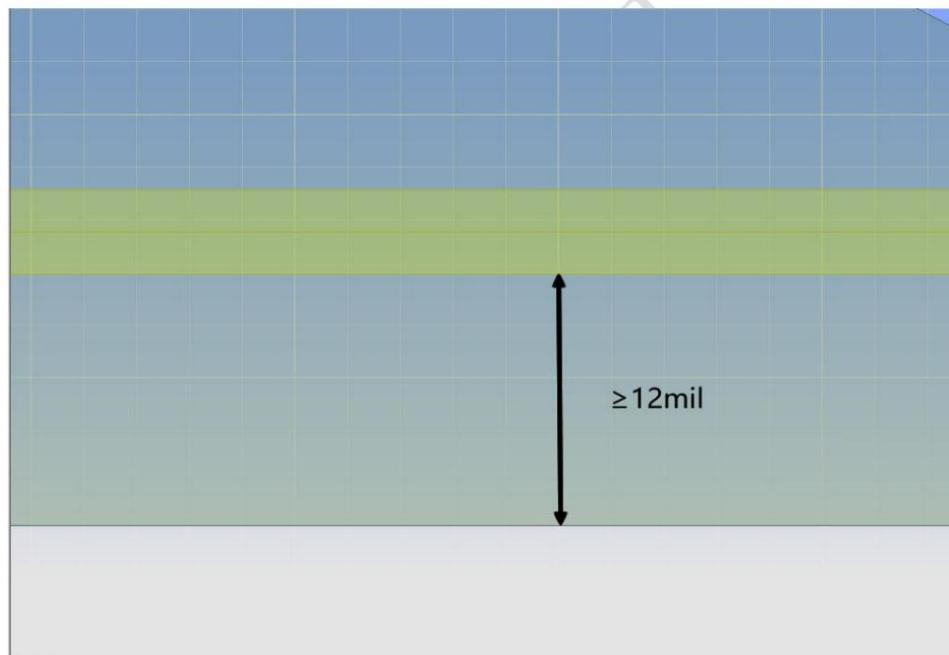


Figure 3-81: Distance between trace and reference layer edge

(4) Before and after the signal layer is changed, when the reference layer is the GND plane, the signal via is 25mil (the distance between the via center and the via center)

GND return vias need to be added within the range to improve the signal return path. GND vias need to be connected to the GND reference plane before and after the signal layer is changed.

Connect them.

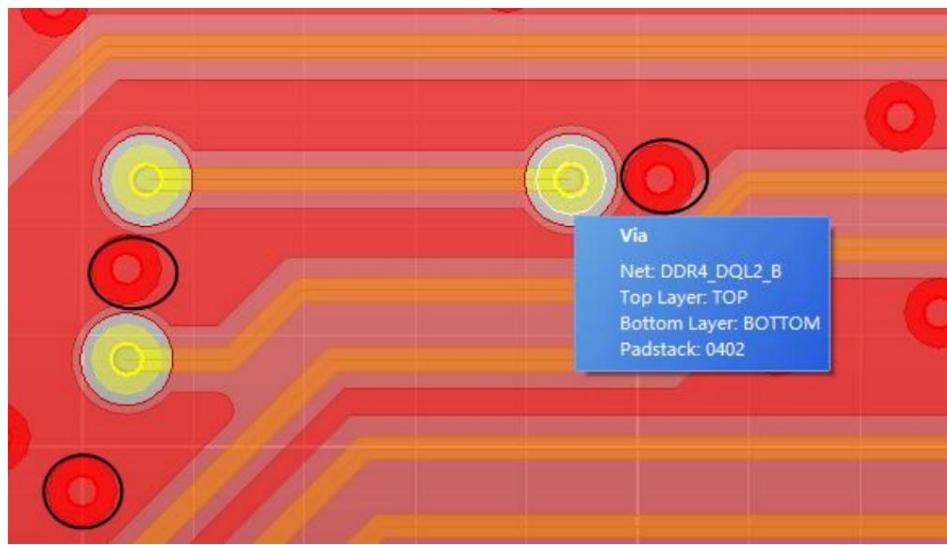


Figure 3-82 Schematic diagram of signal GND return via

(5) DQS and CLK signals, from sending to receiving the entire link, it is recommended to do ground processing, and it is recommended to add a ground line every \approx 500mil. GND via.

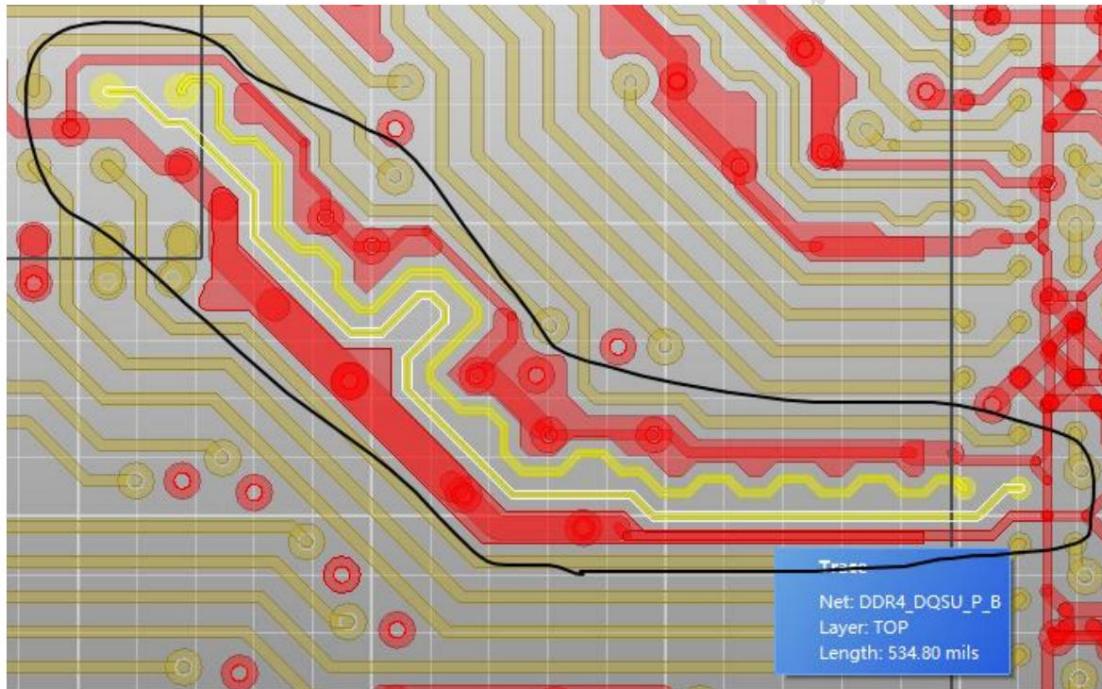


Figure 3-83 DQS signal ground processing diagram

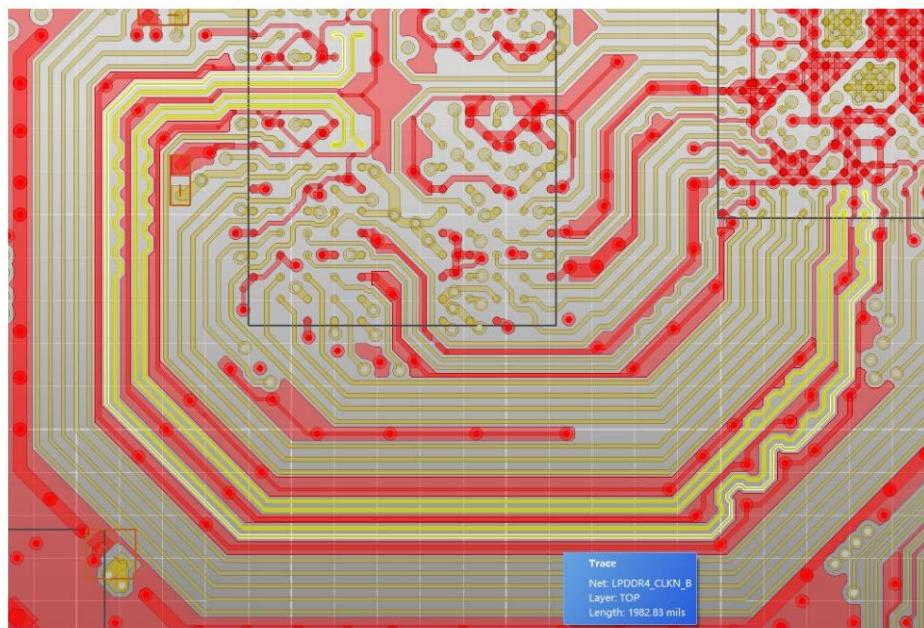


Figure 3-84 CLK signal ground processing diagram

(6) It is recommended to do grounding for the CKE, CS, and ODT signals from the sender to the receiver. It is recommended to add a GND every \approx 600mil.

Via holes. Within the range of 25mil (the distance between the center of the via hole to the center of the via hole) for signal layer switching, it is recommended to add GND return via holes to ensure the return current.

Continuity.

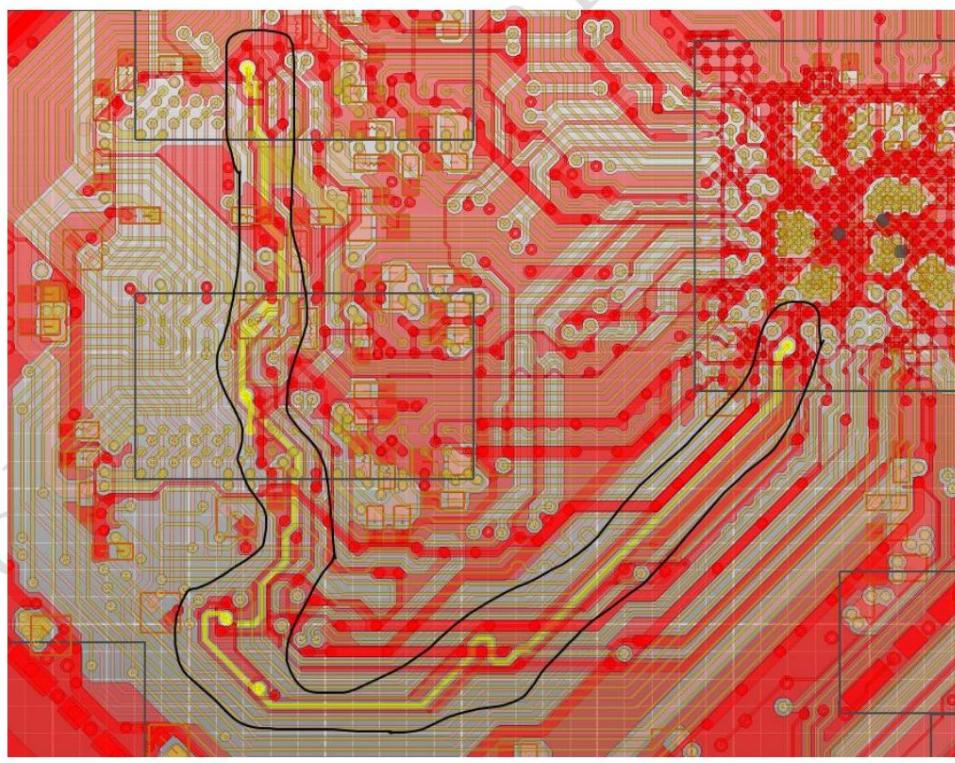


Figure 3-85 CKE, CS, and ODT signal ground diagram

(7) 4-layer PCB, for the design of 4 DDR particles, the address and control signals can only go on the third layer, which is generally the power level.

For the address control lines on the third layer, it is recommended to wrap them in pairs. For the address control lines on the fourth layer, due to the reference power plane, it is recommended to wrap them in pairs.

It is recommended to improve the signal quality by wrapping the ground. From the first layer change via to the entire link at the receiving end, it is recommended to add a GND every \approx 600mil.

Via: Within the 25mil range of the signal layer change via (via midpoint spacing), it is recommended to add GND return vias to ensure the continuity of the return flow.

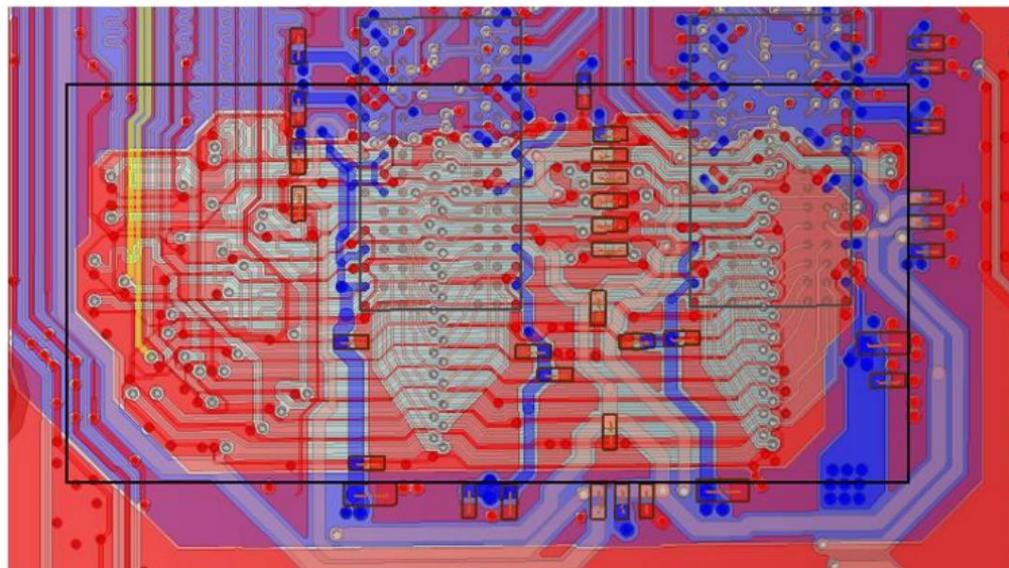


Figure 3-86 Schematic diagram of the third-layer address control line ground processing

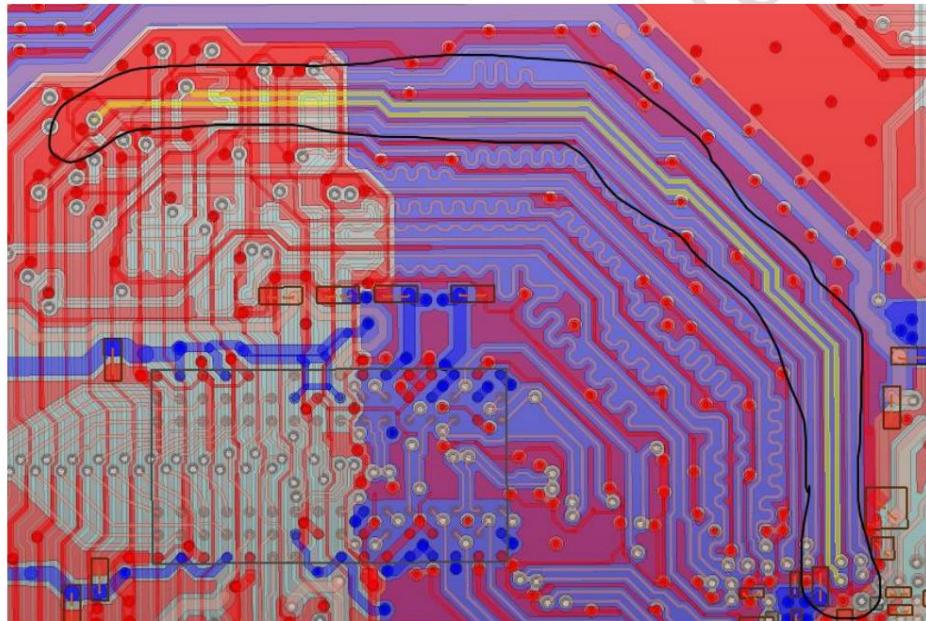


Figure 3-87 Schematic diagram of the fourth layer address control line ground processing

(8) The crosstalk of the winding itself will affect the signal quality. It is recommended that $S \geq 3W$ when the wiring is of equal length.

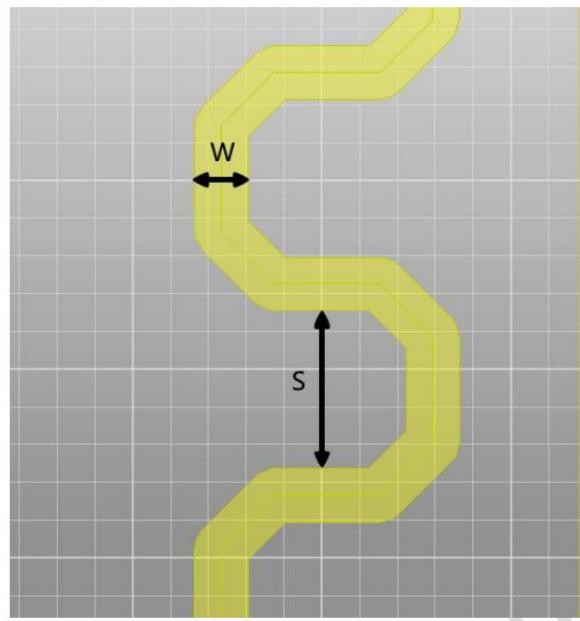


Figure 3-88 Signal winding diagram

(9) When making equal length, the delay of the via needs to be considered.

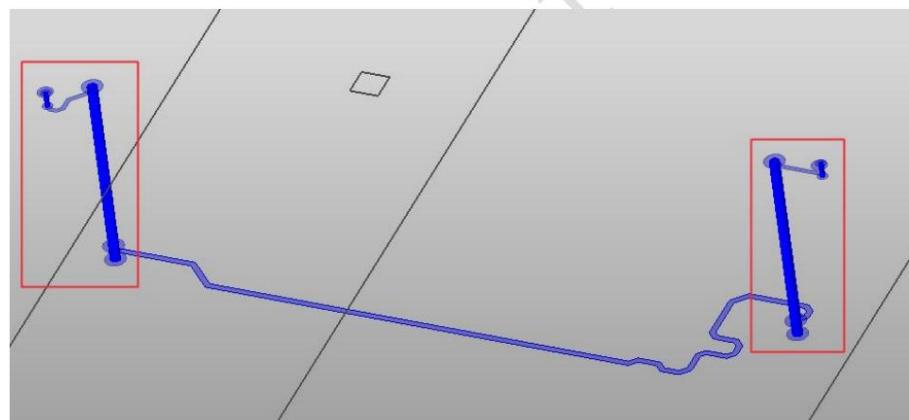


Figure 3-89 Via diagram

(10) Non-functional pads will damage the copper foil and increase the parasitic capacitance of the vias. The non-functional pads of the vias need to be deleted.

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(11) Avoid damage to the copper foil caused by continuous vias.

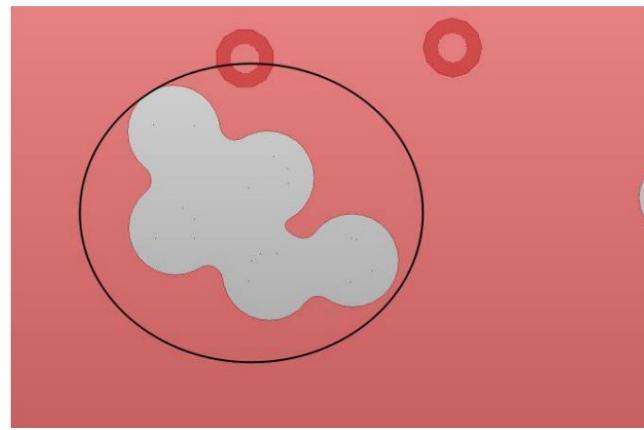


Figure 3-90 Schematic diagram of damage to copper foil caused by row of vias

(12) It is recommended that each capacitor pad has at least one via. For capacitors with 0603 or 0805 packages, it is recommended that one pad corresponds to two vias.

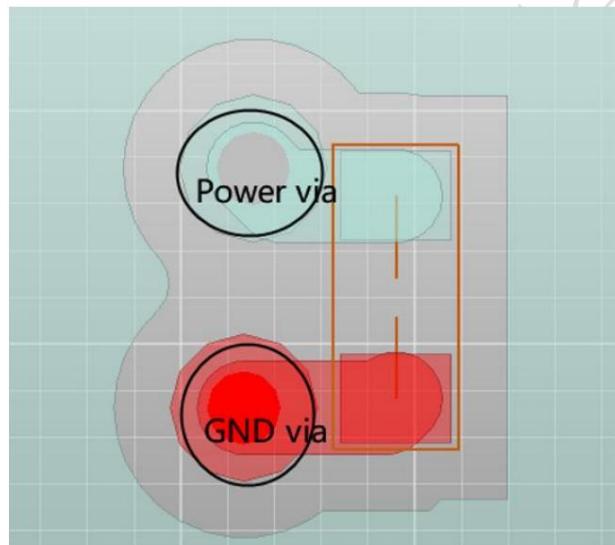


Figure 3-91 Diagram of the number of vias corresponding to capacitor pins

(13) Placing vias close to the pins can reduce loop inductance.

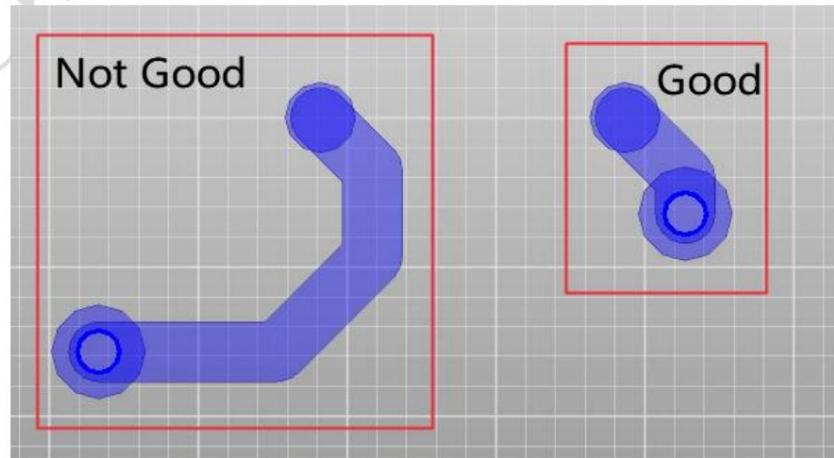


Figure 3-92 Schematic diagram of placing vias close to pins

(14) It is recommended that the capacitors be placed evenly.

(15) Avoid damage to the power layer by routing or continuous vias.

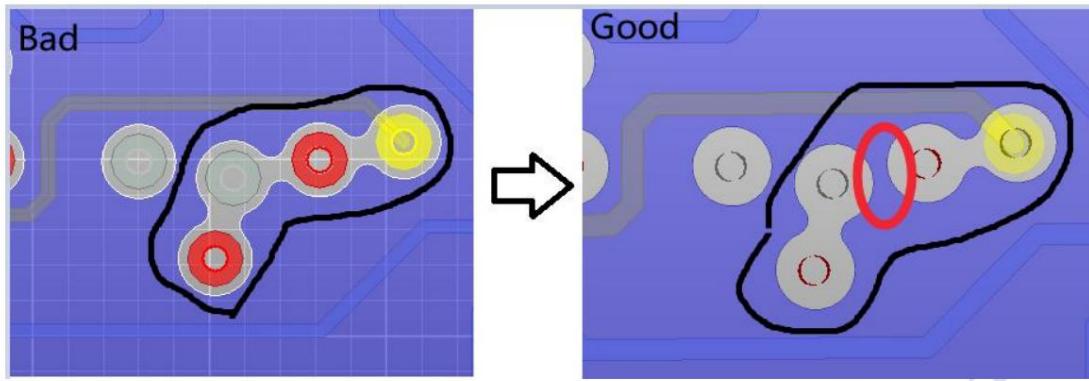


Figure 3-93: Schematic diagram of a power layer being extensively damaged by a row of vias

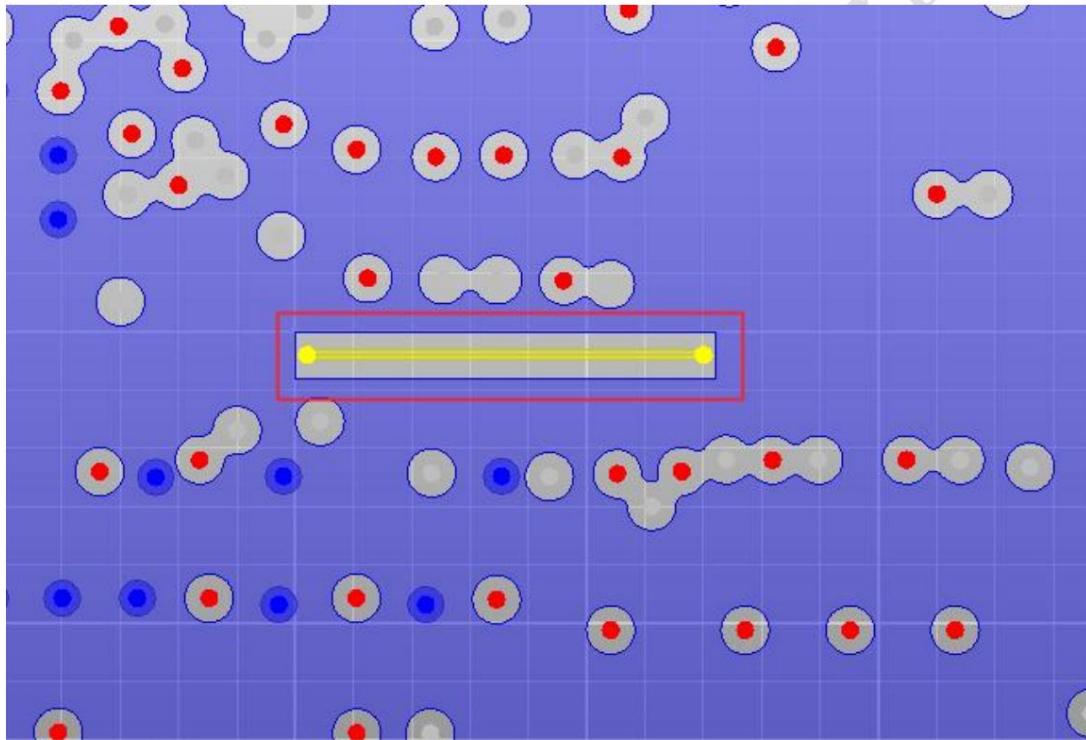


Figure 3-94 Schematic diagram of power layer damaged by routing

(16) Decoupling capacitors should be placed close to the power pins

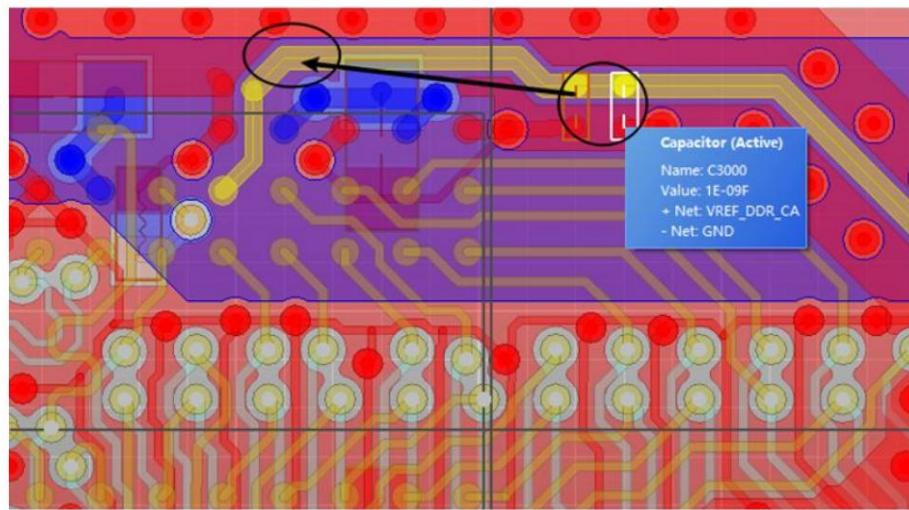


Figure 3-95 Schematic diagram of placing decoupling capacitors close to power pins

(17) DDR chip GND pin, it is recommended that one pin has at least one GND via.

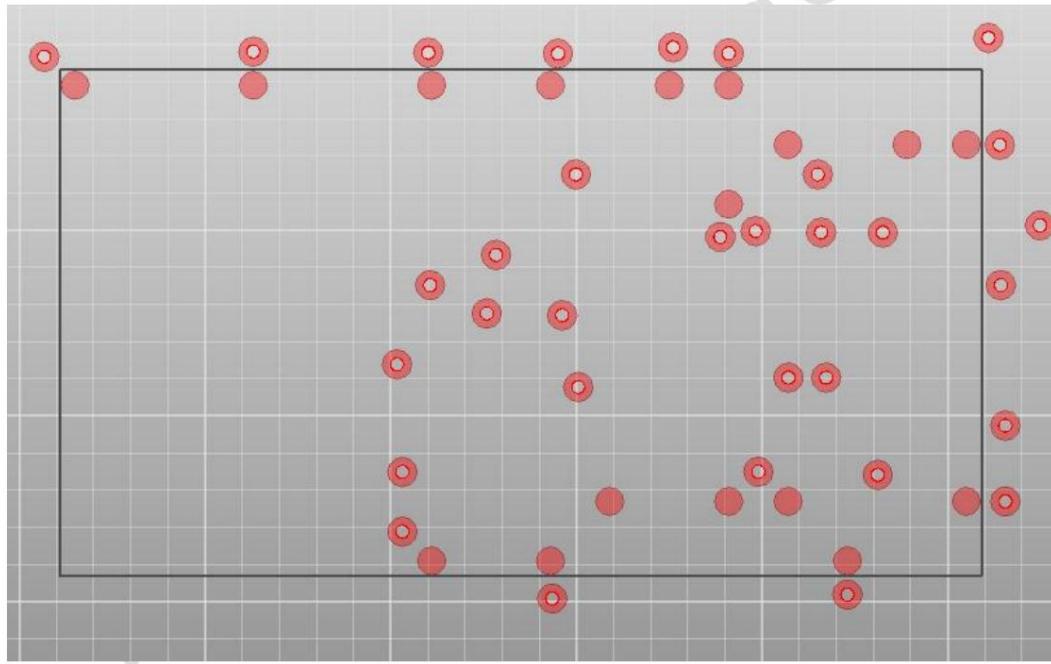


Figure 3-96 Schematic diagram of a GND pin with at least one GND via

(18) If the reference layer of the signal line switches from the GND layer to the power layer, and then switches from the power layer to the GND layer.

Due to area limitations, it is not possible to improve signal quality by wrapping the ground plane. However, it is possible to improve signal quality by adding stitching capacitors.

The hole has at least one stitching capacitor.

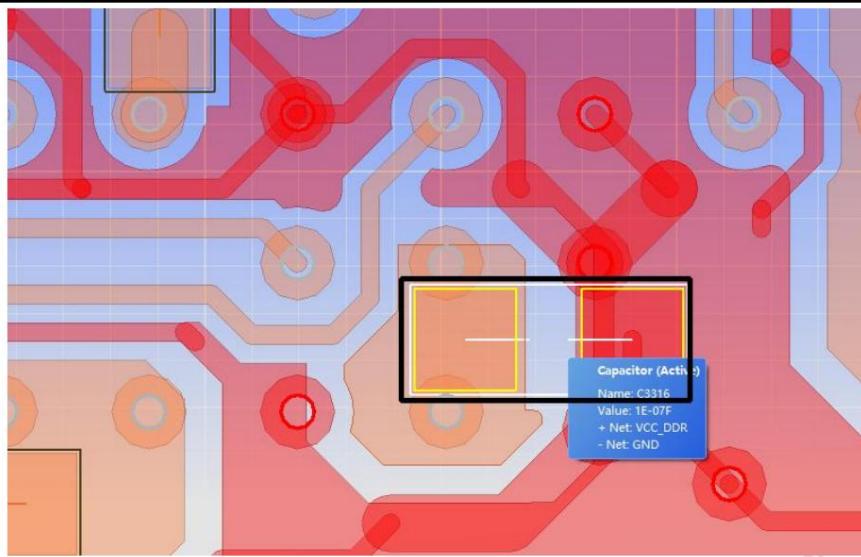


Figure 3-97 Schematic diagram of stitching capacitor

(19) It is recommended that the distance between the signal line and the via pad or drill hole should be ≥ 6 mil.

(20) VREF power supply is sensitive to noise. The air distance between VREF power supply and signal line is recommended to be ≥ 12 mil.

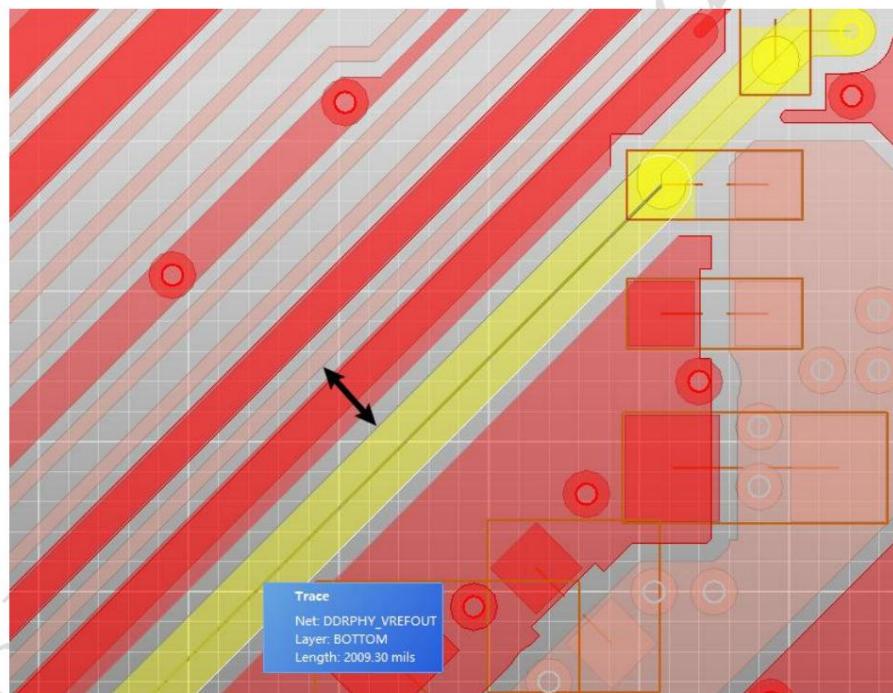


Figure 3-98 Schematic diagram of the air gap between VREF power supply and signal lines

(21) The RK3528 address control line will use a chain topology. The design points are as follows:

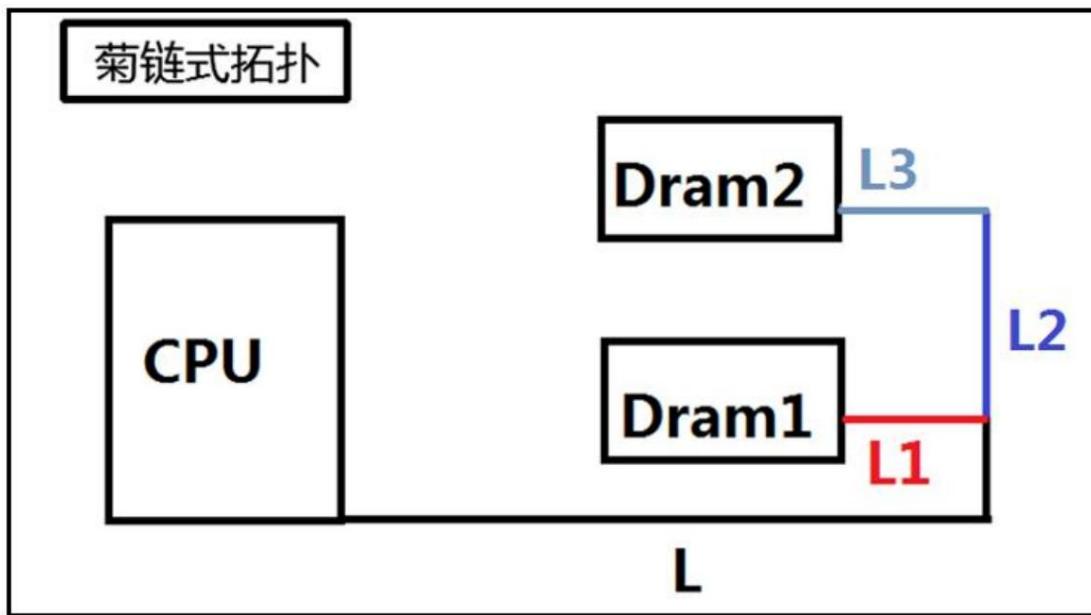


Figure 3-99 Chain topology diagram

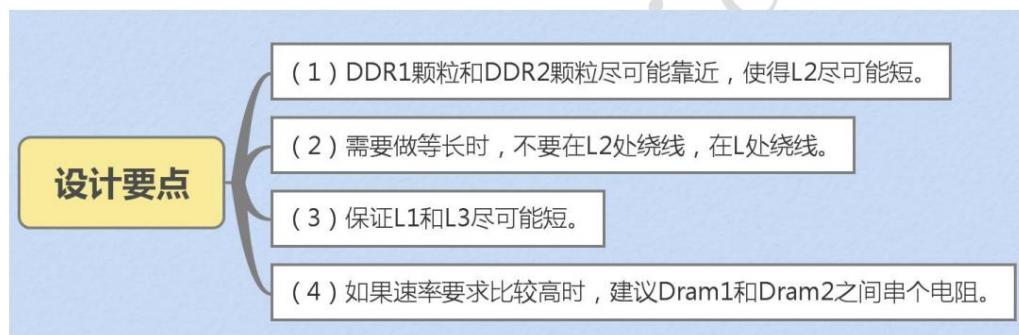


Figure 3-100 Chain topology design points

(22) Where there is space, increase the spacing between traces to reduce crosstalk.

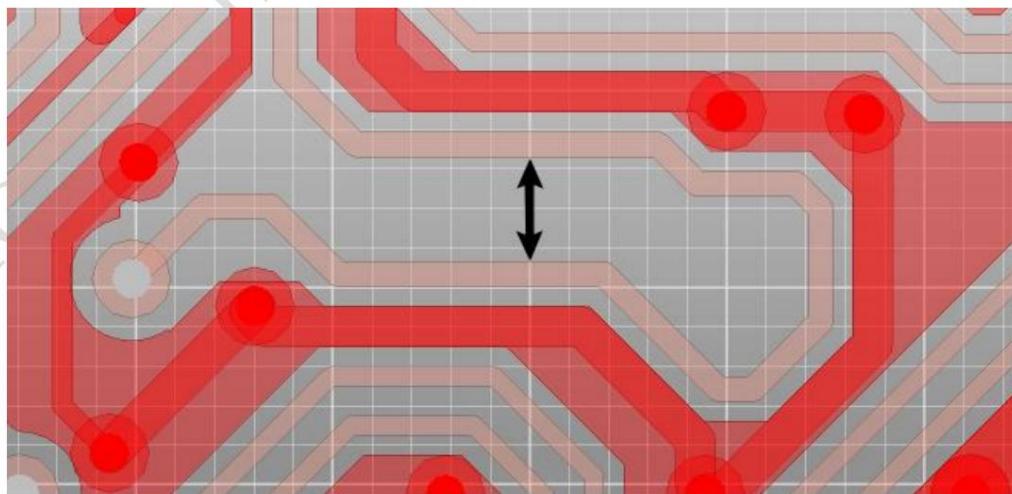


Figure 3-101 Schematic diagram of increasing signal spacing in locations with space

3.3.3.1 LPDDR3

Table 3-7 LPDDR3 routing requirements

parameter	Require
Single-ended signal impedance	50 Ohm ± 10%
Differential signal impedance	100 Ohm ± 10%
The same length between DQ and DQS (within the same byte)	≥ 600mil
Equal length between DM and DQS (within the same byte)	≥ 600mil
Equal length between address, control lines and CLK	≥ 60mil
DQS_P and DQS_N are of equal length (within the same byte)	≥ 12mil
Equal length between CLK_P and CLK_N	≥ 12mil
Equal length between DQS and CLK	≥ 1700mil
The spacing between different bytes (airgap)	≥ 2 times the trace width
The airgap between DQs in the same byte	≥ 2 times the trace width
The airgap between DQ and DQS in the same byte	Recommended ≥ 3 times the trace width At least 2 times the trace width
The distance between address and control lines (airgap)	≥ 2 times the trace width
The airgap between CLK and other signal lines	Recommended ≥ 3 times the trace width At least 2 times the trace width

3.3.3.2 DDR3/DDR3L

Table 3-8 DDR3/DDR3L routing requirements

parameter	Require
Single-ended signal impedance	50 Ohm ± 10%
Differential signal impedance	100 Ohm ± 10%
The same length between DQ and DQS (within the same byte)	≥ 600mil
Equal length between DM and DQS (within the same byte)	≥ 600mil
Equal length between CS, ODT, CKE and CLK	≥ 60mil
The length between address, control lines and CLK except CS, ODT, CKE is ≥ 600mil	
DQS_P and DQS_N are of equal length (within the same byte)	≥ 12mil
Equal length between CLK_P and CLK_N	≥ 12mil
Equal length between DQS and CLK	≥ 2000mil
The airgap between different bytes The airgap	≥ 2 times the trace width
between DQs in the same byte	≥ 2 times the trace width
The airgap between DQ and DQS in the same byte	Recommended ≥ 3 times the trace width At least 2 times the trace width
The distance between address and control lines (airgap)	≥ 2 times the trace width
The airgap between CLK and other signal lines	Recommended ≥ 3 times the trace width At least 2 times the trace width

3.3.3.3 DDR4

Table 3-9 DDR4 routing requirements

parameter	Require
Single-ended signal impedance	50 Ohm ± 10%
Differential signal impedance	100 Ohm ± 10%
The same length between DQ and DQS (within the same byte)	≥ 600mil
Equal length between DM and DQS (within the same byte)	≥ 600mil
Equal length between CS, ODT, CKE and CLK	≥ 60mil
The length between address, control lines and CLK except CS, ODT, CKE is ≥ 600mil	
DQS_P and DQS_N are of equal length (within the same byte)	≥ 12mil
Equal length between CLK_P and CLK_N	≥ 12mil
Equal length between DQS and CLK	≥ 2000mil
The spacing between different bytes (airgap)	≥ 2 times the trace width
The airgap between DQs in the same byte	≥ 2 times the trace width
The airgap between DQ and DQS in the same byte	Recommended ≥ 3 times the trace width At least 2 times the trace width
The distance between address and control lines (airgap)	≥ 2 times the trace width
The airgap between CLK and other signal lines	Recommended ≥ 3 times the trace width At least 2 times the trace width

3.3.3.4 LPDDR4

Table 3-10 LPDDR4 routing requirements

parameter	Require
Single-ended signal impedance	50 Ohm ± 10%
Differential signal impedance	100 Ohm ± 10%
The same length between DQ and DQS (within the same byte)	≥ 600mil
Equal length between DM and DQS (within the same byte)	≥ 600mil
Equal length between address, control lines and CLK	≥ 600mil
DQS_P and DQS_N are of equal length (within the same byte)	≥ 12mil
Equal length between CLK_P and CLK_N	≥ 12mil
Equal length between DQS and CLK	≥ 1700mil
The airgap between different bytes The airgap	≥ 2 times the trace width
between DQs in the same byte	≥ 2 times the trace width
The airgap between DQ and DQS in the same byte	Recommended ≥ 3 times the trace width At least 2 times the trace width
The distance between address and control lines (airgap)	≥ 2 times the trace width
The airgap between CLK and other signal lines	Recommended ≥ 3 times the trace width At least 2 times the trace width

3.3.3.5 LPDDR4X

Table 3-11 LPDDR4X routing requirements

parameter	Require
Single-ended signal impedance	50 Ohm ± 10%
Differential signal impedance	100 Ohm ± 10%
The same length between DQ and DQS (within the same byte)	≥ 600mil
Equal length between DM and DQS (within the same byte)	≥ 600mil
Equal length between address, control lines and CLK	≥ 600mil
DQS_P and DQS_N are of equal length (within the same byte)	≥ 12mil
Equal length between CLK_P and CLK_N	≥ 12mil
Equal length between DQS and CLK	≥ 1700mil
The spacing between different bytes (airgap)	≥ 2 times the trace width
The airgap between DQs in the same byte	≥ 2 times the trace width
The airgap between DQ and DQS in the same byte	Recommended ≥ 3 times the trace width At least 2 times the trace width
The distance between address and control lines (airgap)	≥ 2 times the trace width
The airgap between CLK and other signal lines	Recommended ≥ 3 times the trace width At least 2 times the trace width

3.3.1 PCIe2.0

Table 3-12 Cabling Requirements - PCIE2.0

parameter	Require
Trace impedance	Differential 90ohm ±10%
Maximum delay difference within a differential pair	<6mil
Equal length requirement between differential pairs	<6inches
Trace length	<6inches
Capacitance requirements	100nF ±20%, 0201 package is recommended
Airgap	It is recommended to be greater than or equal to 4 times the PCI-E line width
Maximum delay difference within the differential pair (REFCLK)	<12mil
Trace impedance (REFCLK)	Differential 100ohm±10%
PCI-E and other signal spacing (airgap)	It is recommended to have a width greater than or equal to 5 times the PCI-E line width, and at least 4 times the PCI-E line width.
The number of vias allowed for each signal	No more than 2 are recommended

(1) The number of GND vias in the PCIE interface of the RK3528 BGA area is as follows. It is not recommended to reduce the number of vias, which will affect the signal quality.

quantity.

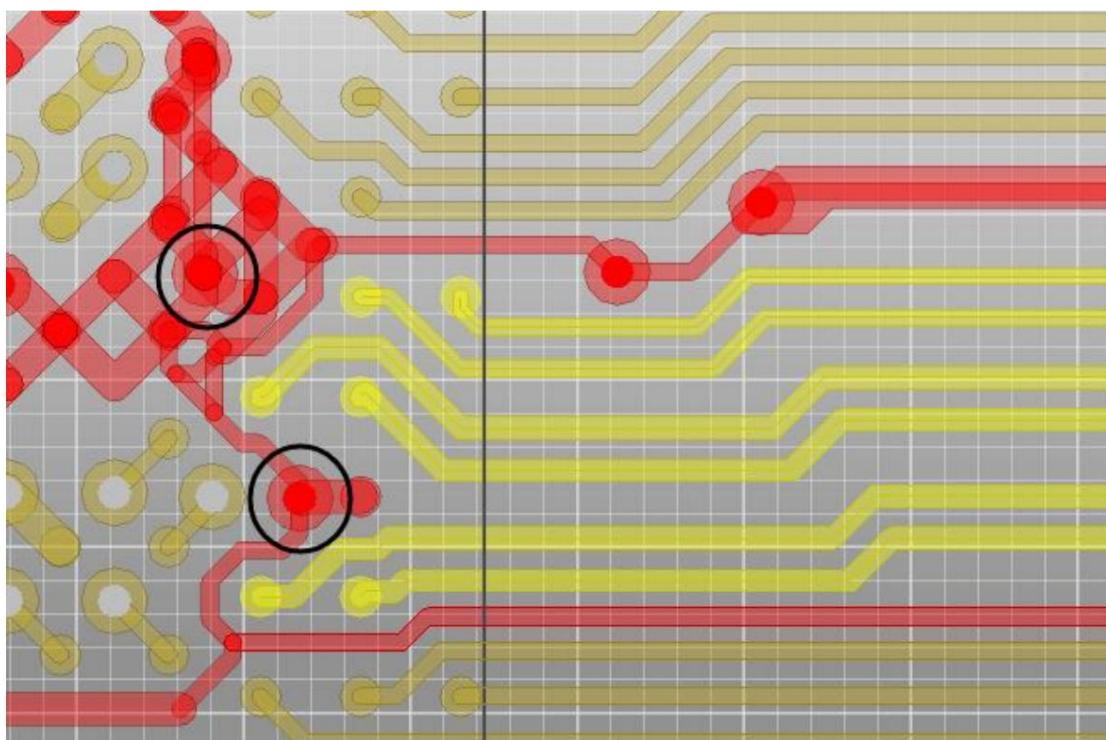


Figure 3-102 Diagram of the number of GND vias

(2) It is recommended to ground the entire PCIE2.0 interface signal group, and drill a GND via every 300mil.

A complete GND plane reference is required.

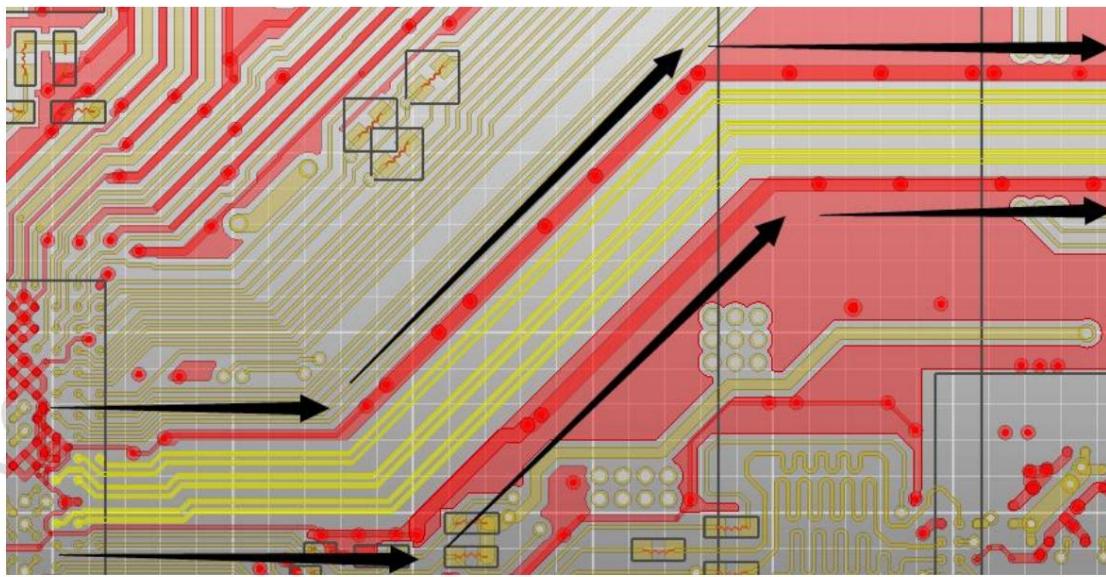


Figure 3-103 Schematic diagram of ground wire

3.3.2 HDMI 2.0

Table 3-13 Cabling Requirements - HDMI 2.0

parameter	Require
Trace impedance	Differential 100ohm ±10%
Maximum delay difference within a differential pair	<6mil
Equal length requirement between differential pairs	<480mil
Trace length	<5 inches
Spacing between differential pairs	It is recommended to be greater than or equal to 4 times the HDMI cable width
HDMI and other signal distance (airgap)	It is recommended to be greater than or equal to 4 times the HDMI cable width
The number of vias allowed for each signal	No more than 2 are recommended
ESD	I/O ground capacitance does not exceed 0.2pF

(1) The number of GND vias for the HDMI interface in the RK3528 BGA area is as follows. It is not recommended to reduce the number of vias, as this will affect the signal quality.

quantity.

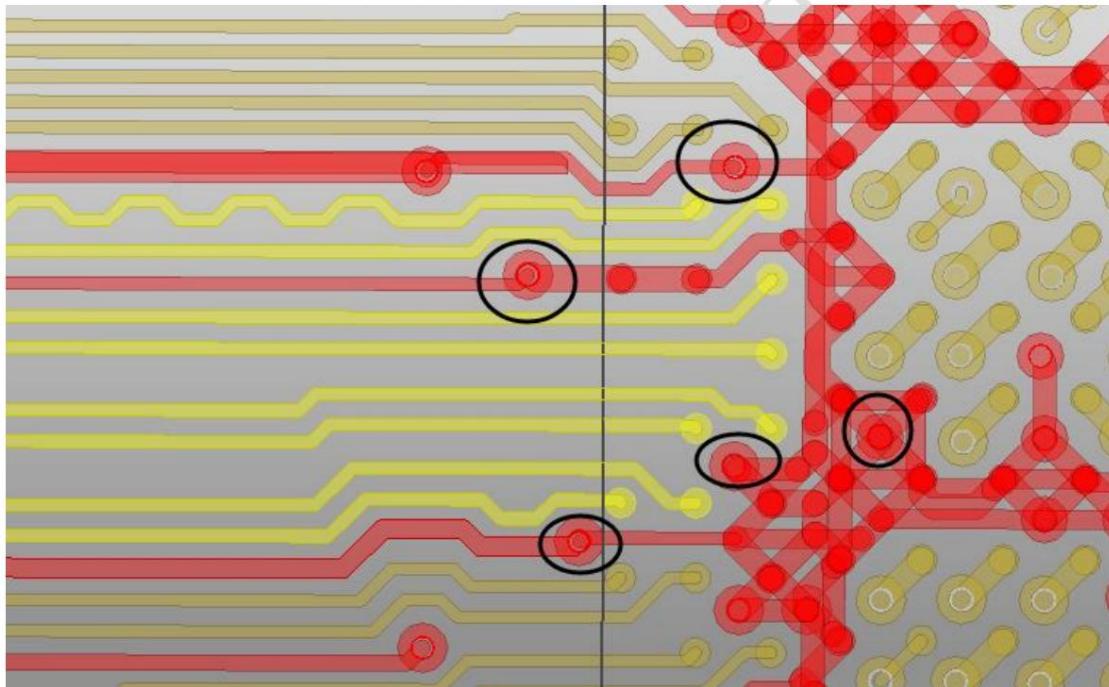


Figure 3-104 Schematic diagram of the number of GND vias

(2) It is recommended that the HDMI2.0 signal be grounded as a whole, and the CLK signal be grounded separately. A GND should be placed every 300mil.

HDMI2.0 signals need to reference a complete GND plane.

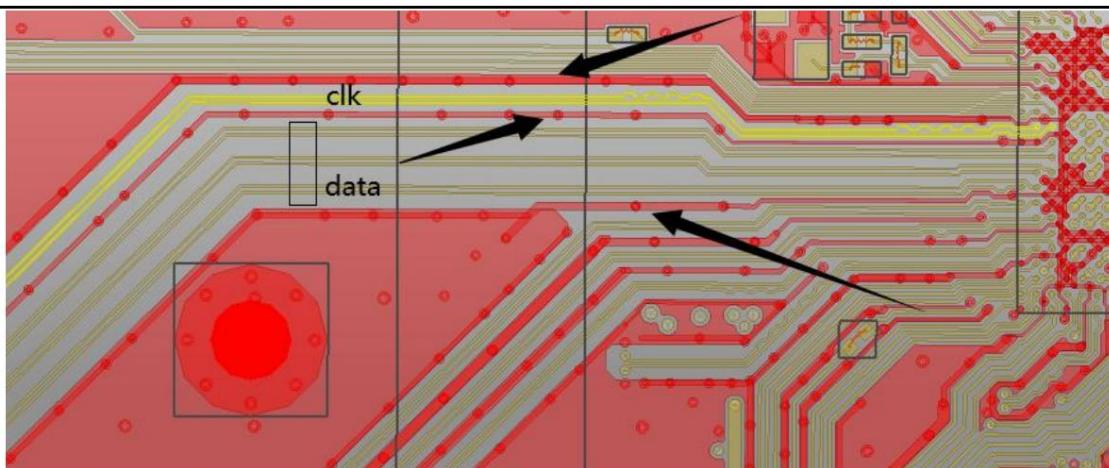


Figure 3-105 Ground wire diagram

3.3.3 USB 2.0

Table 3-14 Cabling Requirements - USB 2.0

parameter	require
Trace impedance	Differential 90ohm ±10%
Maximum delay difference within a differential pair	<20mil
Trace length	<6 inches
The number of vias allowed for each signal	It is recommended that no more than 4 and no more than 6

3.3.4 USB 3.0

Table 3-15 Cabling Requirements - USB 3.0

parameter	require
Trace impedance	Differential 90ohm ±10%
Maximum delay difference within a differential pair	<6mil
Trace length	Host device <6 inches, Device and OTG device <5 inches
Capacitance requirements	100nF ±20%, 0201 package is recommended
Airgap	It is recommended to be greater than or equal to 4 times the USB cable width
Airgap between USB and other signals	It is recommended to be greater than or equal to 4 times the USB cable width
The number of vias allowed for each signal	No more than 2 are recommended
ESD	I/O to ground capacitance does not exceed 0.2pF

(1) The number of GND vias for the USB3.0 interface in the RK3528 BGA area is as follows. It is not recommended to reduce the number of vias, as this will affect the signal quality.

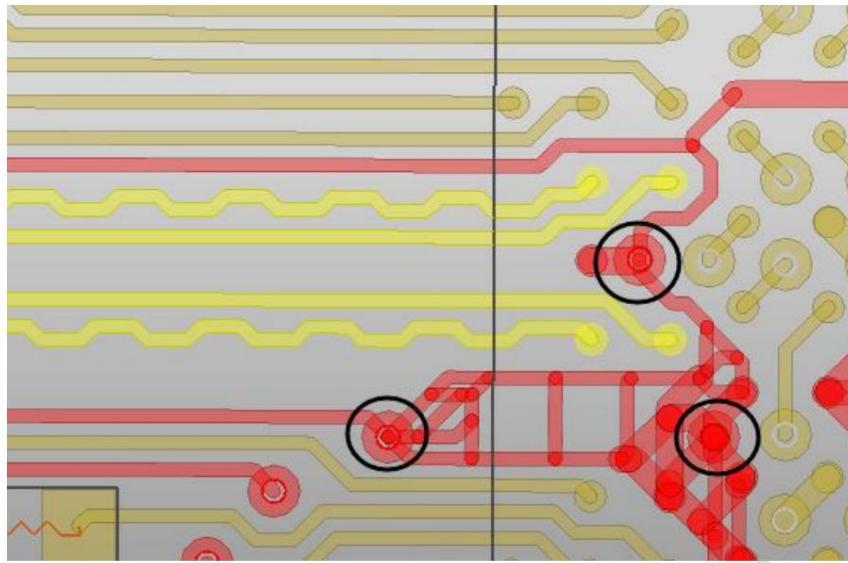


Figure 3-106 Diagram of the number of GND vias

(2) It is recommended that the USB3.0 interface signal be grounded as a whole, and a GND via be drilled every 300mil or less of the ground line.

Refer to the intact GND plane.

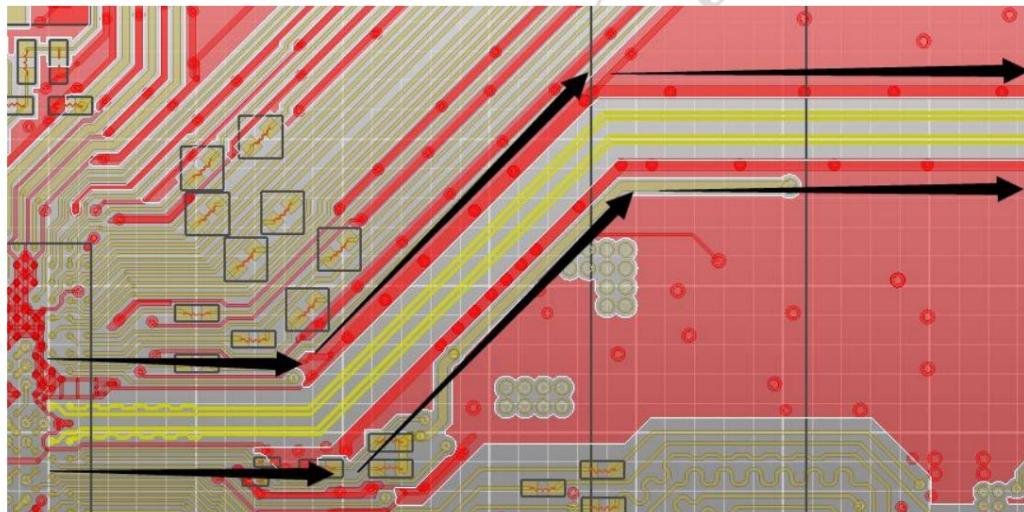


Figure 3-107 Schematic diagram of ground wire

3.3.5 eMMC

Table 3-16 Wiring Requirements - eMMC

parameter	Require
Trace impedance	Single-ended 50ohm±10%
The length between the clock (CLK, STRB) and the data is equal	<120mil
Trace length	<3 inches
The distance between eMMC signal lines (airgap)	At least 2 times the eMMC line width
between eMMC and other signals (airgap)	It is recommended to use 3 times the line width, at least 2 times the eMMC line width
The number of vias allowed for each signal	No more than 2 are recommended

(1) It is recommended to ground the CLK and STRB signals. A GND via should be drilled every 500mil or less of the ground line. For example:

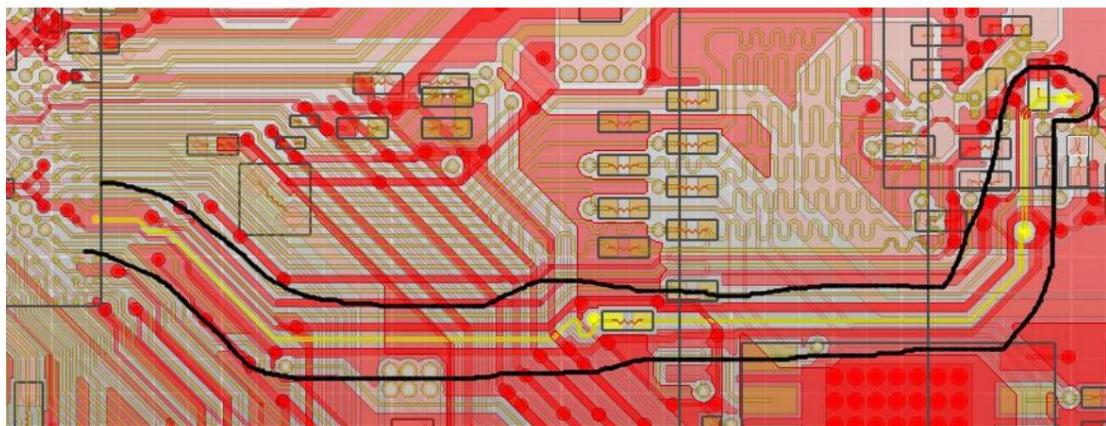


Figure 3-108 Schematic diagram of ground wire

(2) To ensure signal quality, it is recommended that the signal refer to the GND plane. In our reference design, the first layer of signal refers to the second layer of GND plane.

The signal on the fourth layer refers to the GND plane on the third layer, as shown in the figure below.

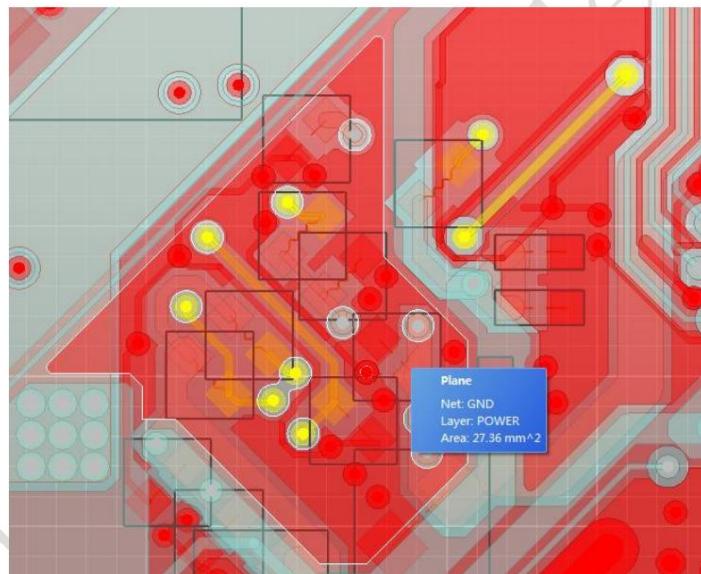


Figure 3-109 Schematic diagram of the fourth layer routing reference third layer GND plane

3.3.6 SDMMC

Table 3-17 Wiring Requirements - SDMMC

parameter	Require
Trace impedance	Single-ended 50ohm ±10%
The length between clock and data is equal	<120mil
Trace length	<4 inches (50MHz\leqCLK frequency \leq200Mhz) <6 inches (CLK frequency \geq 50Mhz)
Spacing between SDMMC signal lines (airgap)	At least 2 times the SDMMC line width
The number of vias allowed for each signal	No more than 2 are recommended

3.3.7 SDIO

Table 3- 18 Cabling Requirements - SDIO

parameter	Require
Trace impedance	Single-ended 50ohm ±10%
The length between clock and data is equal	<120mil
Trace length	<4 inches (50Mhz≤CLK frequency ≤200Mhz) <6 inches (CLK frequency ≥ 50Mhz)
Spacing between SDIO signal lines (airgap)	At least 2 times the SDIO line width
The number of vias allowed for each signal	No more than 2 are recommended

3.3.8 FSPI

Table 3-19 Wiring Requirements - FSPI

parameter	Require
Trace impedance	Single-ended 50ohm ±10%
Clock and data are equal in length	<200mil
Trace length	<4 inches
The distance between FSPI signal lines (airgap)	At least 2 times the line width

3.3.9 RGMII

Table 3-20 Wiring Requirements - RGMII

parameter	Require
Trace impedance	Single-ended 50ohm ±10%
(TXD{0-3}, TXEN) to TXCLK equal length	<120mil
(RXD{0-3}, RXDV) to RXCLK equal length	<120mil
Trace length	<6 inches
Spacing between RGMII signal lines (airgap)	Recommended ≥2 times RGMII line width
RGMII and other signal spacing (airgap)	It is recommended to use 3 times the RGMII line width, at least 2 times the RGMII line width

(1) It is recommended to do grounding for the CLK signal. A GND via should be drilled every 500mil or less of the ground line. For example:

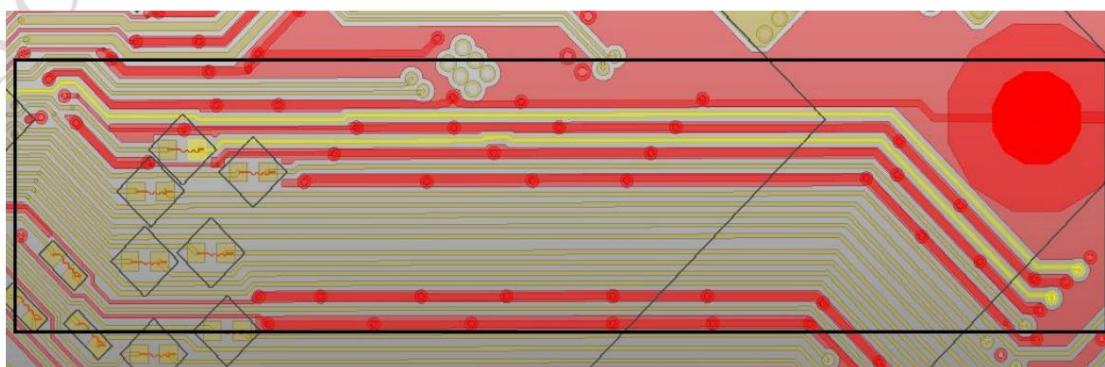


Figure 3-110 Schematic diagram of ground wire

3.3.10 100base-t

Table 3-21 Cabling Requirements - 100base-t

parameter	Require
Trace impedance	Differential 100ohm ±10%
Maximum delay difference within a differential pair	<20mil
Differential pair spacing (airgap)	It is recommended to be greater than or equal to 3 times the line width
Airgap between 100base-t and other signals	It is recommended to be greater than or equal to 3 times the line width
Trace length	<4inches
The number of vias allowed for each signal	No more than 2 are recommended

3.3.11 ACODEC&CVBS Design

ÿ During the overall layout, place the PA and AV connectors as close to the chip as possible, and shorten the ACODEC & CVBS analog signal traces as much as possible;

The decoupling capacitors for the PA chip power supply must be placed as close as possible to the power pins of the PA chip.

ÿ The ACODEC & CVBS trace width should be as thick as possible, and 12 mil or more is recommended;

ÿ The CVBS 75ohm resistor must be placed close to the chip;

ÿ The CVBS filter circuit must be placed close to the AV socket;

ACODEC & CVBS signals require separate grounding throughout the entire process, and ground vias must be provided within 300mil intervals between ground traces.

ÿ The layer adjacent to the ACODEC&CVBS signal must be a ground plane and cannot be a power plane;

ÿ ACODEC & CVBS signals should be kept away from high-speed signal lines such as DRAM, and avoid interference signals such as PWM and DC-DC power

Inductors: Do not route on layers adjacent to high-speed signal lines; Do not drill holes or change layers near high-speed signal lines; Do not route through inductor areas.

Keep away from RF signals and devices;

ÿ The ACODEC and GND lines need to be in differential mode. As shown in the figure below: AOL/AOR are connected from the PA end (terminal position) to the ground.

Follow the GND trace and merge as close to the SOC end (source end) as possible, and connect to the GNDBALL at the bottom of the chip.

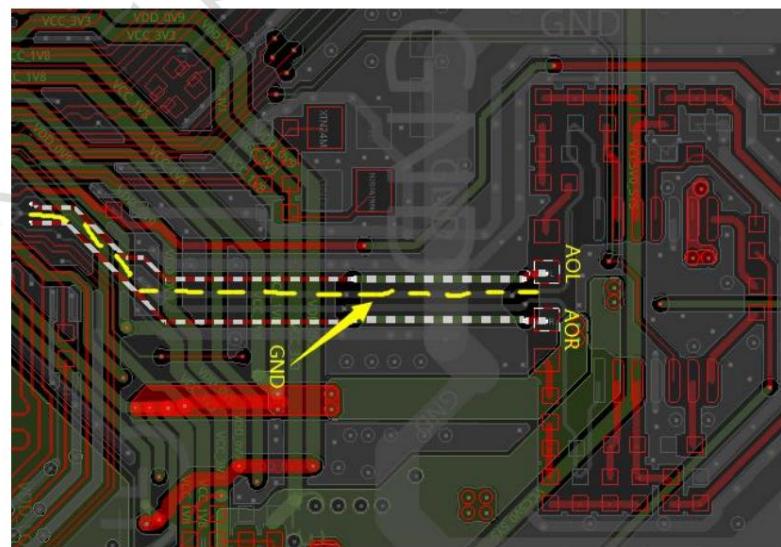


Figure 3-111 ACODEC wiring diagram

ÿ All signal TVS tubes of AV socket should be placed as close to the connector as possible. The signal topology is: AV socket → TVS → chip pins.

When ESD occurs, the ESD current must first pass through the TVS device to attenuate. There should be no stubs on the TVS device traces.

It is recommended to increase the number of ground vias for the TVS ground pin as much as possible, ensuring at least two 0.4*0.2mm vias to enhance the electrostatic discharge capability.

3.3.12 Audio Interface Circuit PCB Design

For the digital audio interface of the RK3528 platform, the routing requirements are as follows:

- ÿ It is recommended to connect a 22ohm resistor in series with all CLK signals and place them close to the RK3528 to improve signal quality;
- ÿ All CLK signal traces must not be close together to avoid crosstalk; they need to be independently grounded, and the trace spacing of the ground must be within 300mil.

There are ground vias:

ÿ The decoupling capacitors of each IO power domain of the chip must be placed on the back of the corresponding power pins; for single-sided mounting, the decoupling capacitors closest to the chip should be placed on the back of the corresponding power pins.

Place close together:

ÿ If an I2S interface is connected to multiple devices, the related CLks should be connected in a daisy-chain topology.

- ÿ If a PDM interface is connected to multiple devices, the related CLks should be connected in a daisy-chain topology.

In the case of margin, both CLks in a group of PDM interfaces can be used to optimize routing branches.

ÿ It is recommended to use ground for the entire SPDIF signal. Ground vias must be provided within 300mil intervals between ground traces.

For the requirements of audio signal routing of peripherals, please refer to the design guide of the corresponding device. If there is no emphasis, please refer to the following instructions:

- ÿ The SPKP/SPKN signal coupling routing of the speaker should be wrapped with ground as a whole. The line width should be calculated according to the peak current of the output and should be minimized.

Short traces are used to control line

resistance. If there are ferrite beads, LC filters and other devices placed on the speaker amplifier output, it is recommended to place them close to the amplifier output to optimize EMI. The left and right

channel outputs of the Headphone should be independently grounded to avoid crosstalk and optimize isolation. The recommended trace width is greater than 10mil. When the microphone is connected single-ended,

the MIC signal is routed separately and grounded separately. When the microphone is connected differentially, especially in

most pseudo-differential cases, it should also be routed differentially and grounded as a whole. The recommended trace width for the microphone signal is more than 8mil. All audio signals

should be separated from high-speed signal lines such as LCD and DRAM. It is forbidden to

route on the adjacent layers of high-speed signal lines. Audio signals

The adjacent layer must be a ground plane, and drilling and changing layers near high-speed signal lines is prohibited;

- ÿ All audio signal lines should be routed away from inductive areas, RF signals, and devices;
- ÿ For the TVS protection diodes of the headphone jack and microphone, they should be placed as close to the connector as possible, and the signal topology is: headphone jack/microphone → TVS → IC; this ensures that when ESD occurs, the ESD current is first attenuated through the TVS device; there should be no stubs on the TVS device routing, and it is recommended to increase the ground vias for the TVS ground pin as much as possible, ensuring at least two 0.4mm*0.2mm vias to enhance the electrostatic discharge capability.

3.3.13 WIFI/BT PCB Design

ÿ When laying out the overall layout, the WIFI module should be placed appropriately, away from DDR, HDMI, USB, LCD circuits and speakers that are prone to interference.

Module or connector:

ÿ The TOP layer below the module is not allowed to be routed. The reference plane must be a complete ground plane. The SDIO/PCIe/UART/PCM signal lines are built

It is recommended to bypass the module projection area and connect to the module pins;

ÿ The crystal circuit layout needs to be given priority. It should be placed on the same layer as the chip and as close as possible to avoid drilling vias. The crystal traces should be as short as possible, away from interference sources, and as close to the antenna area as possible.

ÿ The crystal and clock signals need to be grounded throughout. At least one GND via should be added every 100mil of the ground line.

Verify that the ground reference surface of the adjacent layer is intact;

ÿ When laying out the crystal circuit, if it is placed on a different layer from the chip, the crystal routing and grounding must be done throughout to avoid interference;

ÿ 32.768k should be routed separately and grounded, and at least one GND via should be added every 400mil of the grounding line;

ÿ For SDIO WIFI, the SDIO signal PCB design requirements are as follows: Section 3.4.10;

ŷ For PCIe Wi-Fi, see Section 3.4.4 for PCIe signal PCB design requirements. ŷ When laying out the module's inductor,

ensure that the trace exits the inductor, passes through the capacitor, and then enters the module's power pin.

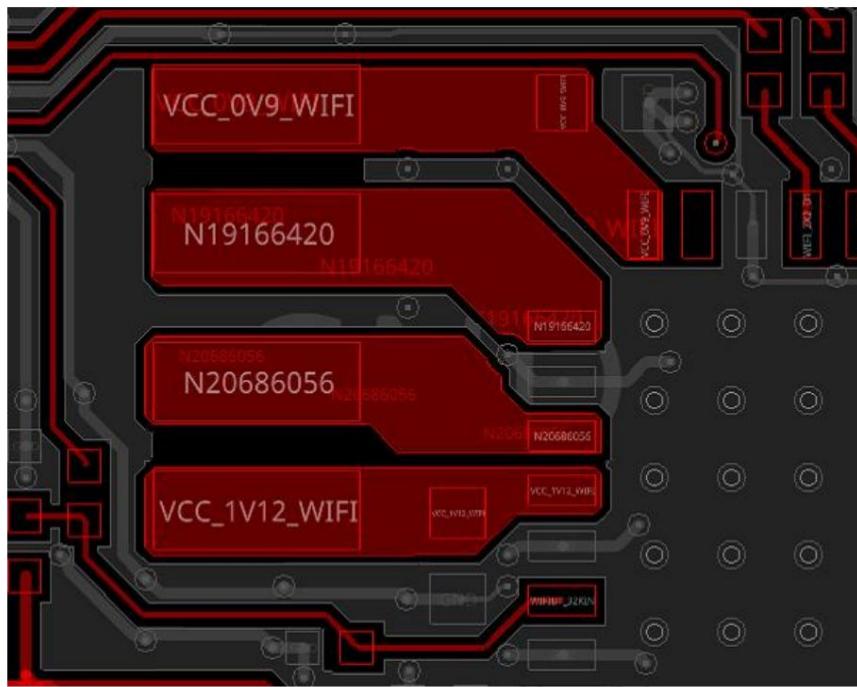


Figure 3-112 Schematic diagram of the inductor and capacitor wiring of the WiFi module

ŷ The module's power decoupling capacitor must be close to the module's power pin; ŷ The

module's VBAT pin trace width must be greater than 40mil; ŷ The longer the antenna wiring,

the greater the energy loss. Therefore, when designing, the antenna path should be as short as possible, without branches, and should be as short as possible.

layer;

ŷ The antenna matching circuit must be close to the antenna base, the antenna line is 50 ohms, and the reference ground is guaranteed to be complete. The impedance should not change suddenly.

There are other signal lines or power supplies; the accompanying ground of the routing needs to be connected to the main ground reference plane using a ground wall;

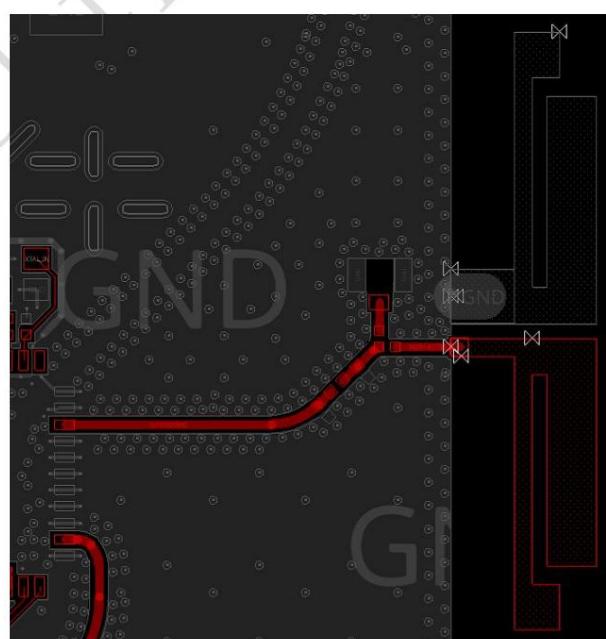


Figure 3-113 WIFI module antenna wiring diagram

No other signal lines or power supplies are allowed on any layers below the module's antenna and antenna routing area.

ÿ If it is a 2X2 MIMO antenna interface, the direction of the line between the two antenna ports needs to consider the positions of the two antennas.

The locations need to be as far away as possible to avoid interference, and consider placing them vertically to avoid interference with each other.

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4 Thermal design recommendations

Good thermal design is particularly important for improving RK3528 product performance, system stability, and product safety.

4.1 Thermal simulation results

For the RK3528 WBBGA401L_13.5x13.3mm_Pitch 0.6mm/0.65mm package, the 4-layer PCB based on EVB adopts Finite Element Modeling (FEM) can produce a thermal resistance simulation report based on JEDEC JESD51-2

The standard provides that the system design and environment during application may be different from the JEDEC JESD51-2 standard and need to be analyzed based on the application conditions.



Notice

Thermal resistance is a reference value when the PCB does not have a heat sink. The specific temperature is related to the design, size, thickness, material and other physical factors of the single board.

4.1.1 Summary of Results

The thermal resistance simulation results are shown in the following table:

Table 4-1 RK3528 thermal resistance simulation report results

Package (PI-ED-FCCSP)	(°C/W)	(°C/W)	(°C/W)
JEDEC PCB	22.81	9.295	6.874

Note: The data is simulated and for reference only. Please refer to the actual test.

4.1.2 PCB Description

The PCB structure used for thermal resistance simulation is as follows:

Table 4-2 PCB structure for RK3528 thermal resistance simulation

JEDEC PCB	PCB Dimension L x W	140 x 180mm
	PCB Thickness	1.6mm
	Number of Cu Layer	4-layers

4.1.3 Explanation of terms

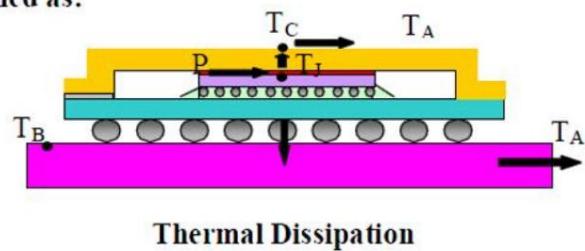
The terms in this chapter are explained as follows:

- ÿ TJÿ The maximum junction temperatureÿ
- ÿ TAÿ The ambient or environment temperatureÿ
- ÿ TCÿ The maximum compound surface temperatureÿ
- ÿ TBÿ The maximum surface temperature of PCB bottomÿ
- ÿ Pÿ Total input power

The thermal parameter can be define as following

1. Junction to ambient thermal resistance, θ_{JA} , defined as:

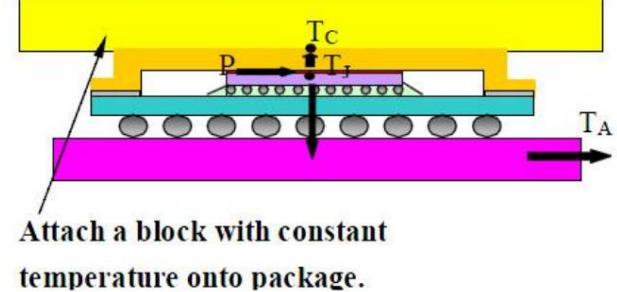
$$\theta_{JA} = \frac{T_J - T_A}{P} ; \quad (1)$$



Definition of Figure 4-1

2. Junction to case thermal resistance, θ_{JC} , defined as:

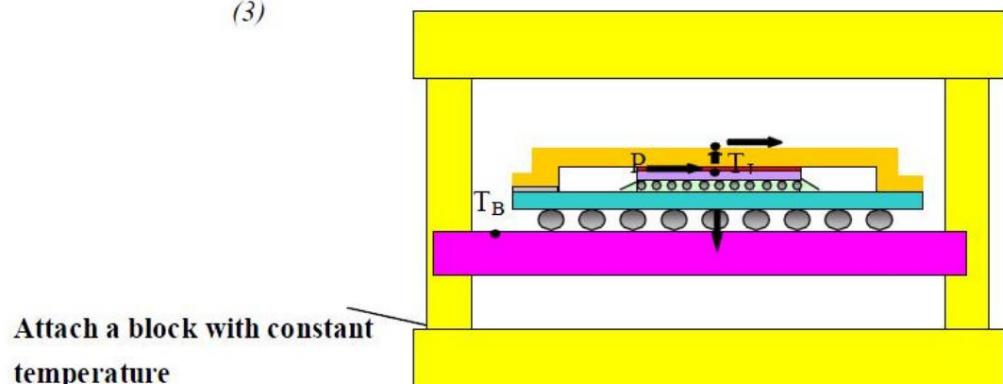
$$\theta_{JC} = \frac{T_J - T_C}{P} ; \quad (2)$$



Definition of Figure 4-2

3. Junction to board thermal resistance, θ_{JB} , defined as:

$$\theta_{JB} = \frac{T_J - T_B}{P} ; \quad (3)$$



Definition of Figure 4-3

4.2 Chip Internal Thermal Control Method

4.2.1 Temperature control strategy

In the Linux kernel, a temperature control framework, Linux Generic Thermal System Drivers, is defined, which can control the temperature through different strategies.

There are three commonly used strategies to control the temperature of the system:

Power allocator: The temperature control strategy introduces PID (proportional-integral-derivative) control to dynamically allocate power to each cooling device based on the current temperature. When the temperature is low, the available power is large, which means the operating frequency is high. As the temperature rises, the available power gradually decreases, and the operating frequency also gradually decreases, thus achieving temperature-based frequency limit.

Step wise: Cooling devices reduce their frequencies step by step based on the current temperature.

Fair share: Cooling devices with more frequency levels are prioritized for frequency reduction.

Userspace: No frequency limit.

The RK3528 chip has a T-sensor inside to detect the on-chip temperature, and uses the Power_allocator strategy by default.

4.2.2 Temperature control configuration

The RK3528 SDK can provide temperature control strategies for CPU and GPU respectively. For specific configuration, please refer to

[Rockchip_Developer_Guide_Thermal_CN.pdf](#) (Please contact our FAE window for a copy).

4.3 Circuit Thermal Design Reference

4.3.1 Circuit Schematic Thermal Design Reference

Under the premise of ensuring stability, improve overall power efficiency, such as using less LDO with high voltage difference, reducing the power supply itself in the power conversion process.

Heat generated during the process;

According to the actual product, try not to power on the modules that are not used by the chip or let the software do the power down processing; Choose materials with high thermal conductivity, and estimate the size of the heat sink required based on the product definition, usage environment and other conditions.

Try to use a larger heat sink.

4.3.2 PCB Thermal Design Reference

Among RK3528 products, the RK3528 chip is the device that generates the most heat, and all heat dissipation treatments are mainly focused on the chip.

In addition to RK3528, other major heat-generating components include: LDO, inductor used in DC-DC.

Reasonable structural design can ensure heat exchange between the inside of the machine and the outside air;

When laying out the overall layout, devices with high power consumption or easy to generate heat should be evenly distributed to avoid local overheating. It is recommended that RK3528 and DC-DC be used.

When placing, do not place them too close or too far away. It is recommended to keep them 20mm-50mm apart. Try not to place them on the edge of the board.

Poor heat dissipation;

It is recommended to increase the copper content of the board as much as possible. It is recommended to use 1oz copper thickness. Try to use multiple layers as ground planes, and the other layers should be used for power supply and signal.

In addition to routing, try to lay out a ground plane to use a large area of copper foil to dissipate heat;

RK3528 VDD_LOGIC, VDD_GPU, VDD_CPU, VCC_DDR have relatively large currents, so the traces or copper must be

Meet the current carrying capacity, otherwise the temperature rise may increase;

For chips with EPAD, the EPAD should be filled with as many vias as possible, the adjacent layer must be a ground plane, and the copper foil on the back should be as complete as possible.

It is recommended to use bare copper on the back to facilitate heat dissipation.

ÿ The GND pins of the RK3528 chip are arranged in a "well" shape on the top layer and cross-connected. The recommended trace width is 10 mil to facilitate chip heat dissipation.

ÿ For the GND pin of the RK3528 chip, it is recommended to ensure that each ball has a corresponding ground via, at least every 1.5 balls

Corresponding to a via, a heat conduction path is increased, and the adjacent layer must be a ground plane, which is conducive to chip heat dissipation;

ÿ For the decoupling capacitor ground pad on the back of the RK3528 chip, it is recommended to use full copper cladding instead of using flower holes for connection. Try to keep the ground copper intact.

To improve heat dissipation;

ÿ In open areas, without damaging the power layer, try to increase ground vias and increase heat conduction paths to improve heat dissipation.

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5. ESD/EMI Protection Design

5.1 Overview

This chapter provides suggestions for ESD/EMI protection design in RK3528 product design to help customers better improve the product's anti-static,

Anti-electromagnetic interference level.

5.2 Terminology

The terms in this chapter are explained as

follows: ý ESD (Electro-Static Discharge): electrostatic discharge; ý EMI (Electromagnetic

Interference): electromagnetic interference, which includes conducted interference and radiated interference.

5.3 ESD Protection

ý Isolate the mold and retract the connector as far as possible into the shell, so that the distance for static electricity to be discharged to the internal circuit is longer.

The quantity becomes weaker, and the test standard changes from contact discharge conditions to air discharge, etc.

ý Protect and isolate sensitive components during PCB layout; ý Place the RK3528 chip and core

components in the middle of the PCB as much as possible during layout. If they cannot be placed in the middle of the PCB, ensure that the shielding cover is away from the PCB.

The distance from the edge of the board should be at least 2mm, and the shielding cover should be reliably grounded;

ý The PCB should be laid out according to the functional modules and signal flow. Each sensitive part should be independent of each other. It is best to isolate the parts that are prone to interference.

isolation;

ý ESD devices must be properly placed, generally at the source, meaning at interfaces or locations where static electricity is released. ý Components should be placed away from the board edges and

at a certain distance from connectors. ý The PCB surface must have a good GND loop, and

each connector must have a good GND connection on the surface. Shielding covers should be connected to the surface ground whenever possible, and multiple ground holes should be drilled at the shield

cover soldering points for grounding. To achieve this, traces should not be routed on the surface of the connectors, and traces should not significantly cut through the surface copper.

ý Avoid routing traces along the edges of the surface board and

drill more ground vias; ý When necessary, isolate the signal from the ground; ý

Expose more copper to enhance electrostatic discharge, or to facilitate remedial measures such as adding foam; ý If board-to-board connections are

achieved via connectors, it is recommended that all signals be connected in series with resistors of a certain resistance (between 2.0ohm and 10ohm, depending on whether they meet SI testing requirements)

and that TVS devices be reserved to improve anti-static surge capabilities;

ý The distance between key signals such as Reset, clock, interrupt and other sensitive signals and the board edge should not be less than 5mm; ý If other

peripheral chips have Reset pins, it is recommended to add a 100nF capacitor close to the pin, and the ground pad of the capacitor must have a

0402 ground vias. If space allows, it is recommended to drill more than two for better grounding.

ý When the whole machine is designed as a floating device, it is recommended that each interface should not be

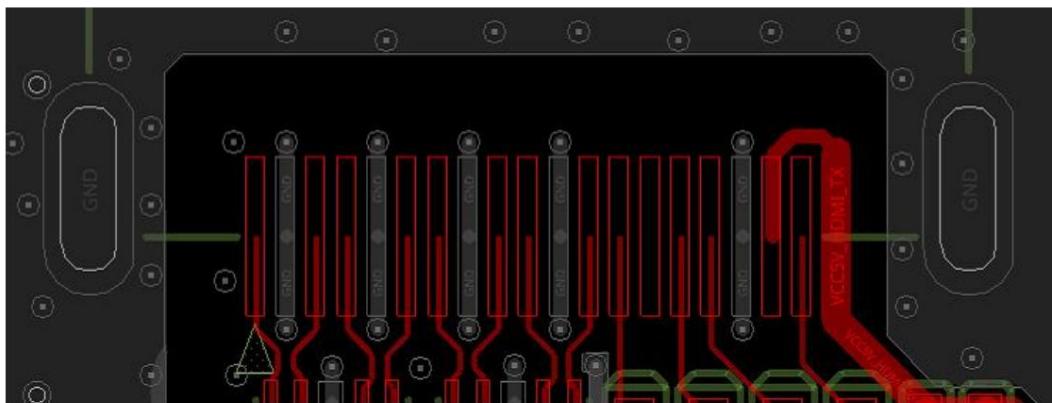
designed separately; ý When the machine shell is metal, the power supply is three-hole, and the metal shell must be well connected to the ground;

ý Reserve a space for the shielding cover, and the shielding cover should be connected to the surface ground as much as possible, and drill more ground holes at the shielding cover welding point to achieve this.

design point requires that the wiring of each connector should not be on the surface, and the wiring should not cut through the surface copper sheet on a large scale;

ÿ Isolate from the PCB so that static electricity can only be released in certain areas, such as the individual vias of the ground pins of the socket and the connection with the inner layer.

Keepout the surface PCB, and keep the surface copper foil and pins as far away as possible, that is, keep sensitive signals away from areas prone to static discharge (surface copper foil), etc. As shown in the figure, the distance between the HDMI signal and GND on the surface is isolated.



5.4 EMI Protection

Electromagnetic interference consists of three elements: interference source, coupling channel, and sensitive equipment. Since we cannot address sensitive equipment, addressing EMI requires addressing the interference source and coupling channel. The best way to resolve EMI is to eliminate the interference source. If this is not possible, find ways to cut off the coupling channel or avoid the antenna effect.

ÿ It is generally difficult to completely eliminate interference sources on a PCB. However, methods such as filtering, grounding, balancing, impedance control, and improving signal quality (such as termination) can be used to address them. These methods are generally combined, but good grounding is the most basic requirement.

ÿ Commonly used materials for EMI include shielding covers, special filters, resistors, capacitors, inductors, magnetic beads, common mode inductors/magnetic rings, and absorbing materials.

Materials, spread spectrum devices, etc.

ÿ Filter selection principle: If the load (receiver) is high impedance (general single-ended signal interfaces are high impedance, such as SDIO,

RBG, CIF, etc.), select capacitive filter components and connect them to the line; if the load (receiver) is low impedance (such as power output

If the signal quality exceeds the SI tolerance, the filter must be connected in series with the circuit.

Interfaces generally use common-mode inductors to suppress EMI;

ÿ The shielding measures on the PCB must be well grounded, otherwise it may cause radiation leakage or the shielding measures to form an antenna effect, and the connector

Shielding must comply with relevant technical standards;

ÿ RK3528 can be used in different modules. The degree of spread spectrum should be determined according to the signal requirements of the relevant parts.

RK3528 Spread Spectrum Description;

It is recommended to retain all matching resistors connected in series with the clock to provide matching impedance and improve signal quality.

ÿ At the DC power input, a power common-mode inductor or EMI filter may be reserved if conditions permit;

ÿ Add reserved common-mode inductors or filtering circuits to interfaces such as USB and HDMI screen connectors;

ÿ When adding a heat sink, be aware that the heat sink may also couple EMI energy and generate radiation. When selecting a heat sink, in addition to meeting the thermal design requirements, it should also meet the

EMI test requirements. The heat sink should reserve grounding conditions. When grounding is required, the heat sink should be grounded. It is not clear here how many grounding points should be used and

how to choose the grounding points. The first version of the hardware needs to be tested in the laboratory based on the actual situation.

Situation rectification;

ÿ EMI and ESD have highly consistent requirements for layout. Most of the aforementioned ESD layout requirements are applicable to EMI.

Protection. In addition, the following requirements are added:

ÿ Ensure signal integrity as much as possible; ÿ

Differential lines should be of equal length and tightly coupled to ensure the symmetry of differential signals, so as to minimize the misalignment of differential signals and clocks.

Avoid converting into common mode signals that cause EMI problems; ÿ

Components with metal shells such as plug-in devices should avoid coupling interference signals and thus radiation. Also avoid interference signals from devices.

The signal is coupled from the housing to other signal lines;

ÿ All clock matching resistors are close to the CPU end (source end), and the traces between the CPU pins and the resistors must be controlled within 400mil.

Within;

ÿ If the PCB has more than 4 layers, it is recommended that all clock signals go to the inner layer as much as possible; ÿ To

prevent power radiation, the power layer copper must be retracted, with one H (the dielectric thickness between the power supply and the ground) as the unit.

Retracted 20H.

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6. Welding process

6.1 Overview

The RK3528 chip is a ROHS-certified product, meaning it is lead-free. This chapter specifies the basic temperature settings for various time periods when using the RK3528 chip for SMT soldering. It also introduces the process control options for reflow soldering of the RK3528 chip, primarily focusing on lead-free and hybrid processes.

6.2 Explanation of terms

The terms in this chapter are explained as

follows:

- ÿ Lead-free: lead-free process;
- ÿ Pb-free:

lead-free process, all components (mainboard, all ICs, resistors and capacitors, etc.) are lead-free components and use lead-free solder paste.

Pure lead-free process;

ÿ Reflow profile: reflow soldering; ÿ Restriction of

Hazardous Substances (ROHS): restrictions on the use of certain hazardous substances in electronic and electrical equipment

make;

ÿ Surface Mount Technology (SMT): Surface mount technology; ÿ Sn-Pb: Tin-lead mixed process, which refers to

the mixed soldering process using lead solder paste and both lead-free BGA and lead IC.

6.3 Reflow Requirements

6.3.1 Solder paste composition requirements

The ratio of solder alloy to flux is 90%:10% by weight; the volume ratio is 50%:50%. The solder paste should be stored at 2~10ÿ and should be kept at room temperature before use.

Return to the temperature for 3 to 4 hours and keep a record of the time.

The solder paste needs to be stirred before brushing the board, manually for 3 to 5 minutes or mechanically for 3 minutes, and it will be in a natural vertical flow after stirring.

6.3.2 SMT Curve

Since the RK3528 chip is made of environmentally friendly materials, it is recommended to use Pb-Free process. The reflow curve in the figure below is only JEDEC J-STD-020D

The process requirements are recommended values, and the client needs to adjust them according to actual production conditions.

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak		
Temperature min (T_{smin})	100 °C	150 °C
Temperature max (T_{smax})	150 °C	200 °C
Time (T_{smin} to T_{smax}) (t_s)	60-120 seconds	60-120 seconds
Average ramp-up rate (T_{smax} to T_p)	3 °C/second max.	3 °C/second max.
Liquidus temperature (T_L)	183 °C	217 °C
Time at liquidous (t_L)	60-150 seconds	60-150 seconds
Peak package body temperature (T_p)*	See classification temp in Table 4.1	See classification temp in Table 4.2
Time (t_p)** within 5 °C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

* Tolerance for peak profile temperature (T_p) is defined as a supplier minimum and a user maximum.
 ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.

Figure 6-1 Reflow curve classification

Package Thickness	Volume mm ³ <350	Volume mm ³ 350 - 2000	Volume mm ³ >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm - 2.5 mm	260 °C	250 °C	245 °C
>2.5 mm	250 °C	245 °C	245 °C

Figure 6-2 Heat resistance standards for lead-free process device packages

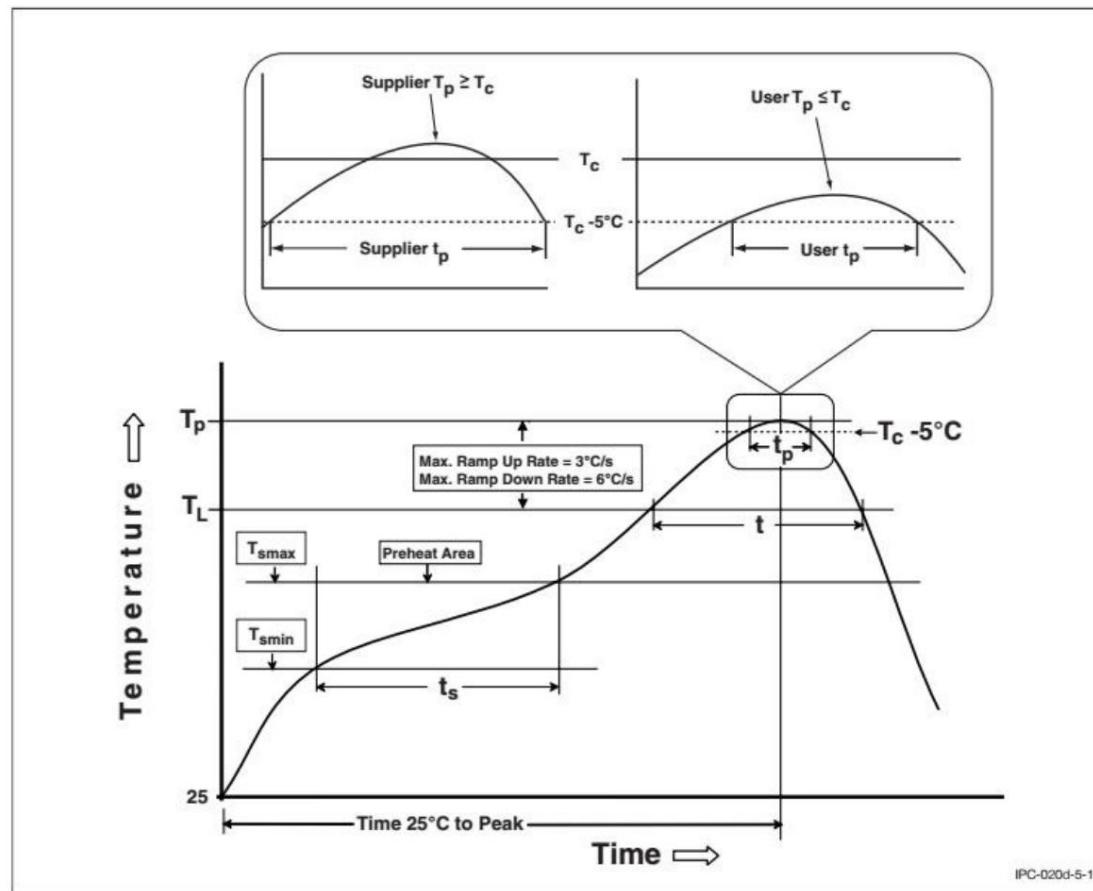


Figure 6-3 Lead-free reflow soldering process curve

6.3.3 SMT Recommended Curve

The SMT curve recommended by our company is shown in Figure 6-4:

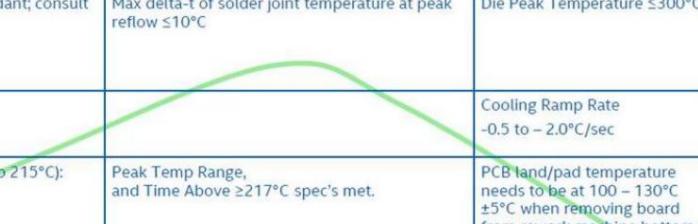
Step 1 Board Preheat	Step 2 Soak Time	Step 3 Peak Reflow & Time Above 220 °C	Step 4 Cool Down
Start with solder joint temp \leq 40°C	After nozzle is lowered prior to peak reflow (Soak Time: Paste dependant; consult paste manufacturer)	Solder Joint Temp 230 – 250°C Above \geq 217°C 60 – 90 sec Max delta-t of solder joint temperature at peak reflow \leq 10°C	Substrate MAX Temperature \leq 260°C Die Peak Temperature \leq 300°C
Rising Ramp Rate 0.5 – 2.5° C/ Sec.	Solder Joint Temp: 200 to 220°C		Cooling Ramp Rate -0.5 to – 2.0°C/sec
Board Preheat Solder Joint Temp: 125 – 150°C	Critical Ramp Rate (205 to 215°C): 0.35 – 0.75°C/sec.	Peak Temp Range, and Time Above \geq 217°C spec's met.	PCB land/pad temperature needs to be at 100 – 130°C \pm 5°C when removing board from rework machine bottom heater at end of component removal operation or \leq 80°C when using stand alone PCB Pre-Heater for PCB land/pad site dress operation.
Preheat with bottom heater, before nozzle is lowered	Nozzle has lowered to reflow component	Nozzle is down during peak reflow	Nozzle raises to home position when solder joint reaches peak temp range

Figure 6-4 Recommended curve parameters for lead-free reflow soldering process

7 Packaging and storage conditions

7.1 Overview

The storage and use specifications of RK3528 are specified to ensure the safe and correct use of the product.

7.2 Explanation of terms

The terms in this chapter are explained

as follows: ý Desiccant: a material used to absorb moisture; ý Floor life: the maximum time the product is allowed to be exposed to the environment, from the time the moisture-proof packaging is unpacked to before reflow soldering; ý Humidity Indicator Card (HIC): humidity indicator card; ý Moisture Sensitivity Level (MSL): moisture sensitivity level; ý Moisture Barrier Bag (MBB): moisture-proof packaging bag; ý Rebake: rebake; ý Solder Reflow: reflow soldering; ý Shell Life: storage period; ý Storage environment: storage environment.

7.3 Moisture-proof packaging

The dry vacuum packaging materials of the product

are as follows: ý

Desiccant; ý Six-point

humidity card; ý Moisture-proof bag, aluminum foil, silver opaque, with moisture sensitivity level logo.



Figure 7-1 Chip drying and vacuum packaging

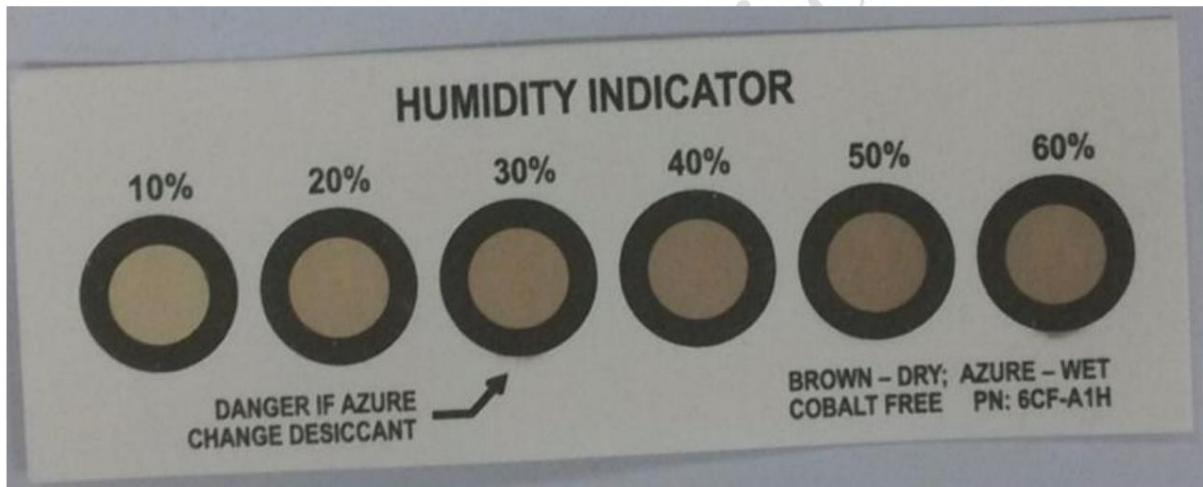


Figure 7-2 Six-point humidity card

7.4 Product Storage

7.4.1 Storage environment

The product is stored in vacuum packaging at a temperature of $\leq 40^{\circ}\text{C}$ and relative humidity of $\leq 90\%$, and the shelf life can reach 12 months.

7.4.2 Exposure time

Under environmental conditions of $\leq 30^{\circ}\text{C}$ and humidity 60%, please refer to the following Table 7-1.

The RK3528 chip has an MSL level of 3 and is very sensitive to humidity. If it is not used immediately after unpacking and is not baked after being left for a long time,

If the chip is not mounted, there is a high probability that the chip will fail.

Table 7-1 Exposure Time Reference Table (MSL)

MSL Level	Exposure time	
	Factory environmental conditions: 30 °C / 60 %RH	
1	Unlimited at 300 °C/85 %RH	
2	1 year	
2a	4 weeks	
3	168 hours	
4	72 hours	
5	48 hours	
5a	24 hours	
6	Mandatory bake before use and must be reflowed within the time limit specified on the label.	

7.5 Use of Moisture-sensitive Products

After the RK3528 chip packaging is opened, the following conditions must be met before the chip is reflowed:

- ÿ Continuous or cumulative exposure time is within 168 hours, and the factory environment is 30°C/60% RH;
- ÿ Stored in an environment with a RH lower than 10%;

In the following cases, the chip must be baked to remove internal moisture to avoid delamination or popcorn problems during reflow:

- ÿ When the humidity indicator card is at 23±5%, the point >10% has changed color. (Please refer to the humidity indicator card for color changes);
- ÿ Failure to meet the requirements of 2a or 2b.

Please refer to the following table 7-2 for the chip re-bake time:

Table 7-2 RK3528 Re-bake Reference Table

Package Body	MSL	High Temp Bake @ 125°C +10/-0%		Medium Temp Bake @ 90°C+8/-0%		Low Temp Bake @ 40°C +5/-0%	
		Exceeding Floor Life by > 72h	Exceeding Floor Life by ≤ 72h	Exceeding Floor Life by > 72h	Exceeding Floor Life by ≤ 72h	Exceeding Floor Life by > 72h	Exceeding Floor Life by ≤ 72h
Thickness ≤1.4mm	3	9 hours	7 hours	33 hours	23 hours	13 days	9 days



Notice

The table shows the minimum baking time required after moisture exposure. Low temperature baking is preferred for re-baking.