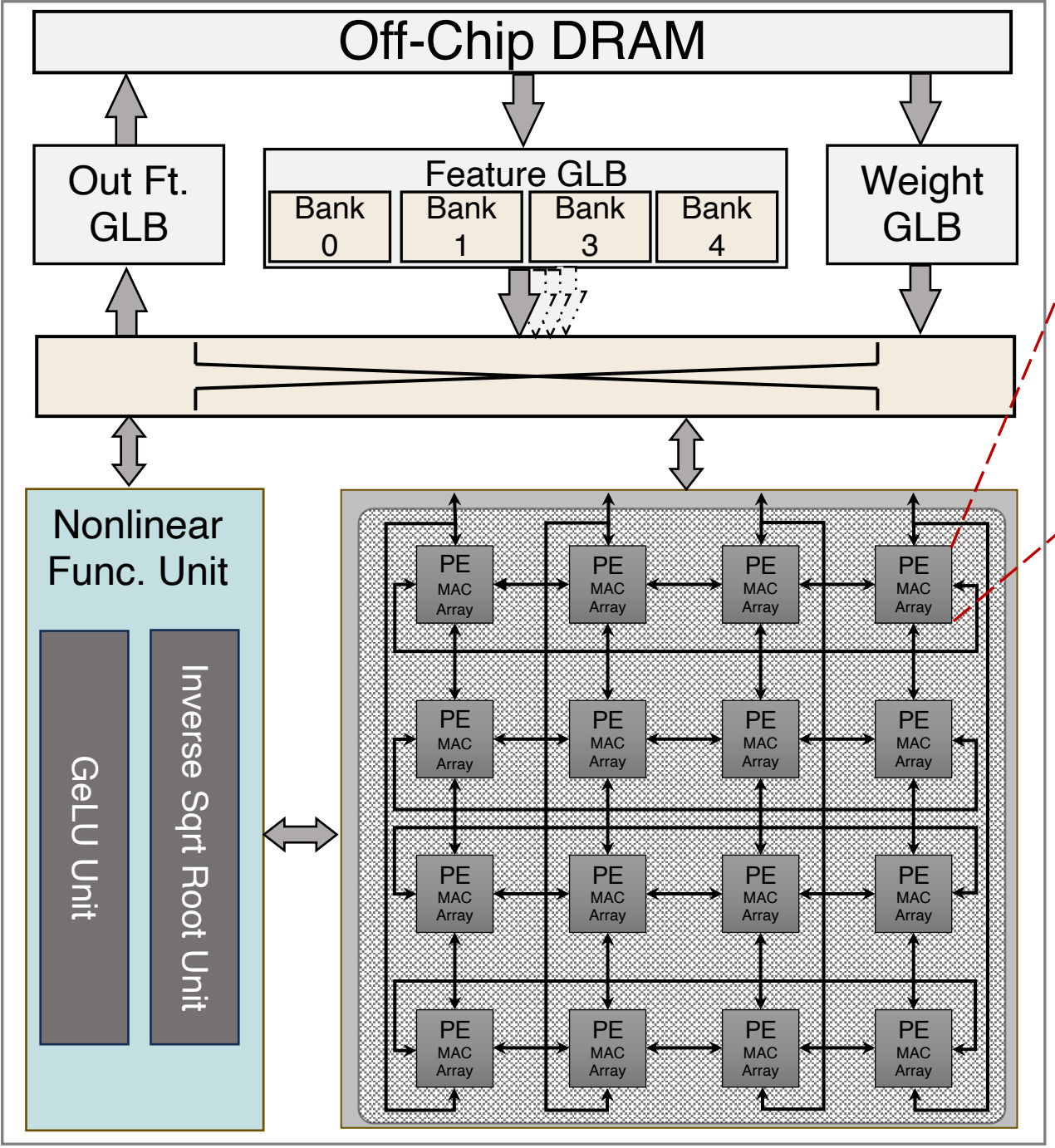
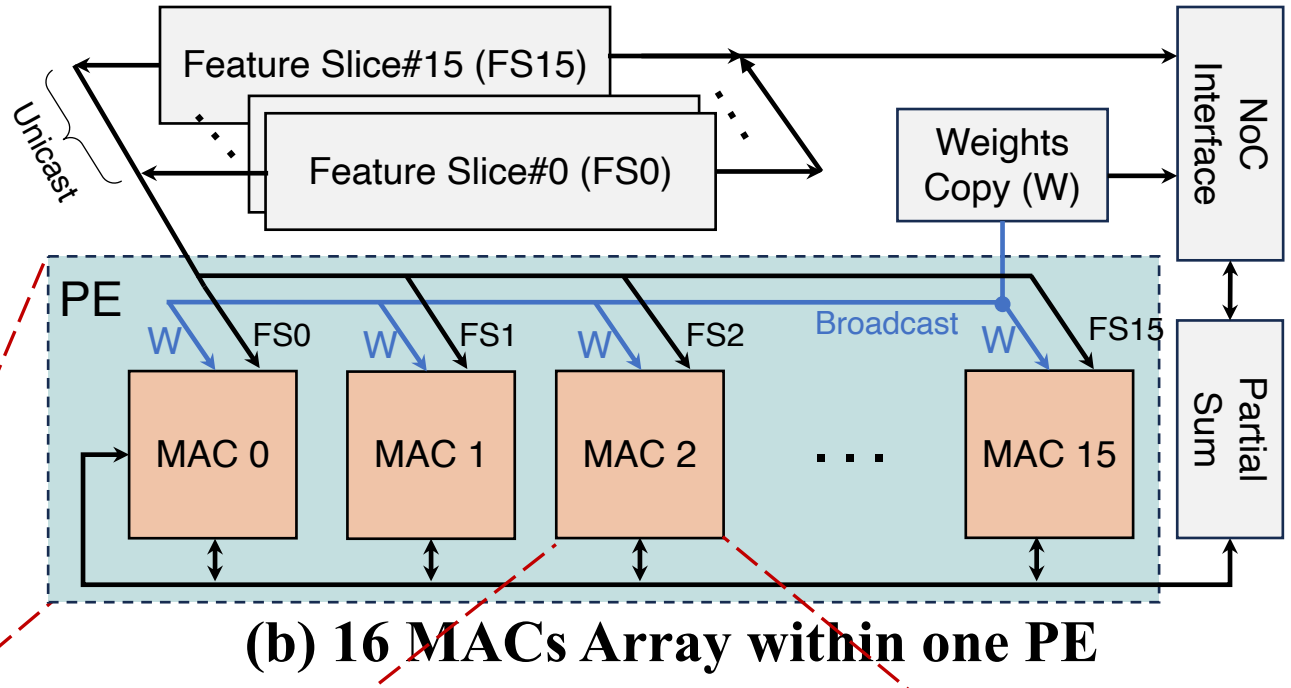
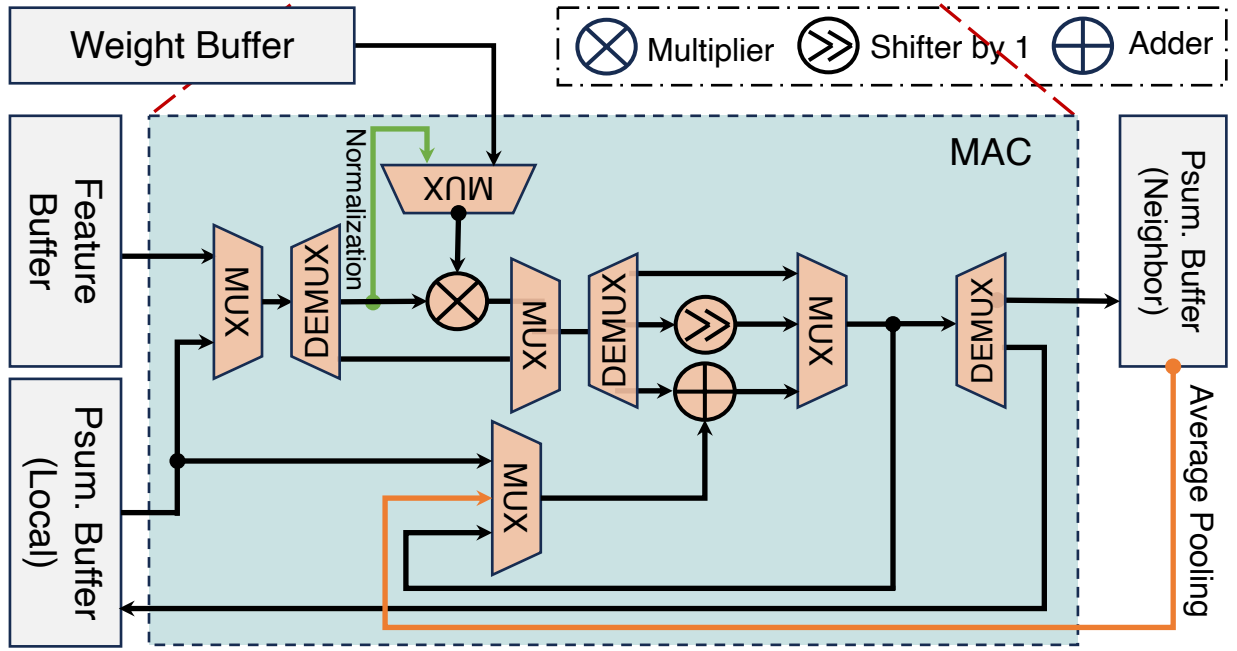


(a) Accelerator Micro-Architecture with 4X4 PEs



(b) 16 MACs Array within one PE



(c) MAC Unit Micro-Architecture