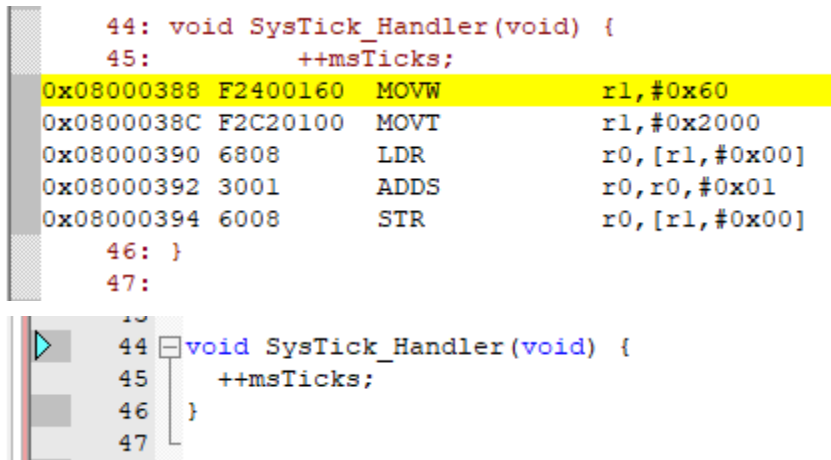


Maxwell Jung
Baron Young
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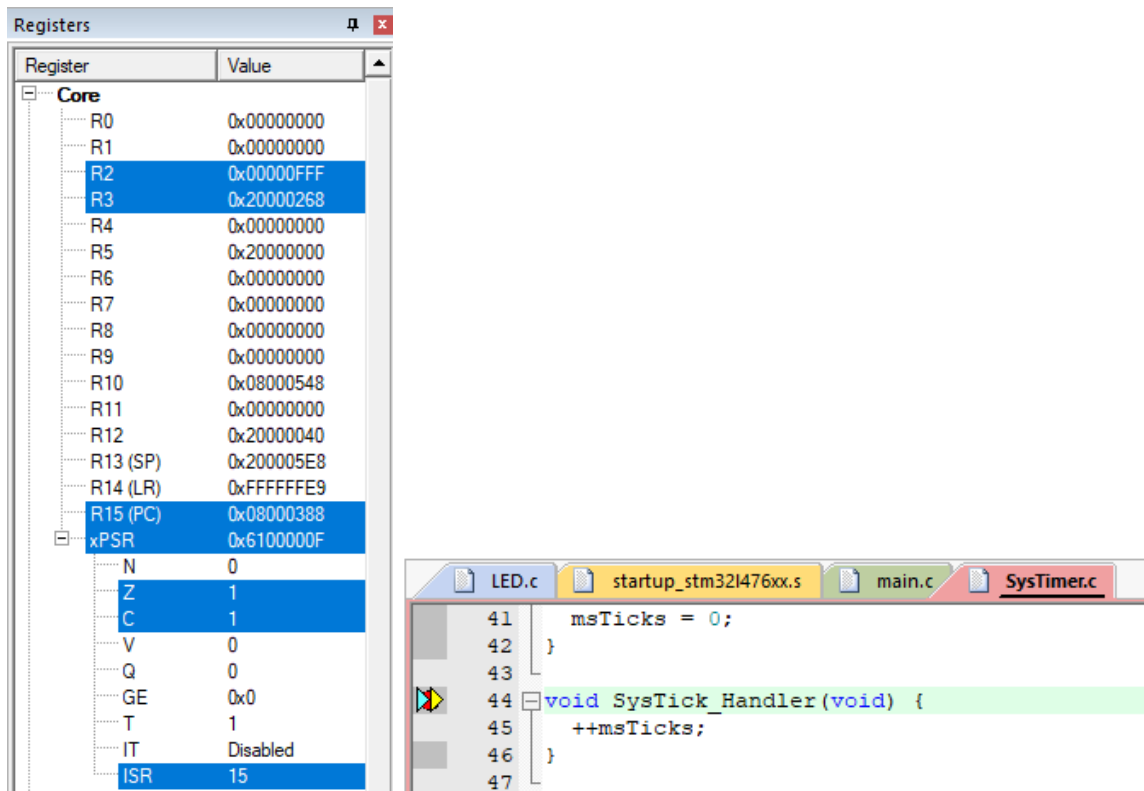
Answers to Lab 2 Questions

1. What is the address of the SysTick_Handler() function? Verify it (i.e. take a screenshot) in the debug environment.

```
44: void SysTick_Handler(void) {  
45:     ++msTicks;  
0x08000388 F2400160 MOVW      r1,#0x60  
0x0800038C F2C20100 MOVT      r1,#0x2000  
0x08000390 6808      LDR        r0,[r1,#0x00]  
0x08000392 3001      ADDS      r0,r0,#0x01  
0x08000394 6008      STR        r0,[r1,#0x00]  
46: }  
47:
```



2. Set up a breakpoint within the SysTick_Handler() function. In the debug environment, find out the exception number in the program status register when the program runs to the breakpoint. Explain what this number means.



Register	Value
R0	0x00000000
R1	0x00000000
R2	0x000000FF
R3	0x20000268
R4	0x00000000
R5	0x20000000
R6	0x00000000
R7	0x00000000
R8	0x00000000
R9	0x00000000
R10	0x08000548
R11	0x00000000
R12	0x20000040
R13 (SP)	0x200005E8
R14 (LR)	0xFFFFFE9
R15 (PC)	0x08000388
xPSR	0x6100000F
N	0
Z	1
C	1
V	0
Q	0
GE	0x0
T	1
IT	Disabled
ISR	15

```
41: msTicks = 0;  
42: }  
43:  
44: void SysTick_Handler(void) {  
45:     ++msTicks;  
46: }  
47:
```

```

/***** Cortex-M4 Processor Exceptions Numbers *****/
NonMaskableInt_IRQn = -14, /*!< 2 Cortex-M4 Non Maskable Interrupt */
HardFault_IRQn      = -13, /*!< 3 Cortex-M4 Hard Fault Interrupt */
MemoryManagement_IRQn = -12, /*!< 4 Cortex-M4 Memory Management Interrupt */
BusFault_IRQn        = -11, /*!< 5 Cortex-M4 Bus Fault Interrupt */
UsageFault_IRQn       = -10, /*!< 6 Cortex-M4 Usage Fault Interrupt */
SVCall_IRQn           = -5,  /*!< 11 Cortex-M4 SV Call Interrupt */
DebugMonitor_IRQn     = -4,  /*!< 12 Cortex-M4 Debug Monitor Interrupt */
PendSV_IRQn           = -2,  /*!< 14 Cortex-M4 Pend SV Interrupt */
SysTick_IRQn          = -1,  /*!< 15 Cortex-M4 System Tick Interrupt */
/***** STM32 specific Interrupt Numbers *****/
WWDG_IRQn             = 0,    /*!< Window WatchDog Interrupt */
PVD_PVM_IRQn          = 1,    /*!< PVD/PVM1/PVM2/PVM3/PVM4 through EXTI Line detection Interrupts */
TAMP_STAMP_IRQn        = 2,    /*!< Tamper and TimeStamp interrupts through the EXTI line */
RTC_WKUP_IRQn          = 3,    /*!< RTC Wakeup interrupt through the EXTI line */
FLASH_IRQn             = 4,    /*!< FLASH global Interrupt */
RCC_IRQn               = 5,    /*!< RCC global Interrupt */
EXTI0_IRQn             = 6,    /*!< EXTI Line0 Interrupt */
EXTI1_IRQn             = 7,    /*!< EXTI Line1 Interrupt */
EXTI2_IRQn             = 8,    /*!< EXTI Line2 Interrupt */

```

The exception number of 15 (ISR=15) indicates that the systick is the 15th exception in the Cortex-M4 processor.

3. Cortex-M series supports up to 256 interrupts. What is the interrupt number of SysTick that is defined in CMSIS?

-1

4. Does a higher priority value represent a higher urgency?

Higher priority number does not represent higher urgency. The lower the number, the higher the urgency.

5. Suppose a clock of 16 MHz is used to drive the system timer. What is the maximum period between two consecutive SysTick interrupts that we can possibly obtain?

The maximum possible reload value is $0x00FFFFFF = 16777215$

$(\text{clock_frequency}) * \text{period} - 1 = \text{reload value}$

$\text{period} = (16777215 + 1) / (16 * 10^6) = 1.048576 \text{ seconds}$