CSE 125 Lab 1: Behavioral Verilog

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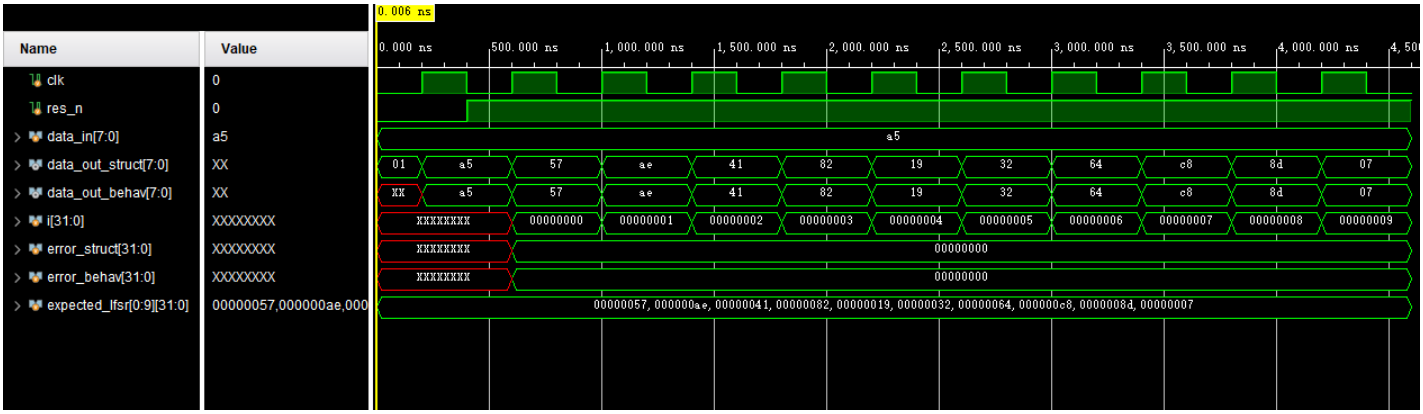
Lab Group: 20

1. Linear Feedback Shift Register
   a. Screenshot



   b. Result

10 outputs:

data_out_struct[7:0]: a5, 57, ae, 41, 82, 19, 32, 64, c8, 8d;

data_out_behav[7:0]: a5, 57, ae, 41, 82, 19, 32, 64, c8, 8d;

lfsr_structural:

resource:

wns = -0.155ns, target clock period =20ns

Fmax:

Fmax = 1/(20 –(-0.155)) = 1/20.155 = 0.05Mhz

lfsr_behavioural:

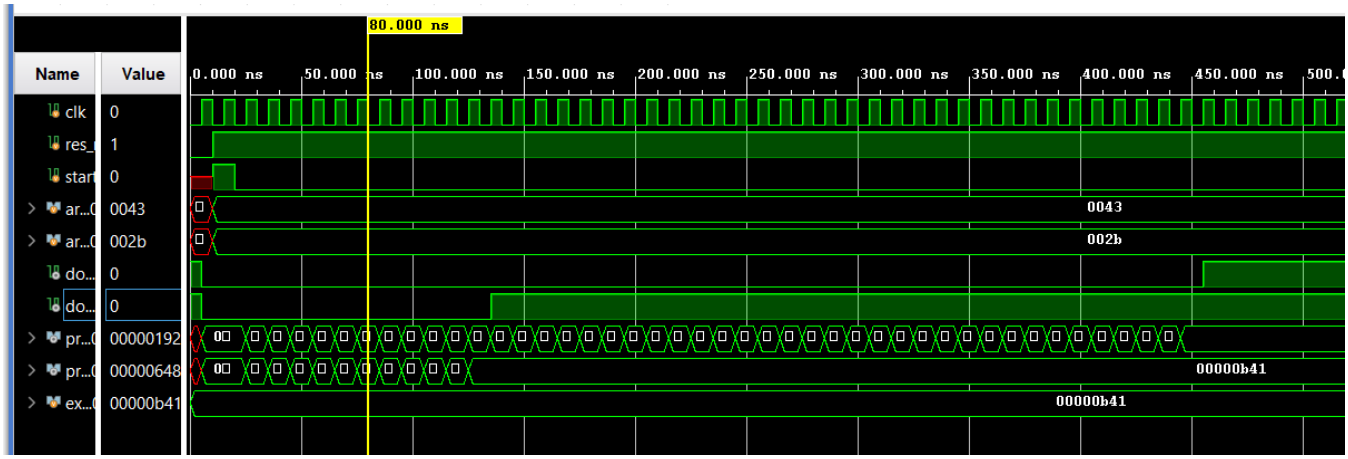
resource:

wns = -0.58ns, target clock period =20ns

Fmax:

Fmax = 1/(20 –(-0.58)) = 1/20.58 = 0.049Mhz

2. Build a Multiplier using an Accumulator
   a. Screenshot

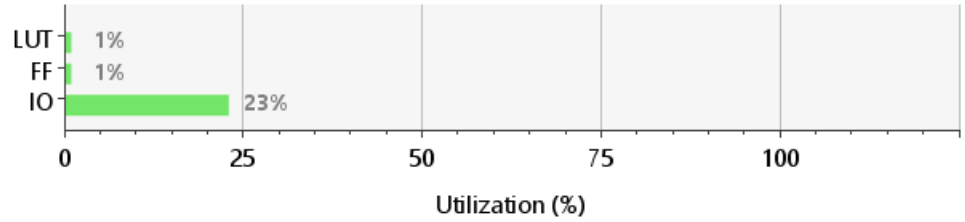


   b. Result

   Multiplier_1:

   LUT and FF:

Resource	Utilization	Available	Utilization%
LUT	52	41000	0.13
FF	65	82000	0.08
IO	68	300	22.67



   Fmax:

   wns = -0.466ns

   target clock period: 11ns

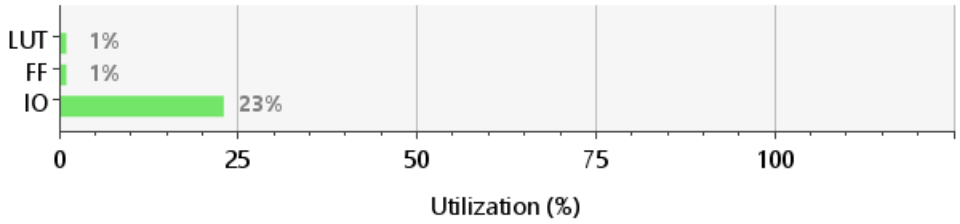
   Fmax = 1/(11+0.466) = 0.0872Mhz

   For computing the result of “67*43”, the runtime is $0.45 \times 10^{-6} s$

multiplier_4:

LUT and FF:

Resource	Utilization	Available	Utilization%
LUT	187	41000	0.46
FF	63	82000	0.08
IO	68	300	22.67



Fmax:

wns = -3.823ns

target clock period: 11ns

Fmax = 1/(11+3.823) = 0.0675Mhz

For computing the result of “67*43”, the runtime is $0.13 \times 10^{-6} s$