# CSE 125 Lab 2: Finite State Machines
# Date: 04/21/2020

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# Lab Group: 20


## I. Regular Expression Checker

a) FSM

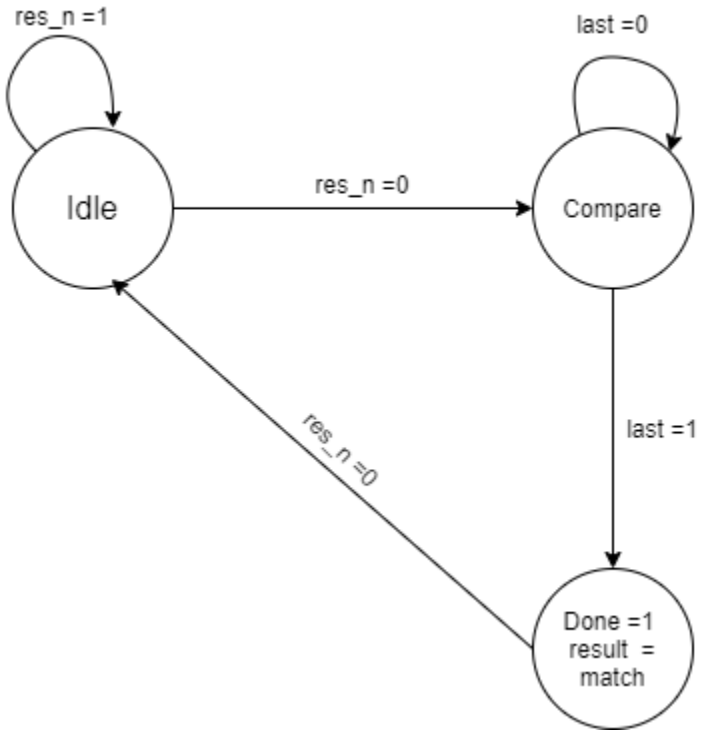



Figure 1. main running of FSM

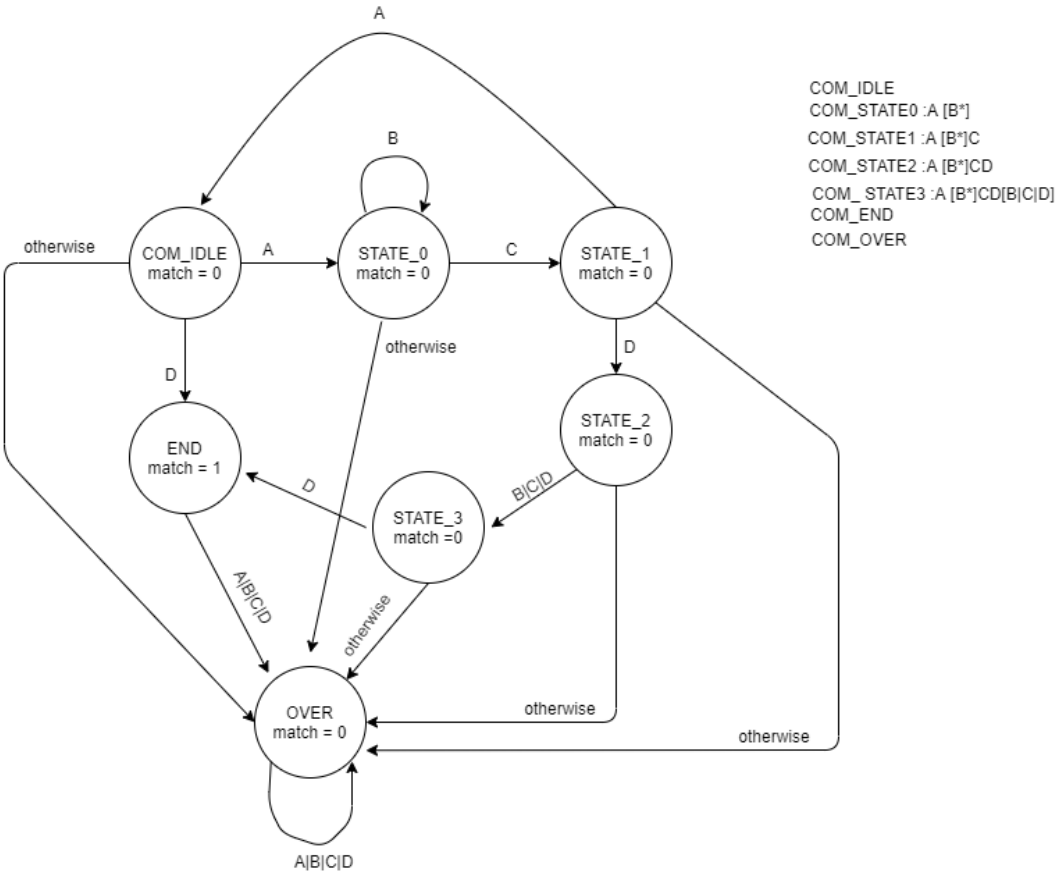



Figure 2. signal comparing of FSM

## b) 7 clock cycles screenshot

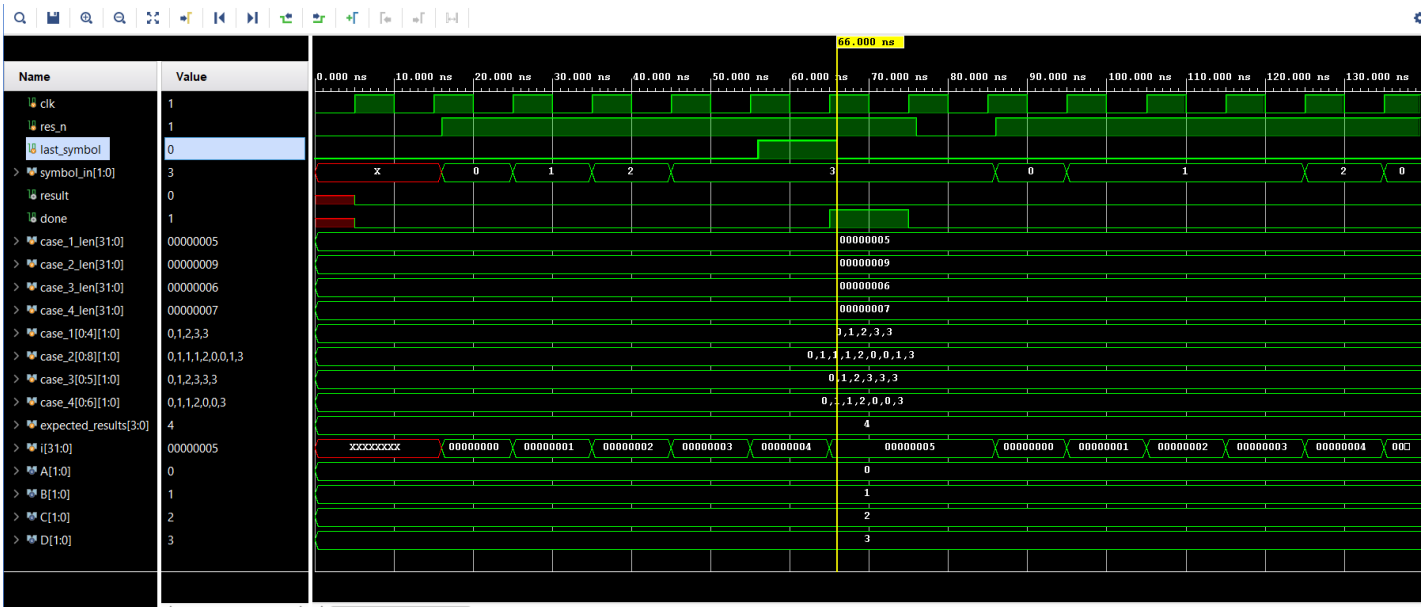



Figure 3. 7 clock cycles for input ABCDD

## c) Synthesis result

| Name | Slice LUTs (134600) | Slice Registers (269200) | Bonded IOB (285) | BUFGCTRL (32) |
|---|---|---|---|---|
| regex | 6 | 8 | 7 | 1 |

| Resource | Utilization | Available | Utilization % |
|---|---|---|---|
| LUT | 6 | 134600 | 0.00 |
| FF | 8 | 269200 | 0.00 |
| IO | 7 | 285 | 2.46 |

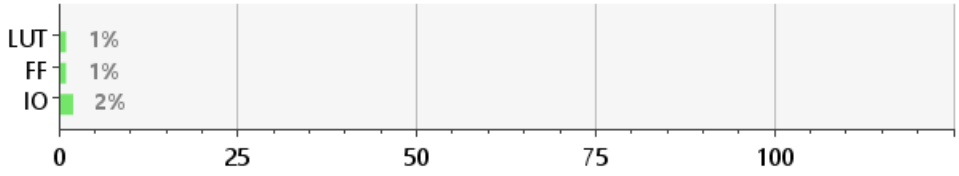
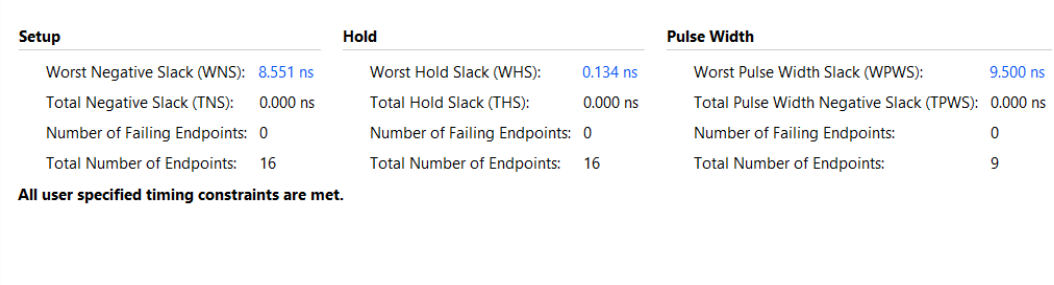



Figure 4. Synthesis result



| Setup | | Hold | | Pulse Width | |
|---|---|---|---|---|---|
| Worst Negative Slack (WNS): | 8.551 ns | Worst Hold Slack (WHS): | 0.134 ns | Worst Pulse Width Slack (WPWS): | 9.500 ns |
| Total Negative Slack (TNS): | 0.000 ns | Total Hold Slack (THS): | 0.000 ns | Total Pulse Width Negative Slack (TPWS): | 0.000 ns |
| Number of Failing Endpoints: | 0 | Number of Failing Endpoints: | 0 | Number of Failing Endpoints: | 0 |
| Total Number of Endpoints: | 16 | Total Number of Endpoints: | 16 | Total Number of Endpoints: | 9 |

**All user specified timing constraints are met.**

Figure 5. Design Timing summary

| Name | Waveform | Period (ns) | Frequency (MHz) |
|---|---|---|---|
| clk | {0.000 10.000} | 20.000 | 50.000 |

Figure 6. clock summary

As we see, the Design Timing summary, WNS = 8.551ns, so

$\mathrm{FMAX} = 1/(\mathrm{T} - \mathrm{WNS}) = 1/(20\mathrm{ns} - 8.551\mathrm{ns}) = 0.08734 \times 10^9 Hz$

$\mathrm{FMAX} = 87.34 MHz$

# II. Timing

a) Identify the critical path

The critical paths :

G1->R1->G2->G4->R2

G1->R1->G3->G4->R2

b) Maximum clock rate

Max clock period = min delay in gates + min delay in clock pulse + setup time

= 3*70ps + 2*30ps + 2*35ps + 40ps

= 415ps

max clk freq = 1/period = 1/415ps = $2.4 \times 10^9 Hz$

=2.4GHz

c) Register hold times

The register hold times couldn't be violated, since Propagation min delay + Clk-to-Q min delay > Hold Time; each register input is previous gate output, and propagation min delay + Clk-to-Q min delay is bigger than hold time delay which 30ps + 70ps > 35ps