**CSE 125 Lab 2: Finite State Machines**

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1. **Regular Expression Checker**
2. FSM

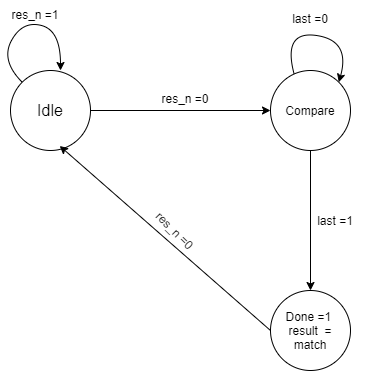


Figure 1. main running of FSM

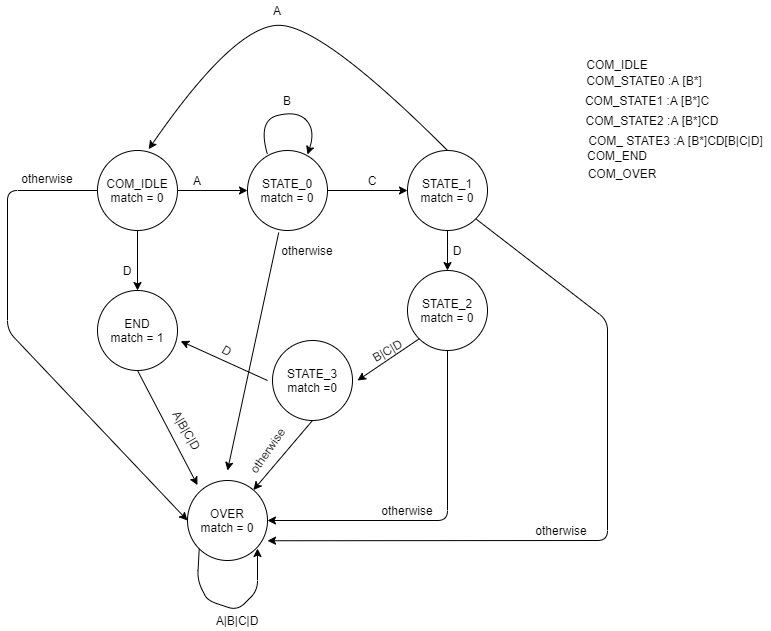


Figure 2. signal comparing of FSM

1. 7 clock cycles screenshot

A screen shot of a computer

Description automatically generated

Figure 3. 7 clock cycles for input ABCDD

1. Synthesis result

A screenshot of a cell phone

Description automatically generated

A screenshot of a cell phone

Description automatically generated

Figure 4. Synthesis result

A screenshot of a cell phone

Description automatically generated

Figure 5. Design Timing summary

A screenshot of a social media post

Description automatically generated

Figure 6. clock summary

As we see, the Design Timing summary, WNS = 8.551ns, so

1. **Timing**
2. Identify the critical path

The critical paths :

G1->R1->G2->G4->R2

G1->R1->G3->G4->R2

1. Maximum clock rate

Max clock period = min delay in gates + min delay in clock pulse + setup time

= 3\*70ps + 2\*30ps + 2\*35ps + 40ps

= 415ps

max clk freq = 1/period = 1/415ps =

=2.4GHz

1. Register hold times

The register hold times couldn’t be violated, since

Propagation min delay + Clk-to-Q min delay > Hold Time;

each register input is previous gate output, and propagation min delay + Clk-to-Q min delay is bigger than hold time delay which 30ps + 70ps > 35ps