14.2.4 I²C Mode

The USI module is configured in I²C mode when USII2C =1, USICKPL = 1, and USICKPH = 0. For I²C data compatibility, USILSB and USI16B must be cleared. USIPE6 and USIPE7 must be set to enable the SCL and SDA port functions.

14.2.4.1 I²C Master Mode

To configure the USI module as an I²C master the USIMST bit must be set. In master mode, clocks are generated by the USI module and output to the SCL line while USIIFG = 0. When USIIFG = 1, the SCL will stop at the idle, or high, level. Multi-master operation is supported as described in the Arbitration section.

The master supports slaves that are holding the SCL line low only when USIDIVx > 0. When USIDIVx is set to /1 clock division (USIDIVx = 0), connected slaves must not hold the SCL line low during data transmission. Otherwise the communication may fail.

14.2.4.2 I²C Slave Mode

To configure the USI module as an I²C slave the USIMST bit must be cleared. In slave mode, SCL is held low if USIIFG = 1, USISTTIFG = 1 or if USICNTx = 0. USISTTIFG must be cleared by software after the slave is setup and ready to receive the slave address from a master.

14.2.4.3 I²C Transmitter

In transmitter mode, data is first loaded into USISRL. The output is enabled by setting USIOE and the transmission is started by writing 8 into USICNTx. This clears USIIFG and SCL is generated in master mode or released from being held low in slave mode. After the transmission of all 8 bits, USIIFG is set, and the clock signal on SCL is stopped in master mode or held low at the next low phase in slave mode.

To receive the I²C acknowledgment bit, the USIOE bit is cleared with software and USICNTx is loaded with 1. This clears USIIFG and one bit is received into USISRL. When USIIFG becomes set again, the LSB of USISRL is the received acknowledge bit and can be tested in software.

```
; Receive ACK/NACK
   BIC.B  #USIOE,&USICTL0    ; SDA input
   MOV.B  #01h,&USICNT       ; USICNTx = 1
TEST_USIIFG
   BIT.B  #USIIFG,&USICTL1   ; Test USIIFG
   JZ     TEST_USIIFG
   BIT.B  #01h,&USISRL       ; Test received ACK bit
   JNZ    HANDLE_NACK        ; Handle if NACK
...Else, handle ACK
```

14.2.4.4 I²C Receiver

In I²C receiver mode the output must be disabled by clearing USIOE and the USI module is prepared for reception by writing 8 into USICNTx. This clears USIIFG and SCL is generated in master mode or released from being held low in slave mode. The USIIFG bit will be set after 8 clocks. This stops the clock signal on SCL in master mode or holds SCL low at the next low phase in slave mode.

To transmit an acknowledge or no-acknowledge bit, the MSB of the shift register is loaded with 0 or 1, the USIOE bit is set with software to enable the output, and 1 is written to the USICNTx bits. As soon as the MSB bit is shifted out, USIIFG will be become set and the module can be prepared for the reception of the next I²C data byte.

```
; Generate ACK
   BIS.B   #USIOE,&USICTL0    ; SDA output
   MOV.B   #00h,&USISRL       ; MSB = 0
   MOV.B   #01h,&USICNT       ; USICNTx = 1
TEST_USIIFG
   BIT.B   #USIIFG,&USICTL1   ; Test USIIFG
   JZ      TEST_USIIFG
...continue...

; Generate NACK
   BIS.B   #USIOE,&USICTL0    ; SDA output
   MOV.B   #0FFh,&USISRL      ; MSB = 1
   MOV.B   #01h,&USICNT       ; USICNTx = 1
TEST_USIIFG
   BIT.B   #USIIFG,&USICTL1   ; Test USIIFG
   JZ      TEST_USIIFG
...continue...
```

14.2.4.5 START Condition

A START condition is a high-to-low transition on SDA while SCL is high. The START condition can be generated by setting the MSB of the shift register to 0. Setting the USIGE and USIOE bits makes the output latch transparent and the MSB of the shift register is immediately presented to SDA and pulls the line low. Clearing USIGE resumes the clocked-latch function and holds the 0 on SDA until data is shifted out with SCL.

```
; Generate START
   MOV.B   #000h,&USISRL           ; MSB = 0
   BIS.B   #USIGE+USIOE,&USICTL0   ; Latch/SDA output enabled
   BIC.B   #USIGE,&USICTL0         ; Latch disabled
...continue...
```

14.2.4.6 STOP Condition

A STOP condition is a low-to-high transition on SDA while SCL is high. To finish the acknowledgment bit and pull SDA low to prepare the STOP condition generation requires clearing the MSB in the shift register and loading 1 into USICNTx. This will generate a low pulse on SCL and during the low phase SDA is pulled low. SCL stops in the idle, or high, state since the module is in master mode. To generate the low-to-high transition, the MSB is set in the shift register and USICNTx is loaded with 1. Setting the USIGE and USIOE bits makes the output latch transparent and the MSB of USISRL releases SDA to the idle state. Clearing USIGE stores the MSB in the output latch and the output is disabled by clearing USIOE. SDA remains high until a START condition is generated because of the external pullup.

```
; Generate STOP
   BIS.B   #USIOE,&USICTL0    ; SDA=output
   MOV.B   #000h,&USISRL      ; MSB = 0
   MOV.B   #001h,&USICNT      ; USICNT = 1 for one clock
TEST_USIIFG
   BIT.B   #USIIFG,&USICTL1   ; Test USIIFG
   JZ      test_USIIFG        ;
   MOV.B   #0FFh,&USISRL      ; USISRL = 1 to drive SDA high
   BIS.B   #USIGE,&USICTL0    ; Transparent latch enabled
   BIC.B   #USIGE+USIOE,&USICTL; Latch/SDA output disabled
...continue...
```

14.2.4.7 Releasing SCL

Setting the USISCLREL bit will release SCL if it is being held low by the USI module without requiring USIIFG to be cleared. The USISCLREL bit will be cleared automatically if a START condition is received and the SCL line will be held low on the next clock.

In slave operation this bit should be used to prevent SCL from being held low when the slave has detected that it was not addressed by the master. On the next START condition USISCLREL will be cleared and the USISTTIFG will be set.

14.2.4.8 Arbitration

The USI module can detect a lost arbitration condition in multi-master I^2C systems. The I^2C arbitration procedure uses the data presented on SDA by the competing transmitters. The first master transmitter that generates a logic high loses arbitration to the opposing master generating a logic low. The loss of arbitration is detected in the USI module by comparing the value presented to the bus and the value read from the bus. If the values are not equal arbitration is lost and the arbitration lost flag, USIAL, is set. This also clears the output enable bit USIOE and the USI module no longer drives the bus. In this case, user software must check the USIAL flag together with USIIFG and configure the USI to slave receiver when arbitration is lost. The USIAL flag must be cleared by software.

To prevent other faster masters from generating clocks during the arbitration procedure SCL is held low if another master on the bus drives SCL low and USIIFG or USISTTIFG is set, or if USICNTx = 0.

14.2.4.9 I^2C Interrupts

There is one interrupt vector associated with the USI module with two interrupt flags relevant for I^2C operation, USIIFG and USISTTIFG. Each interrupt flag has its own interrupt enable bit, USIIE and USISTTIE. When an interrupt is enabled, and the GIE bit is set, a set interrupt flag will generate an interrupt request.

USIIFG is set when USICNTx becomes zero, either by counting or by directly writing 0 to the USICNTx bits. USIIFG is cleared by writing a value > 0 to the USICNTx bits when USIIFGCC = 0, or directly by software.

USISTTIFG is set when a START condition is detected. The USISTTIFG flag must be cleared by software.

The reception of a STOP condition is indicated with the USISTP flag but there is no interrupt function associated with the USISTP flag. USISTP is cleared by writing a value > 0 to the USICNTx bits when USIIFGCC = 0 or directly by software.

14.3 USI Registers

The USI registers are listed in Table 14-1.

Table 14-1. USI Registers

Register	Short Form	Register Type	Address	Initial State
USI control register 0	USICTL0	Read/write	078h	01h with PUC
USI control register 1	USICTL1	Read/write	079h	01h with PUC
USI clock control	USICKCTL	Read/write	07Ah	Reset with PUC
USI bit counter	USICNT	Read/write	07Bh	Reset with PUC
USI low byte shift register	USISRL	Read/write	07Ch	Unchanged
USI high byte shift register	USISRH	Read/write	07Dh	Unchanged

The USI registers can be accessed with word instructions as shown in Table 14-2.

Table 14-2. Word Access to USI Registers

Register	Short Form	High-Byte Register	Low-Byte Register	Address
USI control register	USICTL	USICTL1	USICTL0	078h
USI clock and counter control register	USICCTL	USICNT	USICKCTL	07Ah
USI shift register	USISR	USISRH	USISRL	07Ch

14.3.1 USICTL0, USI Control Register 0

7	6	5	4	3	2	1	0
USIPE7	**USIPE6**	**USIPE5**	**USILSB**	**USIMST**	**USIGE**	**USIOE**	**USISWRST**
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-1

USIPE7 Bit 7 USI SDI/SDA port enable. Input in SPI mode, input or open drain output in I^2C mode.
- 0 USI function disabled
- 1 USI function enabled

USIPE6 Bit 6 USI SDO/SCL port enable. Output in SPI mode, input or open drain output in I^2C mode.
- 0 USI function disabled
- 1 USI function enabled

USIPE5 Bit 5 USI SCLK port enable. Input in SPI slave mode, or I^2C mode, output in SPI master mode.
- 0 USI function disabled
- 1 USI function enabled

USILSB Bit 4 LSB first select. This bit controls the direction of the receive and transmit shift register.
- 0 MSB first
- 1 LSB first

USIMST Bit 3 Master select
- 0 Slave mode
- 1 Master mode

USIGE Bit 2 Output latch control
- 0 Output latch enable depends on shift clock
- 1 Output latch always enabled and transparent

USIOE Bit 1 Data output enable
- 0 Output disabled
- 1 Output enabled

USISWRST Bit 0 USI software reset
- 0 USI released for operation.
- 1 USI logic held in reset state.

14.3.2 USICTL1, USI Control Register 1

7	6	5	4	3	2	1	0
USICKPH	**USII2C**	**USISTTIE**	**USIIE**	**USIAL**	**USISTP**	**USISTTIFG**	**USIIFG**
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-1

USICKPH Bit 7 Clock phase select
- 0 Data is changed on the first SCLK edge and captured on the following edge.
- 1 Data is captured on the first SCLK edge and changed on the following edge.

USII2C Bit 6 I^2C mode enable
- 0 I^2C mode disabled
- 1 I^2C mode enabled

USISTTIE Bit 5 START condition interrupt-enable
- 0 Interrupt on START condition disabled
- 1 Interrupt on START condition enabled

USIIE Bit 4 USI counter interrupt enable
- 0 Interrupt disabled
- 1 Interrupt enabled

USIAL Bit 3 Arbitration lost
- 0 No arbitration lost condition
- 1 Arbitration lost

USISTP Bit 2 STOP condition received. USISTP is automatically cleared if USICNTx is loaded with a value > 0 when USIIFGCC = 0.
- 0 No STOP condition received
- 1 STOP condition received

USISTTIFG Bit 1 START condition interrupt flag
- 0 No START condition received. No interrupt pending.
- 1 START condition received. Interrupt pending.

USIIFG Bit 0 USI counter interrupt flag. Set when the USICNTx = 0. Automatically cleared if USICNTx is loaded with a value > 0 when USIIFGCC = 0.
- 0 No interrupt pending
- 1 Interrupt pending

14.3.3 USICKCTL, USI Clock Control Register

7	6	5	4	3	2	1	0
USIDIVx			**USISSELx**			**USICKPL**	**USISWCLK**
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

USIDIVx	Bits 7-5	Clock divider select	
		000	Divide by 1
		001	Divide by 2
		010	Divide by 4
		011	Divide by 8
		100	Divide by 16
		101	Divide by 32
		110	Divide by 64
		111	Divide by 128
USISSELx	Bits 4-2	Clock source select. Not used in slave mode.	
		000	SCLK (Not used in SPI mode)
		001	ACLK
		010	SMCLK
		011	SMCLK
		100	USISWCLK bit
		101	TACCR0
		110	TACCR1
		111	TACCR2 (Reserved on MSP430F20xx devices)
USICKPL	Bit 1	Clock polarity select	
		0	Inactive state is low
		1	Inactive state is high
USISWCLK	Bit 0	Software clock	
		0	Input clock is low
		1	Input clock is high

14.3.4 USICNT, USI Bit Counter Register

7	6	5	4	3	2	1	0
USISCLREL	**USI16B**	**USIIFGCC**	**USICNTx**				
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

USISCLREL	Bit 7	SCL release. The SCL line is released from low to idle. USISCLREL is cleared if a START condition is detected.	
		0	SCL line is held low if USIIFG is set
		1	SCL line is released
USI16B	Bit 6	16-bit shift register enable	
		0	8-bit shift register mode. Low byte register USISRL is used.
		1	16-bit shift register mode. Both high and low byte registers USISRL and USISRH are used. USISR addresses all 16 bits simultaneously.
USIIFGCC	Bit 5	USI interrupt flag clear control. When USIIFGCC = 1 the USIIFG will not be cleared automatically when USICNTx is written with a value > 0.	
		0	USIIFG automatically cleared on USICNTx update
		1	USIIFG is not cleared automatically
USICNTx	Bits 4-0	USI bit count. The USICNTx bits set the number of bits to be received or transmitted.	

14.3.5 USISRL, USI Low Byte Shift Register

7	6	5	4	3	2	1	0
USISRLx							
rw	rw	rw	rw	rw	rw	rw	rw

USISRLx	Bits 7-0	Contents of the USI low byte shift register

14.3.6 USISRH, USI High Byte Shift Register

7	6	5	4	3	2	1	0
USISRHx							
rw	rw	rw	rw	rw	rw	rw	rw

USISRHx	Bits 7-0	Contents of the USI high byte shift register. Ignored when USI16B = 0.