



## 1. Description

### 1.1. Project

Project Name	BasicTraining
Board Name	custom
Generated with:	STM32CubeMX 6.15.0
Date	09/27/2025

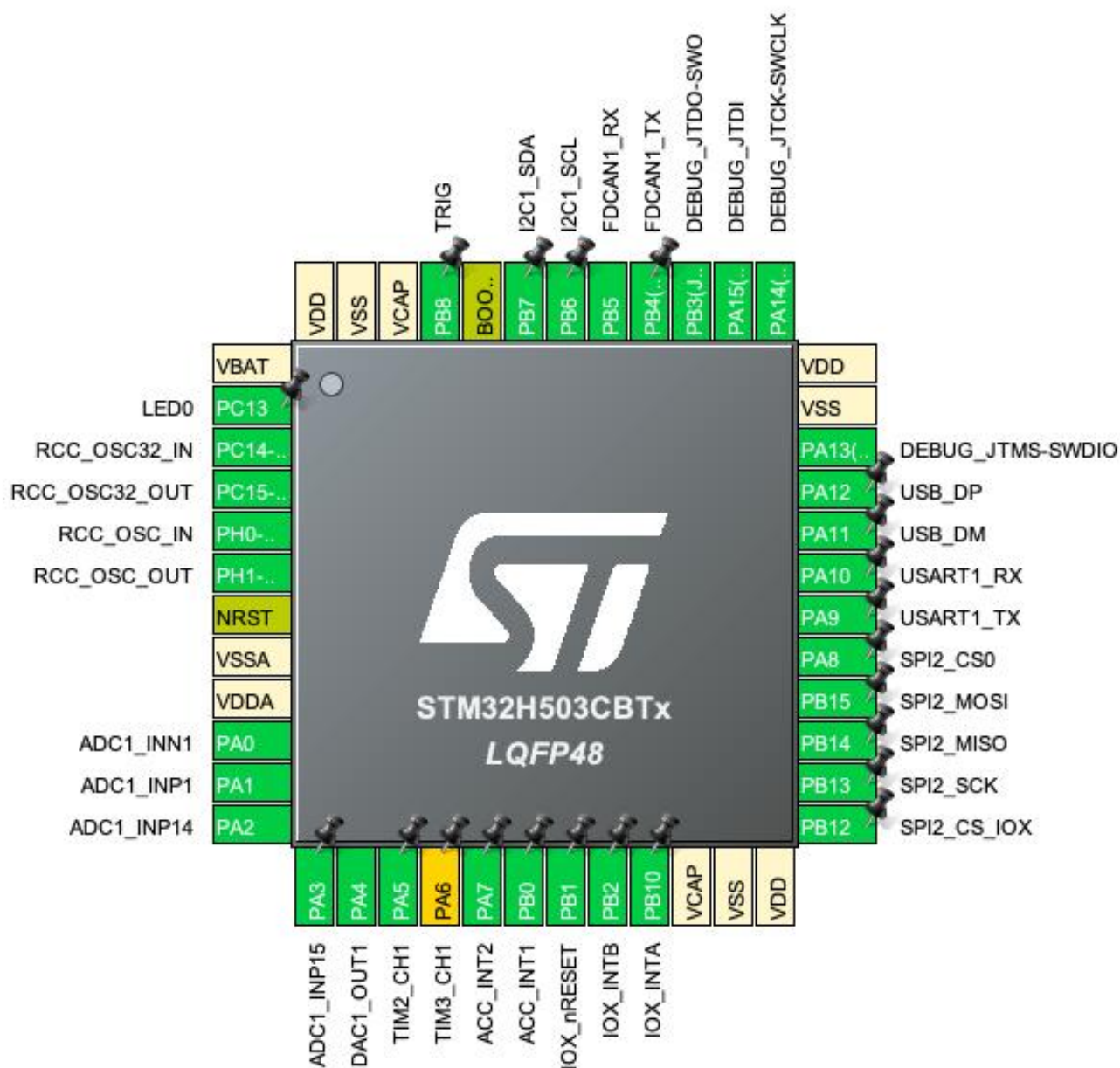
### 1.2. MCU

MCU Series	STM32H5
MCU Line	STM32H503
MCU name	STM32H503CBTx
MCU Package	LQFP48
MCU Pin number	48

### 1.3. Core(s) information

Core(s)	Arm Cortex-M33
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## 2. Pinout Configuration



### 3. Pins Configuration

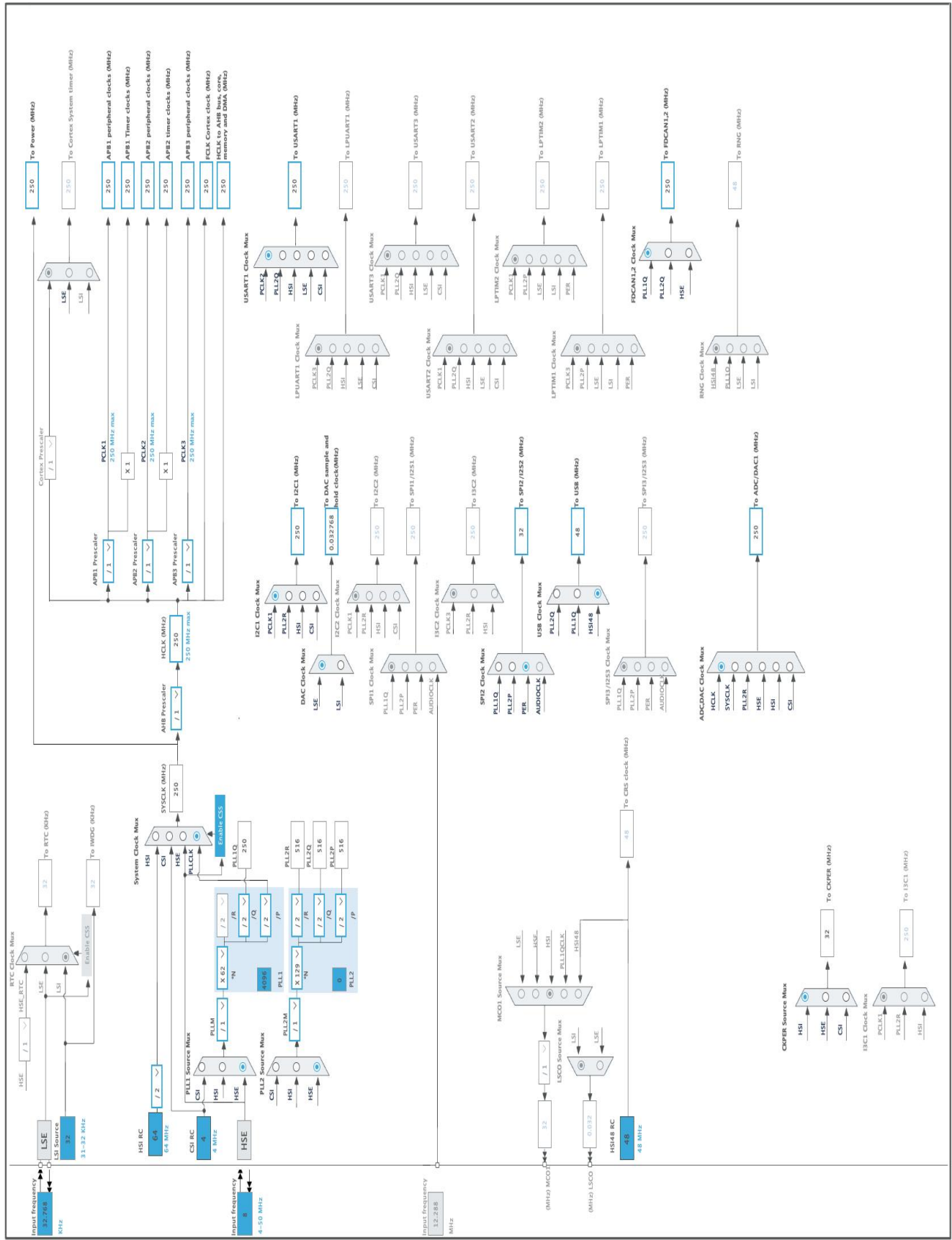
Pin Number LQFP48	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
2	PC13 *	I/O	GPIO_Output	LED0
3	PC14- OSC32_IN(OSC32_IN)	I/O	RCC_OSC32_IN	
4	PC15- OSC32_OUT(OSC32_OUT)	I/O	RCC_OSC32_OUT	
5	PH0-OSC_IN(PH0)	I/O	RCC_OSC_IN	
6	PH1-OSC_OUT(PH1)	I/O	RCC_OSC_OUT	
7	NRST	Reset		
8	VSSA	Power		
9	VDDA	Power		
10	PA0	I/O	ADC1_INN1	
11	PA1	I/O	ADC1_INP1	
12	PA2	I/O	ADC1_INP14	
13	PA3	I/O	ADC1_INP15	
14	PA4	I/O	DAC1_OUT1	
15	PA5	I/O	TIM2_CH1	
16	PA6 **	I/O	TIM3_CH1	
17	PA7	I/O	GPIO_EXTI7	ACC_INT2
18	PB0	I/O	GPIO_EXTI0	ACC_INT1
19	PB1 *	I/O	GPIO_Output	IOX_nRESET
20	PB2	I/O	GPIO_EXTI2	IOX_INTB
21	PB10	I/O	GPIO_EXTI10	IOX_INTA
22	VCAP	Power		
23	VSS	Power		
24	VDD	Power		
25	PB12 *	I/O	GPIO_Output	SPI2_CS_IOX
26	PB13	I/O	SPI2_SCK	
27	PB14	I/O	SPI2_MISO	
28	PB15	I/O	SPI2_MOSI	
29	PA8 *	I/O	GPIO_Output	SPI2_CS0
30	PA9	I/O	USART1_TX	
31	PA10	I/O	USART1_RX	
32	PA11	I/O	USB_DM	
33	PA12	I/O	USB_DP	
34	PA13(JTMS/SWDIO)	I/O	DEBUG_JTMS-SWDIO	

Pin Number LQFP48	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
35	VSS	Power		
36	VDD	Power		
37	PA14(JTCK/SWCLK)	I/O	DEBUG_JTCK-SWCLK	
38	PA15(JTDI)	I/O	DEBUG_JTDI	
39	PB3(JTDO/TRACESWO)	I/O	DEBUG_JTDO-SWO	
40	PB4(NJTRST)	I/O	FDCAN1_TX	
41	PB5	I/O	FDCAN1_RX	
42	PB6	I/O	I2C1_SCL	
43	PB7	I/O	I2C1_SDA	
44	BOOT0	Boot		
45	PB8 *	I/O	GPIO_Output	TRIG
46	VCAP	Power		
47	VSS	Power		
48	VDD	Power		

\* The pin is affected with an I/O function

\*\* The pin is affected with a peripheral function but no peripheral mode is activated

## 4. Clock Tree Configuration



## 1. Power Consumption Calculator report

### 1.1. Microcontroller Selection

Series	STM32H5
Line	STM32H503
MCU	STM32H503CBTx
Datasheet	DS00000_Rev0

### 1.2. Parameter Selection

Temperature	25
Vdd	3.0

### 1.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

#### 1.4. Sequence

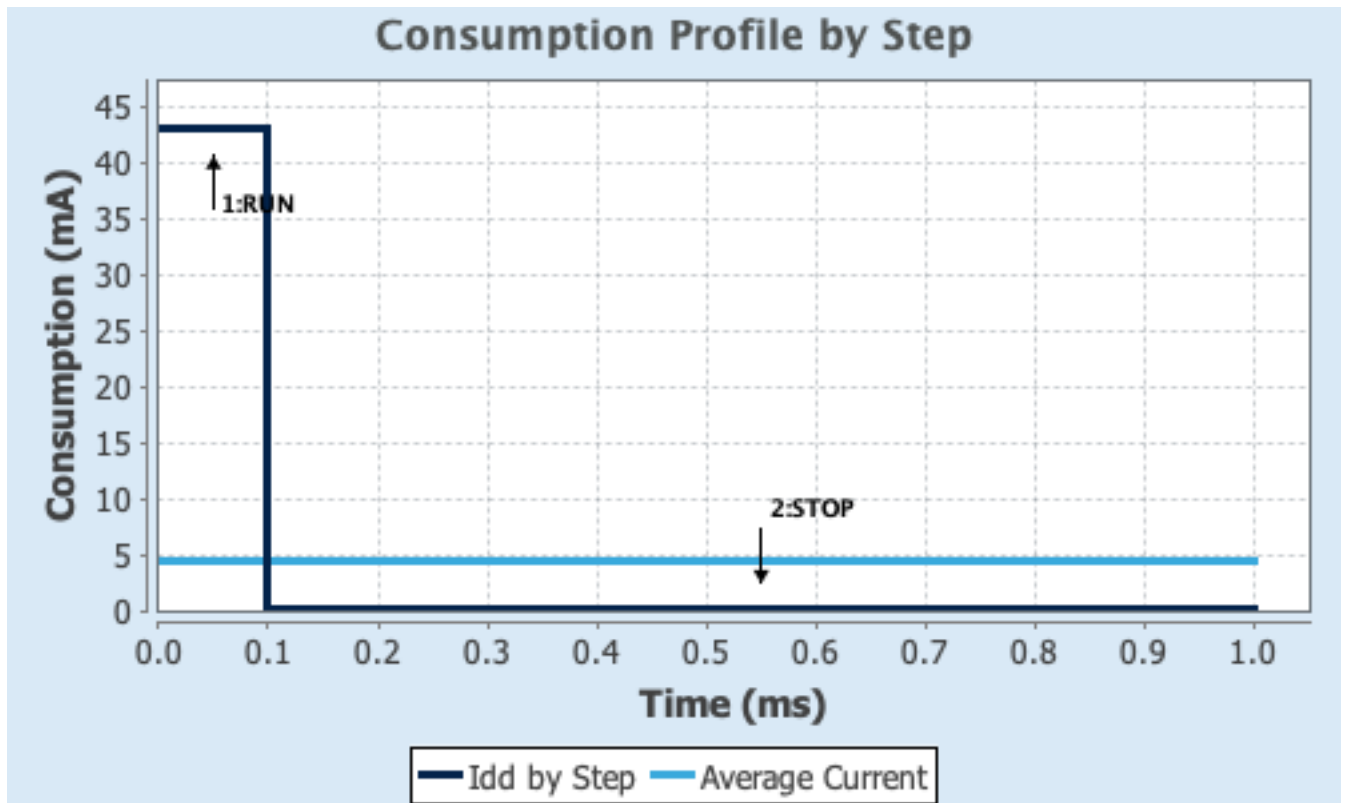
<b>Step</b>	Step1	Step2
<b>Mode</b>	RUN	STOP
<b>Vdd</b>	3.0	3.0
<b>Voltage Source</b>	Battery	Battery
<b>Range</b>	VOS0: Scale0	SVOS5: System-Scale5
<b>Fetch Type</b>	FLASH/Cache 2Ways	Flash-PowerDownSleep
<b>CPU Frequency</b>	250 MHz	0 Hz
<b>Clock Configuration</b>	HSE BYP PLL ALL_IPs_ON ALL RAM RETENTION	ALL_CLOCKS_OFF
<b>Clock Source Frequency</b>	8 MHz	0 Hz
<b>Peripherals</b>		
<b>Additional Cons.</b>	0 mA	0 mA
<b>Average Current</b>	43 mA	52 $\mu$ A
<b>Duration</b>	0.1 ms	0.9 ms
<b>DMIPS</b>	535.0	0.0
<b>Ta Max</b>	119.19	124.99
<b>Category</b>	In DS Table	In DS Table

#### 1.5. Results

Sequence Time	1 ms	Average Current	4.35 mA
Battery Life	1 month, 2 days, 3 hours	Average DMIPS	535.0 DMIPS

#### 1.6. Chart





## 2. Software Project

### 2.1. Project Settings

Name	Value
Project Name	BasicTraining
Project Folder	/Users/m/Desktop/ucSolarCar/BMS WorkSpace/BasicTraining
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_H5 V1.5.0
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

### 2.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

### 2.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_ADC1_Init	ADC1
4	MX_DAC1_Init	DAC1
5	MX_FDCAN1_Init	FDCAN1
6	MX_I2C1_Init	I2C1
7	MX_SPI2_Init	SPI2
8	MX_TIM3_Init	TIM3
9	MX_USART1_UART_Init	USART1
10	MX_USB_PCD_Init	USB
11	MX_TIM2_Init	TIM2

Rank	Function Name	Peripheral Instance Name
12	MX_TIM1_Init	TIM1

### 3. Peripherals and Middlewares Configuration

#### 3.1. ADC1

##### IN1: IN1 Differential

mode: IN14

mode: IN15

##### 3.1.1. Parameter Settings:

###### **ADC\_Settings:**

Clock Prescaler	Asynchronous clock mode divided by 8
Resolution	ADC 12-bit resolution
Scan Conversion Mode	Disabled
Data Alignment	Right alignment
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data preserved
Conversion Data Management Mode	Regular Conversion data stored in DR register only
Low Power Auto Wait	Disabled

###### **ADC\_Regular\_ConversionMode:**

Enable Regular Conversions	Enable
Enable Regular Oversampling	Disable
Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Sampling Mode	Normal
<u>Rank</u>	1
Channel	Channel 1
Sampling Time	2.5 Cycles
Offset Number	No offset
Monitored by	None

###### **ADC\_Injected\_ConversionMode:**

Enable Injected Conversions	Disable
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###### **Analog Watchdog 1:**

Enable Analog WatchDog1 Mode	false
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###### **Analog Watchdog 2:**

Enable Analog WatchDog2 Mode	false
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###### **Analog Watchdog 3:**

Enable Analog WatchDog3 Mode	false
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### 3.2. BOOTPATH

mode: Activated

### 3.3. DAC1

OUT1 connected to: only external pin

#### 3.3.1. Parameter Settings:

##### Common DAC Settings:

DAC High Frequency Mode	Disable
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##### DAC Out1 Settings:

Mode selected	Normal Mode
Output Buffer	Enable
DMA double data mode	Disable
Signed Format	Disable
Trigger	None
User Trimming	Factory trimming

### 3.4. DEBUG

Debug: JTAG (4 pins)

### 3.5. FDCAN1

mode: Activated

#### 3.5.1. Parameter Settings:

##### Basic Parameters:

Clock Divider	Divide kernel clock by 1
Frame Format	Classic mode
Mode	Normal mode
Auto Retransmission	Disable
Transmit Pause	Disable
Protocol Exception	Disable
Nominal Sync Jump Width	1
Data Prescaler	1
Data Sync Jump Width	1
Data Time Seg1	1
Data Time Seg2	1

Std Filters Nbr	0
Ext Filters Nbr	0
Tx Fifo Queue Mode	FIFO mode

#### Bit Timings Parameters:

Nominal Prescaler	<b>32 *</b>
Nominal Time Quantum	<b>128.0 *</b>
Nominal Time Seg1	<b>2 *</b>
Nominal Time Seg2	<b>3 *</b>
Nominal Time for one Bit	<b>768 *</b>
Nominal Baud Rate	<b>1302083 *</b>

### 3.6. I2C1

#### I2C: I2C

##### 3.6.1. Parameter Settings:

#### Timing configuration:

I2C Speed Mode	<b>Fast Mode *</b>
I2C Speed Frequency (KHz)	400
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	<b>0x10C043E5 *</b>

#### Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

### 3.7. MEMORYMAP

**mode: Activated**

### 3.8. PWR

**mode: Power saving mode**

## mode: Privilege attributes

### 3.8.1. PWR Privilege :

#### Privilege PWR:

PWR Privilege	Disable
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## 3.9. RCC

**High Speed Clock (HSE): Crystal/Ceramic Resonator**

**Low Speed Clock (LSE) : Crystal/Ceramic Resonator**

### 3.9.1. Parameter Settings:

#### System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	5 WS (6 CPU cycle)
Flash Programming Delay	2

#### RCC Parameters:

HSI Calibration Value	64
CSI Calibration Value	16
HSE Startup Timeout Value (ms)	100
LSE Startup Timeout Value (ms)	5000
LSE Drive Capability	LSE oscillator low drive capability

#### Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 0
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#### PLL1/2/3 Parameters:

PLL1 input frequency range	Between 8 and 16 MHz
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## 3.10. SPI2

**Mode: Full-Duplex Master**

### 3.10.1. Parameter Settings:

#### Basic Parameters:

Frame Format	Motorola
Data Size	<b>8 Bits *</b>
First Bit	MSB First

#### Clock Parameters:

Prescaler (for Baud Rate)	<b>4 *</b>
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Baud Rate	<b>8.0 MBits/s *</b>
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge
<b>CRC Parameters:</b>	
CRC Calculation	Disabled
<b>Advanced Parameters:</b>	
NSSP Mode	Enabled
NSS Signal Type	Software
Fifo Threshold	Fifo Threshold 01 Data
Nss Polarity	Nss Polarity Low
Master Ss Idleness	00 Cycle
Master Inter Data Idleness	00 Cycle
Master Receiver Auto Susp	Disable
Master Keep Io State	Master Keep Io State Disable
IO Swap	Disabled
Ready Master Management	Internal
Ready Signal Polarity	High

### 3.11. SYS

**Timebase Source: SysTick**

### 3.12. TIM1

**Channel1: Output Compare No Output**

#### 3.12.1. Parameter Settings:

##### **Counter Settings:**

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Dithering	Disable
Counter Period (AutoReload Register - 16 bits value )	65535
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	Disable

##### **Trigger Output (TRGO) Parameters:**

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

##### **Break And Dead Time management - BRK Configuration:**

BRK State	Disable
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BRK Polarity	High
BRK Filter (4 bits value)	0
BRK Sources Configuration	
- Digital Input	Disable
- COMP1	Disable

#### Break And Dead Time management - BRK2 Configuration:

BRK2 State	Disable
BRK2 Polarity	High
BRK2 Filter (4 bits value)	0
BRK2 Sources Configuration	
- Digital Input	Disable
- COMP1	Disable

#### Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

#### Clear Input:

Clear Input Source	Disable
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#### Output Compare No Output Channel 1:

Mode	Frozen (used for Timing base)
Pulse (16 bits value)	0
Output compare preload	Disable
CH Polarity	High
CH Idle State	Reset

### 3.13. TIM2

**Clock Source : Internal Clock**

**Channel1: Input Capture direct mode**

#### 3.13.1. Parameter Settings:

##### Counter Settings:

Prescaler (PSC - 16 bits value)	<b>250 -1 *</b>
Counter Mode	Up
Dithering	Disable
Counter Period (AutoReload Register - 32 bits value )	4294967295
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

##### Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

#### Input Capture Channel 1:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

### 3.14. TIM3

**Clock Source : Internal Clock**

**Channel1: PWM Generation No Output**

#### 3.14.1. Parameter Settings:

##### Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Dithering	Disable
Counter Period (AutoReload Register - 16 bits value )	65535
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

##### Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

##### Clear Input:

Clear Input Source	Disable
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##### PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

### 3.15. USART1

**Mode: Asynchronous**

#### 3.15.1. Parameter Settings:

##### Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

#### Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

#### Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

### 3.16. USB

#### Mode: Device\_Only

##### 3.16.1. Parameter Settings:

#### Basic Parameters:

Speed	Full Speed 12MBit/s
Physical interface	Internal Phy
Signal start of frame	Disabled

#### Power Parameters:

Low Power	Disabled
Link Power Management	Disabled
Battery Charging	Disabled

#### EndPoint Parameters:

Bulk double buffer	Disabled
Iso single buffer	Disabled

**\* User modified value**

## 4. System Configuration

### 4.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA0	ADC1_INN1	Analog mode	No pull-up and no pull-down	n/a	
	PA1	ADC1_INP1	Analog mode	No pull-up and no pull-down	n/a	
	PA2	ADC1_INP14	Analog mode	No pull-up and no pull-down	n/a	
	PA3	ADC1_INP15	Analog mode	No pull-up and no pull-down	n/a	
DAC1	PA4	DAC1_OUT1	Analog mode	No pull-up and no pull-down	n/a	
DEBUG	PA13(JTMS/SWDIO)	DEBUG_JTMS-SWDIO	n/a	n/a	n/a	
	PA14(JTCK/SWCLK)	DEBUG_JTCK-SWCLK	n/a	n/a	n/a	
	PA15(JTDI)	DEBUG_JTDI	n/a	n/a	n/a	
	PB3(JTDO/TRACESWO)	DEBUG_JTDO-SWO	n/a	n/a	n/a	
FDCAN1	PB4(NJTRST)	FDCAN1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB5	FDCAN1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
I2C1	PB6	I2C1_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Low	
	PB7	I2C1_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Low	
RCC	PC14-OSC32_IN(OSC32_IN)	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15-OSC32_OUT(OSC32_OUT)	RCC_OSC32_OUT	n/a	n/a	n/a	
	PH0-OSC_IN(PH0)	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-OSC_OUT(PH1)	RCC_OSC_OUT	n/a	n/a	n/a	
SPI2	PB13	SPI2_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB14	SPI2_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB15	SPI2_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM2	PA5	TIM2_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART1	PA9	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA10	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USB	PA11	USB_DM	n/a	n/a	n/a	
	PA12	USB_DP	n/a	n/a	n/a	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
Single Mapped Signals	PA6	TIM3_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
GPIO	PC13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED0
	PA7	GPIO_EXTI7	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	ACC_INT2
	PB0	GPIO_EXTI0	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	ACC_INT1
	PB1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	IOX_nRESET
	PB2	GPIO_EXTI2	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	IOX_INTB
	PB10	GPIO_EXTI10	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	IOX_INTA
	PB12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SPI2_CS_IOX
	PA8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SPI2_CS0
	PB8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	TRIG

#### 4.2. GPDMA1

#### 4.3. GPDMA2

#### 4.4. LINKEDLIST

## 4.5. NVIC configuration

### 4.5.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	15	0
EXTI Line0 interrupt	true	0	0
EXTI Line2 interrupt	true	0	0
EXTI Line7 interrupt	true	0	0
EXTI Line10 interrupt	true	0	0
TIM2 global interrupt	true	0	0
Flash non-secure global interrupt	unused		
RCC non-secure global interrupt	unused		
ADC1 global interrupt	unused		
DAC1 interrupt	unused		
FDCAN1 interrupt 0	unused		
FDCAN1 interrupt 1	unused		
TIM1 Break interrupt	unused		
TIM1 Update interrupt	unused		
TIM1 Trigger and Commutation interrupts	unused		
TIM1 Capture Compare interrupt	unused		
TIM3 global interrupt	unused		
I2C1 Event interrupt	unused		
I2C1 Error interrupt	unused		
SPI2 global interrupt	unused		
USART1 global interrupt	unused		
USB FS global interrupt	unused		
FPU global interrupt	unused		

### 4.5.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
EXTI Line0 interrupt	false	true	true
EXTI Line2 interrupt	false	true	true
EXTI Line7 interrupt	false	true	true
EXTI Line10 interrupt	false	true	true
TIM2 global interrupt	false	true	true

\* User modified value



## 5. System Views

### 5.1. Category view

#### 5.1.1. Current

Middleware										
System Core	Analog	Timers	Connectivity	Multimedia	Security	Computing	Trace and Debug	Power and Therma	Utilities	Other
CORTEX_M33_NS	ADC1 ✓	TIM1 ✓	FDCAN1 ✓				DEBUG ✓	PWR ✓	LINKEDLIST	
GPDMA1	DAC1 ✓	TIM2 ✓	I2C1 ✓							
GPDMA2		TIM3 ✓	SPI2 ✓							
GPIO ⚠			USART1 ✓							
NVIC ✓			USB ✓							
RCC ✓										
SYS ✓										

## 6. Docs & Resources

Type	Link
BSDL files	<a href="https://www.st.com/resource/en/bsdl_model/stm32h5-bsdl.zip">https://www.st.com/resource/en/bsdl_model/stm32h5-bsdl.zip</a>
IBIS models	<a href="https://www.st.com/resource/en/ibis_model/stm32h5-ibis.zip">https://www.st.com/resource/en/ibis_model/stm32h5-ibis.zip</a>
System View Description	<a href="https://www.st.com/resource/en/svd/stm32h5-svd.zip">https://www.st.com/resource/en/svd/stm32h5-svd.zip</a>
Presentations	<a href="https://www.st.com/resource/en/product_presentation/stm32-stm8_embedded_software_solutions.pdf">https://www.st.com/resource/en/product_presentation/stm32-stm8_embedded_software_solutions.pdf</a>
Presentations	<a href="https://www.st.com/resource/en/product_presentation/stm32_eval_tools_portfolio.pdf">https://www.st.com/resource/en/product_presentation/stm32_eval_tools_portfolio.pdf</a>
Presentations	<a href="https://www.st.com/resource/en/product_presentation/stm32-stm8_software_development_tools.pdf">https://www.st.com/resource/en/product_presentation/stm32-stm8_software_development_tools.pdf</a>
Presentations	<a href="https://www.st.com/resource/en/product_presentation/microcontrollers-stm32h5-series-overview.pdf">https://www.st.com/resource/en/product_presentation/microcontrollers-stm32h5-series-overview.pdf</a>
Presentations	<a href="https://www.st.com/resource/en/product_presentation/microcontrollers-stm32-family-overview.pdf">https://www.st.com/resource/en/product_presentation/microcontrollers-stm32-family-overview.pdf</a>
Presentations	<a href="https://www.st.com/resource/en/product_presentation/microcontrollers-stm32-entry-level-graphics.pdf">https://www.st.com/resource/en/product_presentation/microcontrollers-stm32-entry-level-graphics.pdf</a>
Presentations	<a href="https://www.st.com/resource/en/product_presentation/stm32-graphics-solution-overview.pdf">https://www.st.com/resource/en/product_presentation/stm32-graphics-solution-overview.pdf</a>
Presentations	<a href="https://www.st.com/resource/en/product_presentation/stm32-graphics-solutions-detailed.pdf">https://www.st.com/resource/en/product_presentation/stm32-graphics-solutions-detailed.pdf</a>
Brochures	<a href="https://www.st.com/resource/en/brochure/products-and-solutions-for-plcs-and-smart-i-os.pdf">https://www.st.com/resource/en/brochure/products-and-solutions-for-plcs-and-smart-i-os.pdf</a>
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Datasheet	<a href="https://www.st.com/resource/en/datasheet/dm00903063.pdf">https://www.st.com/resource/en/datasheet/dm00903063.pdf</a>
Programming Manuals	<a href="https://www.st.com/resource/en/programming_manual/pm0264-stm32-cortexm33-mcus-and-mpus-programming-manual-stmicroelectronics.pdf">https://www.st.com/resource/en/programming_manual/pm0264-stm32-cortexm33-mcus-and-mpus-programming-manual-stmicroelectronics.pdf</a>
Reference Manuals	<a href="https://www.st.com/resource/en/reference_manual/rm0492-stm32h503-line-armbased-32bit-mcus-stmicroelectronics.pdf">https://www.st.com/resource/en/reference_manual/rm0492-stm32h503-line-armbased-32bit-mcus-stmicroelectronics.pdf</a>
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Technical Notes & Articles	<a href="https://www.st.com/resource/en/technical_note/tn1204-tape-and-reel-shipping-media-for-stm32-microcontrollers-in-bga-packages-stmicroelectronics.pdf">https://www.st.com/resource/en/technical_note/tn1204-tape-and-reel-shipping-media-for-stm32-microcontrollers-in-bga-packages-stmicroelectronics.pdf</a>
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