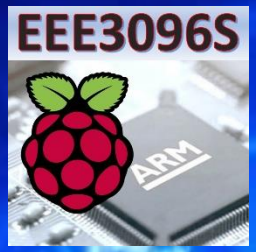


ADC Metrics, DACs

…and towards a cosy digital world ☺

Embedded Systems II

L21

Dr Simon Winberg

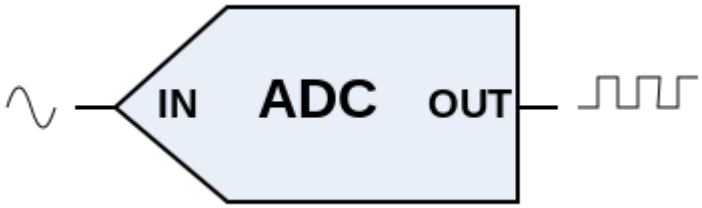
Electrical Engineering
University of Cape Town

Outline of Lecture

- ADC metrics
- DACs

This presentation contains some slides adapted from course textbook "Embedded System Design Embedded Systems Foundations of Cyber-Physical Systems, and the Internet of Things" by Peter Marwedel

ADCs Metrics



Analogue to Digital Convertors (ADCs)

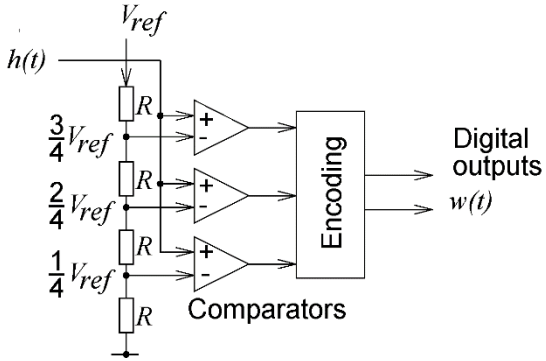
ADC Resolution

- Resolution (in bits): number of bits produced
- Resolution Q (in volts): difference between two input voltages causing the output to be incremented by 1

$$Q = \frac{V_{FSR}}{n}$$ with

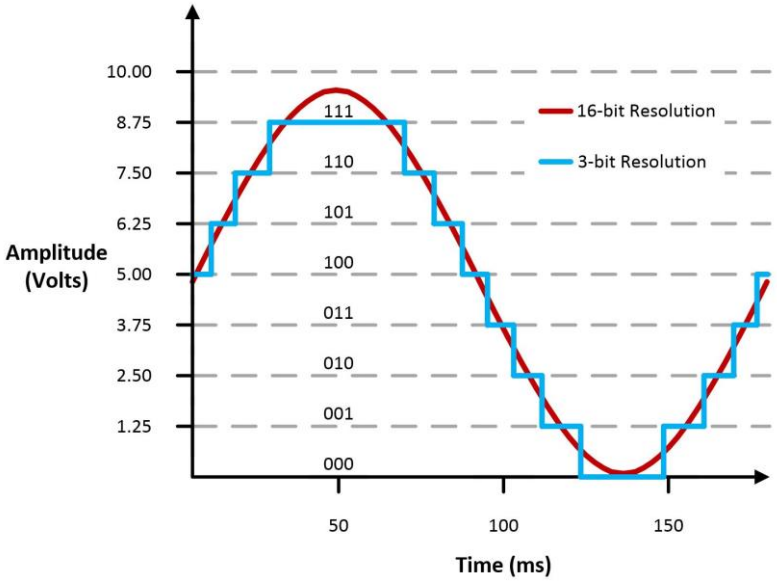
Q: resolution in volts per step
V_{FSR}: difference between largest and smallest voltage
n: number of voltage intervals

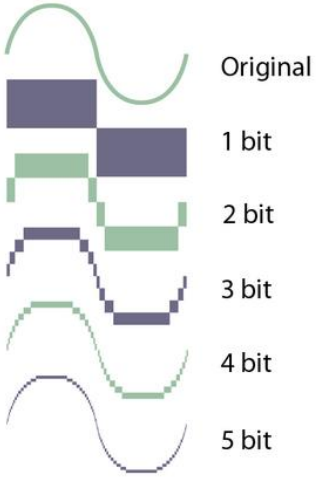
Example:
$Q = V_{ref}/4$ for this flash ADC example



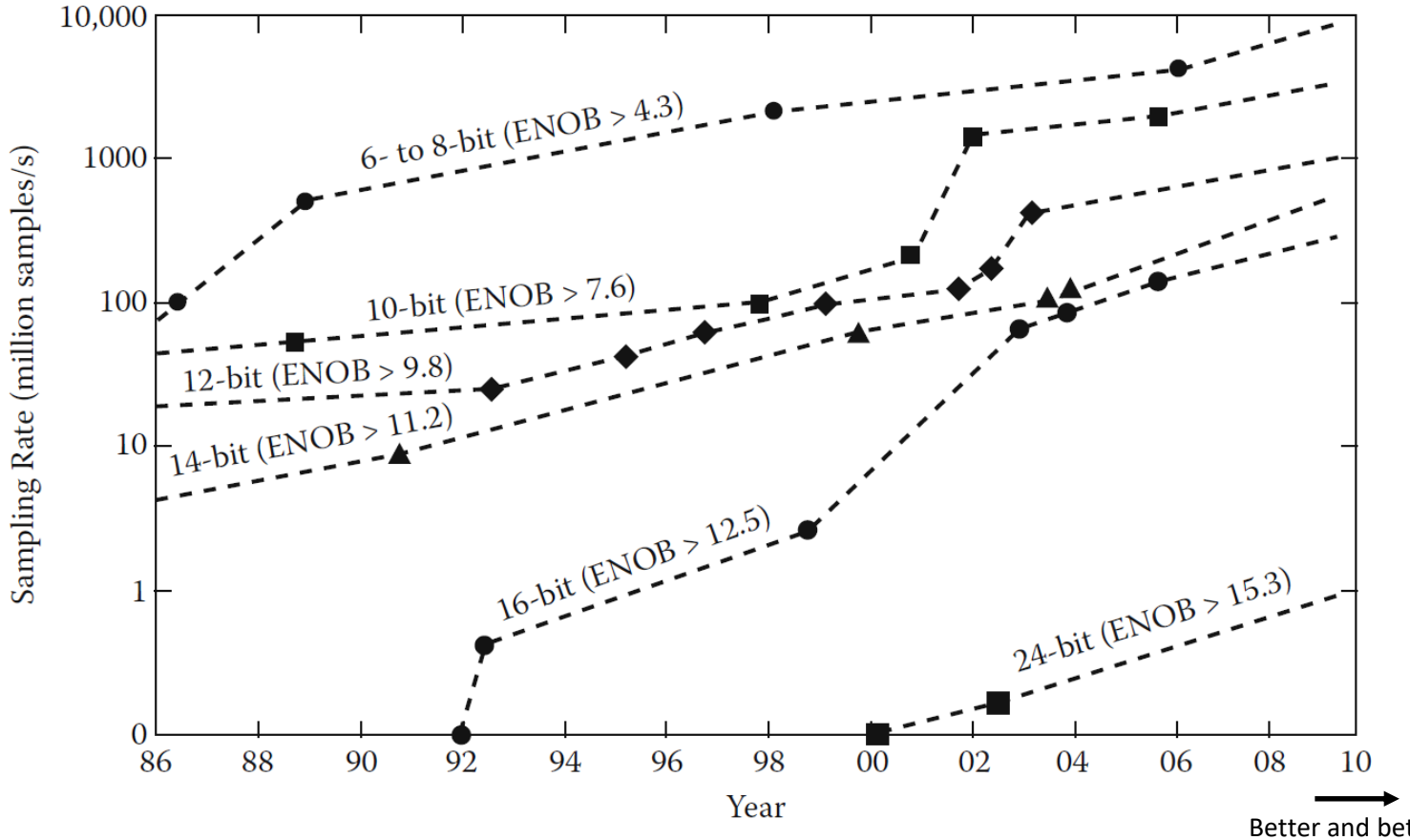
Resolution of an ADC

$$Number\ of\ Unique\ Codes = 2^N\ , where\ N\ is\ the\ number\ of\ bits$$





Trends over the years in resolution



Static metrics for an ADC

- Most simple but also very important ADC performance metrics is the
  - Static, DC (direct current, or zero-frequency constant input) performance of the devices.
  - i.e. does it read 0 when the input is 0V?

Static Metrics: Offset Error

OFFSET ERROR:

The offset error of an ADC, which is similar to the offset error of an amplifier, is defined as a deviation of the ADC output code transition points that is present across all output codes.

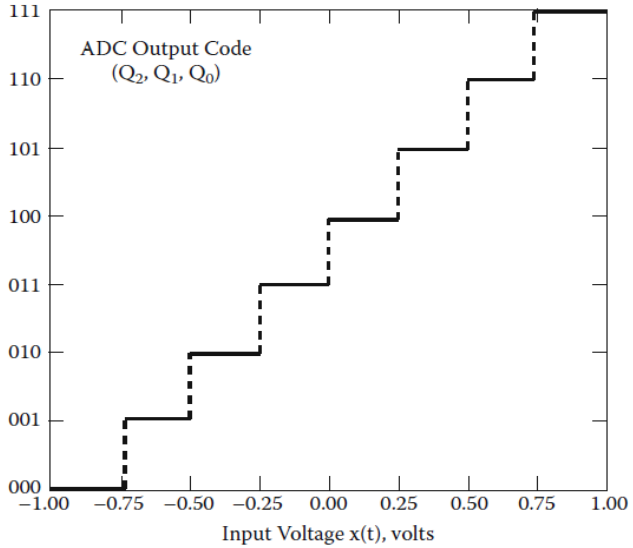


FIGURE 7-2 Conceptual ADC transfer function.

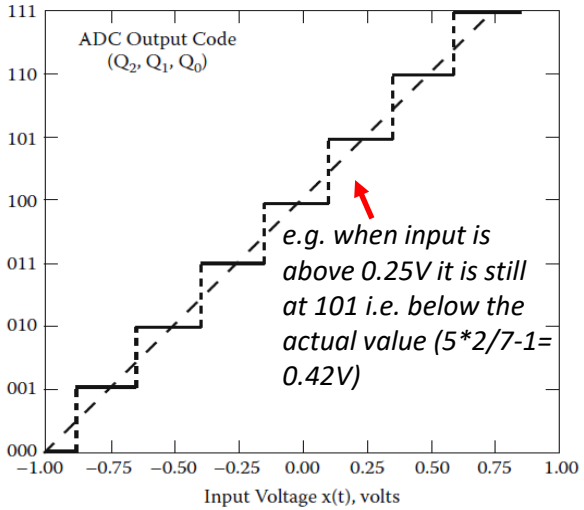
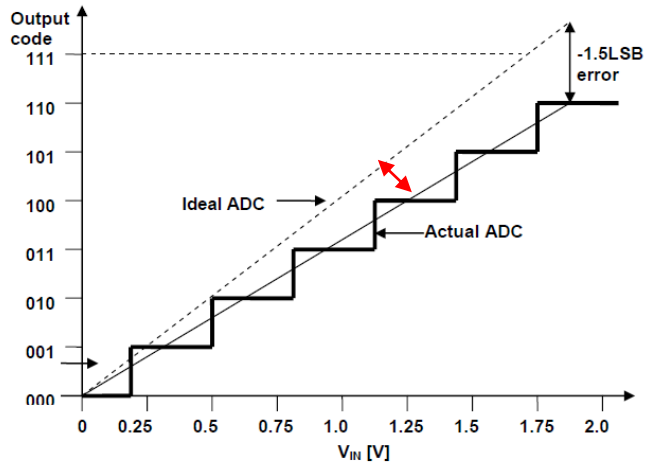


FIGURE 7-3 Ideal ADC transfer function.

Static metrics: Gain Error

- GAIN ERROR:
  - The gain error of an ADC is similar to the gain error of an amplifier.
  - Assuming ADC's offset error removed, then:
    - The gain error determines the amount of "rotational" deviation away from the ADC's ideal transfer function slope (i.e., the dashed diagonal line of the figure).
  - Once the gain error has been characterized, it may be possible to compensate for this error source.

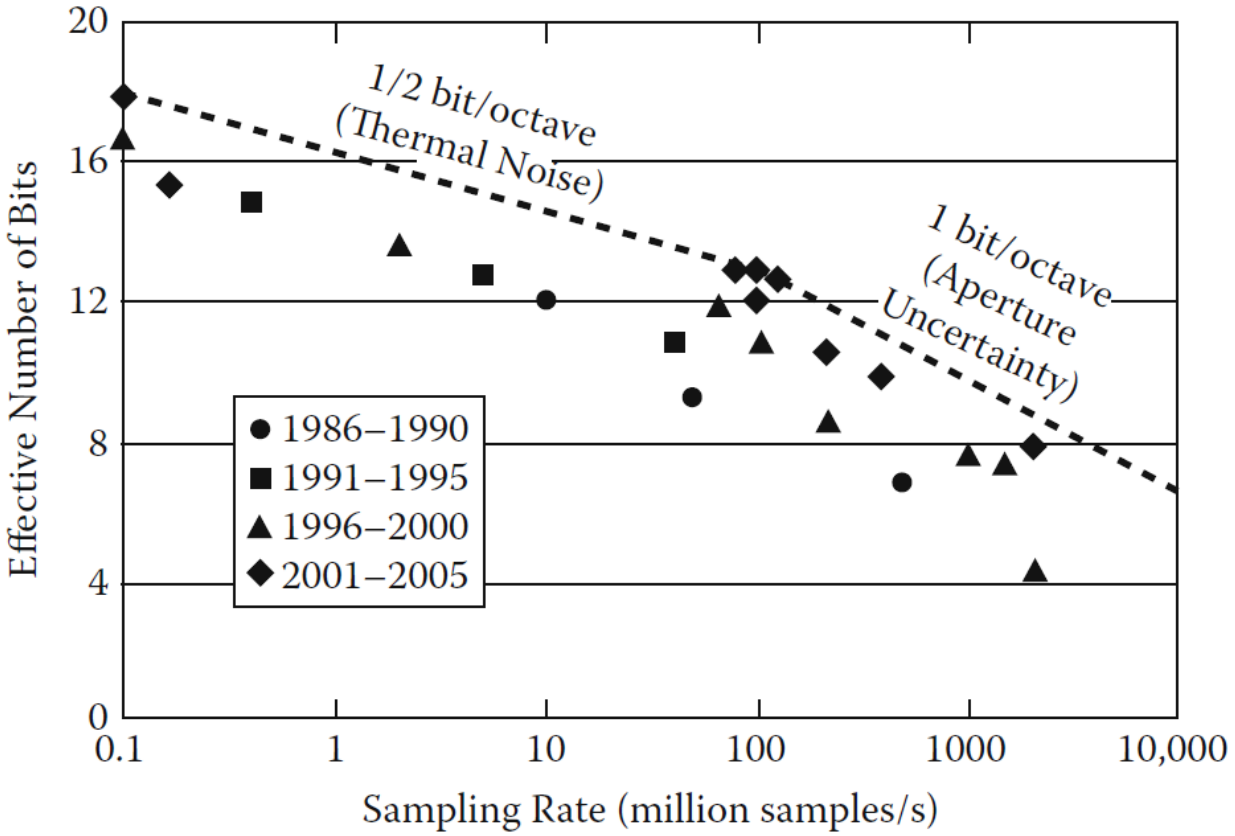


Dynamic Measures: Effective Number of Bits (ENOB)

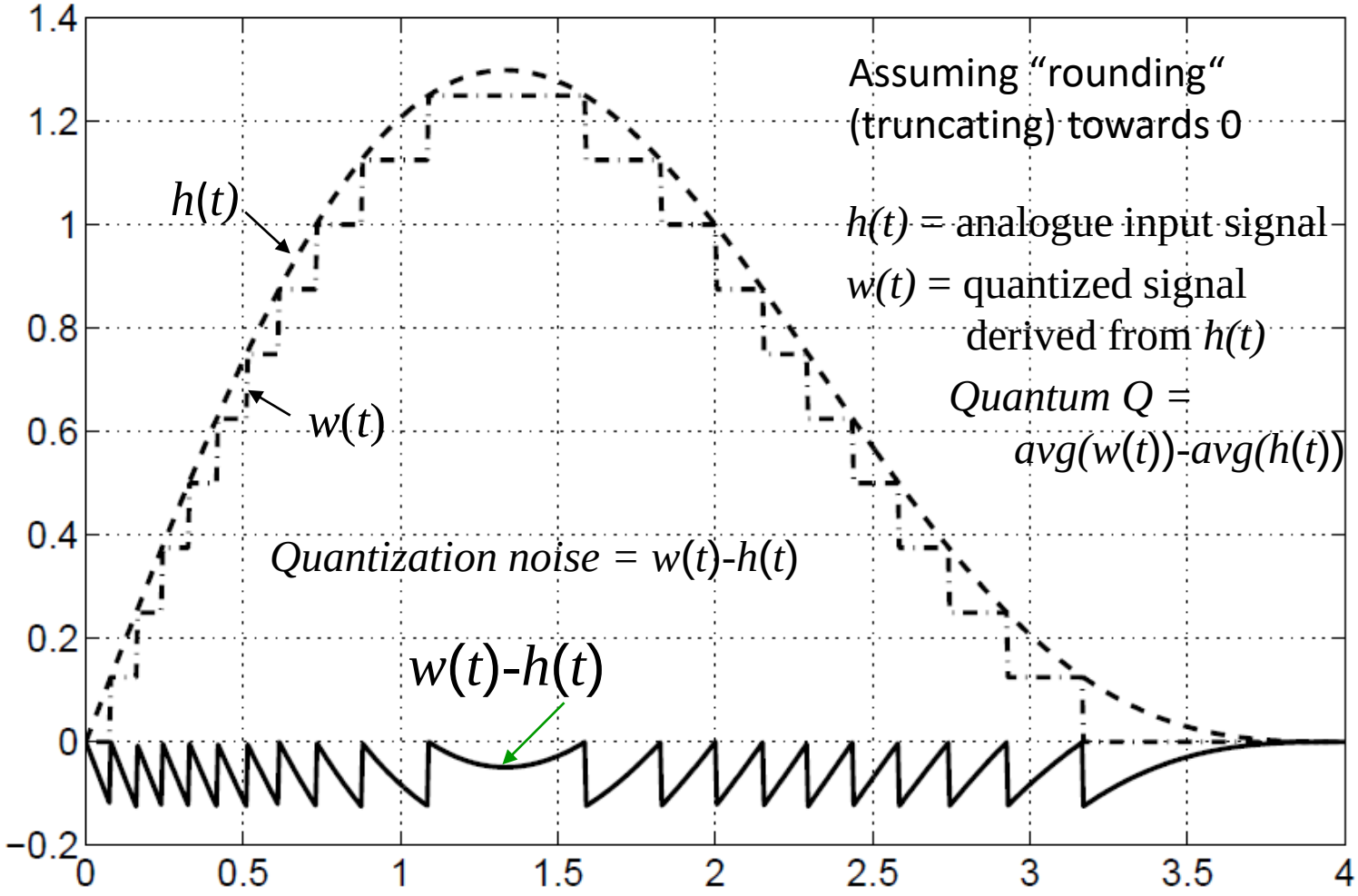
- Effective number of bits (ENOB)
  - The resolution of an ADC is specified by the number of bits used to represent the analogue value, in principle giving $\mathbf{2}^{N}$ signal levels for an N-bit signal.
  - The ENOB indicates how many bits effectively contribute towards representing the sampled input.

Bad ENOBs are like bad apples for an embedded engineer

Trends in ENOB vs Speed

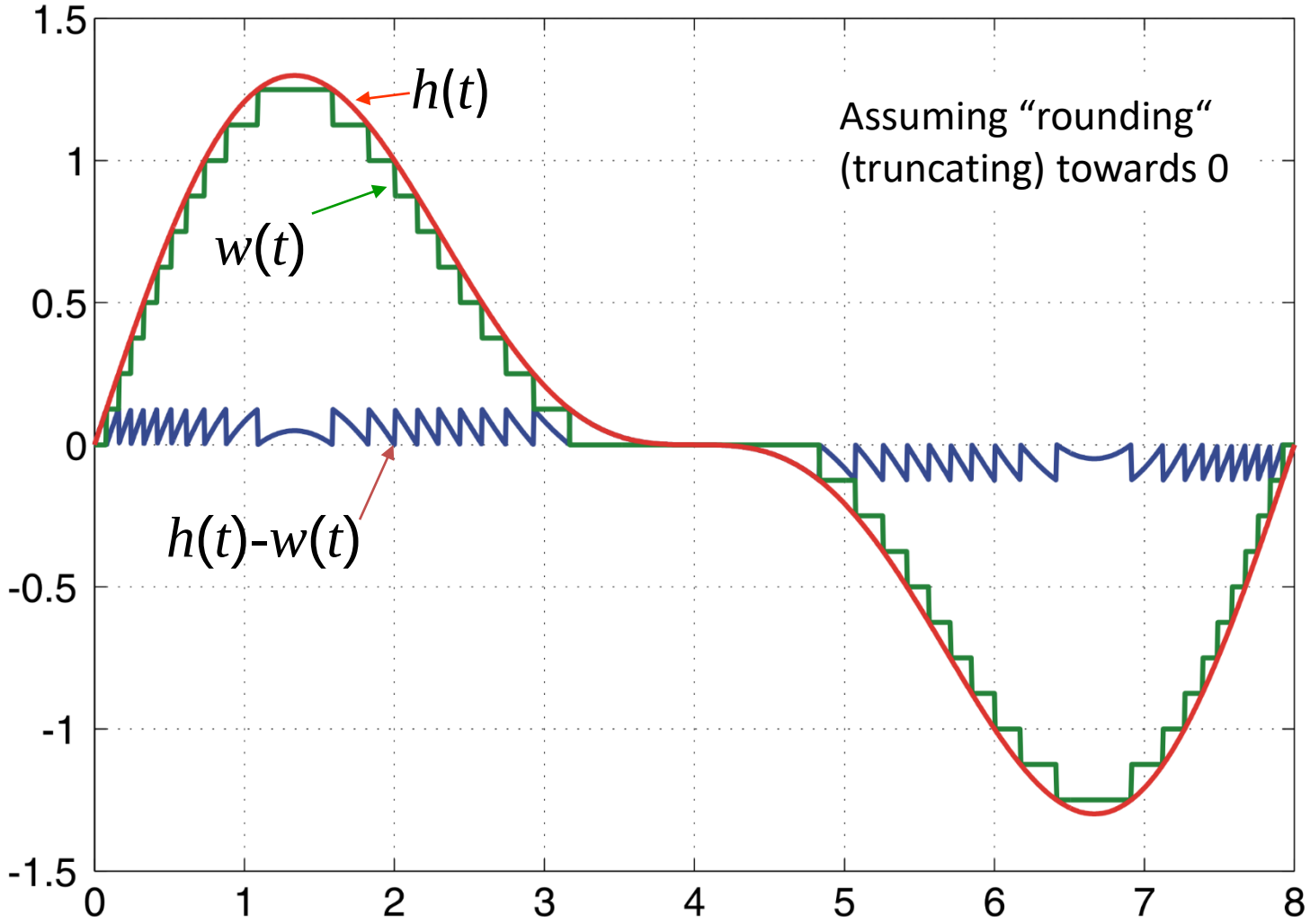


Quantization Noise



So, if I asked you to graph how the difference between the input signal (i.e. *h(t)*) and the quantization transfer (i.e. *w(t)*) looks you would be able to show that pretty easy now.

Quantization Noise



h(t) = analogue input signal *w(t)* = quantized signal derived from *h(t)*

Quantization Noise Impacts SNR

- Remember what we said about Shannon and channel capacity. Part of that exercise was working out the SNR. The quantization noise adds to other noise that may be hindering the channel.
- SNR = signal/noise
  SNR in bB = $10\log_{10}(\text{signal/noise})$

  SNR in bB = $20\log_{10}(\text{Vsignal/Vnoise})$ *

  SNR_Q in dB = $20\log_{10}(n/\alpha Q)$

  α characterizes how well w(t) tracks h(t)

  α=0 → h(t) = w(t) α=1 → w(t) a little off from h(t)

  clearly α=0 → perfect (infinite) SNR α=1 → strong signal

* For voltage the power is proportional to V^2 hence the x2 for in the 2nd equation

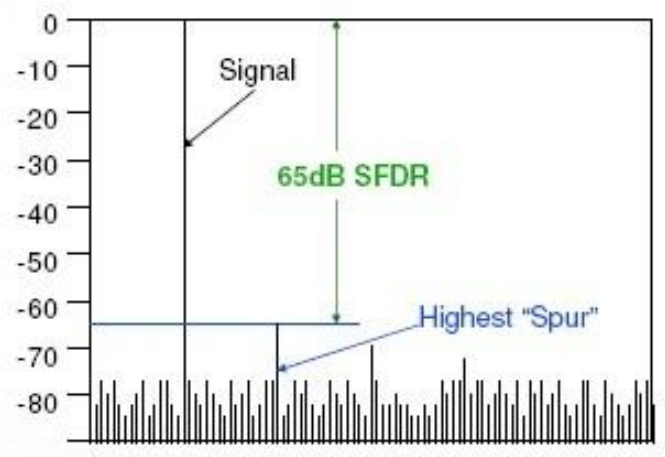
Spurious-Free Dynamic Range (SFDR)

Spurious-free Dynamic Range (SFDR):

- This is a frequency-domain measurement that determines the minimum signal level that can be distinguished from spurious components, and includes all spurious components over the full Nyquist band regardless of their origin
- SFDR for a ADC typically decreases as sampling rate increases. (It is generally indicate as a power or S/N ratio value)

This can be calculated for sampling real systems by sampling a known sinusoidal reference (or carrier signal) with minimum interference, sample it for a period and perform a Fourrier transfer to find the difference between the max. of the spurious signals and the full scale range (P_{FS} corresponds to the maximal power measured). Note: must put the spectrum in dBs i.e. $10\log_{10}(P_S/P_{REF})$.

Example of measuring SFDR



noise spurs are at the bottom of the plot

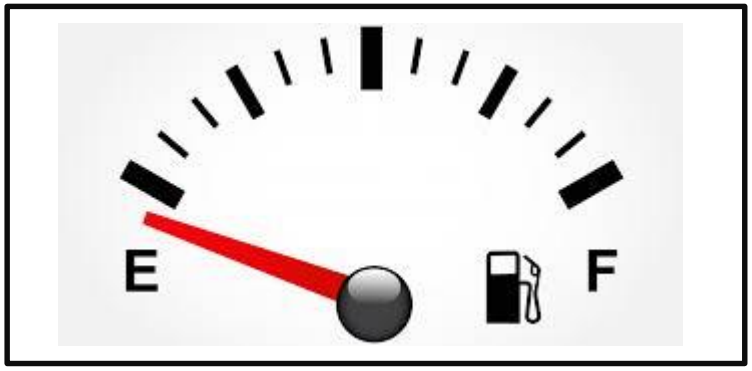
Done with ADCs

Now were are DONE with ADCs ☺

and

Full up on knowledge of ADC

for likely embedded systems needs

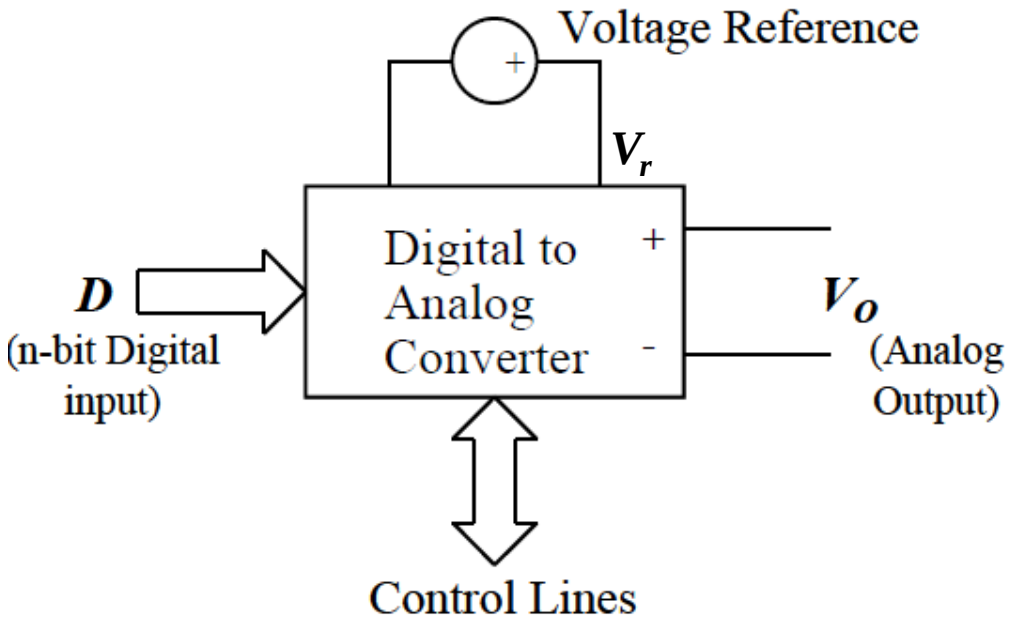


Out of patience

for any more ADC theories

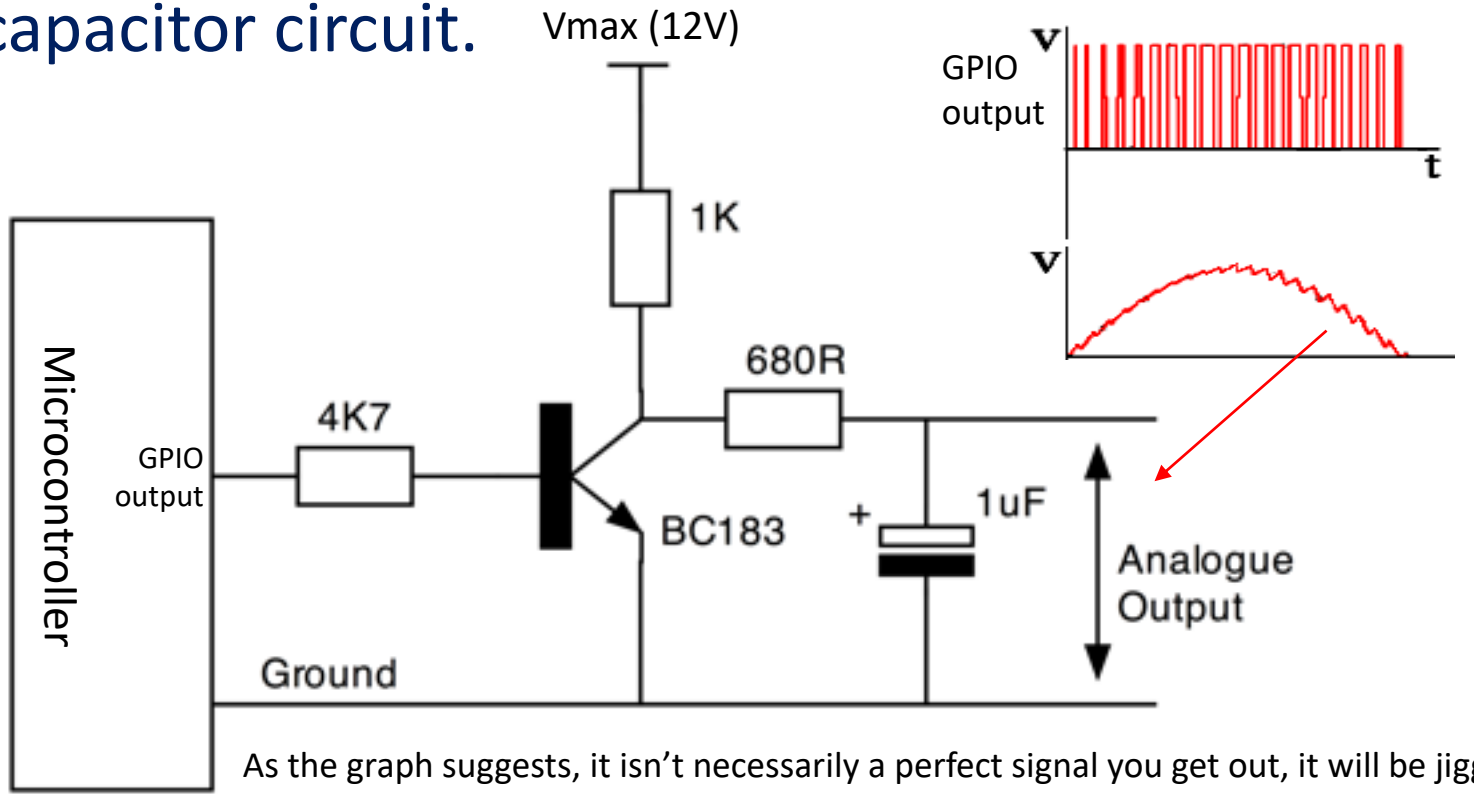
DAC Conceptual Design

- $\boldsymbol{D}$ is the digital input
- $\boldsymbol{V_O}$ is the Analog output
- $\boldsymbol{V_r}$ is a precise, stable, known voltage reference
- Some control lines: e.g. activate DAC to convert the input signal.



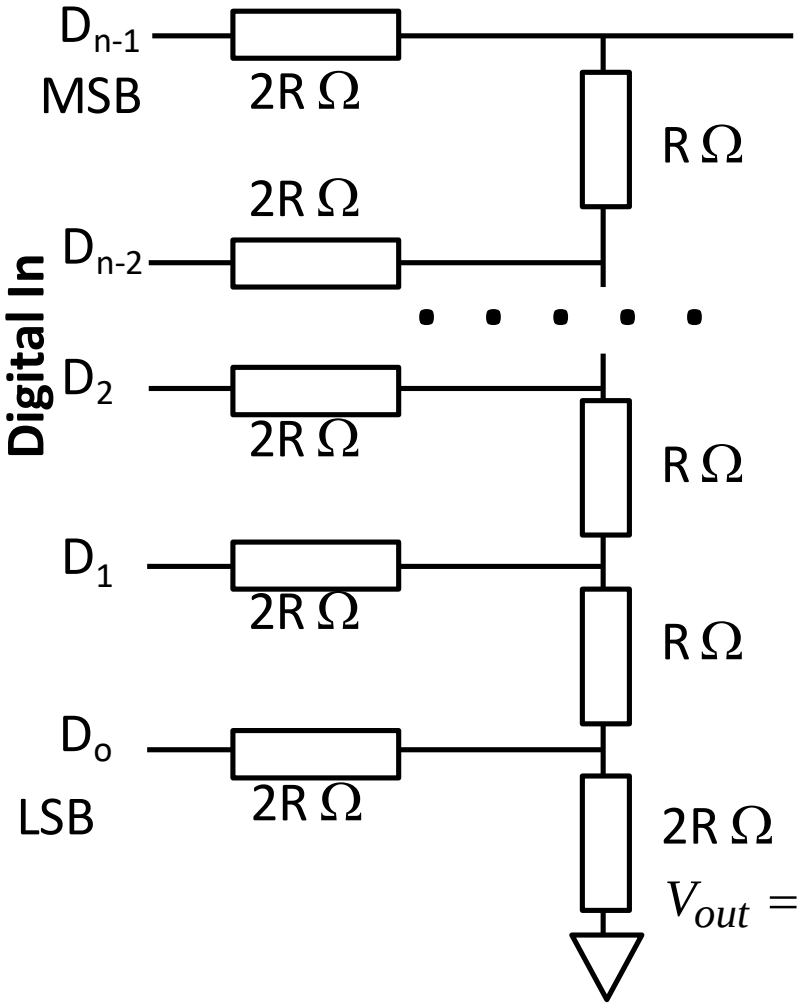
PWM DAC – Cheap and Nasty

- This hardly needs explaining, basically you change the duty cycle of a PWM digital signal sent (best practice) through a buffer or amp and a simple LPF capacitor circuit.



As the graph suggests, it isn't necessarily a perfect signal you get out, it will be jiggered around the edges due to the cap continueously charging and discharging, and sudden big voltage changes (e.g. from 0000_2 -> 1111_2 form one sample to the next may be impossible.

Standard Decent DAC



V_{out} – Analog Out

This is how you can essentially built one from first principles. It is pretty much efficient and a typical approach to implement a DAC. It is well suited to being fabricated as a silicon chip. Assume the D values are either 0 or 5V, there are things like FETs hidden.

Check what you get for Vout given n=4, D_i inputs set to 1V or 0V – e.g. see what 1001_2 will output, it's a good test of your knowledge of Thévenin's theorem:

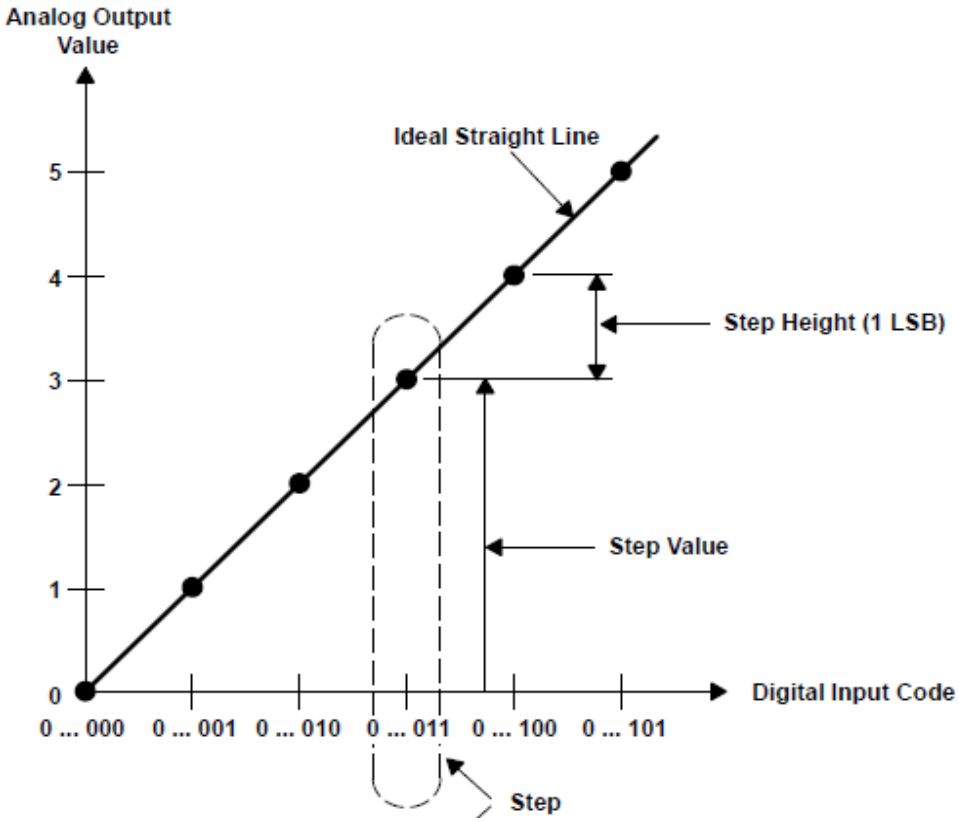
$$V_{out} = \frac{V_r}{2^n}\left(D_{n-1}2^{n-1} + D_{n-2}2^{n-2} + \ldots + D_o 2^0\right)$$

Answer:

1000_2 → 5V / 16 (1*8 + 0*4 + 0*2 + 1*1) = 5*(8 + 1) / 16 = 2.8125V

DACs Metrics

- You can apply pretty much most of the metrics we discussed for ADCs to DACs



Generally the difference (what you change for the ADC case) is that *h(t)* becomes the ideal transfer function, what the ADC should ideally output for the quantized inputs, and *w(t)* becomes the actual output.

(generally you want the DAC to have an ideal transfer function that is linear, but this isn't necessarily always the case)

Done with DACs

- Generally the basic design of a DAC is fast, efficient and not demanding on resources as is the case with responsive ADCs.
- Therefore I find it unnecessary to explore other DAC design (like switch capacitor network, chained DACs, etc.) for the purposes of this course.

Full up on knowledge of DAC
for likely embedded systems needs

End of Term 3

Have a happy mid-term break!

The Next Episode…

Lecture L22

Over to Dr Gaffar