# FINN Radio ML on FPGA

## Report from building and training model (VGG10 - 27modulations)

- The model followed the architecture (VGG10) mentioned in *RadioML Meets FINN: Enabling Future RF Applications With FPGA Streaming Architectures*

| Building Model |
|---|
| • Seven 1D-Convolutional layers, kernel size of 3, each followed by Batch Normalization, ReLU activation, and 1D Maxpool that reduces the layer by half<br>• One Flatten Layer<br>• Two Linear Layers, each follwed by Batch Normalization and ReLU activation<br>• One Final Linear Layers performing modulation classification |
| Total parameters (all trainable): 160932 |

- The model ran for 15 epochs (stopped early due to no improvements), and has accuracy of 61.5746% for all SNRs. At the highest SNR (30dB), the model has an accuracy of 95.4291%



*Confusion Matrix (across all SNRs)*
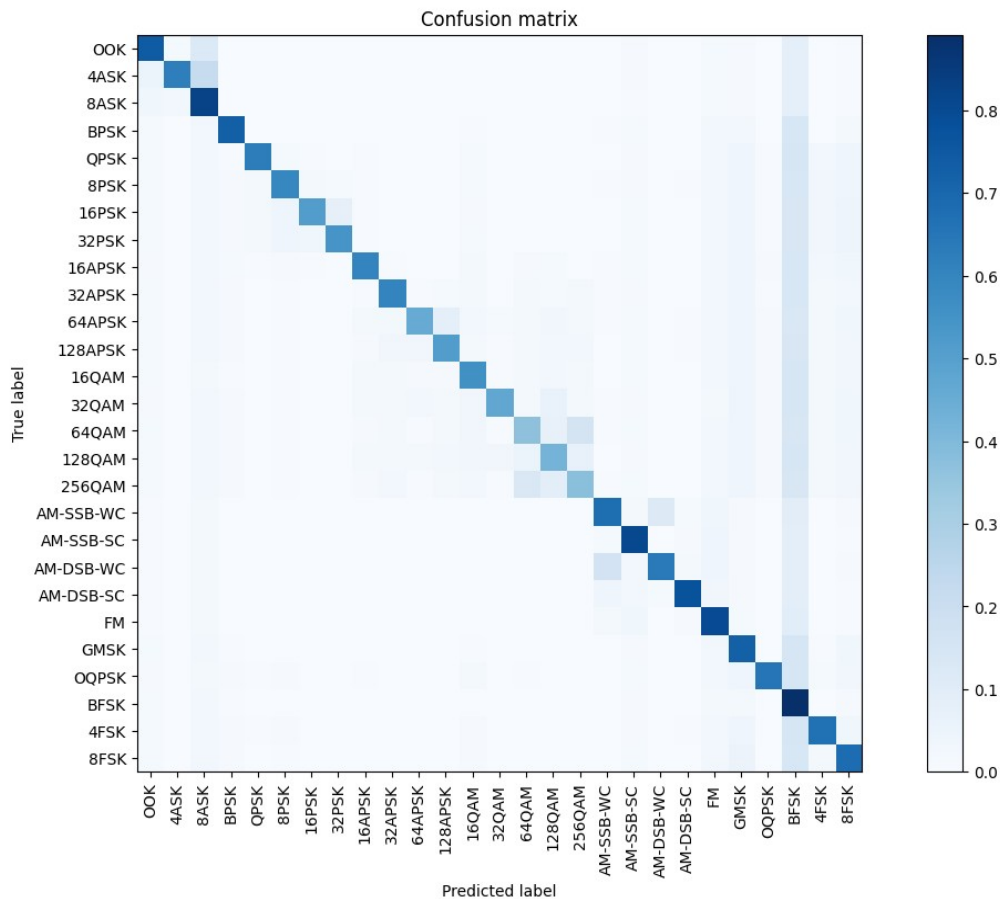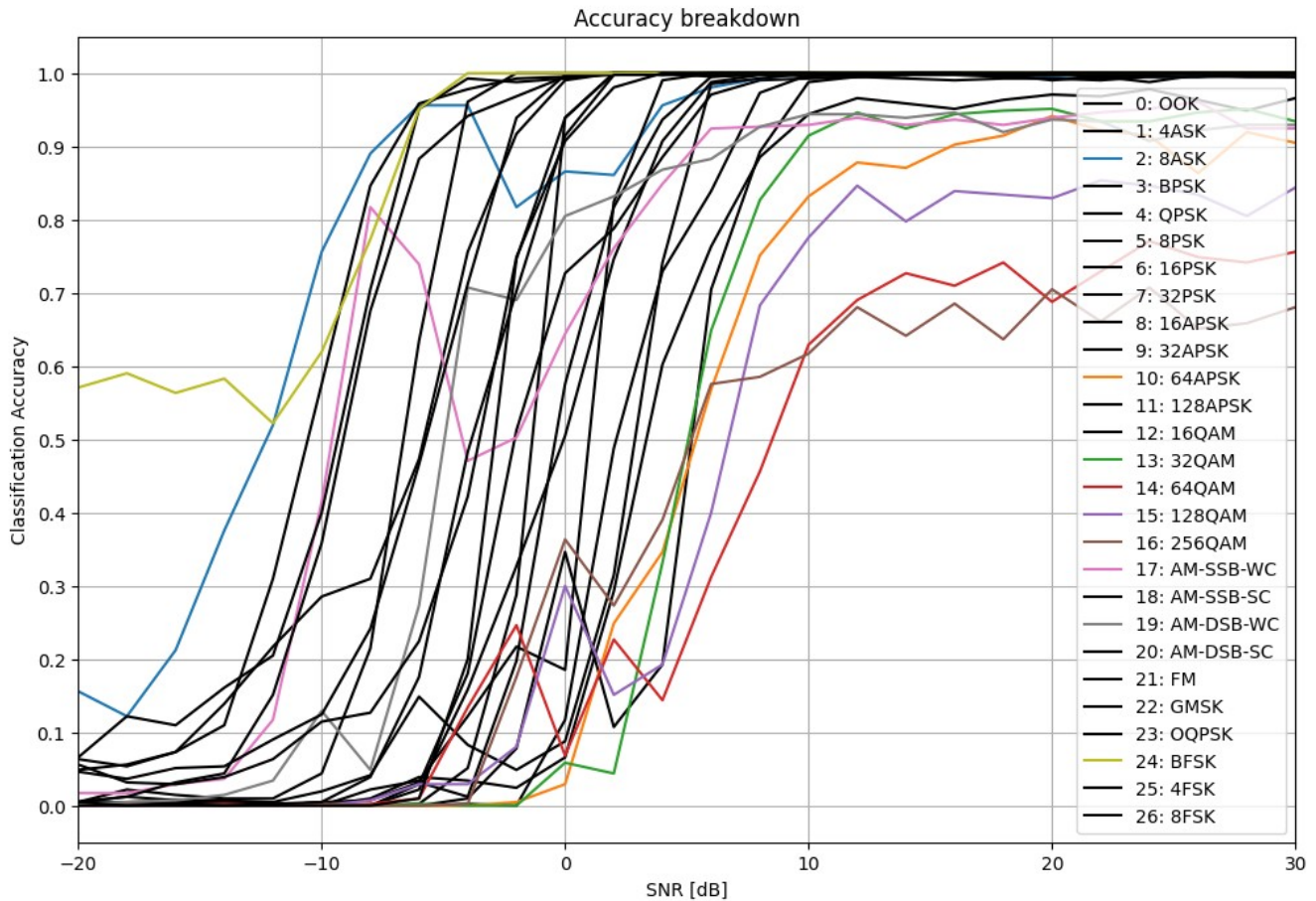
*Accuracy Breakdown of Each Classification (across all SNRs)*

## Report from running throughput and verification on FPGA

- Throughput or FPS is measured in [images/s] or frames per second.
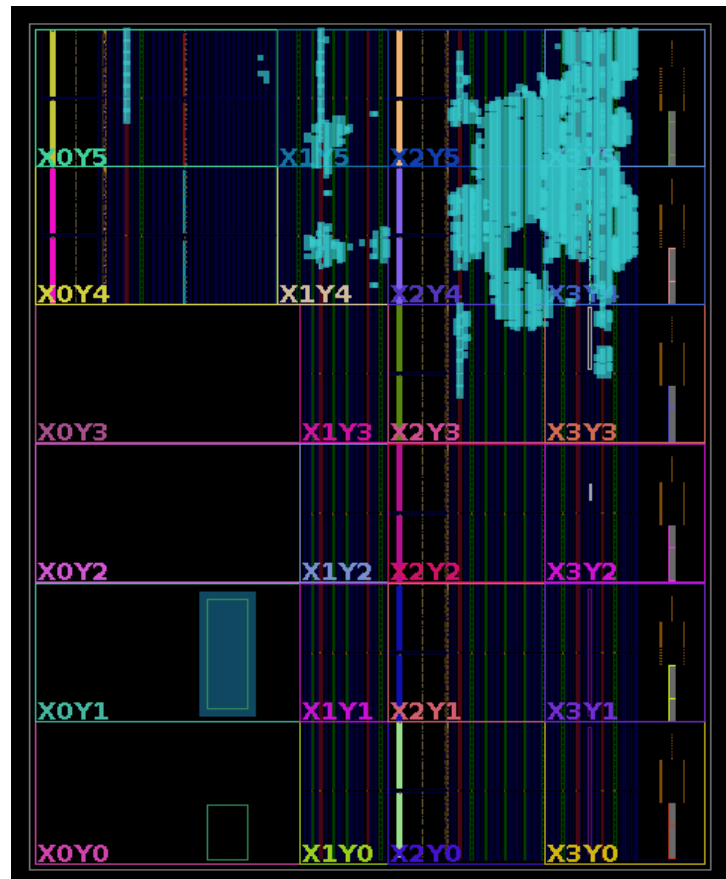- For runtime, the model is tested on 1 batch with size 1024 frames with 27 modulations.

| VGG10 (27 modulations) – 8 bits for weights and activations (w8a8) |
| --- |
| runtime[ms]: 420.3033447265625, |
| throughput[images/s]: 2436.3355962969686, |
| DRAM_in_bandwidth[MB/s]: 4.989615301216191, |
| DRAM_out_bandwidth[MB/s]: 0.0024363355962969684, |
| fclk[mhz]: 249.9975, |
| batch_size: 1024, |
| fold_input[ms]: 0.0896453857421875, |
| pack_input[ms]: 0.0667572021484375, |
| copy_input_data_to_device[ms]: 2.5424957275390625, |
| copy_output_data_from_device[ms]: 0.1270771026611328, |
| unpack_output[ms]: 0.5090236663818359, |
| unfold_output[ms]: 0.064849853515625 |

| Accuracy at 30db on FPGA:<br>10564 / 11070 = 95.42908762420957% | Accuracy at 30db before FINN compiling:<br>95.4291% |
|---|---|
| Accuracy at all SNRS on FPGA:<br>177222 / 287820= 61.57390035438816% | Accuracy at all SNRS before FINN<br>compiling: 61.5746% |

## Report from analyzing the final stitch project on Vivado

| Running implementation on Vivado |
|---|
| Total Flip flops: 231<br>Total Look-up Tables: 1587<br>BRAM: 69.5 |



*Hardware Design Layout*