FPGA Need and Usage

PULSE-A Optics Payload Design
University of Chicago

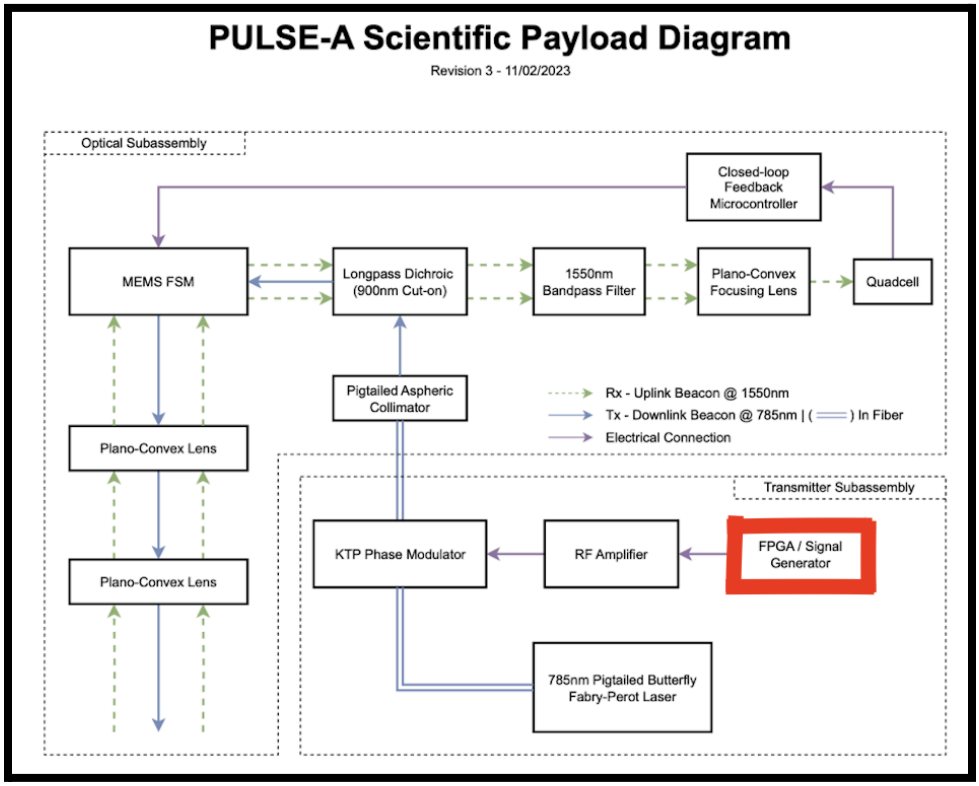

Image 1.A: Pulse-A UChicago Proposal NASA CSLI (modified)

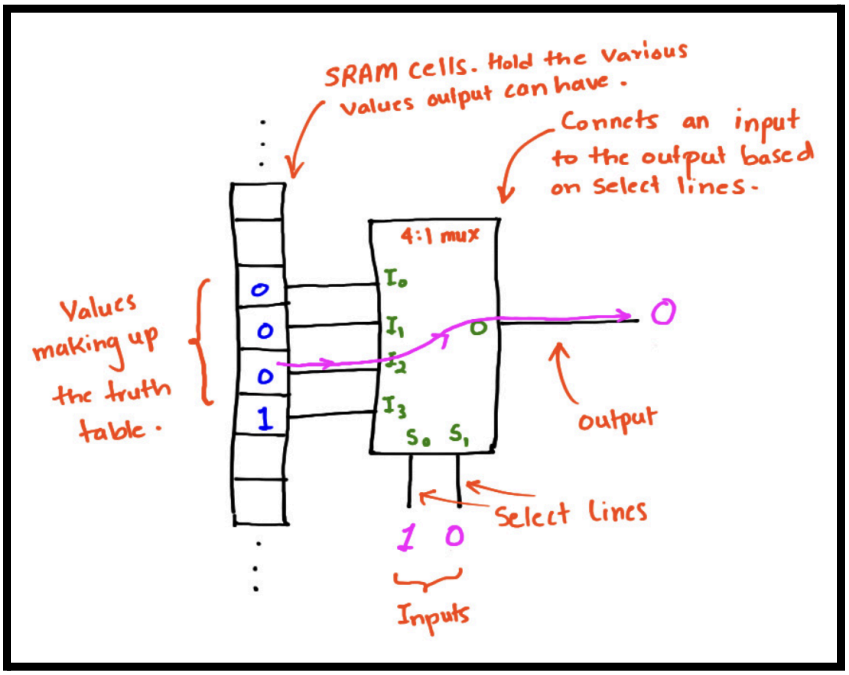

Image 1.B: Look-Up Table Visualization[7]

FPGA Investigation

Do we need the FPGA? If so, how will it be used?

The current modeling for the optical payload demonstrates an FPGA connecting to an RF amplifier which links to the KTP Phase modulator. FPGA stands for "Field Programmable Gate Array." A FPGA is a form of semiconductor technology that utilizes a CLB matrix. CLBs are configurable logic blocks, and the FPGA can be programmed to "configure" them through different orientations. It serves as an alternative to an ASIC (Application Specific Integrated Circuit). ASICs are designed specifically for a certain application. In comparison, FPGAs can be reprogrammed to meet essentially any application post-manufacturing. Modern FPGAs can handle 500 MHz, or more, in terms of RF frequency, so consider what they could do on the PULSE-A CubeSat in terms of optic nanometric measurements[1].

Although FPGAs can be made in-house, the majority are procured COTS (commercial off-the-shelf)[2]. PULSE-A likely recommend purchasing FPGA COTS considering the budgetable price point variance, with options available for as low as several USD (ex. Xilinx spartan 6 for $12.00, Xilinx Spartan 7 for $22.00, low-end Artix model for $28.00, and Artix 7 for $35.00). Models obviously increase in complexity with an increase in price point, with more elite Artix and Spartan models ranging up to several hundred USD[5]. However, a single larger FPGAs chip can cost several thousand USD. The increase in expense is due to an increase in silicon material used in a greater size chip[3]. In addition to quality, size also increases price point. Higher-end models exist up to several hundred thousand dollars, which is obviously not a viable PULSE-A option. However, it is not unreasonable to expect our needs to be met with a lower-end, or medium-end, small-sized FPGA chip. Thus, the problem is not the budget, but rather the unnecessary weight, volume, and most critically power strain on an already limited-size CubeSAT[5].

LUTs (Look-Up Tables) utilize a high number of transistors. Every transistor utilized requires power[3]. The LUT is a value matrix that modifies inputs to outputs[6]. This is depicted in image 1.B[7]. In camera imaging, it is stored in a nonvolatile semiconductor and manipulates files contained in a digital camera. The digital camera uses an LUT for pixel correction[6]. A FPGA utilizes LUTs to manage computing that can be reconfigured (the skill that distinguishes it from an ASIC). LUTs themselves are an alternative to conventional logic gates. Logic gates do one task. LUTs are, essentially, the mechanical magic behind the reconfigurable functioning we see in the FPGA because they enable the device to

reorganize its cells, and thus be as flexible as desired[8]. In short, FPGAs cost power. They cost power due to LUTs. The LUTs cannot be removed or changed because that would inhibit the key circuit flexibility that is the point of the FPGA design. Hence, the power cost is non-negotiable[3].

The power cost is the biggest FPGA drawback to the PULSE-A CubeSAT. Because the LUT transistors require so much power, FPGAs are largely considered an inefficient option for battery powered devices. It almost doesn't matter how efficient the PULSE-A optic payload circuit is because FPGAs require power even to do nothing. For example, the Alchitry Au FPGA uses more than 100 mA doing nothing. Again, this is the power cost for minimal activity. With actual activity, the power cost for an Alchitry Au FPGA will run well over 1000 mA. To reiterate, 1000 mA. In comparison to the 1000 mA power cost of the Alchitry Au FPGA chip, the ATmega32U4 (the chip type used on the Arduino Leonardo) has a power cost of 27 mA. That means the power cost of an FPGA chip doing nothing is more electronically expensive that an Arduino chip running full speed with 5V power. So, with the high power cost, and possible high financial cost depending on the chip selected, this item needs to return the CubeSAT with indispensable benefit[3].

What benefits does an FPGA hold? As mentioned above in regards to their LUT power cost, FPGAs are extremely flexible. It can be programmed and re-programmed to allow for modulation in parallel with the overall design of the optic payload system. Additionally, their data processing is not sequential. Instead, an FPGA uses "sea of gate" mechanics to process all data operations at once. This mechanical technique allows the device better processing performance with less power than some similar sequential chips, such as MCU-ICs, ASIC-ICs, and ASSP ICs, although in other cases despite their data processing power efficiency, they still net out a higher power cost[4].

Mahmoodi et al. describes a FPGA utilization for linearizing radio frequency amplifiers, which is comparable to the optic payload circuit design. Their work describes a non-linear pattern between a radio frequency PA's input/output where the circuitry is tested using a MATLAB-FPGA. It appears that the MATLAB-FPGA is Spartan-6 LXT45 Xilinx FPGA, and a viable PULSE-A option, possibly superior to Alchitry Au and Artix, due to its evidenced use in accordance with an RF amplifier in this paper. Additionally, the MATLAB-FPGA possesses rapid speed and minimal financial burden.

In the work, Mahmoodi et al. uses the MATLAB-FPGA to train and test the optics circuitry system. They examined the non-linear RF outputs in combination with the MATLAB-FPGA training/testing with simulations, comparable to

proposed PULSE-A Zemax simulations, and derived that this technique minimized spectral regrowth for non-constant envelope signaling in adjoining channels. This system minimized spectral regrowth by 20dB. This system minimized ACPR by 26dB. The non-envelope signaling examined in the proposal was QPSK[9].

ACLR, or adjacent channel leakage radio, is a way of examining the maximum spectral regrowth in an adjoining channel. Spectral regrowth is the intermodulation created by a digital transmitter that is part of an analog transmission circuit. In terms of signaling, adjacent channel leakage radio can be calculated using a fraction with bandwidth power in an adjacent channel divided by power in the intended signal channel. The equations look like this:

$$\mathrm{ACLR} = \frac{\int_{f_c + f_0}^{f_c + f_0 + B'} S(f)\mathrm{df}}{\int_{f_c - B/2}^{f_c + B/2} S(f)\mathrm{df}}$$

Image 1.C: ACLR Equation for 2-Tone Analysis[11]

$$\mathrm{ACLR} = P_{\mathrm{IM}} - 10\log_{10}\left(\frac{3N^3}{4N^3 - 3N^2 - 4N + 3(1 - \mathrm{mod}_2(N))}\right)$$

Image 1.D ACLR Equation for N-Tone Analysis[11]

$$P_{\mathrm{IM}} = 2(P_i - \mathrm{OIP3}) - 6\ \mathrm{dB}$$

Image 1.E: ACLR N-Tone Analysis for Average Single Tone Power[11]

Variable	**Translation**
S(f)	Power spectral density
f_C	Carrier frequency
B	Desired signal bandwidth
f_o	Offset frequency on adjacent channel
B’	Bandwidth in adjacent channel measuring spectral regrowth

Using these equations, PULSE-A could potentially calculate the maximum allowable spectral regrowth in adjoining channels. The ACLR equation examines this[11]. The reduction of spectral regrowth could potentially ensure the power drain to be worth it for the usage of a FPGA in optics payload circuitry, but there would need to be a mapped analysis of the spectral regrowth reduction against the exact power cost of the chosen FPGA (or potentially testing multiple FPGAs if lower cost options are selected). Mahmoodi et al. used one of these lower cost FPGA options (i.e. MATLAB FPGA), and used a UDP data management core to link with the FPGA, where the technology is initiated by MATLAB inputting data packets into the FPGA device, and then processed in a flexible decision system that is the hallmark of the device.

The system's increase in effectiveness was examined utilizing simulations in Xilinx Integrated Software Environment in accordance with ISim, which could be a potential supplement to Zemax simulations for PULSE-A. Mahmoodi et. al. examines the resource usage with the following table[9].

Block	Utilization	Available
Slice Reg	2460	54576
Slice LUT	2531	27288
Bonded IOBs	101	296
RAMB16BWERs	8	116
RAMB8BWERs	2	232
DCM/DCM_CLKGENs	1	8
MCB	1	2
PLL_ADV	1	4
DSP48A1	1	58

Image 2.A: Resource Utilization
Ratio of FPGA Model System With RF Amplifier[9]

However, the modeled and demonstrated improvement is not due to the FPGA usage, but rather to predistortion injection technique. Mahmoodi's technique does improve PA use without requiring additional radio frequency circuitry, and such technique could be a useful PULSE-A addition in combination with the FPGA, which would eliminate materials issue that source from the digital predistortion system inhibiting spectral regrowth. Here, the field

programmable gate array gives the baseband injection signal to the circuit's radio frequency transmitter, which is potentially akin to the PULSE-A radio frequency amplifier. The spectral regrowth reduction actually alternated for different signal variants. So, the amount of spectral regrowth would need to be individually examined for the signal consumed by the optics circuit for our project specifically and could not be derived from this paper alone[9].

An alternative paper, Gilabret et al. describes an FPGA circuit with "radio frequency power amplifier dynamic supply with real-time digital adaptive predistortion." This work utilizes envelope tracking in combination with RF power amplifier biasing[10]. Envelope tracking is often used in combination with transmitter power amplifiers. Although basically ancient in terms of technology (developed by Kah in 52'), it has been modernized to work in smaller systems (ex. IOT devices w/ sub 1-watt outputs - good for a PULSE-A system wanting minimal power usage). Envelope tracking modifies power amplifier rail voltage to be simultaneously more linear and more efficient. The conventional power amplifier is fundamentally flawed in that it only becomes energy efficient when using a peak supply voltage. PULSE-A doesn't possess the excess energy necessary to support continuous maximum energy input to ensure efficiency, especially considering that excess voltage means excess heat dissipation from the power amplifier (the PA doesn't need that max energy for functioning, it needs that max energy for efficiency).

Envelope tracking offers a solution to the voltage waste and excess heat that sources from maximizing power amplifier efficiency. See Image 2.B It does so by dynamically manipulating the signal's instantaneous amplitude, which results in continuous efficiency without the aforementioned losses. If an FPGA is going to be used, it should be in accordance with an envelope tracking system on the PA, rather than the conventional RF PA currently listed. Ideally, envelope tracking would shift the DC supply rail-rail voltage in correspondence with PA efficiency patterns.

However, envelope tracking is not without major hypothetical detriment to the PULSE-A optical system. Broadly speaking, device circuits with shifting loops present multitudes more technical issues because the ET tracking would purposefully create variation in the DC rail voltage. Constantly moderating dynamic loops would create a more efficient radio frequency power amplifier, especially in accordance with a small-sized low-cost field gate array, but it introduces supply variations that could ~~fuck up~~ inhibit the success of other more delicate aspects of the circuit (i.e. KTP phase modulator or pigtailed aspheric collimator). To combat the dynamic power supply variation damage to the

detailed circuitry, it would be potentially worthwhile to examine the PSRR (power supply rejection ratio) of the circuitry components, which would indicate their functionality in response to dynamic power change[12].

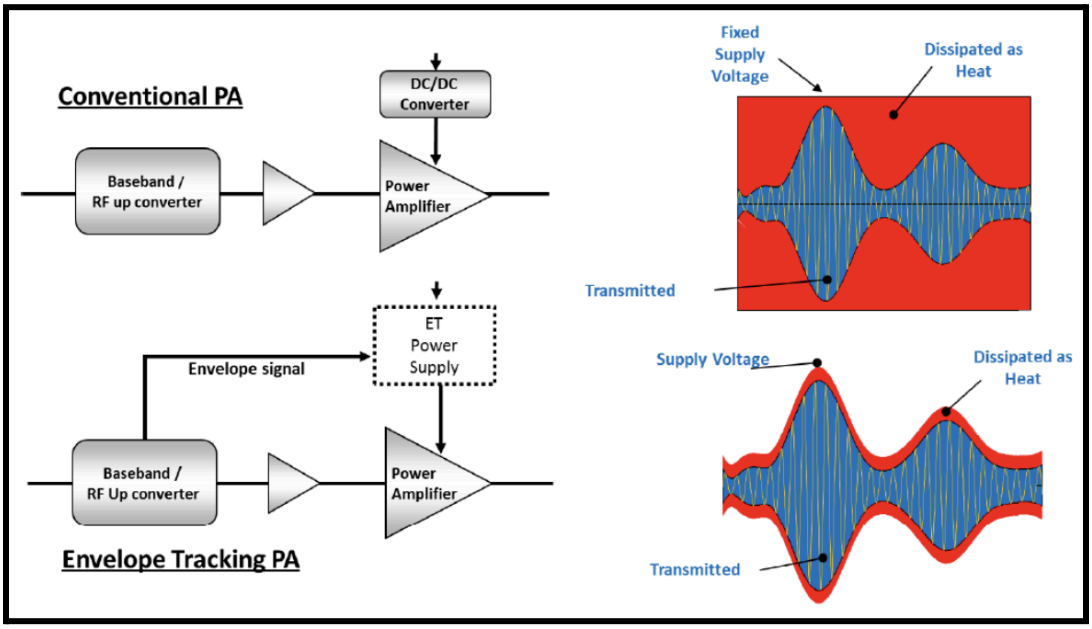

Image 2.B: Conventional versus Envelope Tracking Power Amps.[12]

Rebiai et al. utilized an improved variant of envelope tracking in coordination with field programmable gate array usage, although their abstract details the technique on rotating machinery bearing faults rather than optics circuitry. They used a Teager energy operator (TEO) to remove the envelope from the signal, and then applied a Fourier transform to create the spectrum the envelope uses in correspondence with the signal. Then , they apply TEO again. Based on this paper, the TEO-Fourier-TEO technique (TFTT) detects errors much earlier than other strategies for envelope correction. Their characteristic frequency ratio fault analysis found that FCFR values are roughly 250% percent higher without TFTT analysis. In accordance with TFTT, they use a field programmable gate array to mitigate the risk of envelope tracking. Rebiai et al. need to mitigate these risks for their industrial applications in machinery rotation, but the same mitigation applied with optics. Ideally, TFTT could be applied in combination with envelope-tracking and an FPGA for an energy efficient, flexibly programmable circuit system with minimal risk[13].

There are a multitude of RF FPGAs available. Although Artix and Xilinx both provide viable options, I am going to attach an example of an RF PGA with the ideal key elements necessary for the PULSE-A circuitry to the next page[14].

RF FPGA for 0.4 to 18 GHz DoD Multi-function Systems

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Abstract: *Northrop Grumman Electronic Systems (NGES) is developing a dynamically reconfigurable, wide band programmable RF FPGA transceiver which, if successful, will provide reduced life cycle cost, reduced re-design cost, and service for multiple DoD platforms, while maintaining near-optimal performance for each application. This RF FPGA transceiver has the flexibility to implement communications, radar, EW, EA, and other functions covering the 0.4 to 18 GHz band.*

Keywords: RF FPGA; Phase Change Switch; Low Loss switch; GaN; SiGe; adaptable; reconfigurable.

Introduction: State of the art RF ICs achieve high performance via custom circuit elements with dedicated signal paths for application-specific functions, but long design lead times and non-recurring fabrication costs increase cost and schedule for new applications and limit reuse. The key to developing an RF FPGA (radio frequency field programmable gate array) is to provide RF switching components with very low insertion loss and high isolation, which can be integrated with high performance RF circuits in SiGe and GaN technologies, and integrating these circuits in a reconfigurable topology to allow an RF FGPA to perform a wide variety of functions.

Summary of Approach: Key elements of the RF FPGA approach are:

- Extremely low loss, high isolation RF switches using phase change materials (PCM). Multiport RF switch designs that optimize thermal design to improve PCM performance, and integrate arrays of these switches on thermally and electrically optimized substrates.
- Multiport switch designs with low simulated RF losses of 0.1 - 0.2 dB up to 20 GHz and have 35dB - 60dB isolation between ports, based on measured and extrapolated PCM data. They consume no prime power except for 100 nsec heater pulses during reconfiguration.
- An architecture that connects these switches in a fully interconnected matrix to allow total flexibility in interconnecting and switching between RF elements and to inputs / outputs.
- Dynamically RF tuned banks of wideband (~3:1 BW (band width)), high performance LNAs (low noise amplifiers), mixers, vector modulators, driver amplifiers, and power amplifiers using programmable circuit bias and circuit mission reconfiguration techniques.
- Development of a family of RF FGPAs that can be configured in a variety of ways; e.g., as a standalone RF transceiver, as T/R (transmit receive) elements in an AESA (active electronic scanned array), or as an IF (intermediate frequency) or baseband receiver. Packaging in 12mm x 12mm QFNs (quad-flat no-leads packages) with matched RF I/O for low package insertion loss is used to allow multiple RF FPGAs to be integrated in flexible configurations.
- Demonstration of the RF FPGA technology against multiple DoD system applications with transition potential to a wide range of DoD systems.

Detailed Technical Approach

Robust Low Loss Switch Technologies: To produce an efficient RF FPGA, a compact low loss RF switch is the essential technology needed. Our unique solution for the switch leverages previous completed GeTe/GeSbTe phase change material RF switches. These phase change materials have demonstrated a dynamic range for R_{off} to R_{on} ratio of 10^7. We have designed 4 to 12 port multiport RF switches (8 port design shown in Figure 1) with RF losses in the 0.2dB range, which need a R_{off}/R_{on} range of only 2×10^5. This margin in dynamic range requirement improves switch producibility and cycle lifetimes.

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