SYNTHESIS

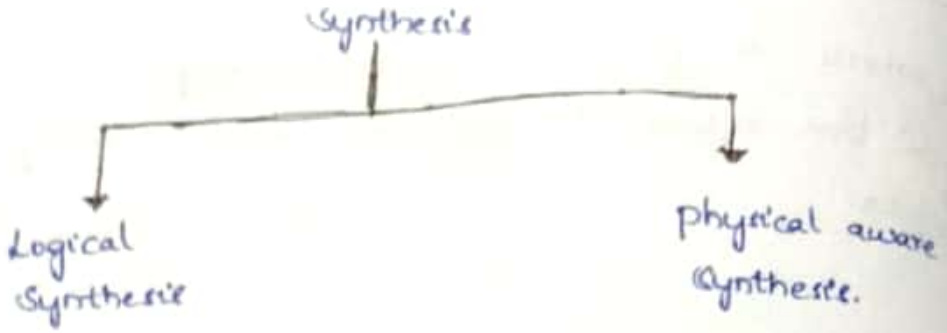
What is synthesis?

Synthesis is process of converting RTL code to gate level netlist to optimize area, timing and power.

Goals of synthesis:-

* To get gate level netliet
* Insert clock gating
* Logic optimization
* Insert DFT logic
* Logic equivalence of RTL and gate leve netliet should be maintained.

In synthesis, there are two types.



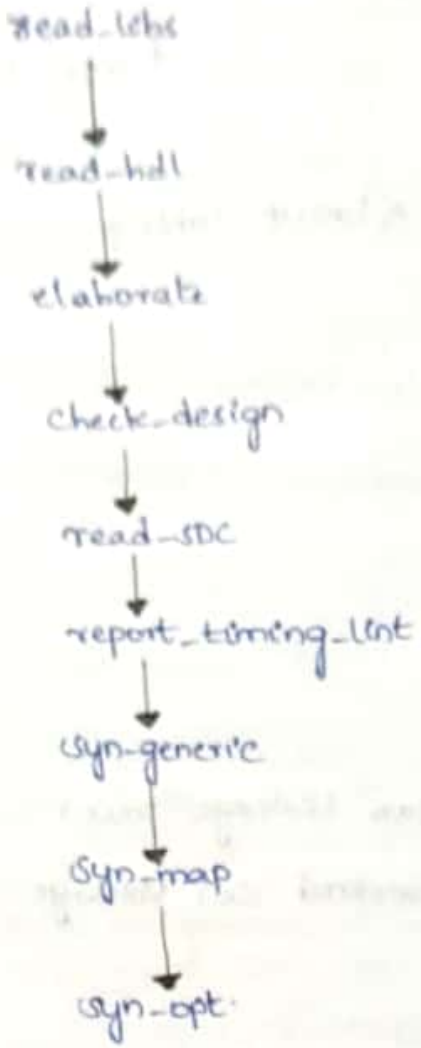
Logical synthesis

When we work on low frequency we go for logical synthesis.

Physical_aware synthesis.

When we work on higher frequency we go to physical aware synthesis.

Logical synthesis flows—



Inputs for logical synthesis flows—

libs

rtl

SDC

•lib:—

- cell-functionality
- Timing info
  - Cell rise, cell-fall, cell-delay
  - rise transition, fall transition
- Delay info & lookup table
- PVT
- DRV
- power & max leakage power, default voltage, standard cell voltage,

PVT:—

slow	fast	typical
P=1 V=0.7 temp=125°c	P=1 V=1.2 temp=-40°c	P=1 V=0.9 temp=25°c

Elaborate:—

* It will search all sub-blocks and will convert RTL files into single design (Top).

* Convert code and arithmatic operators to GTech (or) DW (design ware) (or) Technology independent cell.

GTech → Combinational, Sequential.

DW → FIFO, Counters.

Check design:—

To validate our design we do check design.

Issues in check design:—

1. Unresolved references
   - missing submodules
   - missing i/p ports
   - missing libs.
2. Empty modules
3. floating inputs
4. Combinational loops
5. multidriven nets
6. Constant nets
7. Undriven i/p ports
8. unloaded o/p ports.

Read SDC:—

SDC → Synopsys Design Constraint.

SDC's are used to specify the intent of the design

Clock definition:—

Create_clock

Create_generated clock

Create clock —ve virtual clock

i/p & o/p delay:—

set_input_delay

set_output_delay

DRV:—

set_max_capacitance

set_min_capacitance

set_max_transition

set_max_fanout

path exceptions:—

set multicycle path

set_falsepath

set max delay

set min delay

set case analysis

set clock transition

set clock uncertainty

set clock latency

set_drive

set_load.

Report_timing_list:—

In order to validate SDC, we do report_timing_list.

seq-data pins driven clk signal

seq- clock pins without clk waveforms

seq clock pins with multiple clock waveforms

Generated clock with master clock waveforms

Generated clock without master clock.

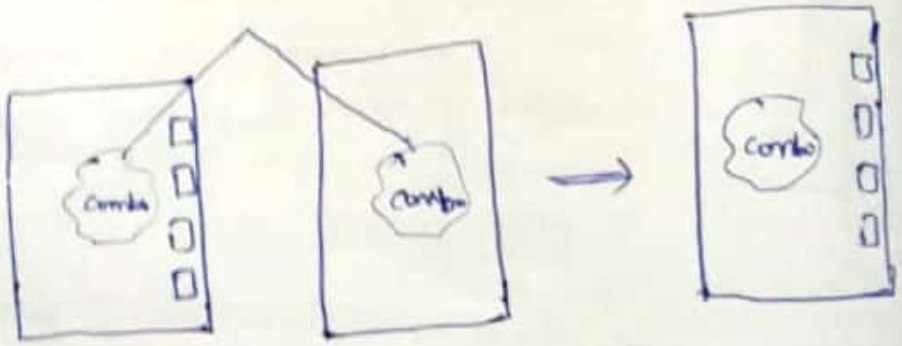
Syn_generics:—

3

1. Auto_ungrouping
2. mux_opt
3. Boundary opt
4. Constant propagation
5. resource sharing
6. Speculation.
7. CSA opt
8. Seq merging.

-Auto_ungrouping:—

Removal of hierarchies is ntg but autoungro



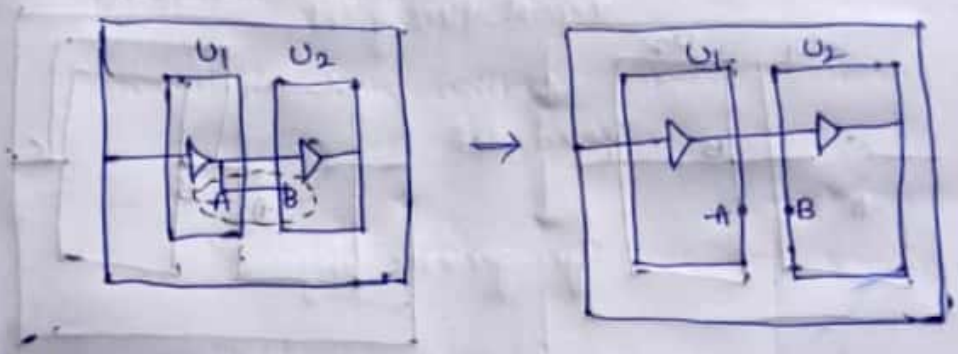
Boundary optimization:—

1. Constant propogation across hierarchies.
2. Removing undriven (or) unloaded logic connected.
3. Collapsing equal and opposite pins.
4. hierarchial pin inverter
5. Rewiring of equivalent signals across hierarchy

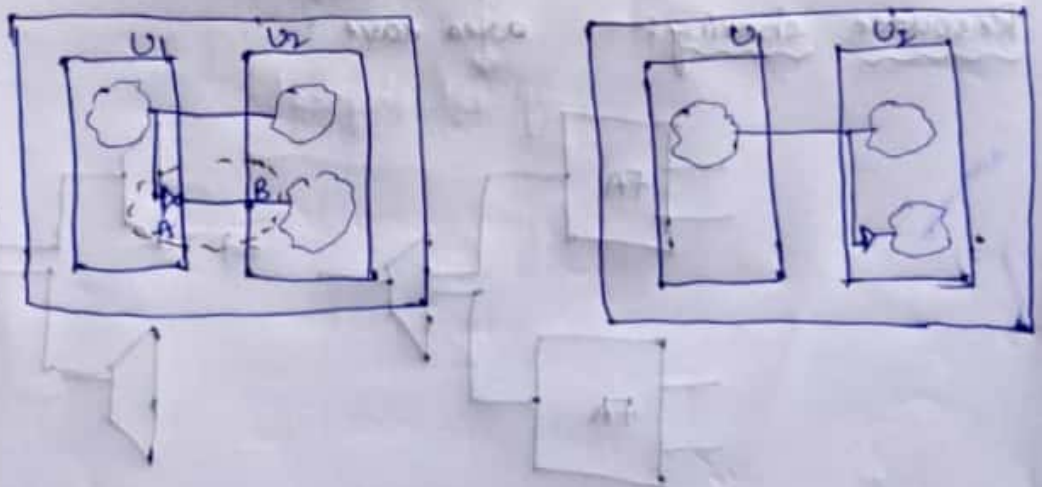
Constant propogation:—

This includes constant propogation through both input ports and o/p ports.

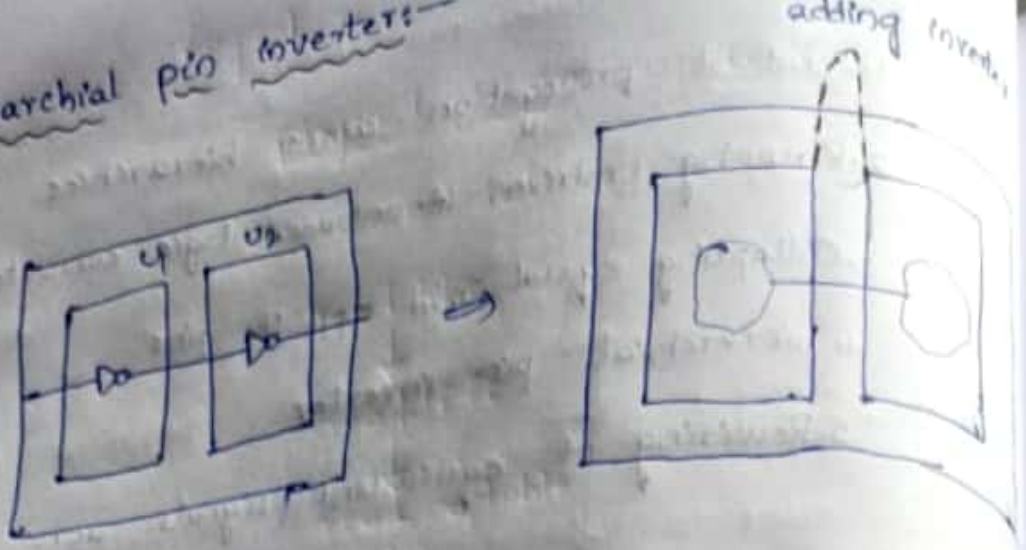
Removing undriven (or) unloaded logic connected:—



Collapsing equal and opp. pins:—

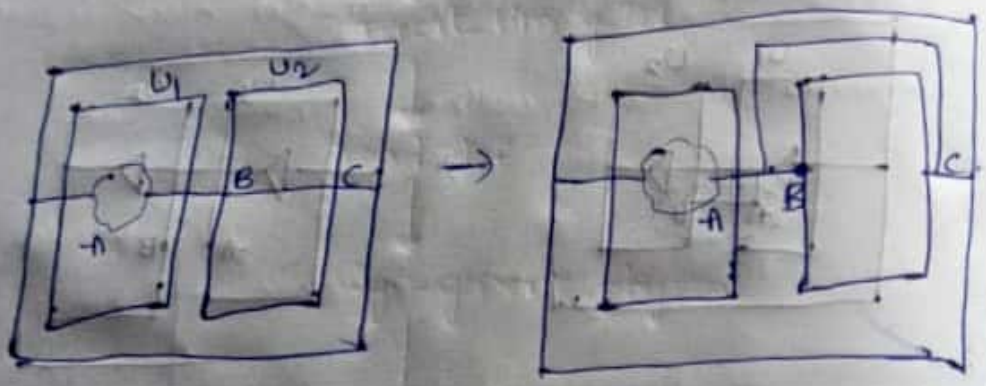


Hierarchial pin inverter:

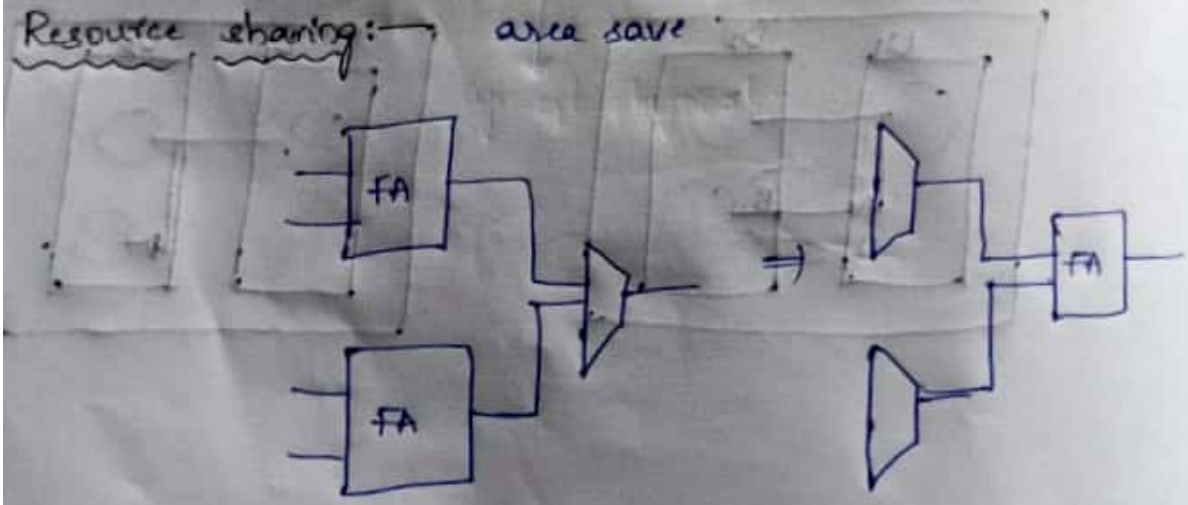


RTL compiler might invert the polarity of a hierarchial boundary pin to improve QOR improvement

Rewiring of equivalent signals across hierarchy.



Resource sharing: → area save



Syn_map:—

1. structuring
2. restructing
3. redundancy removal
4. mapping.

structuring:—

ab+ac

a(b+c)

redundancy removal:—

Syn_opt:—

- delay opt
- area opt
- DRV's fixing.

Syn_map:—

1. structuring
2. restructing
3. redundancy removal
4. mapping.

structuring:—

ab+ac

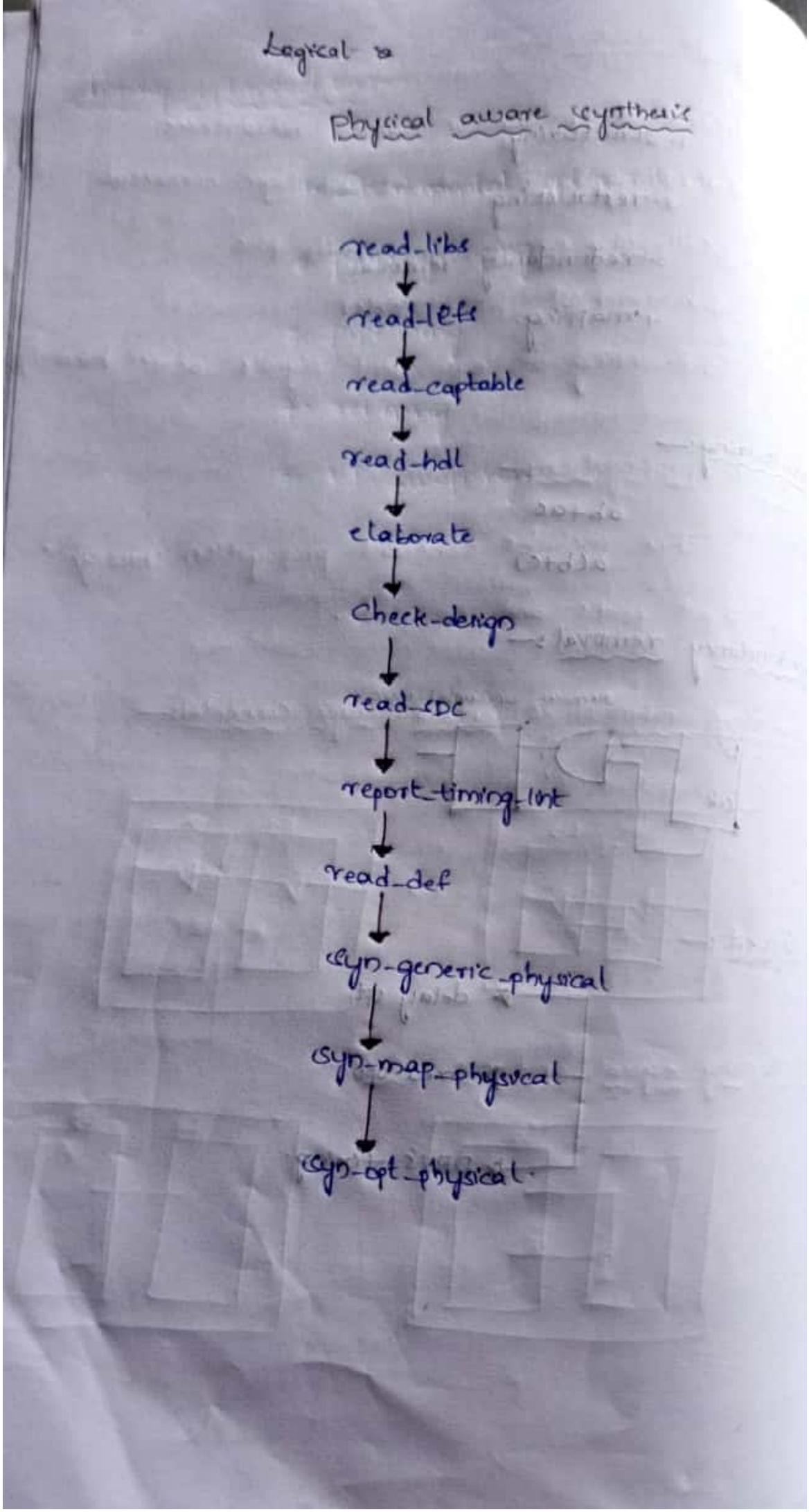
a(b+c)

redundancy removal:—

Syn_opt:—

Logical :

Physical aware synthesis



LEF (Layer exchange format)	DEF (Design exchange format)	Captable
R	Die area	R
C	Core area	C
Via	rows	CC
site	tracks	CF
Width	grids	Ca
pitch	macros	CT
height	pins	width
area	ports	height
	Components	pitch
	blockage	spacing.
	special nets.	

Timing optimization:-

1. Incremental optimization
2. path grouping
3. pipelining
4. retiming
5. VT swapping.