數位系統設計作業-3
DW8051 – I2C Master

溫進坤

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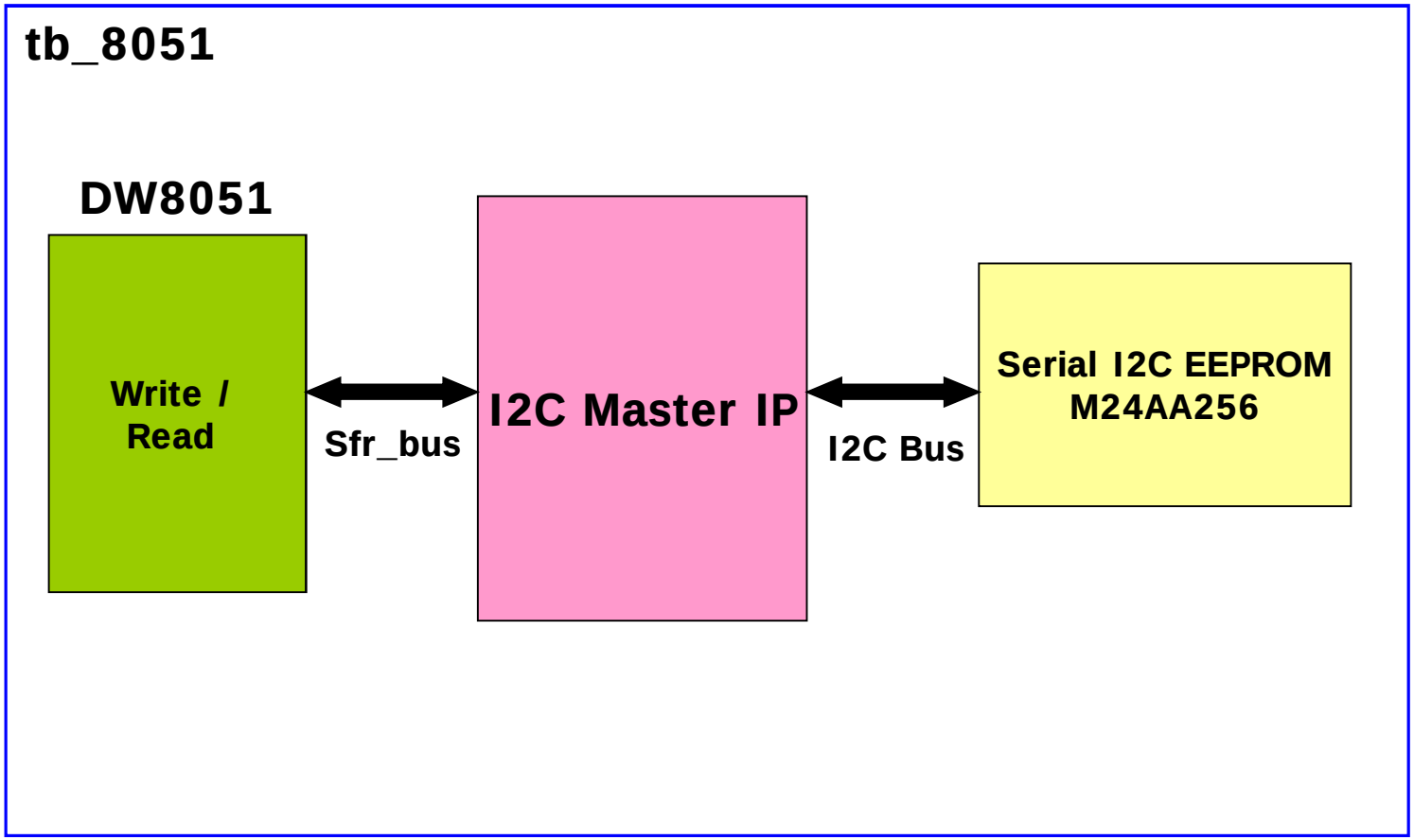
作業題目

1. 設計一個DW8051的I2C MASTER IP 。
2. 在DW8051程式中透過I2C MASTER Register，將EEPROM的位址0寫入0x12，位址1寫入0x34。
3. 使用M24AA256.v當I2C Slave EEPROM model。
4. Modelsim的文字輸出結果，不能有Error Message 。
5. 使用同步式設計，只能使用clk_50M或reset當clock，不能使用其他輸入信號當clock使用。

Block Diagram



I2C Master Register Map

SFR Addr	Description	Note
0x9A	I2C Control Byte	Bit0:Write Bit1:Read Bit4:Start Bit5:Stop
0x9B	I2C Status Byte	Bit0:Complete Bit1:Error
0x9C	I2C Write/Read Data Byte	I2C write or read data

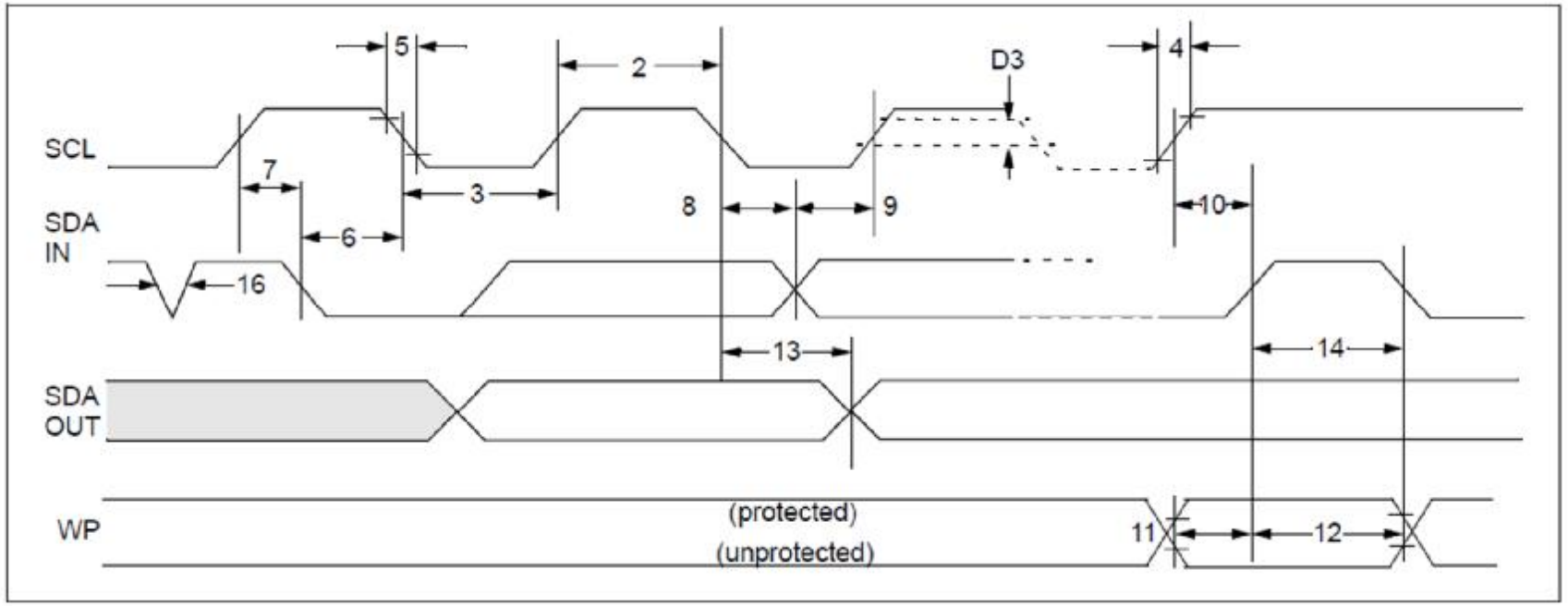
AC CHARACTERISTICS

AC CHARACTERISTICS			Electrical Characteristics: Industrial (I): Vcc = +1.7V to 5.5V TA = -40°C to +85°C Automotive (E): Vcc = +1.7V to 5.5V TA = -40°C to +125°C			
Param. No.	Sym.	Characteristic	Min.	Max.	Units	Conditions
1	FCLK	Clock frequency	— — — —	100 400 400 1000	kHz	1.7V ≤ Vcc < 2.5V 2.5V ≤ Vcc ≤ 5.5V 1.7V ≤ Vcc < 2.5V 24FC256 2.5V ≤ Vcc ≤ 5.5V 24FC256
2	THIGH	Clock high time	4000 600 600 500	— — — —	ns	1.7V ≤ Vcc < 2.5V 2.5V ≤ Vcc ≤ 5.5V 1.7V ≤ Vcc < 2.5V 24FC256 2.5V ≤ Vcc ≤ 5.5V 24FC256
3	TLOW	Clock low time	4700 1300 1300 500	— — — —	ns	1.7V ≤ Vcc < 2.5V 2.5V ≤ Vcc ≤ 5.5V 1.7V ≤ Vcc < 2.5V 24FC256 2.5V ≤ Vcc ≤ 5.5V 24FC256
4	TR	SDA and SCL rise time (Note 1)	— — —	1000 300 300	ns	1.7V ≤ Vcc < 2.5V 2.5V ≤ Vcc ≤ 5.5V 1.7V ≤ Vcc ≤ 5.5V 24FC256
5	TF	SDA and SCL fall time (Note 1)	— —	300 100	ns	All except, 24FC256 1.7V ≤ Vcc ≤ 5.5V 24FC256
6	THD:STA	Start condition hold time	4000 600 600 250	— — — —	ns	1.7V ≤ Vcc < 2.5V 2.5V ≤ Vcc ≤ 5.5V 1.7V ≤ Vcc < 2.5V 24FC256 2.5V ≤ Vcc ≤ 5.5V 24FC256
7	TSU:STA	Start condition setup time	4700 600 600 250	— — — —	ns	1.7V ≤ Vcc < 2.5V 2.5V ≤ Vcc ≤ 5.5V 1.7V ≤ Vcc < 2.5V 24FC256 2.5V ≤ Vcc ≤ 5.5V 24FC256
8	THD:DAT	Data input hold time	0	—	ns	(Note 2)
9	TSU:DAT	Data input setup time	250 100 100	— — —	ns	1.7V ≤ Vcc < 2.5V 2.5V ≤ Vcc ≤ 5.5V 1.7V ≤ Vcc ≤ 5.5V 24FC256
10	TSU:STO	Stop condition setup time	4000 600 600 250	— — — —	ns	1.7V ≤ Vcc < 2.5V 2.5V ≤ Vcc ≤ 5.5V 1.7V ≤ Vcc < 2.5V 24FC256 2.5V ≤ Vcc ≤ 5.5V 24FC256
11	TSU:WP	WP setup time	4000 600 600	— — —	ns	1.7V ≤ Vcc < 2.5V 2.5V ≤ Vcc ≤ 5.5V 1.7V ≤ Vcc ≤ 5.5V 24FC256
12	THD:WP	WP hold time	4700 1300 1300	— — —	ns	1.7V ≤ Vcc < 2.5V 2.5V ≤ Vcc ≤ 5.5V 1.7V ≤ Vcc ≤ 5.5V 24FC256

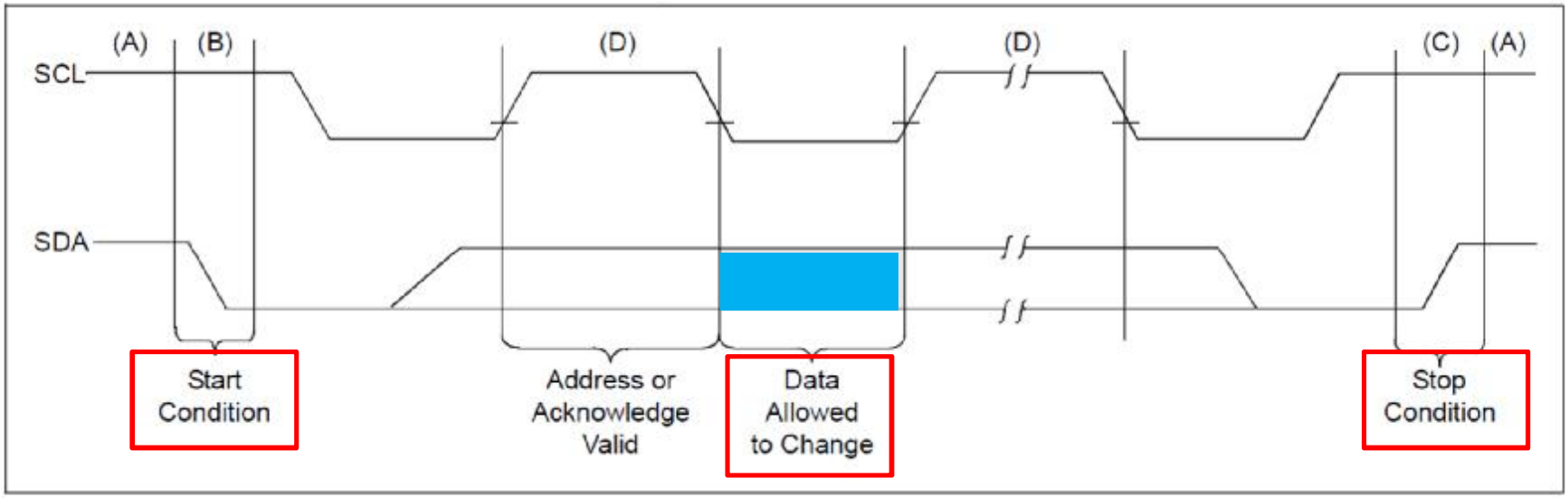
AC CHARACTERISTICS

AC CHARACTERISTICS (Continued)			Electrical Characteristics: Industrial (I): VCC = +1.7V to 5.5V TA = -40°C to +85°C Automotive (E): VCC = +1.7V to 5.5V TA = -40°C to +125°C			
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Max.**	**Units**	**Conditions**
13	TAA	Output valid from clock (Note 2)	— — — —	3500 900 900 400	ns	1.7 V ≤ VCC < 2.5V 2.5 V ≤ VCC ≤ 5.5V 1.7V ≤ VCC < 2.5V 24FC256 2.5 V ≤ VCC ≤ 5.5V 24FC256
14	TBUF	Bus free time: Time the bus must be free before a new transmission can start	4700 1300 1300 500	— — — —	ns	1.7V ≤ VCC < 2.5V 2.5V ≤ VCC ≤ 5.5V 1.7V ≤ VCC < 2.5V 24FC256 2.5V ≤ VCC ≤ 5.5V 24FC256
15	TOF	Output fall time from VIH minimum to VIL maximum CB ≤ 100 pF	10 + 0.1CB	250 250	ns	All except, 24FC256 (Note 1)
16	TSP	Input filter spike suppression (SDA and SCL pins)	—	50	ns	All except, 24FC256 (Notes 1 and 3)
17	TWC	Write cycle time (byte or page)	—	5	ms	—
18	—	Endurance	1,000,000	—	cycles	Page mode, 25°C, 5.5V (Note 4)

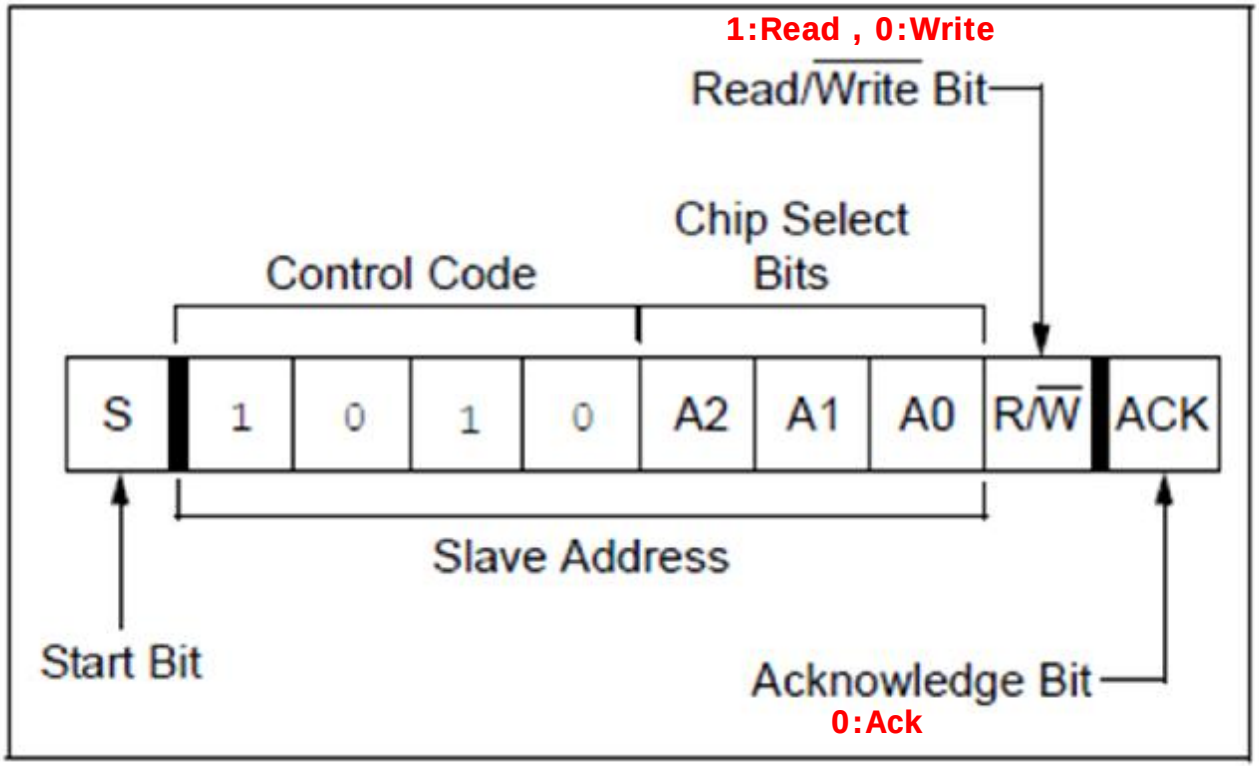
I2C BUS TIMING DATA



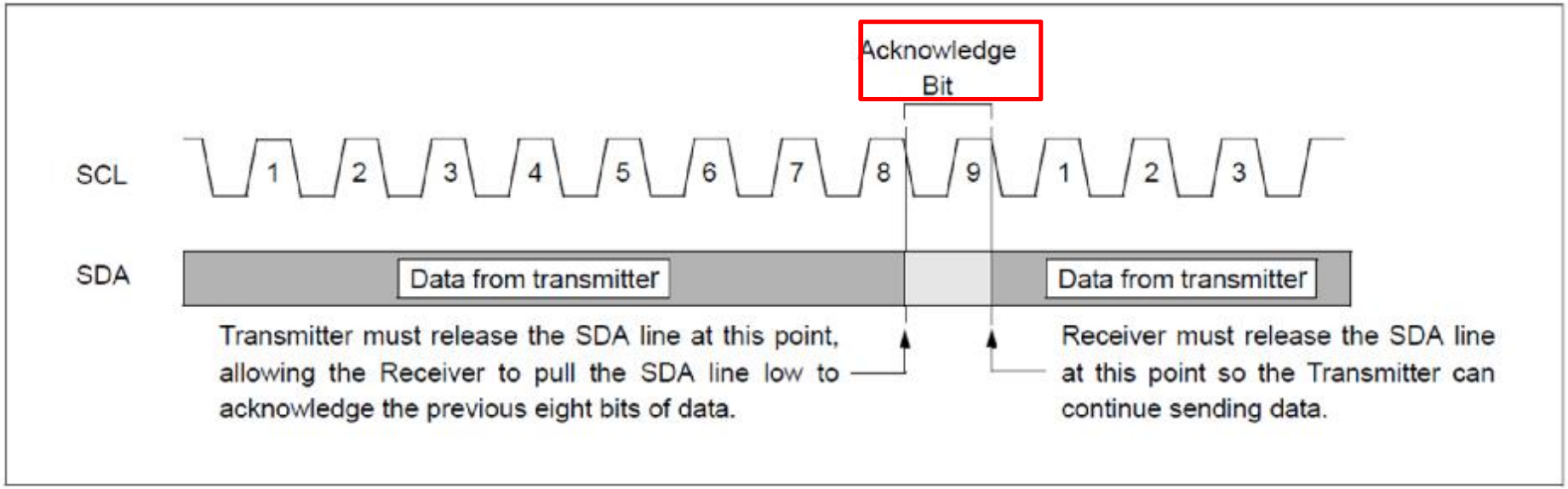
I2C DATA TRANSFER SEQUENCE ON THE SERIAL BUS



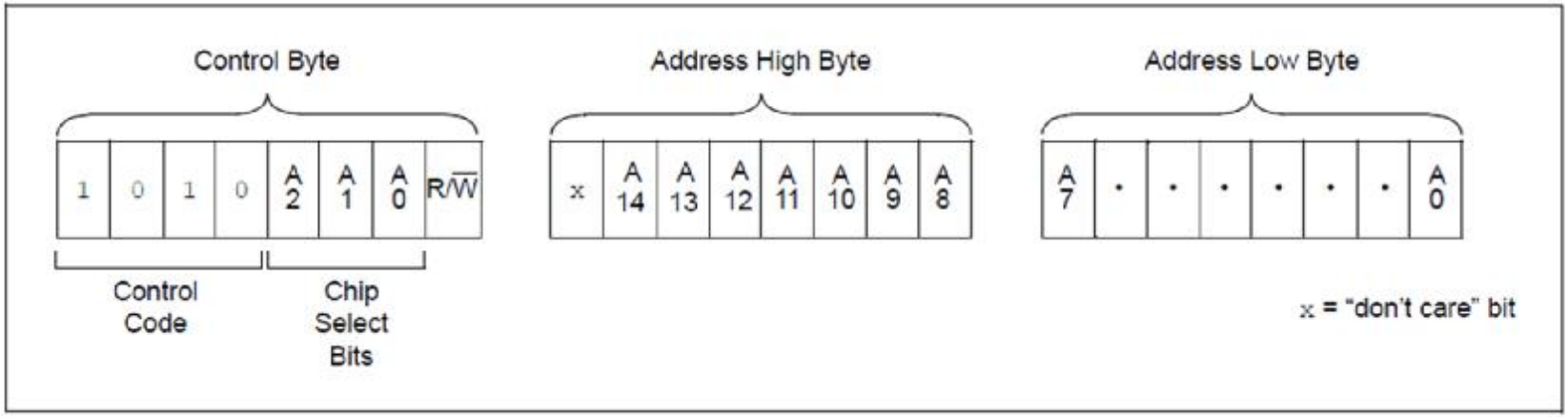
I2C Control Byte Format



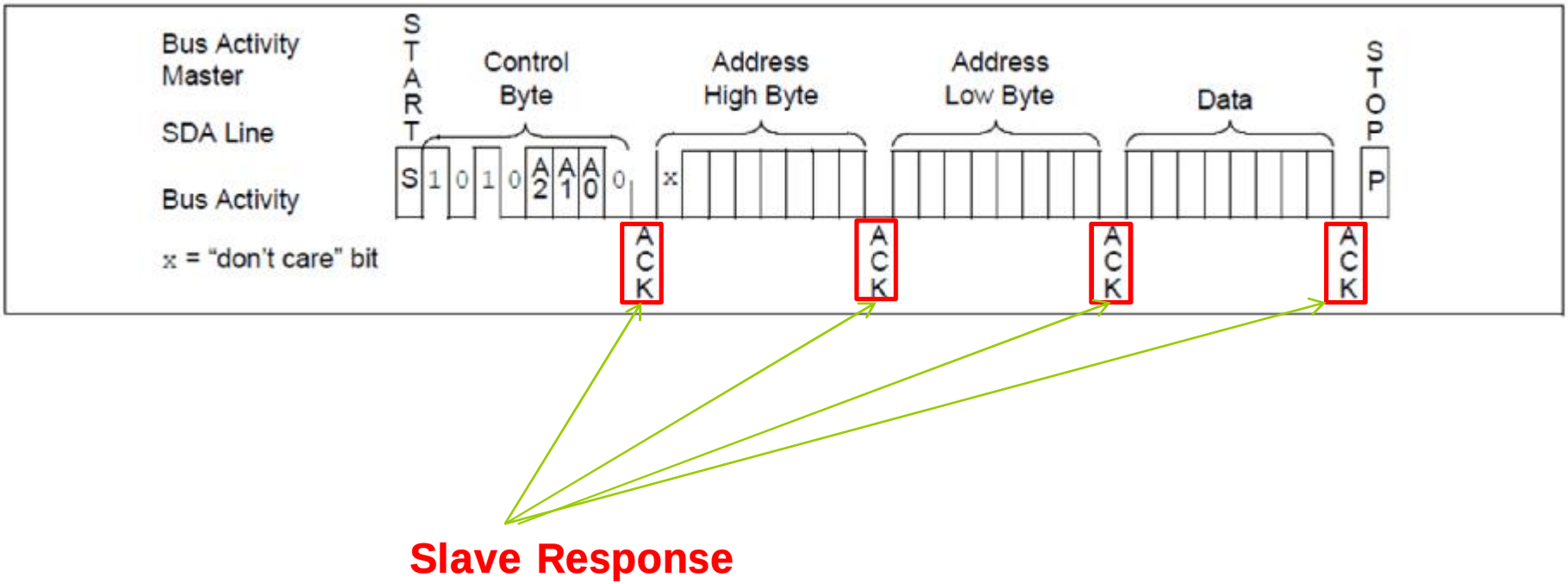
24AA256 ACKNOWLEDGE TIMING



24AA256 ADDRESS SEQUENCE BIT ASSIGNMENTS

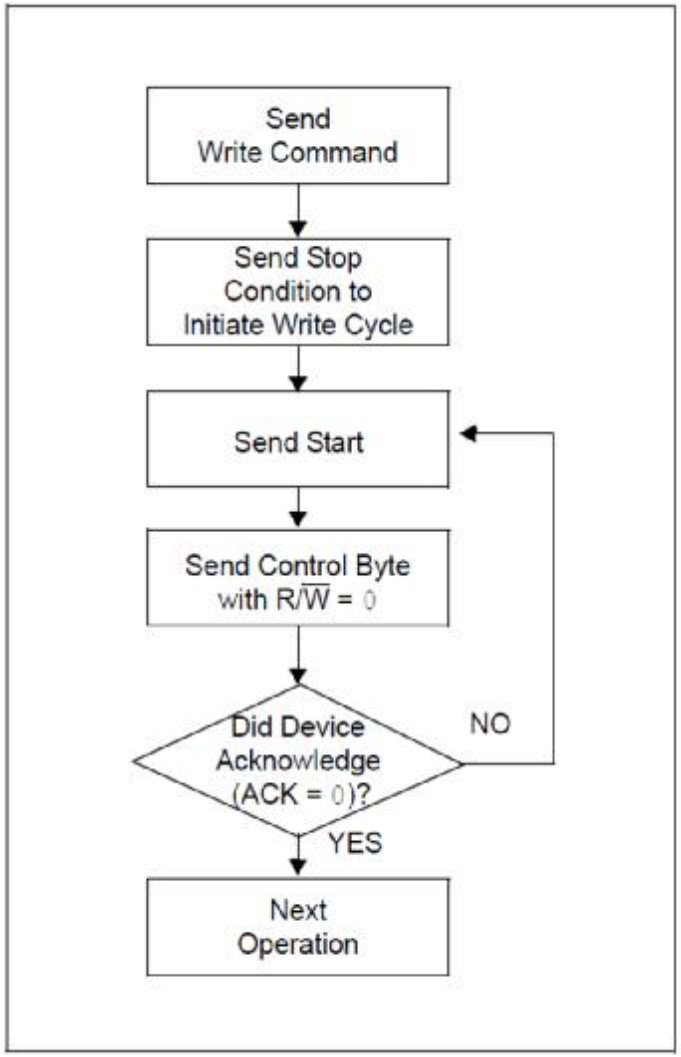


24AA256 BYTE WRITE



Slave Response

ACKNOWLEDGE POLLING FLOW



文字輸出結果

Transcript

```
sim:/hw4_tb/write_control \
sim:/hw4_tb/write_addr \
sim:/hw4_tb/write_value \
sim:/hw4_tb/i2c_sda \
sim:/hw4_tb/i2c_scl
VSIM 6> run -all
# time=  0 memory_000=0xxx memory_001=0xxx
# time=1002030 control=0xa0 addr=0x0000 data=0x12
# time=6382471 memory_000=0x12 memory_001=0xxx
# time=7004030 control=0xa0 addr=0x0001 data=0x34
# time=12384471 memory_000=0x12 memory_001=0x34
# ** Note: $stop    : D:/work/NTUST/Verilog/hw4/hw4_tb.v(65)
#    Time: 13004030 ns  Iteration: 0  Instance: /hw4_tb
# Break in Module hw4_tb at D:/work/NTUST/Verilog/hw4/hw4_tb.v line 65
```

計分方式

1. 將全部Verilog程式及modelsim模擬結果、波形截圖壓縮成ZIP檔，上傳至Moodle[繳交作業]，並在檔名依序寫上學號、作業號。
2. 上傳檔案名稱：學號_HW3.zip
3. 計分標準依完成順序及程式內容給分，若發現程式或輸出畫面結果有複製狀況，該員此次作業分數為0分。