

# 數位系統設計作業-2

## SPI Master



溫進坤

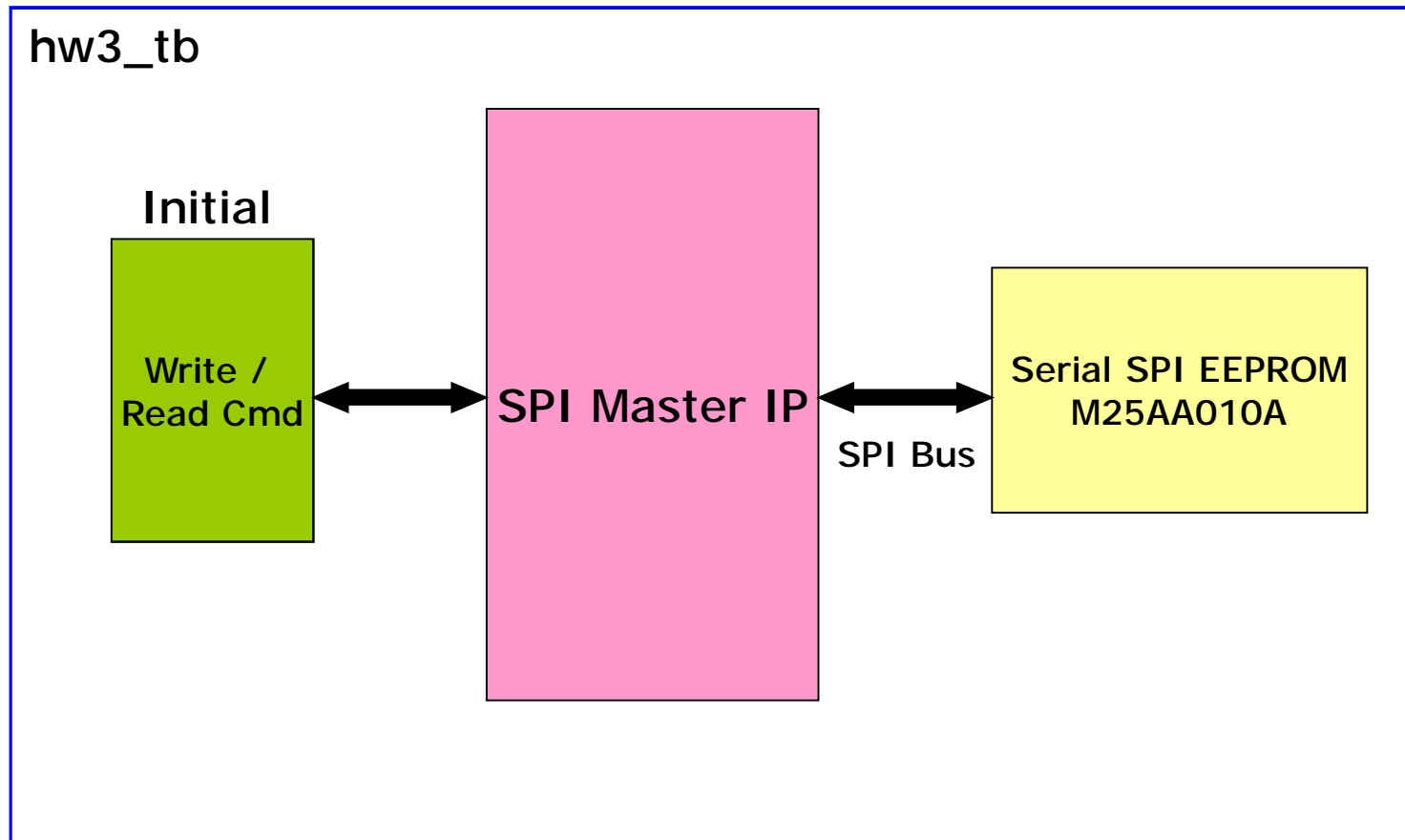
[james\\_wen@hotmail.com](mailto:james_wen@hotmail.com)

# 作業題目

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1. 設計一個SPI MASTER IP。
2. 在Testbench中透過SPI MASTER，在EEPROM的位址0寫入0x78，位址1寫入0x9A，位址2寫入0xBC。
3. 使用M25AA010A.v當SPI Slave EEPROM model。
4. 使用同步式設計，只能使用clk\_50M或reset當clock，不能使用其他輸入信號當clock使用。

# Block Diagram



# Instruction Set for the AT25AA010A

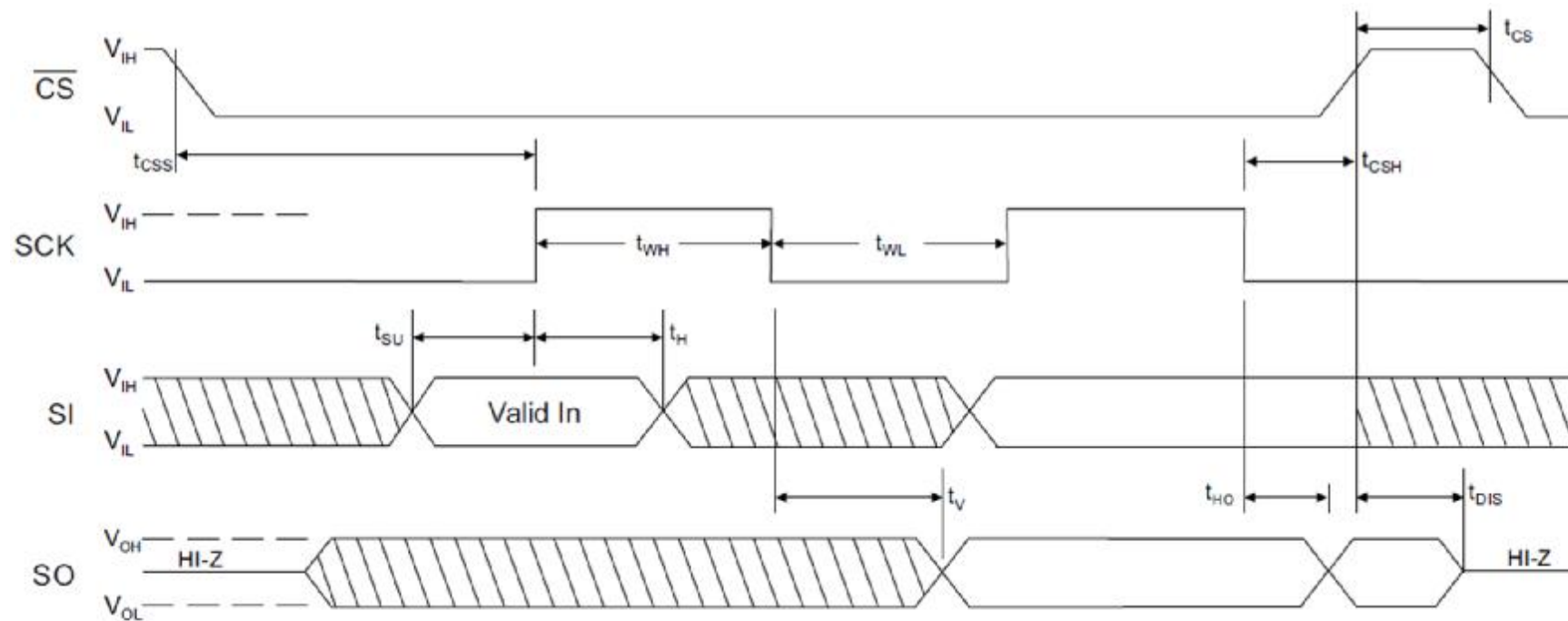
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Instruction Name	Instruction Format	Operation
WREN	0000 X110	Set Write Enable Latch
WRDI	0000 X100	Reset Write Enable Latch
RDSR	0000 X101	Read Status Register
WRSR	0000 X001	Write Status Register
READ	0000 A011	Read Data from Memory Array
WRITE	0000 A010	Write Data to Memory Array

Note: 1. "A" represents MSB address bit A8 for the AT25040B.

# AT25AA010A SPI Protocol

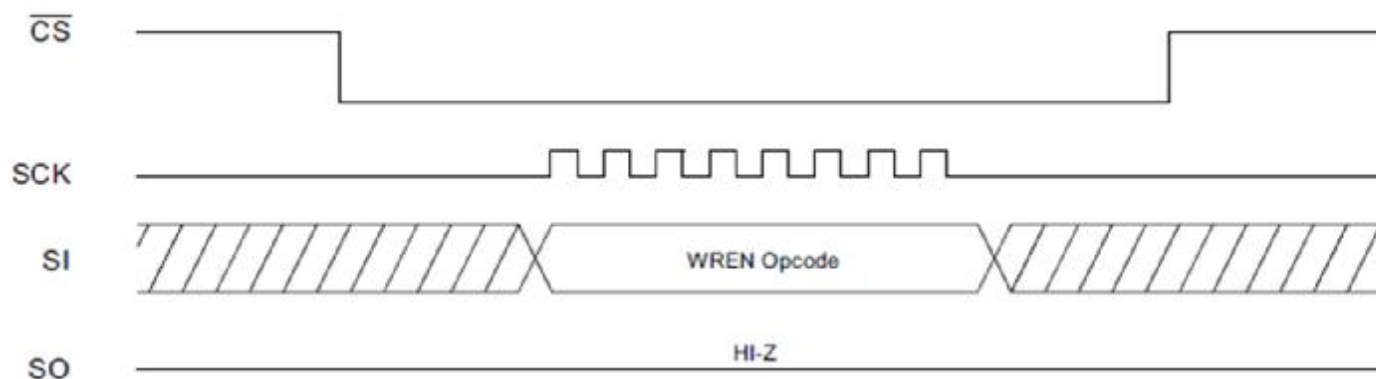
## Synchronous Data Timing (for Mode 0)



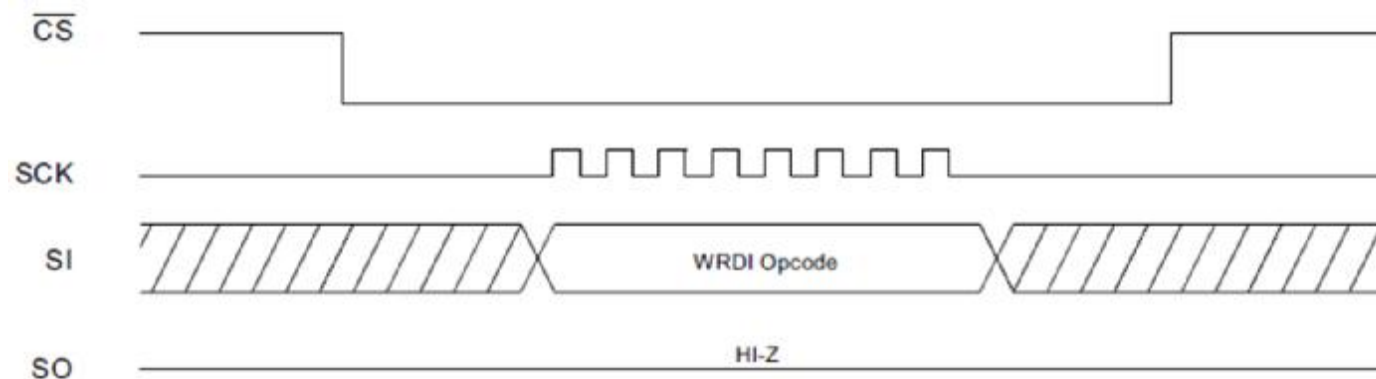
$t_{WH} , t_{WL} , t_{SU} , t_H > 40\text{ns}$

# AT25AA010A SPI Protocol

## •WREN Timing

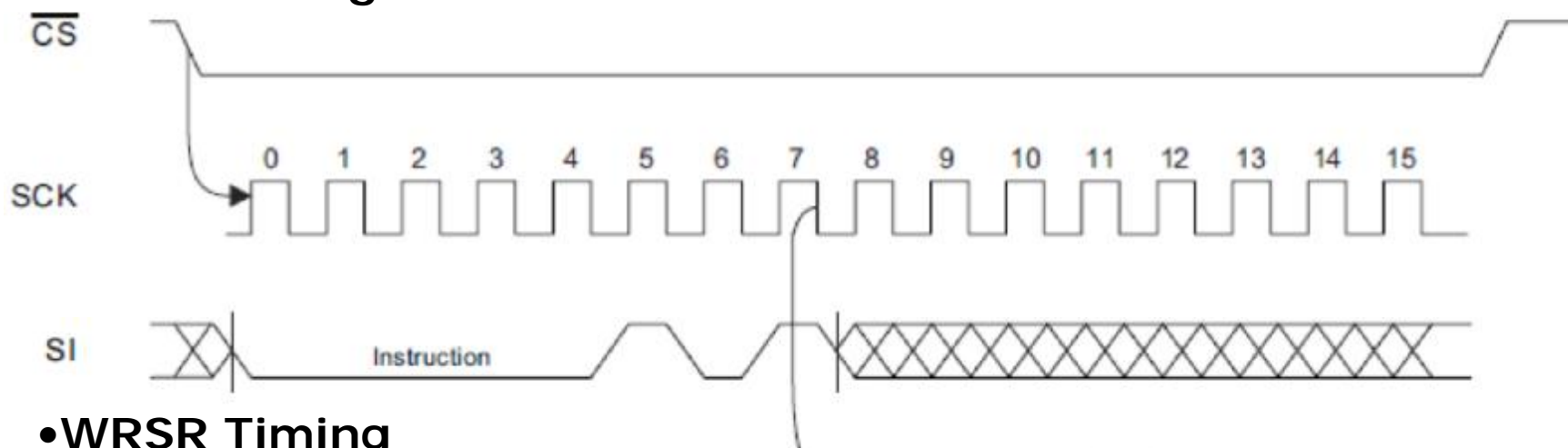


## •WRDI Timing

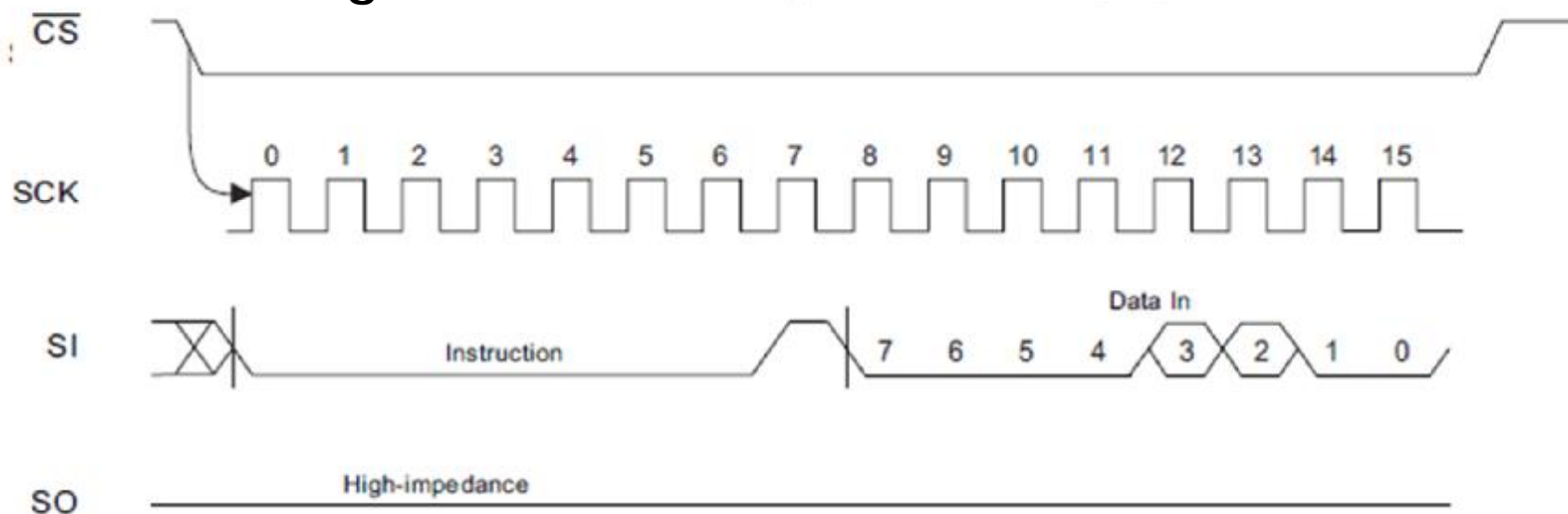


# AT25AA010A SPI Protocol

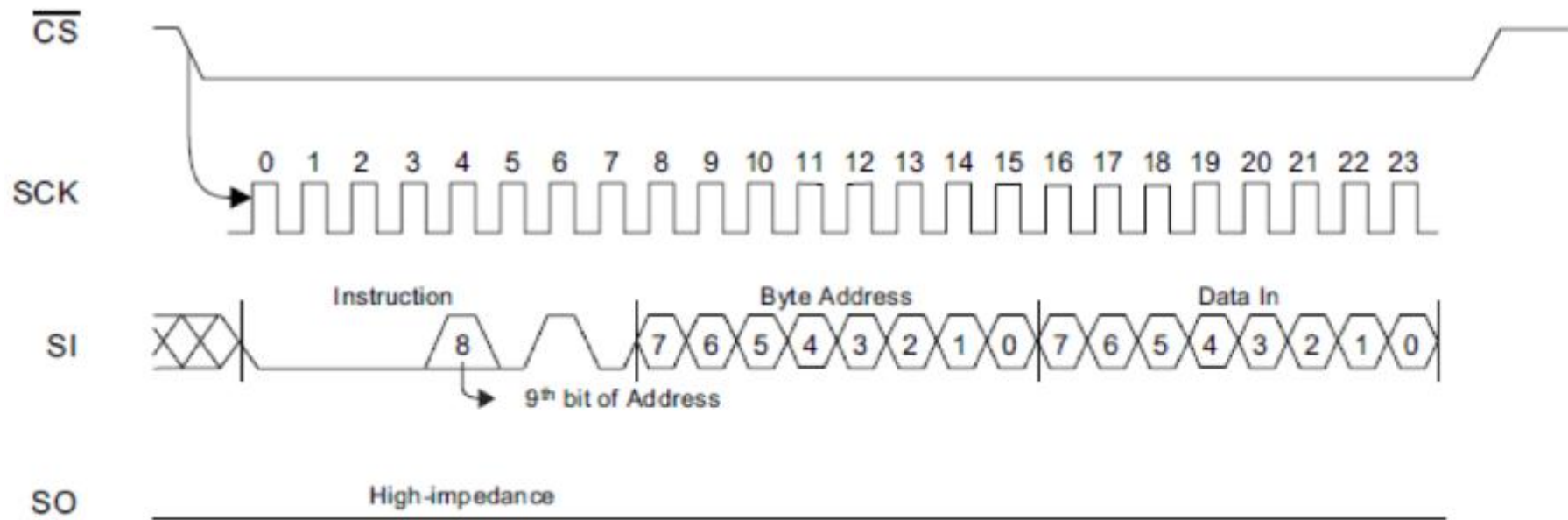
## •RDSR Timing



## •WRSR Timing

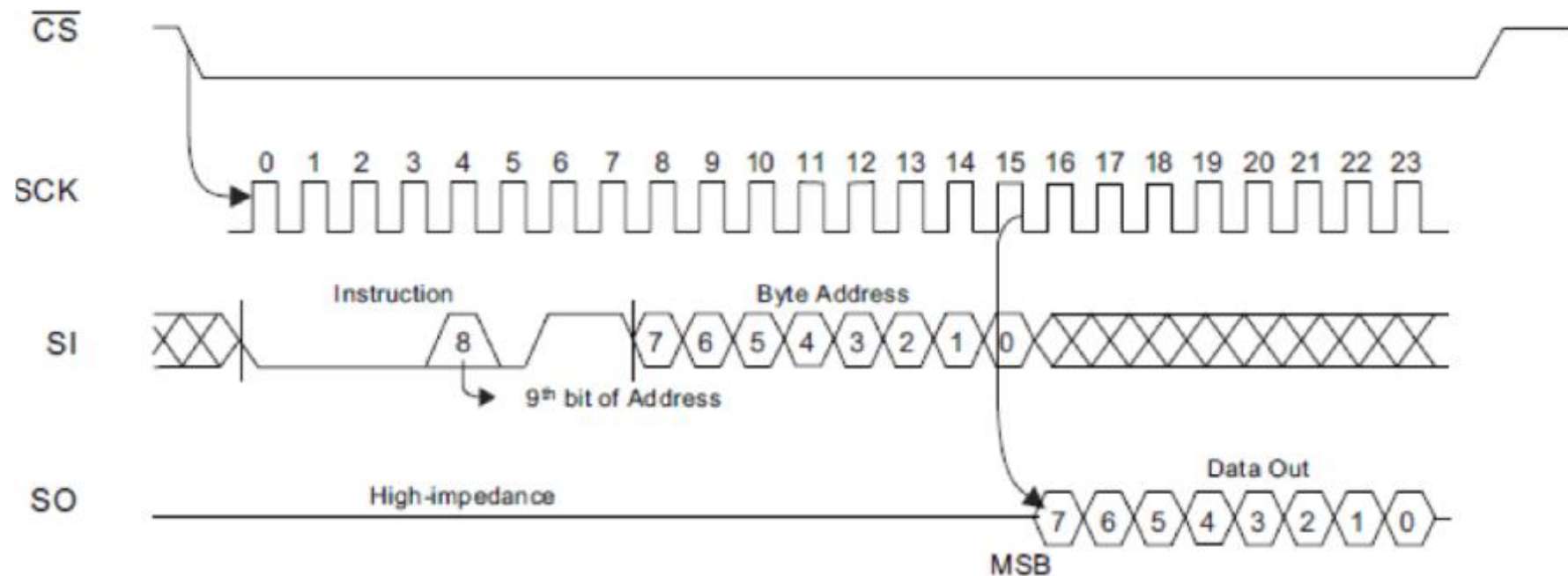


# AT25AA010A SPI Protocol - WRITE Timing



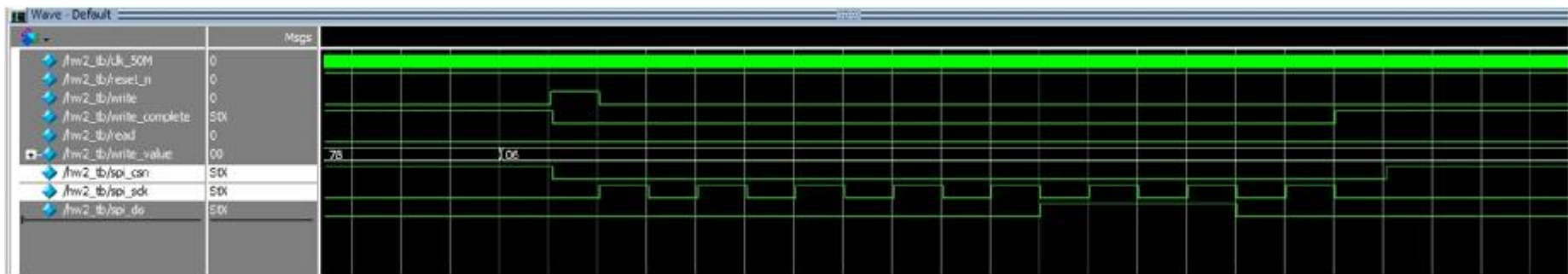


# AT25AA010A SPI Protocol - READ Timing



# 波形結果

SPI Write : 0x06



SPI Write : 0x02,0x00,0x78



# 文字輸出結果

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```
VSIM 2> run -all
# time= 0 memory_00=0xxx memory_01=0xxx memory_02=0xxx
# time=17031 write_date=0x06
# time=1034031 write_date=0x02
# time=1051031 write_date=0x00
# time=1068031 write_date=0x78
# time=6069071 memory_00=0x78 memory_01=0xxx memory_02=0xxx
# time=7085031 write_date=0x06
# time=8102031 write_date=0x02
# time=8119031 write_date=0x01
# time=8136031 write_date=0x9a
# time=13137071 memory_00=0x78 memory_01=0x9a memory_02=0xxx
# time=14153031 write_date=0x06
# time=15170031 write_date=0x02
# time=15187031 write_date=0x02
# time=15204031 write_date=0xbc
# time=20205071 memory_00=0x78 memory_01=0x9a memory_02=0xbc
# ** Note: $finish      : D:/work/NTUST/verilog/hw2_spi_master/hw2_tb.v(87)
#   Time: 21204031 ns  Iteration: 0   Instance: /hw2_tb
# 1
# Break in Module hw2_tb at D:/work/NTUST/verilog/hw2_spi_master/hw2_tb.v line 87

VSIM 3>
```

# 計分方式

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1. 將全部Verilog程式及modelsim模擬結果、波形截圖壓縮成ZIP檔，上傳至Moodle[繳交作業]，並在檔名依序寫上學號、作業號。
2. 上傳檔案名稱：學號\_HW2.zip
3. 計分標準依完成順序及程式內容給分，若發現程式或輸出畫面結果有複製狀況，該員此次作業分數為0分。