VLSI Backend Design

Topic: ANALYSIS OF HIGH-SPEED HYBRID FULL ADDER

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Abstract: Multiplier plays an important role in the design of FIR filters in digital signal processors (DSP). In VLSI the multipliers performance speed affects the overall speed of the system. Moreover, multiplication process uses execution time in most of the DSP devices. Hence, high speed is required in multiplier. This paper presents the analysis of a high-speed new adder using Shannon adder. The proposed hybrid adder is implemented in order to achieve higher reduction of power. The circuit simulations are done using Tanner EDA/Cadence/Hspice software. The obtained simulation results exhibit that the proposed structure performance is better in terms of Propagation delay, low power consumption and Power delay product when compared with the advanced technology in CMOS.

Keywords- Shannon adder, hybrid full adder, Power delay product.

Existing Method: In this article, a new XOR–XNOR circuit is proposed, which provides good driving capabilities and full swing XOR–XNOR outputs without using any external inverter. In this design, a feedback circuitry and internal NOT gate help in getting full swing output for all the transitions.

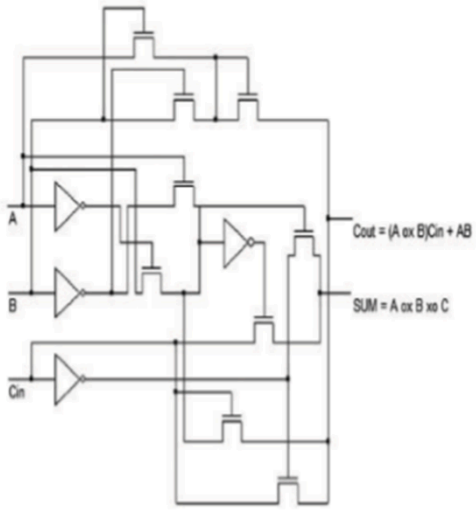
Disadvantages:

- Area is more
- Delay is more.

Proposed Method: Multiplier plays an important role in the design of FIR filters in digital signal processors (DSP). In VLSI the multipliers performance speed affects the overall speed of the system. Moreover, multiplication process uses execution time in most of the DSP devices. Hence, high speed is required in multiplier. This paper presents the analysis of a high-speed new

adder using Shannon adder. The proposed hybrid adder is implemented in order to achieve higher reduction of power.

Block Diagrams:



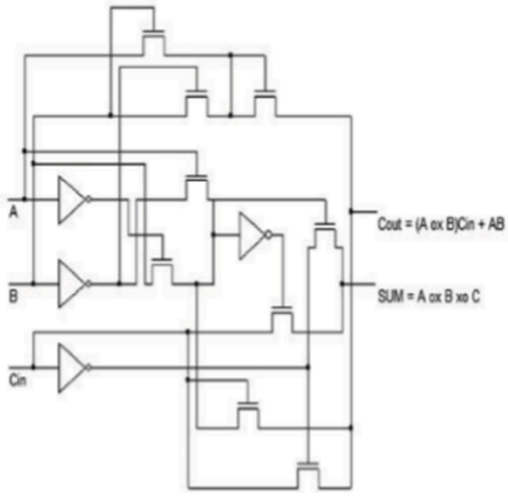


Fig: Shannon Adder

Fig: Modified Hybrid Adder

Advantages:

- Transistor count is reduced

- Better power consumption is achieved

Applications:

- Multipliers
- DSP
- Airthematic logics

Specifications:

Software Requirements:

- Tanner EDA/Cadence
- Technology files: 45nm

Hardware Requirements:

- Microsoft® Windows XP
- Intel® Pentium® 4 processor or Pentium 4 equivalent with SSE support
- 512 MB RAM
- 100 MB of available disk space

Learning Outcomes:

- Introduction to Digital electronics
- Introduction to Combinational circuits.
    - Knowledge on Adders
    - Applications of different types of adders
- Importance of Transistors
    - MOS Fundamentals
    - NMOS/PMOS/CMOS Technologies
    - How to design circuits using Transistor logic?
    - Transistor level design for Shannon adder
    - How to design Proposed circuits of Hybrid adder
    - Introduction to Hybrid Adders
    - Importance of Hybrid logic

    - Scope of Low power and fast performance adders in today's world
    - Applications in Real time.
- Tanner EDA/Cadence/H spice tool for design and simulation
- Solution providing for real time problems
    - Project Development Skills:
        - Problem Analysis Skills
        - Problem Solving Skills
        - Logical Skills
        - Designing Skills
        - Testing Skills
        - Debugging Skills
        - Presentation skills
        - Thesis Writing Skills