1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
C	0000734528	PRODUCTION RELEASED	2009-06-04

K24 MLB SCHEMATIC

6/12/2009

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22	MCP Standard Decoupling	T18_MLB 04/04/2008
23	MCP Graphics Support	T18_MLB 12/12/2007
24	SB Misc	RAYMOND 04/05/2008
25	FSB/DDR3 Vref Margining	BEN 03/31/2008
26	DDR3 SO-DIMM Connector A	BEN 06/30/2008
27	DDR3 SO-DIMM Connector B	BEN 05/09/2008
28	DDR3 Support	T18_MLB 04/04/2008
29	Right Clutch Connector	YITE 04/22/2008
30	SECUREDIGITAL CARD READER	VEMURI 01/30/2009
31	Ethernet PHY (RTL8211CL)	SUMA 05/23/2008
32	Ethernet & AirPort Support	SUMA 07/01/2008
33	ETHERNET CONNECTOR	SUMA 04/04/2008
34	FireWire LLC/PHY (FW643)	K19_MLB 11/02/2008
35	FireWire Port Power	YUN_K19_MLB 12/22/2008
36	FireWire Ports	K19_MLB 11/02/2008
37	SATA Connectors	K19_MLB 12/04/2008
38	External USB Connectors	YUAN.MA 01/18/2008
39	Front Flex Support	YUAN.MA 05/28/2008
40	SMC	T18_MLB 06/26/2008
41	SMC Support	YUAN.MA 05/28/2008
42	LPC+SPI Debug Connector	CHANGZHANG 05/09/2008
43	K24 SMBUS CONNECTIONS	BEN 04/21/2008
44	VOLTAGE SENSING	YUNWU 02/04/2008
45	Current Sensing	YUNWU 12/17/2008
46	Thermal Sensors	YUNWU 03/20/2008
47	Fan	CHANGZHANG 01/18/2008
48	WELLSPRING 1	YUAN.MA 04/22/2008
49	WELLSPRING 2	YUAN.MA 05/09/2008
50	SMS	YUNWU 06/26/2008
51	SPI ROM	CHANGZHANG 05/02/2008
52	AUDIO: CODEC/REGULATOR	AUDIO 03/04/2009
53	AUDIO: LINE INPUT FILTER	AUDIO 01/31/2009
54	AUDIO: HEADPHONE FILTER	AUDIO 02/03/2009
55	AUDI0: SPEAKER AMP	AUDIO 12/18/2008
56	AUDIO: JACK	AUDIO 03/20/2009
57	AUDIO: JACK TRANSLATORS	AUDIO 03/20/2009
58	DC-In & Battery Connectors	YUNWU 12/11/2008
59	PBUS Supply/Battery Charger	RAYMOND 01/31/2008
60	5V/3.3V SUPPLY	RAYMOND 02/08/2008
61	1.5V/0.75V DDR3 SUPPLY	RAYMOND 01/31/2008
62	IMVP6 CPU VCore Regulator	RAYMOND 01/31/2008
63	MCP CORE REGULATOR	K19_MLB 12/10/2008
64	CPU VTT(1.05V) SUPPLY	RAYMOND 02/08/2008
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77	Ethernet Constraints	T18_MLB 03/19/2008
78	FireWire Constraints	K19_MLB 12/01/2008
79	SMC Constraints	T18_MLB 01/04/2008
80	K24 SPECIAL CONSTRAINTS	M97_MLB
81	K24 RULE DEFINITIONS	M97_MLB

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7898	1	SCHEM,MLB,K24	SCH	CRITICAL	
820-2530	1	PCBF,MLB,K24	PCB	CRITICAL	

DRAWING TITLE: SCHEM,MLB,K24

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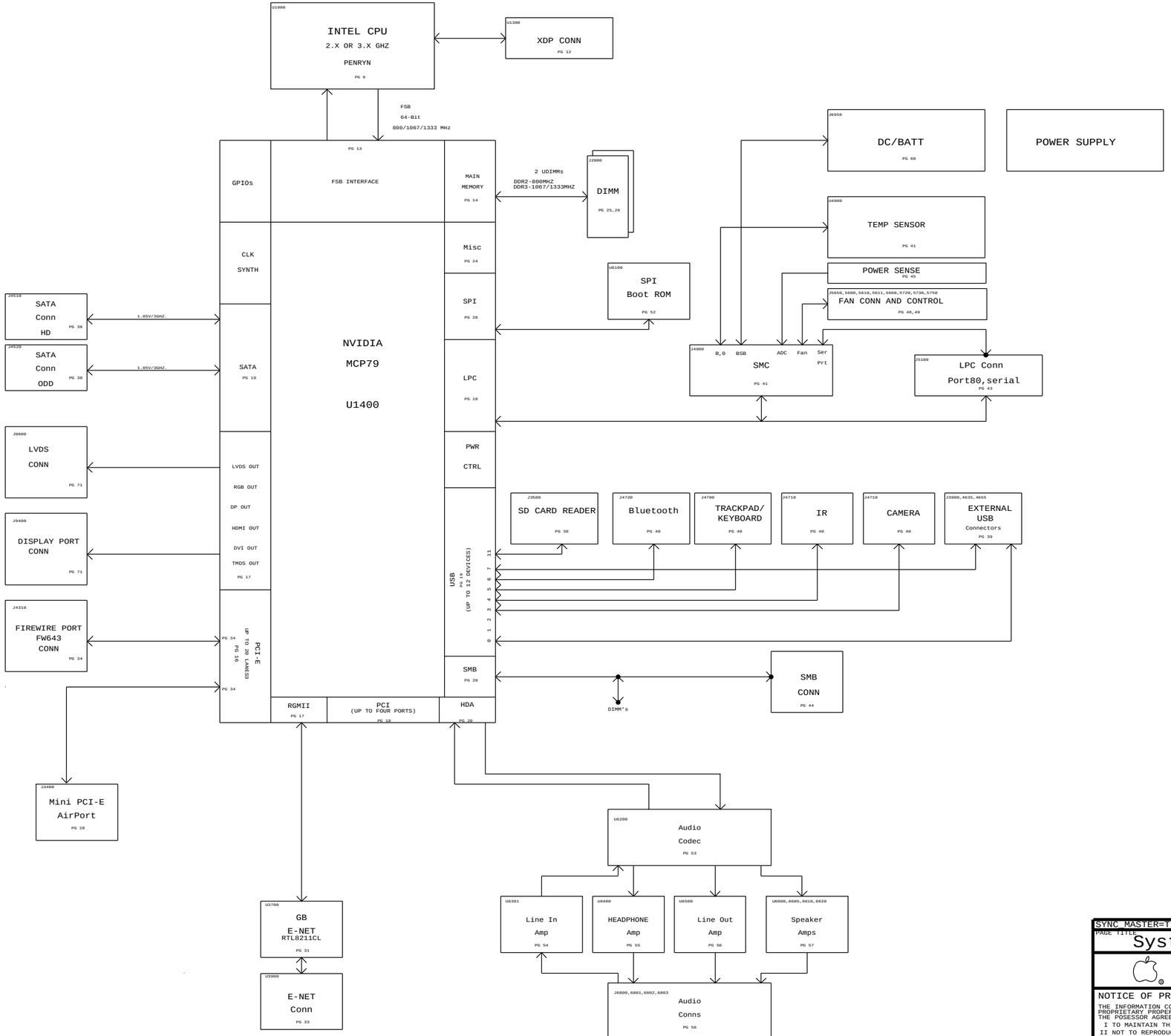

SYNC_MASTER=T18_MLB SYNC_DATE=12/12/2007

PAGE TITLE

System Block Diagram

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K24 POWER SYSTEM ARCHITECTURE

PP18V5_DCIN_CONN
D6905
PPVIN_G3H_P3V42G3H
D6905
PBUS_VSENSE
ENABLE
3.425V G3HOT
LT3470
U6990
VOUT
PP3V42_G3H_REG
SMC PWRGD
RN5VD30A-F
U5000
7A FUSE
F7000
PPVBAT_G3H_CHGR_REG
PPBUS_G3H
Q5315
PPBUS_G3H_CPU_ISNS_R
R5492 PPBUS_G3H_CPU_ISNS
PP5V_S0_CPUVTTS0
CPUVTTS0_EN
(S0)
VIN
EN_PSV
VOUT
CPUVTT
(1.05V)
TPS51117
U7600
PGOOD
PP1V05_S0
(8A MAX CURRENT)
CPUVTTS0_PGOOD
AC
ADAPTER
IN
DCIN(16.5V)
F6905
6A FUSE
CHGR_EN
(S5)
ENABLES
VIN
VOUT
PBUS SUPPLY/
BATTERY CHARGER
ISL6258A
U7000
U5403
SMC_BATT_ISENSE
SMC_CPU_VSENSE
SMC_CPU_ISENSE
CPU VCORE
ISL9504B
U7400
PPVCORE_S0_CPU
(44A MAX CURRENT)
J6950
3S2P
(9 TO 12.6V)
BATT_POS_F
Q7050
CHGR_BGATE
PPVBAT_G3H_CHGR_OUT
IMVP_VR_ON
VR_ON
PGOOD
VR_PWRGOOD_DELAY
P1V05ENET_EN
1.05V S0
FETS
(Q3841)
PP1V05_ENET_FET
PPBUS_G3H
MCP79
PM_SLP_S4_L
SLP_S3#
U1400
PCI_RESET0#
P3V3S3_EN
DDRREG_EN
P5VLTS3_EN
RC
DELAY
SMC
U4900
P16
P60
SMC_PM_G2_EN
(S5)
P1V05_S5_EN
RC DELAY
1.05V (S5)
ISL8009
U7750
VOUT
PP1V05_S5_REG
P5VRTS0_EN_L
5V
(RT)
3.3V
TPS51125
U7200
EN1
EN2
VOUT1
VOUT2
PGOOD1,2
VREG3
PP5V_S3_REG
(4A MAX CURRENT)
PP3V3_S5_REG
(4A MAX CURRENT)
P5V3V3_PGOOD
Q7800
SMC_PM_G2_EN
P3V3S5_EN_L
Q7910
P3V3S3_EN
Q7940
PP5V_S0_FET
P5VS0_EN
PP5V_S3
PP3V3_S5
PP3V3_S3_FET
4.5V AUDIO
TPS7174S
U6200
PP4V5_AUDIO_ANALOG
MCP79
PWRBTN*
PLTRST*
RSMRST*
CPUPWRGD(GPIO49)
CPU_RESET#
U1400
LPC_RESET_L
CPU_PWRGD
MCP_PS_PWRGD
PS_PWRGD
U2850
FSB_CPURST_L
CPU
PWRGOOD
RESET*
U1000
Q7930
P3V3S0_EN
PP3V3_S0_FET
Q3810
P3V3ENET_EN_L
P3V3_ENET_FET
SMC
RSMRST_OUT(P15)
PWRGD(P12)→99ms DLY→
IMVP_VR_ON(P16)
RSMRST_IN(P13)
PLT_RST*
PWR_BUTTON(P90)
P17(BTN_OUT)
PM_RSMRST_L
IMVP_VR_ON
PM_PWRBTN_L
SMC_RESET_L
ALL_SYS_PWRGD
RSMRST_PWRGD
SMC_ONOFF_L
P5V3V3_PGOOD
MCPCORES0_PGOOD
CPUVTTS0_PGOOD
P5V_LT_S3_PGOOD
S0PGOOD_PWROK
SLP_S5_L
SLP_S4_L
SLP_S3_L
SLP_S5_L(P95)
SLP_S4_L(P94)
SLP_S3_L(P93)
U4900
PM_SLP_S3_L
Q3801
PM_ENET_EN_L
Q3802
WOL_EN
SMC_ADAPTER_EN
LP8543
U9701
BKLT_EN
ENA
VOUT
PPVOUT_S0_LCDBKLT
P5V3V3_PGOOD
S3 TO S0
FETS
(Q7901 & Q7971)
PP1V5_S0_FET
PP1V5_S0
1.8V LDO
TPS62202
U7760
PP1V8_S0_REG
=DDRREG_EN
=DDTVTT_EN
1.5V
0.75V
TPS51116
U7300
PP1V5_S3_REG
(12A MAX CURRENT)
PP0V75_S0_REG
(1A MAX CURRENT)
PP3V3_S0
PP1V5_S0
PP1V05_S0
RST*
LTC2909
U7870
P1V8S0_EN
MCPDDR_EN
CPUVTTS0_EN
MCPCORES0_EN
P1V05S0_EN
(S0)
P3V3S0_EN
(S0)
PBUSVSENS_EN
(S0)
P5VRTS0_EN_L
(S0)
MCP_CORE
EN2
5V (LT)
EN1
VOUT2
VOUT1
ISL6236
U7500
MCPCORES0_EN
PPVCORE_S0_MCP_REG_R
R7572
PPVCORE_S0_MCP
(25A MAX CURRENT)

SYNC_MASTER=DRAGON	SYNC_DATE=03/13/2008
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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
630-9923	PCBA,MLB,BETTER,K24	K24_COMMON,CPU_2_26GHZ,EEE_6GC,KB_BL
630-9924	PCBA,MLB,BEST,K24	K24_COMMON,CPU_2_53GHZ,EEE_6GD,KB_BL

Bar Code Labels / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:6G4]	CRITICAL	EEE_6G4
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:6GC]	CRITICAL	EEE_6GC
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:6GD]	CRITICAL	EEE_6GD

BOM Groups

BOM GROUP	BOM OPTIONS
K24_COMMON	COMMON,ALTERNATE,K24_MCP,K24_MISC,K24_DEBUG_PROD,K24_PROGPARTS
K24_MCP	MCP_B03,BOOT_MODE_USER,MCPSEQ_SMC
K24_MISC	ONEWIRE_PU,DP_ESD,MIKEY,BKLT_PROD,SUPERCAP_NO,LDO_NO
K24_PROGPARTS	BOOTROM_PROG,SMC_PROG,IR_PROG,WELLSPRING_PROG
K24_DEBUG_ENG	DEVEL_BOM,SMC_DEBUG_YES,XDP
K24_DEBUG_PVT	DEVEL_BOM,BMON_PROD,SMC_DEBUG_YES,XDP,NO_VREFMRGN
K24_DEBUG_PROD	BMON_PROD,SMC_DEBUG_YES,XDP,LPCPLUS_NOT,NO_VREFMRGN
K24_DEVEL_ENG	BMON_ENG,XDP_CONN,LPCPLUS,VREFMRGN,FWPHY_WAKE_YES
K24_DEVEL_PVT	LPCPLUS

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3646	1	PDC,SLGBE,PRQ,2.0,25W,1066,M0,3M,BGA	U1000	CRITICAL	CPU_2_0GHZ
337S3704	1	PDC,SLGE2,PRQ,2.26,25W,1066,R0,3M,BGA	U1000	CRITICAL	CPU_2_26GHZ
337S3639	1	PDC,SLB4N,PRQ,2.4,25W,1066,M0,3M,BGA	U1000	CRITICAL	CPU_2_4GHZ
337S3756	1	PDC,SLGFG,PRQ,2.53,25W,1066,R0,3M,BGA	U1000	CRITICAL	CPU_2_53GHZ
337S3761	1	PDC,SLGLA,PRQ,2.66,25W,1066,E0,3M,BGA	U1000	CRITICAL	CPU_2_66GHZ
338S0710	1	IC,GMCP,MCP79,35X35MM,BGA1437,B03	U1400	CRITICAL	MCP_B03

Programmable Parts

338S0563	1	IC,SMC,HSB/2117,9X9MM,TLP,HF	U4900	CRITICAL	SMC_BLANK
341S2445	1	IC,SMC,K24	U4900	CRITICAL	SMC_PROG
335S0610	1	IC,FLASH,SPI,32MBIT,3.3V,86MHZ,8-SOP	U6100	CRITICAL	BOOTROM_BLANK
341S2441	1	IC,PRGRM,EFI BOOTROM,UNLOCK,K24	U6100	CRITICAL	BOOTROM_PROG
338S0375	1	IC,CY7C63833,ENCORE II,USB CONTROLLER	U4800	CRITICAL	IR_BLANK
341S2093	1	IC,IR CONTROLLER,M97	U4800	CRITICAL	IR_PROG
337S2983	1	IC,PSOC+ W/ USB,56 PIN,MLF,CY8C24794	U5701	CRITICAL	WELLSPRING_BLANK
341S2503	1	IC,PRGRM,WELLSPRING CONTROLLER	U5701	CRITICAL	WELLSPRING_PROG

LOCKED BOOTROM APN IS 341S2443

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S0778	152S0693		ALL	CYNTEC AS ALTERNATE
152S0796	152S0685		ALL	CYNTEC AS ALTERNATE
157S0058	157S0055		ALL	DELTA AS ALTERNATE
104S0018	104S0023		ALL	DALE/VISHAY AS ALTERNATE
128S0093	128S0218		ALL	KEMET AS ALTERNATE
152S0874	152S0516		ALL	MAGLAYERS AS ALTERNATE
152S0847	152S0586		ALL	MAGLAYERS AS ALTERNATE
152S1025	152S1024		ALL	TOKO AS ALTERNATE
337S3769	337S3704		ALL	INTEL P7550 CPU AS ALTERNATE
353S2718	353S2310		ALL	INTERSIL AS ALTERNATE

DEVELOPMENT BOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
085-0741	1	K24 MLB DEVELOPMENT BOM	DEVEL	CRITICAL	DEVEL_BOM

K24 BOARD STACK-UP

Top	SIGNAL
2	GROUND
3	SIGNAL(High Speed)
4	SIGNAL(High Speed)
5	GROUND
6	POWER
7	POWER
8	GROUND
9	SIGNAL(High Speed)
10	SIGNAL(High Speed)
11	GROUND
BOTTOM	SIGNAL

SYNC MASTER=M97 MLB

PAGE TITLE: BOM Configuration

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Revision History

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Functional Test Points

Fan Connectors

J4100	TRUE	PP5V_S0	(NEED 3 TP) 6D3 7D5
J4105	TRUE	FAN_RT_PWM	47B4
J4110	TRUE	FAN_RT_TACH	47C4

(NEED TO ADD 3 GND TP)

MIC FUNC_TEST

J2810	TRUE	BI_MIC_LO	56C2 57B1
J2820	TRUE	BI_MIC_HI	56C2 57B1
J2830	TRUE	MIC_SHIELD	56C2 57B1

SPEAKER FUNC_TEST

J4200	TRUE	SPKRAMP_L_N_OUT	55A2 56B2
J4205	TRUE	SPKRAMP_L_P_OUT	55B2 56B2
J4210	TRUE	SPKRAMP_R_N_OUT	55C2 56A2
J4215	TRUE	SPKRAMP_R_P_OUT	55C2 56B2
J4220	TRUE	SPKRAMP_SUB_N_OUT	55B2 56B2
J4225	TRUE	SPKRAMP_SUB_P_OUT	55C2 56B2

THERMAL FUNC_TEST

J4400	TRUE	MCPTHMSNS_D2_P	46B5 80D3
J4405	TRUE	MCPTHMSNS_D2_N	46B5 80D3

LVDS FUNC_TEST

J4500	TRUE	PP3V3_LCDVDD_SW_F	6C3 68C2
J4505	TRUE	PP3V3_S0_LCD_F	68C3
J4510	TRUE	PPVOUT_S0_LCDBKLT	6C3 68B2 71C1
J4515	TRUE	LVDS_IG_DDC_CLK	17B3 68C5
J4520	TRUE	LVDS_IG_DDC_DATA	17A3 68C5
J4600	TRUE	LVDS_IG_A_DATA_N<0>	17B3 68C2 75B3
J4605	TRUE	LVDS_IG_A_DATA_P<0>	17B3 68C2 75B3
J4610	TRUE	LVDS_IG_A_DATA_N<1>	17B3 68C2 75B3
J4615	TRUE	LVDS_IG_A_DATA_P<1>	17B3 68C2 75B3
J4620	TRUE	LVDS_IG_A_DATA_N<2>	17B3 68C2 75B3
J4625	TRUE	LVDS_IG_A_DATA_P<2>	17B3 68C2 75B3
J4630	TRUE	LVDS_IG_A_CLK_F_N	68C2 75B3
J4635	TRUE	LVDS_IG_A_CLK_F_P	68C2 75B3
J4640	TRUE	LED_RETURN_1	68B3 71B1
J4645	TRUE	LED_RETURN_2	68B3 71B1
J4650	TRUE	LED_RETURN_3	68B3 71B1
J4655	TRUE	LED_RETURN_4	68B3 71B1
J4660	TRUE	LED_RETURN_5	68B3 71B1
J4665	TRUE	LED_RETURN_6	68B3 71A1
J4670	TRUE	TP_BKL_SYNC	68C2

(NEED TO ADD 5 GND TP)

SATA ODD CONN

J2600	TRUE	PP5V_SW_ODD	(NEED 4 TP) 6C3 37D3
J2605	TRUE	SMC_ODD_DETECT	37C7 40B8
J2610	TRUE	SATA_ODD_D2R_C_P	37C6 75A3
J2615	TRUE	SATA_ODD_D2R_C_N	37C6 75A3
J2620	TRUE	SATA_ODD_R2D_P	37C6 75A3
J2625	TRUE	SATA_ODD_R2D_N	6A7 37C6 75A3

(NEED TO ADD 4 GND TP)

SATA HDD/IR/SIL

J3100	TRUE	PP5V_S0_HDD_FLT	(NEED 4 TP) 6C3 37B6
J3105	TRUE	SATA_HDD_R2D_P	37A5 75A3
J3110	TRUE	SATA_HDD_R2D_N	37A5 75A3
J3115	TRUE	SATA_HDD_D2R_C_P	37B5 75A3
J3120	TRUE	SATA_HDD_D2R_C_N	37B5 75A3
J3125	TRUE	SYS_LED_ANODE_R	37A7
J3130	TRUE	IR_RX_OUT	37A7 39D4
J3135	TRUE	PP5V_S3_IR_R	37A7

(NEED TO ADD 4 GND TP)

BATT POWER CONN

J8500	TRUE	SMBUS_SMC_BSA_SCL	6A7 43C5 79D3
J8505	TRUE	SMBUS_SMC_BSA_SDA	43C5 79D3
J8510	TRUE	SYS_DETECT_L	58A8
J8515	TRUE	BATT_POS_F	(NEED 3 TP) 58A7 58B8 59A3

(NEED TO ADD 3 GND TP)

BATT SIGNAL CONN

J8520	TRUE	PP3V42_G3H	(NEED 3 TP) 6B5 6D3 7D1
J8525	TRUE	SMBUS_SMC_BSA_SCL	6A7 43C5 79D3
J8530	TRUE	SMBUS_SMC_BSA_SCL	6A7 43C5 79D3
J8535	TRUE	SMC_BIL_BUTTON_L	40C5 58C4
J8540	TRUE	SMC_LID_R	58C2

(NEED TO ADD 5 GND TP)

RIGHT CLUTCH CONN

J3800	TRUE	PP5V_S3_BTCAMERA_F	29C7
J3805	TRUE	PCIE_MINI_D2R_P	16B6 29C7 75D3
J3810	TRUE	PCIE_MINI_D2R_N	16B6 29C7 75D3
J3815	TRUE	PCIE_MINI_R2D_P	29C7 75D3
J3820	TRUE	PCIE_MINI_R2D_N	29C7 75D3
J3825	TRUE	PCIE_CLK100M_MINI_CONN_P	29C7 75D3
J3830	TRUE	PCIE_CLK100M_MINI_CONN_N	29C7 75D3
J3835	TRUE	USB_CAMERA_CONN_P	29B7 76C3
J3840	TRUE	USB_CAMERA_CONN_N	29B7 76C3
J3845	TRUE	PP5V_WLAN	(NEED 2 TP) 6C3 29C5
J3850	TRUE	PCIE_WAKE_L	16B6 29C7
J3855	TRUE	SMBUS_SMC_A_S3_SCL	6C5 43D2 79D3
J3860	TRUE	SMBUS_SMC_A_S3_SDA	6C5 43D2 79D3
J3865	TRUE	CONN_USB2_BT_P	29B7 76C3
J3870	TRUE	CONN_USB2_BT_N	29B7 76B3
J3875	TRUE	MINI_CLKREQ_O_L	29C7
J3880	TRUE	MINI_RESET_CONN_L	29A7

(NEED TO ADD 6 GND TP)

IPD_FLEX_CONN

J4000	TRUE	PP3V3_S3_LDO	6C3 49B4 49C3
J4005	TRUE	PP18V5_S3	6C3 49C1 49D3
J4010	TRUE	Z2_CS_L	48C8 49C3
J4015	TRUE	Z2_DEBUG3	48C8 49C3
J4020	TRUE	Z2_MOSI	48C8 49C3
J4025	TRUE	Z2_MISO	48C8 49C3
J4030	TRUE	Z2_SCLK	48C8 49C3
J4035	TRUE	Z2_BOOST_EN	49C3 49C5
J4040	TRUE	Z2_HOST_INTN	48D8 49C3
J4045	TRUE	Z2_CLKIN	48C6 49C3
J4050	TRUE	Z2_KEY_ACT_L	48C8 49C1
J4055	TRUE	Z2_RESET	48C8 49C1
J4060	TRUE	PSOC_MISO	48C8 49C1
J4065	TRUE	PSOC_MOSI	48C8 49C1
J4070	TRUE	PSOC_SCLK	48C8 49C1
J4075	TRUE	SMBUS_SMC_A_S3_SDA	6D5 43D2 79D3
J4080	TRUE	SMBUS_SMC_A_S3_SCL	6D5 43D2 79D3
J4085	TRUE	PSOC_F_CS_L	48C8 49C1
J4090	TRUE	PICKB_L	48D8 49C1

KEYBOARD CONN

J4500	TRUE	PP3V3_S3	6D3 7D3
J4505	TRUE	PP3V42_G3H	6A7 6D3 7D1
J4510	TRUE	WS_KBD1	48C6 48D2
J4515	TRUE	WS_KBD2	48C6 48D2
J4520	TRUE	WS_KBD3	48C6 48D2
J4525	TRUE	WS_KBD4	48C6 48D2
J4530	TRUE	WS_KBD5	48C6 48D2
J4535	TRUE	WS_KBD6	48C6 48D2
J4540	TRUE	WS_KBD7	48C6 48D2
J4545	TRUE	WS_KBD8	48C6 48D2
J4550	TRUE	WS_KBD9	48C6 48D2
J4555	TRUE	WS_KBD10	48C6 48D2
J4560	TRUE	WS_KBD11	48C6 48D2
J4565	TRUE	WS_KBD12	48C6 48D2
J4570	TRUE	WS_KBD13	48C6 48D2
J4575	TRUE	WS_KBD14	48C6 48D2
J4580	TRUE	WS_KBD15_CAP	48C2 48C6
J4585	TRUE	WS_KBD16_NUM	48C2
J4590	TRUE	WS_KBD17	48C2
J4595	TRUE	WS_KBD18	48C2 48D6
J4600	TRUE	WS_KBD19	48C2 48D7
J4605	TRUE	WS_KBD20	48C2 48D7
J4610	TRUE	WS_KBD21	48C2 48D7
J4615	TRUE	WS_KBD22	48C2 48D7
J4620	TRUE	WS_KBD23	48C2 48D7
J4625	TRUE	WS_KBD_ONOFF_L	48C2
J4630	TRUE	WS_LEFT_SHIFT_KBD	48B3 48B5 48C2
J4635	TRUE	WS_LEFT_OPTION_KBD	48B3 48B5 48C2
J4640	TRUE	WS_CONTROL_KBD	48B3 48B5 48C2

(NEED TO ADD 1 GND TP)

KBD BACKLIGHT CONN

J4650	TRUE	KBDLED_ANODE	(NEED 2 TP) 49A4
J4655	TRUE	SMC_KDBLED_PRESENT_L	49A4 49A6

(NEED TO ADD 2 GND TP)

DEBUG VOLTAGE

J4300	TRUE	PPVCORE_S0_CPU	7D7
J4305	TRUE	PPVCORE_S0_MCP	7C7
J4310	TRUE	PP0V75_S0	7C7
J4315	TRUE	PP1V05_S0	7D7
J4320	TRUE	PP1V5_S0	7C6
J4325	TRUE	PP1V8_S0	78B6
J4330	TRUE	PP5V_S0	6D7 7D5
J4335	TRUE	PP3V3_S0	7D5
J4340	TRUE	PP1V5_S3	7D3
J4345	TRUE	PP3V3_S3	68B5 7D3
J4350	TRUE	PP5V_S3	7C3
J4355	TRUE	PP1V1R1V05_S5	78B3
J4360	TRUE	PP3V3_S5	78B3
J4365	TRUE	PP3V42_G3H	6A7 68B5 7D1
J4370	TRUE	PPBUS_G3H	7C1
J4375	TRUE	PP3V3_ENET_PHY	78B5
J4380	TRUE	PP1V2R1V05_ENET	78B5
J4385	TRUE	PP3V3_G3_RTC	20C8 21A5 24D4
J4390	TRUE	PP5V_WLAN	6D5 29C5
J4395	TRUE	PP5V_SW_ODD	6B7 37D3
J4400	TRUE	PP5V_S0_HDD_FLT	6B7 37B6
J4405	TRUE	PP3V3_S5_AVREF_SMC	40D4 41C6
J4410	TRUE	PP18V5_S3	6C5 49C1 49D3
J4415	TRUE	PP3V3_S3_LDO	6C5 49B4 49C3
J4420	TRUE	PP3V3_LCDVDD_SW_F	6C7 68C2
J4425	TRUE	PPVOUT_S0_LCDBKLT	6C7 68B2 71C1
J4430	TRUE	PP4V5_AUDIO_ANALOG	52A5 52D2 52D7
J4435	TRUE	SMC_PM_G2_EN	40D5 60C5 66D8
J4440	TRUE	PM_SLP_S4_L	20C3 40C5 41A2 66C8
J4445	TRUE	PM_SLP_S3_L	20C3 32B7 35A5 40C5 66D5 70D8

(NEED TO ADD 4 GND TP)

DC POWER CONN

J4700	TRUE	PP18V5_DCIN_FUSE	(NEED 3 TP) 58D6
J4705	TRUE	ADAPTER_SENSE	58D7

(NEED TO ADD 4 GND TP)

SYNC_MASTER=M97_MLB

PAGE TITLE: FUNC TEST

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SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

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"S0,S0M" RAILS

62D1 =PPVCORE_S0_CPU_REG (CPU VCORE PWR)
- PPVCORE_S0_CPU — 6D3
  MIN_LINE_WIDTH=0.6 MM
  MIN_NECK_WIDTH=0.3 MM
  VOLTAGE=1.25V
  MAKE_BASE=TRUE
  - =PPVCORE_S0_CPU — 10B5 10D6 11D6
  - =PPVCORE_S0_CPU_VSENSE — 44D8

64C2 =PPCPUVTT_S0_REG
- PP1V05_S0 — 6D3
  MIN_LINE_WIDTH=0.6 mm
  MIN_NECK_WIDTH=0.2 mm
  VOLTAGE=1.05V
  MAKE_BASE=TRUE
  - =PP1V05_S0_CPU — 9D5 10C6 11B6 12D6
  - =PP1V05_S0_MCP_FSB — 13A2 13B7 21D3 22C8
  - =PP1V05_S0_SMC_LS
  - =PP1V05_S0_MCP_PEX_DVDD — 7A8 22D8
  - =PP1V05_S0_MCP_AVDD_UF — 22D4
  - =PP1V05_S0_MCP_SATA_DVDD — 7A8 22D6
  - =PP1V05_S0_MCP_HDMI_VDD — 17A6 23D7
  - =PP1V05_S0_VMON — 66A8
  - =PP1V05_S0_MCP_PLL_UF_R — 65B3
  - =PP1V05_FW_P1V05FWFET — 35C6
  - =PP1V05_FWPWRCTL — 35B4

63C7 63C1 63B8 =PPMCPCORE_S0_REG (MCP VCORE AFTER SENSE RES)
- PPVCORE_S0_MCP — 6D3
  MIN_LINE_WIDTH=0.6 MM
  MIN_NECK_WIDTH=0.2 MM
  VOLTAGE=1.25V
  MAKE_BASE=TRUE
  - =PPVCORE_S0_MCP — 21D5 22D8
  - =PPVCORE_S0_MCP_VSENSE — 44D8

61C8 =PP0V75_S0_REG
- PP0V75_S0 — 6D3
  MIN_LINE_WIDTH=0.4 mm
  MIN_NECK_WIDTH=0.2 mm
  VOLTAGE=0.75V
  MAKE_BASE=TRUE
  - =PPVTT_S0_VTTCLAMP — 67B3
  - =PP0V75_S0_MEM_VTT_A — 26A4
  - =PP0V75_S0_MEM_VTT_B — 27A4

67D1 =PP1V5_S0_FET
- PP1V5_S0 — 6D3
  MIN_LINE_WIDTH=0.5 mm
  MIN_NECK_WIDTH=0.2 mm
  VOLTAGE=1.5V
  MAKE_BASE=TRUE
  - =PP1V5_S0_CPU — 10B6 11B6
  - =PP1V5_S0_VMON — 66A8
  - =PP1V8R1V5_S0_MCP_MEM — 15C3 15C7 22C8
  - =PP1V5_S0_MEM_MCP — 27B3
  - =PP1V5_S0_MCP_PLL_VLDO — 65B6

65C5 =PP1V8_S0_REG
- PP1V8_S0 — 6D3
  MIN_LINE_WIDTH=0.5 MM
  MIN_NECK_WIDTH=0.2 mm
  VOLTAGE=1.8V
  MAKE_BASE=TRUE
  - =PP3V3R1V8_S0_MCP_IFP_VDD — 17B6 23D7
  - =PP1V8_S0_AUDIO — 52D7

65B1 22C4 =PP1V05_S0_MCP_PLL_UF
- PP1V05_S0_MCP_PLL_UF
  MIN_LINE_WIDTH=0.6 MM
  MIN_NECK_WIDTH=0.2 mm
  VOLTAGE=1.05V
  MAKE_BASE=TRUE

67B6 =PP5V_S0_FET
- PP5V_S0 — 6D3 6D7
  MIN_LINE_WIDTH=0.6 mm
  MIN_NECK_WIDTH=0.2 mm
  VOLTAGE=5V
  MAKE_BASE=TRUE
  - =PP5V_S0_HDD — 37B3
  - =PP5V_S0_LPCPLUS — 42D5
  - =PP5V_S0_FAN_RT — 47C5
  - =PP5V_S0_CPU_IMVP — 62D8
  - =PP5V_S0_KBDLED — 49A5
  - =PP5V_S0_DP_AUX_MUX — 69B6
  - =PP5V_S0_CPUVTTS0 — 64C8
  - =PP5V_S0_BKL — 71D4
  - =PP5V_S0_MCPREG — 63D4
  - =PP5V_S0_VMON — 66B5

67C6 =PP3V3_S0_FET
- PP3V3_S0 — 6D3
  MIN_LINE_WIDTH=0.6 mm
  MIN_NECK_WIDTH=0.2 mm
  VOLTAGE=3.3V
  MAKE_BASE=TRUE
  - =PP3V3_S0_XDP — 12D6
  - =PP3V3_S0_MCP — 20C2 21B3 22B8
  - =PP3V3_S0_MCP_DAC_UF — 23D4
  - =PP3V3_S0_MCP_VPLL_UF — 23C7
  - =PP3V3_S0_ODD — 37C7 37D6
  - =PP3V3_S0_SMBUS_SMC_0_S0 — 43D5
  - =PP3V3_S0_SMBUS_SMC_B_S0 — 43C3
  - =PP3V3_S0_SMBUS_MCP_0 — 43D8
  - =PP3V3_S0_FAN_RT — 47C5
  - =PP3V3_S0_AUDIO — 52A8 52D2 56D8 57B8 57D3
  - =PP3V3_S0_IMVP — 62D8
  - =PP3V3_S0_LCD — 68C5
  - =PP3V3_S0_MCP_GPIO — 17C1 18D1 20A4
  - =PP3V3_S0_MCP_PLL_UF — 22B6
  - =PP3V3R1V5_S0_MCP_HDA — 20D3 20D8 22A8
  - =PP3V3_S0_SMC — 41A1 41D3
  - =PP3V3_S0_MCPTHMSNS — 46B6
  - =PP3V3_S0_CPUTHMSNS — 46D6
  - =PP3V3_S0_DPCONN — 70B8 70C8
  - =PPSPD_S0_MEM_A — 26A8
  - =PPSPD_S0_MEM_B — 27A8
  - =PP3V3_S0_PWRCTL — 66A5
  - =PP3V3_S0_VMON — 66A8
  - =PP3V3_S0_CPUVTTISNS — 45C7
  - =PP3V3_S0_TPAD — 49A6
  - =PP3V3_S0_SMBUS_MCP_1 — 43C8
  - =PP3V3_S0_P1V8S0 — 65D8
  - =PP3V3_S0_BKL_VDDIO — 71C7
  - =PP3V3_S0_MCPDDRISNS — 45D8
  - =PP3V3_S0_MCP_PLL_VLDO — 65C6
  - =PP3V3_S0_P3V3FWFET — 35D6
  - =PP3V3_S0_FWPWRCTL — 35B1 35D2

"ENET" RAILS

32D2 =PP3V3_ENET_FET
- PP3V3_ENET_PHY — 6C3
  MIN_LINE_WIDTH=0.4 MM
  MIN_NECK_WIDTH=0.2 MM
  VOLTAGE=3.3V
  MAKE_BASE=TRUE
  - =PP3V3_ENET_MCP_RMGT — 17D3 17D7 22A5 22B6
  - =PP3V3_ENET_PHY — 31D7

32B2 =PP1V05_ENET_FET
- PP1V2R1V05_ENET — 6C3
  MIN_LINE_WIDTH=0.4 MM
  MIN_NECK_WIDTH=0.2 MM
  VOLTAGE=1.05V
  MAKE_BASE=TRUE
  - =PP1V05_ENET_MCP_PLL_MAC — 22A8
  - =PP1V05_ENET_MCP_RMGT — 17D3 22D6
  - =PP1V05_ENET_PHY — 31D2

PEX & SATA AVDD/DVDD aliases

22D1 PP1V05_S0_MCP_PEX_AVDD (MAKE_BASE=TRUE)
206 mA (A01)
- =PP1V05_S0_MCP_PEX_AVDD0 — 16B3
- =PP1V05_S0_MCP_PEX_AVDD1 — 16A3

206 mA (A01)

22D8 7D7 =PP1V05_S0_MCP_PEX_DVDD
- =PP1V05_S0_MCP_PEX_DVDD0 — 16B6
- =PP1V05_S0_MCP_PEX_DVDD1 — 16A6

57 mA (A01)

22D2 PP1V05_S0_MCP_SATA_AVDD (MAKE_BASE=TRUE)
127 mA (A01)
- =PP1V05_S0_MCP_SATA_AVDD0 — 19B6
- =PP1V05_S0_MCP_SATA_AVDD1 — 19B6

127 mA (A01)

22D6 7D7 =PP1V05_S0_MCP_SATA_DVDD
- =PP1V05_S0_MCP_SATA_DVDD0 — 19B6
- =PP1V05_S0_MCP_SATA_DVDD1 — 19B6

43 mA (A01)

"S3" RAILS

61C1 =PP1V5_S3_REG
- PP1V5_S3 — 6D3
  MIN_LINE_WIDTH=0.6 mm
  MIN_NECK_WIDTH=0.2 mm
  VOLTAGE=1.5V
  MAKE_BASE=TRUE
  - =PP1V5_S3_P1V5S0FET — 67D3
  - =PP1V5_S3_MEM_A — 26D7
  - =PP1V5_S3_MEM_B — 27D7
  - =PP1V5_S3_MEMRESET — 28C6
  - =PP1V5_S3_HDD — 37B8

67D6 =PP3V3_S3_FET
- PP3V3_S3 — 6B5 6D3
  MIN_LINE_WIDTH=0.6 mm
  MIN_NECK_WIDTH=0.2 mm
  VOLTAGE=3.3V
  MAKE_BASE=TRUE
  - =PP3V3_S3_SMBUS_SMC_A_S3 — 43D3
  - =PP3V3_S3_PDCISENS — 61B3
  - =PP3V3_S3_SMBUS_SMC_MGMT — 43B5
  - =PP3V3_S3_VREFMRGN — 25D8
  - =PP3V3_S3_WLAN — 29A6
  - =PP3V3_S3_MCP_GPIO — 20A3
  - =PP3V3_S3_TPAD — 48A6 48B5 48C5 48D2
  - =PP3V3_S3_SMS — 50B7
  - =PP3V3_S3_CARDREADER — 30D7

60B8 =PP5V_S3_REG
- PP5V_S3 — 6D3
  MIN_LINE_WIDTH=0.6 mm
  MIN_NECK_WIDTH=0.2 mm
  VOLTAGE=5V
  MAKE_BASE=TRUE
  - =PP5V_S3_EXTUSB — 38C7
  - =PP5V_S3_IR — 37A8 39D7
  - =PP5V_S3_BTCAMERA — 29C3
  - =PP5V_S3_VTTCLAMP — 67A3
  - =PP5V_S3_MCPDDRFET — 67D4
  - =PP5V_S3_SYSLED — 41B8
  - =PP5V_S3_TPAD — 49B6 49D7
  - =PP5V_S3_WLAN — 29C1
  - =PP5V_S3_1V5S30V75S0 — 61C5
  - =PP5V_S3_AUDIO — 52A8 52D2 54D5 56B6
  - =PP5V_S3_AUDIO_AMP — 55B7 55C7 55D7
  - =PP5V_S3_P5VS0FET — 67B8
  - =PP5V_S3_ODD — 37D5

61D8 25D9 =PPVTT_S3_DDR_BUF
- PPVTT_S3_DDR_BUF
  MIN_LINE_WIDTH=0.3 MM
  MIN_NECK_WIDTH=0.2 MM
  VOLTAGE=0.75V
  MAKE_BASE=TRUE

"S5" RAILS

65A5 =PP1V05_S5_REG
- PP1V1R1V05_S5 — 6D3
  MIN_LINE_WIDTH=0.6 MM
  MIN_NECK_WIDTH=0.2 MM
  VOLTAGE=1.05V
  MAKE_BASE=TRUE
  - =PP1V05_S5_MCP_VDD_AUXC — 21A3 22D8
  - =PP1V05_ENET_P1V05ENETFET — 32C4

60B1 =PP3V3_S5_REG
- PP3V3_S5 — 6D3
  MIN_LINE_WIDTH=0.6 mm
  MIN_NECK_WIDTH=0.2 mm
  VOLTAGE=3.3V
  MAKE_BASE=TRUE
  - =PP3V3_S5_MCP_GPIO — 17C7 19C1
  - =PP3V3_S5_ROM — 42B5 42C7 51C6
  - =PP3V3_S5_LCD — 68C8
  - =PP3V3_S5_MCP — 21B3 22B8
  - =PP3V3_S5_MCPPWRGD — 24B8
  - =PP3V3_S5_PWRCTL — 66B3
  - =PP3V3_S5_P1V05ENETFET — 32C5
  - =PP3V3_S5_P3V3S3FET — 67D8
  - =PP3V3_S5_P3V3S0FET — 67C8
  - =PP3V3_S5_P1V05S5 — 65B8
  - =PP3V3_S5_MEMRESET — 28C4
  - =PP3V3_S5_P3V3ENETFET — 32D5
  - =PP3V3_S5_DP_PORT_PWR — 70D8
  - =PP3V3_FW_LATEVG — 36A7
  - =PP3V3_FW_LATEVG_ACTIVE — 35A8
  - =PP3V3_S5_P1V05FWFET — 35C7

"G3H" RAILS

58B4 =PP3V42_G3H_REG
- PP3V42_G3H — 6A7 6B5 6D3
  MIN_LINE_WIDTH=0.6 MM
  MIN_NECK_WIDTH=0.2 MM
  VOLTAGE=3.42V
  MAKE_BASE=TRUE
  - =PPVIN_S5_SMCVREF — 41C8
  - =PP3V42_G3H_SMBUS_SMC_BSA — 43C5
  - =PP3V42_G3H_PWRCTL — 66B3 66C8 66D8
  - =PP3V42_G3H_CHGR — 59A8 59C6 59D5
  - =PP3V42_G3H_SMCUSBMUX — 38B8
  - =PP3V42_G3H_TPAD — 48B5 48C2 48C3 48C6
  - =PP3V42_G3H_BATT — 58C2 58C4
  - =PP3V3_S5_SMC — 40D4 41C1 41C3 41C7 41D8
  - =PP3V3_S5_LPCPLUS — 42C7 42C8 42D5
  - =PP3V42_G3H_RTC_D — 24D8
  - =PP3V42_G3H_BMON_ISNS — 45B8
  - =PP3V42_G3H_ONEWIRE — 58D2
  - =PP3V42_G3H_AUDIO — 66B6

58D1 58C8 =PP18V5_DCIN_CONN
- PP18V5_G3H — 6C3
  MIN_LINE_WIDTH=0.6 MM
  MIN_NECK_WIDTH=0.3 MM
  VOLTAGE=18.5V
  MAKE_BASE=TRUE
  - =PP18V5_G3H_CHGR — 59D8

59C1 =PPBUS_G3H
- PPBUS_G3H — 6C3
  MIN_LINE_WIDTH=0.6 MM
  MIN_NECK_WIDTH=0.3 MM
  VOLTAGE=12.6V
  MAKE_BASE=TRUE
  - =PPBUS_S0_LCDBKLT — 72D8
  - =PPVIN_S0_MCPCORE — 63D5
  - =PPVIN_S5_1V5S30V75S0 — 61C2
  - =PPVIN_S5_3V3S5 — 60C3
  - =PPVIN_S3_5VS3 — 60C6 60C7
  - =PPBUS_G3HRS5 — 44B8
  - =PPBUS_S5_FWPWRSW — 35B7
  - =PPCPUVCORE_VTT_ISNS_R — 45B8
  (BEFORE HIGH SIDE SENSING RES.)

45B7 =PPCPUVCORE_VTT_ISNS (AFTER HIGH SIDE CPU VCORE & CPU VTT SENSING RES.)
- PPBUS_G3H_CPU_ISNS — 6C3
  MIN_LINE_WIDTH=0.6 mm
  MIN_NECK_WIDTH=0.3 MM
  VOLTAGE=12.6V
  MAKE_BASE=TRUE
  - =PPVIN_S0_CPUVTTS0 — 64C6
  - =PPVIN_S5_CPU_IMVP — 62C3 62D4 62D8

"FIREWIRE" RAILS

35D4 =PP3V3_FW_FET
- PP3V3_FW — 6C3
  MIN_LINE_WIDTH=0.6 MM
  MIN_NECK_WIDTH=0.2 MM
  VOLTAGE=3.3V
  MAKE_BASE=TRUE
  - =PP3V3_FW_FWPHY — 34D5 34D6 34D8 34B1 34D2
  - =PP3V3_S0_P1V05FWFET — 35C7

35B1 =PPBUS_S5_FW_FET
- PPVP_FW — 6C3
  MIN_LINE_WIDTH=0.4 MM
  MIN_NECK_WIDTH=0.2 MM
  VOLTAGE=12.6V
  MAKE_BASE=TRUE
  - =PPVP_FW_PORT1 — 36C3
  - =PPVP_FW_PHY_CPS_FET — 36C6

35C5 =PP1V0_FW_FET
- PP1V05_FW — 6C3
  MIN_LINE_WIDTH=0.6 MM
  MIN_NECK_WIDTH=0.2 MM
  VOLTAGE=1.05V
  MAKE_BASE=TRUE
  - =PP1V0_FW_FWPHY — 34D6 35D3

SYNC_MASTER=BEN SYNC_DATE=04/21/2008

PAGE TITLE
Power Aliases

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D
REVISION C.0.0
BRANCH
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SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

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HEATSINK STANDOFFS

Z0902
STDOFF-4.50D.98H-1.1-3.48-TH
LEFT OF CPU

Z0901
STDOFF-4.50D.98H-1.1-3.48-TH
ABOVE CPU

Z0903
STDOFF-4.50D.98H-1.1-3.48-TH
BELOW MCP

Z0904
STDOFF-4.50D.98H-1.1-3.48-TH
BELOW CPU

FAN STANDOFF

Z0905
STDOFF-4.50D.98H-1.1-3.48-TH
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=0V

MLB MOUNTING (TO C. BRACKET) SCREW HOLES

Z0906 OMIT 3R2P5
Z0907 OMIT 3R2P5

MLB MOUNTING (TO TOPCASE) SCREW HOLES

Z0908 OMIT 3R2P5
Z0909 OMIT 3R2P5
Z0910 OMIT 3R2P5
Z0911 OMIT 3R2P5
Z0912 OMIT 3R2P5

PCI-E ALIASES

UNUSED GPU LANES

16D6 16C6	=PEG_D2R_N<15:0>	NC_PEG_D2R_N<15:0>	NO_TEST=TRUE MAKE_BASE=TRUE
16D6 16C6	=PEG_D2R_P<15:0>	NC_PEG_D2R_P<15:0>	NO_TEST=TRUE MAKE_BASE=TRUE
16D3 16C3	=PEG_R2D_C_N<15:0>	NC_PEG_R2D_C_N<15:0>	NO_TEST=TRUE MAKE_BASE=TRUE
16D3 16C3	=PEG_R2D_C_P<15:0>	NC_PEG_R2D_C_P<15:0>	NO_TEST=TRUE MAKE_BASE=TRUE
16C6	PEG_PRSNT_L	TP_PEG_PRSNT_L	MAKE_BASE=TRUE
16C3	PEG_CLK100M_P	TP_PEG_CLK100M_P	MAKE_BASE=TRUE
16C3	PEG_CLK100M_N	TP_PEG_CLK100M_N	MAKE_BASE=TRUE

UNUSED EXPRESS CARD LANE

16B6	PCIE_EXCARD_D2R_P	TP_PCIE_EXCARD_D2R_P	MAKE_BASE=TRUE
16B6	PCIE_EXCARD_D2R_N	TP_PCIE_EXCARD_D2R_N	MAKE_BASE=TRUE
16B3	PCIE_EXCARD_R2D_C_P	TP_PCIE_EXCARD_R2D_C_P	MAKE_BASE=TRUE
16B3	PCIE_EXCARD_R2D_C_N	TP_PCIE_EXCARD_R2D_C_N	MAKE_BASE=TRUE
16C6	PCIE_EXCARD_PRSNT_L	TP_PCIE_EXCARD_PRSNT_L	MAKE_BASE=TRUE
16C6	EXCARD_CLKREQ_L	TP_EXCARD_CLKREQ_L	MAKE_BASE=TRUE
16C3	PCIE_CLK100M_EXCARD_P	TP_PCIE_CLK100M_EXCARD_P	MAKE_BASE=TRUE
16C3	PCIE_CLK100M_EXCARD_N	TP_PCIE_CLK100M_EXCARD_N	MAKE_BASE=TRUE

FIREWIRE PRESENT SIGNALS

35D3 16C6 PCIE_FW_PRSNT_L — R0950 0 5% 1/16W MF-LF 402 — NOSTUFF

USB ALIASES

UNUSED USB PORTS

19C3	USB_EXTC_P	TP_USB_EXTC_P	MAKE_BASE=TRUE
19C3	USB_EXTC_N	TP_USB_EXTC_N	MAKE_BASE=TRUE
19D3	USB_EXTD_P	TP_USB_EXTD_P	MAKE_BASE=TRUE
19D3	USB_EXTD_N	TP_USB_EXTD_N	MAKE_BASE=TRUE
19C3	USB_EXCARD_P	TP_USB_EXCARD_P	MAKE_BASE=TRUE
19C3	USB_EXCARD_N	TP_USB_EXCARD_N	MAKE_BASE=TRUE
19D3	USB_MINI_P	TP_USB_MINI_P	MAKE_BASE=TRUE
19D3	USB_MINI_N	TP_USB_MINI_N	MAKE_BASE=TRUE

DACS ALIASES

UNUSED CRT & TV-OUT INTERFACE

17C6	MCP_TV_DAC_RSET	NC_MCP_TV_DAC_RSET	NO_TEST=TRUE MAKE_BASE=TRUE
17C6	MCP_TV_DAC_VREF	NC_MCP_TV_DAC_VREF	NO_TEST=TRUE MAKE_BASE=TRUE
17C6	MCP_CLK27M_XTALIN	NC_MCP_CLK27M_XTALIN	NO_TEST=TRUE MAKE_BASE=TRUE
17C6	MCP_CLK27M_XTALOUT	NC_MCP_CLK27M_XTALOUT	NO_TEST=TRUE MAKE_BASE=TRUE
17C3	CRT_IG_R_C_PR	NC_CRT_IG_R_C_PR	NO_TEST=TRUE MAKE_BASE=TRUE
17C3	CRT_IG_G_Y_Y	NC_CRT_IG_G_Y_Y	NO_TEST=TRUE MAKE_BASE=TRUE
17C3	CRT_IG_B_COMP_PB	NC_CRT_IG_B_COMP_PB	NO_TEST=TRUE MAKE_BASE=TRUE
17C3	CRT_IG_HSYNC	NC_CRT_IG_HSYNC	NO_TEST=TRUE MAKE_BASE=TRUE
17C3	CRT_IG_VSYNC	NC_CRT_IG_VSYNC	NO_TEST=TRUE MAKE_BASE=TRUE

LVDS ALIASES

UNUSED LVDS SIGNALS

17B3	LVDS_IG_A_DATA_P<3>	NC_LVDS_IG_A_DATA_P3	NO_TEST=TRUE MAKE_BASE=TRUE
17B3	LVDS_IG_A_DATA_N<3>	NC_LVDS_IG_A_DATA_N3	NO_TEST=TRUE MAKE_BASE=TRUE
17B3	LVDS_IG_B_CLK_P	NC_LVDS_IG_B_CLK_P	NO_TEST=TRUE MAKE_BASE=TRUE
17B3	LVDS_IG_B_CLK_N	NC_LVDS_IG_B_CLK_N	NO_TEST=TRUE MAKE_BASE=TRUE
17B3	LVDS_IG_B_DATA_P<3:0>	NC_LVDS_IG_B_DATA_P<3:0>	NO_TEST=TRUE MAKE_BASE=TRUE
17B3	LVDS_IG_B_DATA_N<3:0>	NC_LVDS_IG_B_DATA_N<3:0>	NO_TEST=TRUE MAKE_BASE=TRUE

MISC MCP79 ALIASES

13B6	CPU_PECI_MCP	TP_CPU_PECI_MCP	MAKE_BASE=TRUE
16B6	GMUX_JTAG_TCK_L	TP_GMUX_JTAG_TCK_L	MAKE_BASE=TRUE
16B6	GMUX_JTAG_TDO	TP_GMUX_JTAG_TDO	MAKE_BASE=TRUE
18D4	GMUX_JTAG_TDI	TP_GMUX_JTAG_TDI	MAKE_BASE=TRUE
18D4	GMUX_JTAG_TMS	TP_GMUX_JTAG_TMS	MAKE_BASE=TRUE

LAN ALIASES

17D6 =MCP_MII_RXER — MCP_MII_PD (MAKE_BASE=TRUE)
17D6 =MCP_MII_COL
17D6 =MCP_MII_CRS
R0930 47K 5% 1/16W MF-LF 402

DP HOTPLUG PULL-DOWN

17B6 =DVI_HPD_GMUX_INT — HPLUG_DET2 (MAKE_BASE=TRUE)
R0940 20K 5% 1/16W MF-LF 402

SO-DIMM ALIASES

UNUSED ADDRESS PINS

26D5	MEM_A_A<15>	TP_MEM_A_A15	MAKE_BASE=TRUE
27D5	MEM_B_A<15>	TP_MEM_B_A15	MAKE_BASE=TRUE

ETHERNET ALIASES

32C5	=P3V3ENET_EN	PM_SLP_RMGT_L (29C3)	MAKE_BASE=TRUE
32B5	=P1V05ENET_EN		
31C2	=PP3V3_ENET_PHY_VDDREG	TP_PP3V3_ENET_PHY_VDDREG	MAKE_BASE=TRUE
31C2	=RTL8211_REGOUT	NC_RTL8211_REGOUT	MAKE_BASE=TRUE
31C6	=RTL8211_ENSWREG		MAKE_BASE=TRUE
31B6	TP_RTL8211_CLK125		

R0931 22 5% 1/16W MF-LF 402

FW ALIASES

18B7	FW_PME_L	FW_PLUG_DET_L (35B1 35D7)	MAKE_BASE=TRUE
35C8 34B2	=FW_PME_L	FW643_WAKE_L	MAKE_BASE=TRUE

CPU FSB FREQUENCY STRAPS

73C3 9B4 IN CPU_BSEL<0:2> MAKE_BASE=TRUE — =MCP_BSEL<0:2> OUT 13A7

BSEL<2..0>	FSB MHZ
0 0 0	266
0 0 1	133
0 1 0	200
0 1 1	(166)
1 0 0	333
1 0 1	100
1 1 0	(400)
1 1 1	(RSVD)

EMI IO POGO PINS

ZS0900	1.4DIA-SHORT-EMI-MLB-M97-M98	SM OMIT
ZS0901	1.4DIA-SHORT-EMI-MLB-M97-M98	SM OMIT
ZS0902	1.4DIA-SHORT-EMI-MLB-M97-M98	SM OMIT
ZS0903	1.4DIA-SHORT-EMI-MLB-M97-M98	SM OMIT
ZS0908	1.4DIA-SHORT-EMI-MLB-M97-M98	SM OMIT
ZS0909	1.4DIA-SHORT-EMI-MLB-M97-M98	SM OMIT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
870-1801	6	POGO PIN,SHORT,EMI,MLB,K19/K24	ZS0900,ZS0901,ZS0902,ZS0903,ZS0908,ZS0909	CRITICAL	

EMI POGO PINS

ZS0904	2.0DIA-TALL-EMI-MLB-M97-M98	SM
ZS0905	2.0DIA-TALL-EMI-MLB-M97-M98	SM
ZS0906	2.0DIA-TALL-EMI-MLB-M97-M98	SM
ZS0907	2.0DIA-TALL-EMI-MLB-M97-M98	SM

SYNC_MASTER=M97_MLB
PAGE TITLE: SIGNAL ALIAS

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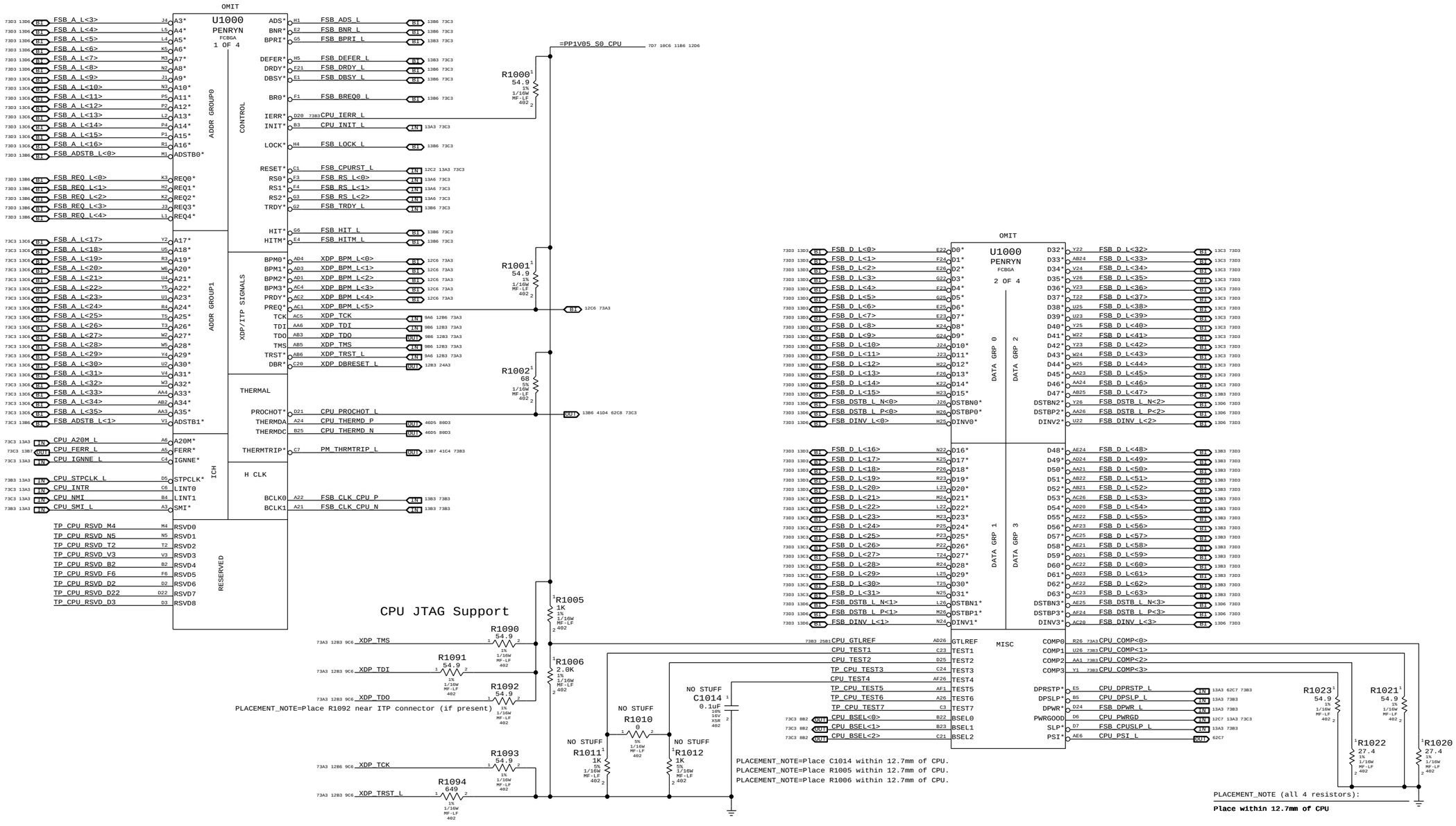

SYNC FROM T18
CHANGE CPU FROM SOCKET TO BGA SYMBOL

SYNC_MASTER=T18_MLB SYNC_DATE=12/12/2007

PAGE TITLE: CPU FSB

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DRAWING NUMBER: 051-7898 SIZE: D
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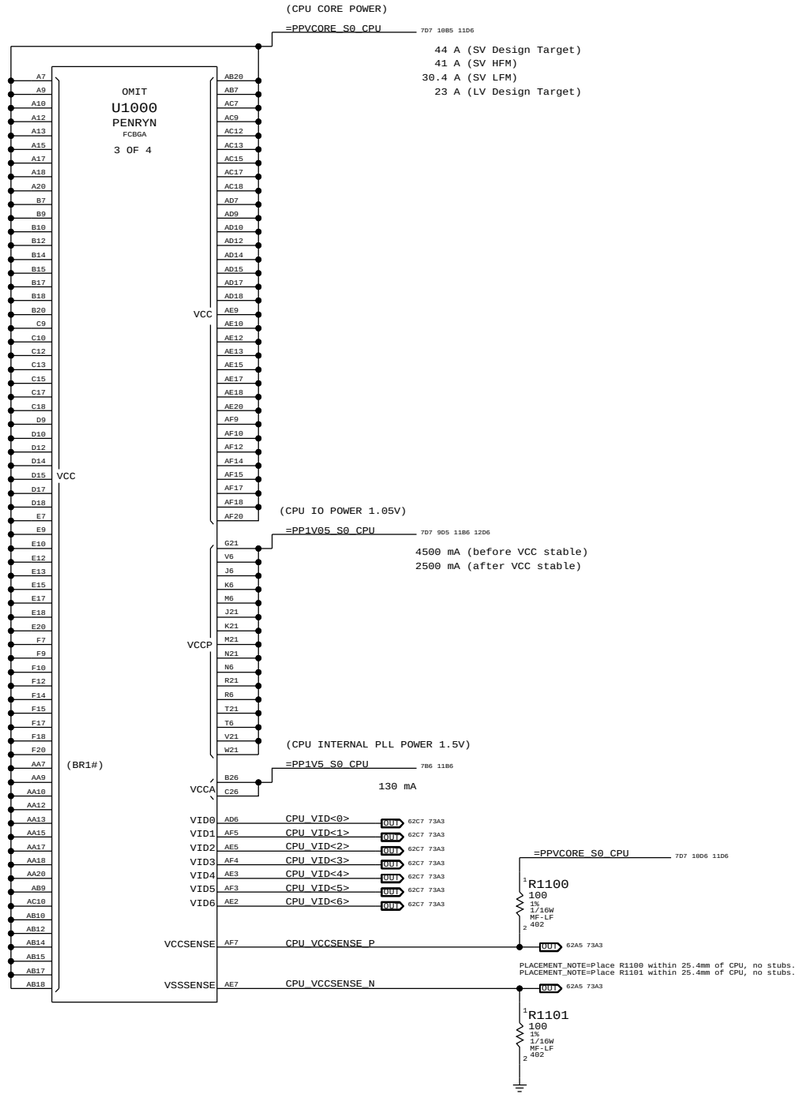

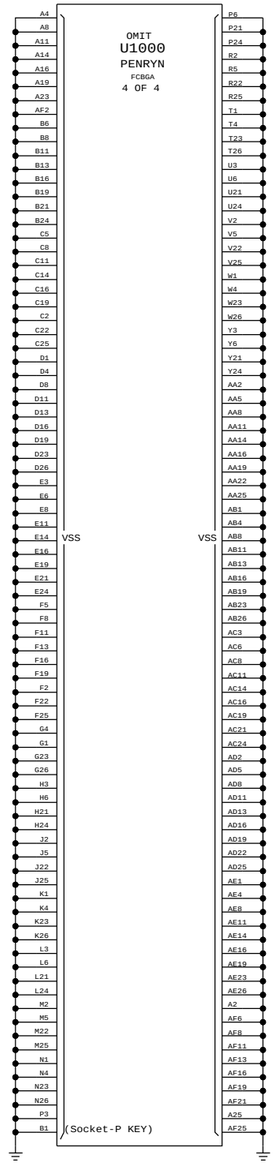

SYNC FROM T18
CHANGE CPU FROM SOCKET TO BGA SYMBOL

Current numbers from Merom for Santa Rosa EMTS, doc #20905.

SYNC MASTER=T18_MLB SYNC DATE=12/12/2007

PAGE TITLE
CPU Power & Ground

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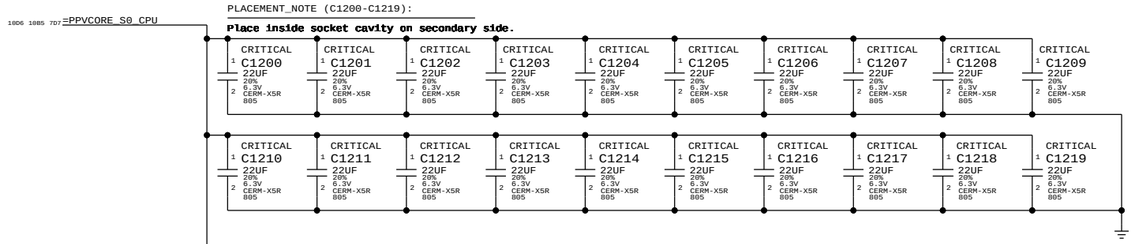
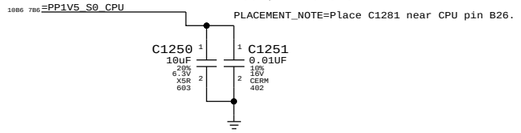
CPU VCore HF and Bulk Decoupling

4X 330UF. 20X 22UF 0805



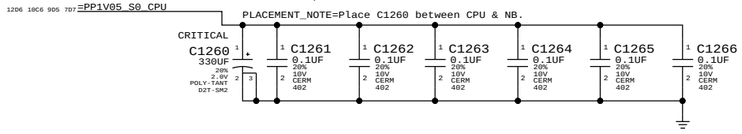
VCCA (CPU AVdd) DECOUPLING

1x 10uF, 1x 0.01uF



VCCP (CPU I/O) DECOUPLING

1x 330uF, 6x 0.1uF 0402



SYNC FROM T18
REMOVE NO STUFF CAPS C1220 TO C1231
REMOVE C1244 & C1245
CHANGE C1240-C1243 AND C1260 FROM 128S0241(9 MILLI-OHM) TO 128S0231(6 MILLI-OHM)

SYNC_MASTER=RAYMOND SYNC_DATE=03/31/2008

PAGE TITLE: CPU Decoupling

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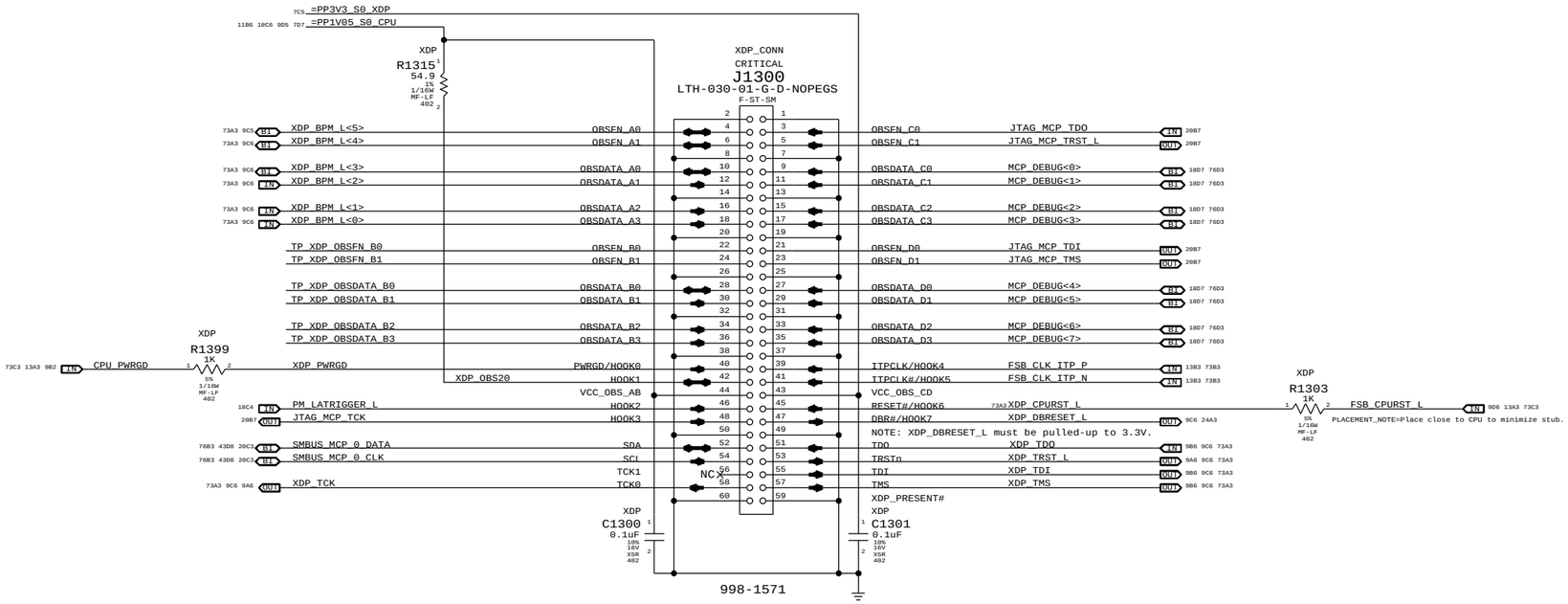
Mini-XDP Connector

NOTE: This is not the standard XDP pinout.

Use with 920-0620 adapter board to support CPU, MCP debugging.

MCP79-specific pinout



Direction of XDP module

Please avoid any obstructions
on even-numbered side of J1300

SYNC_MASTER=K19_MLB SYNC_DATE=11/07/2008

PAGE TITLE
eXtended Debug Port(MiniXDP)

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OMIT

U1400
MCP79-TOPO-B
BGA
(1 OF 11)

FSB

73D3 9C4	IN	FSB_DSTB_L_P<0>	T48	CPU_DSTBP0#	Y43	CPU_D0#	FSB_D_L<0>	IN	9C4 73D3
73D3 9C4	IN	FSB_DSTB_L_N<0>	U48	CPU_DSTBN0#	W42	CPU_D1#	FSB_D_L<1>	IN	9C4 73D3
73D3 9C4	IN	FSB_DINV_L<0>	V41	CPU_DBI0#	Y40	CPU_D2#	FSB_D_L<2>	IN	9C4 73D3
					W41	CPU_D3#	FSB_D_L<3>	IN	9C4 73D3
73D3 9B4	IN	FSB_DSTB_L_P<1>	W39	CPU_DSTBP1#	Y39	CPU_D4#	FSB_D_L<4>	IN	9C4 73D3
73D3 9B4	IN	FSB_DSTB_L_N<1>	W37	CPU_DSTBN1#	V42	CPU_D5#	FSB_D_L<5>	IN	9C4 73D3
73D3 9B4	IN	FSB_DINV_L<1>	V35	CPU_DBI1#	Y41	CPU_D6#	FSB_D_L<6>	IN	9C4 73D3
					Y42	CPU_D7#	FSB_D_L<7>	IN	9C4 73D3
73D3 9C2	IN	FSB_DSTB_L_P<2>	N37	CPU_DSTBP2#	P42	CPU_D8#	FSB_D_L<8>	IN	9C4 73D3
73D3 9C2	IN	FSB_DSTB_L_N<2>	L36	CPU_DSTBN2#	U41	CPU_D9#	FSB_D_L<9>	IN	9C4 73D3
73D3 9C2	IN	FSB_DINV_L<2>	N35	CPU_DBI2#	R42	CPU_D10#	FSB_D_L<10>	IN	9C4 73D3
					T39	CPU_D11#	FSB_D_L<11>	IN	9C4 73D3
73D3 98Z	IN	FSB_DSTB_L_P<3>	M39	CPU_DSTBP3#	T42	CPU_D12#	FSB_D_L<12>	IN	9C4 73D3
73D3 98Z	IN	FSB_DSTB_L_N<3>	M41	CPU_DSTBN3#	T41	CPU_D13#	FSB_D_L<13>	IN	9C4 73D3
73D3 98Z	IN	FSB_DINV_L<3>	J41	CPU_DBI3#	R41	CPU_D14#	FSB_D_L<14>	IN	9C4 73D3
					T43	CPU_D15#	FSB_D_L<15>	IN	9C4 73D3
73D3 90B	IN	FSB_A_L<3>	AC34	CPU_A3#	W35	CPU_D16#	FSB_D_L<16>	IN	9C4 73D3
73D3 90B	IN	FSB_A_L<4>	AE38	CPU_A4#	AA37	CPU_D17#	FSB_D_L<17>	IN	9C4 73D3
73D3 90B	IN	FSB_A_L<5>	AE34	CPU_A5#	W33	CPU_D18#	FSB_D_L<18>	IN	9C4 73D3
73D3 90B	IN	FSB_A_L<6>	AC37	CPU_A6#	W34	CPU_D19#	FSB_D_L<19>	IN	9C4 73D3
73D3 90B	IN	FSB_A_L<7>	AE37	CPU_A7#	AA36	CPU_D20#	FSB_D_L<20>	IN	9C4 73D3
73D3 90B	IN	FSB_A_L<8>	AE35	CPU_A8#	AA34	CPU_D21#	FSB_D_L<21>	IN	9B4 73D3
73D3 90B	IN	FSB_A_L<9>	AB35	CPU_A9#	AA38	CPU_D22#	FSB_D_L<22>	IN	9B4 73D3
73D3 90B	IN	FSB_A_L<10>	AF36	CPU_A10#	AA35	CPU_D23#	FSB_D_L<23>	IN	9B4 73D3
73D3 90B	IN	FSB_A_L<11>	AG35	CPU_A11#	U38	CPU_D24#	FSB_D_L<24>	IN	9B4 73D3
73D3 90B	IN	FSB_A_L<12>	AG39	CPU_A12#	U36	CPU_D25#	FSB_D_L<25>	IN	9B4 73D3
73D3 90B	IN	FSB_A_L<13>	AE33	CPU_A13#	U35	CPU_D26#	FSB_D_L<26>	IN	9B4 73D3
73D3 90B	IN	FSB_A_L<14>	AG37	CPU_A14#	U33	CPU_D27#	FSB_D_L<27>	IN	9B4 73D3
73D3 90B	IN	FSB_A_L<15>	AG38	CPU_A15#	U34	CPU_D28#	FSB_D_L<28>	IN	9B4 73D3
73D3 90B	IN	FSB_A_L<16>	AG34	CPU_A16#	W38	CPU_D29#	FSB_D_L<29>	IN	9B4 73D3
73C3 90B	IN	FSB_A_L<17>	AN38	CPU_A17#	R33	CPU_D30#	FSB_D_L<30>	IN	9B4 73D3
73C3 9CB	IN	FSB_A_L<18>	AL39	CPU_A18#	U37	CPU_D31#	FSB_D_L<31>	IN	9B4 73D3
73C3 9CB	IN	FSB_A_L<19>	AG33	CPU_A19#	N34	CPU_D32#	FSB_D_L<32>	IN	9C2 73D3
73C3 9CB	IN	FSB_A_L<20>	AL33	CPU_A20#	N33	CPU_D33#	FSB_D_L<33>	IN	9C2 73D3
73C3 9CB	IN	FSB_A_L<21>	AJ33	CPU_A21#	R34	CPU_D34#	FSB_D_L<34>	IN	9C2 73D3
73C3 9CB	IN	FSB_A_L<22>	AN36	CPU_A22#	R35	CPU_D35#	FSB_D_L<35>	IN	9C2 73D3
73C3 9CB	IN	FSB_A_L<23>	AJ35	CPU_A23#	P35	CPU_D36#	FSB_D_L<36>	IN	9C2 73D3
73C3 9CB	IN	FSB_A_L<24>	AJ37	CPU_A24#	R39	CPU_D37#	FSB_D_L<37>	IN	9C2 73D3
73C3 9CB	IN	FSB_A_L<25>	AJ36	CPU_A25#	R37	CPU_D38#	FSB_D_L<38>	IN	9C2 73D3
73C3 9CB	IN	FSB_A_L<26>	AJ38	CPU_A26#	R38	CPU_D39#	FSB_D_L<39>	IN	9C2 73D3
73C3 9CB	IN	FSB_A_L<27>	AL37	CPU_A27#	L37	CPU_D40#	FSB_D_L<40>	IN	9C2 73D3
73C3 9CB	IN	FSB_A_L<28>	AL34	CPU_A28#	L39	CPU_D41#	FSB_D_L<41>	IN	9C2 73D3
73C3 9CB	IN	FSB_A_L<29>	AN37	CPU_A29#	L38	CPU_D42#	FSB_D_L<42>	IN	9C2 73D3
73C3 9CB	IN	FSB_A_L<30>	AJ34	CPU_A30#	N36	CPU_D43#	FSB_D_L<43>	IN	9C2 73D3
73C3 9CB	IN	FSB_A_L<31>	AL38	CPU_A31#	N38	CPU_D44#	FSB_D_L<44>	IN	9C2 73D3
73C3 9CB	IN	FSB_A_L<32>	AL35	CPU_A32#	J39	CPU_D45#	FSB_D_L<45>	IN	9C2 73D3
73C3 9CB	IN	FSB_A_L<33>	AN34	CPU_A33#	J38	CPU_D46#	FSB_D_L<46>	IN	9C2 73D3
73C3 9CB	IN	FSB_A_L<34>	AR39	CPU_A34#	J37	CPU_D47#	FSB_D_L<47>	IN	9C2 73D3
73C3 9CB	IN	FSB_A_L<35>	AN35	CPU_A35#	L42	CPU_D48#	FSB_D_L<48>	IN	9C2 73D3
					M42	CPU_D49#	FSB_D_L<49>	IN	9C2 73D3
73D3 90B	IN	FSB_ADSTB_L<0>	AE36	CPU_ADSTB0#	P41	CPU_D50#	FSB_D_L<50>	IN	9C2 73D3
73C3 9CB	IN	FSB_ADSTB_L<1>	AK35	CPU_ADSTB1#	N41	CPU_D51#	FSB_D_L<51>	IN	9C2 73D3
					N40	CPU_D52#	FSB_D_L<52>	IN	9C2 73D3
73D3 90B	IN	FSB_REQ_L<0>	AC38	CPU_REQ0#	M40	CPU_D53#	FSB_D_L<53>	IN	9B4 73D3
73D3 90B	IN	FSB_REQ_L<1>	AA33	CPU_REQ1#	H40	CPU_D54#	FSB_D_L<54>	IN	9B4 73D3
73D3 90B	IN	FSB_REQ_L<2>	AC39	CPU_REQ2#	K42	CPU_D55#	FSB_D_L<55>	IN	9B4 73D3
73D3 90B	IN	FSB_REQ_L<3>	AC33	CPU_REQ3#	H41	CPU_D56#	FSB_D_L<56>	IN	9B4 73D3
73D3 90B	IN	FSB_REQ_L<4>	AC35	CPU_REQ4#	L41	CPU_D57#	FSB_D_L<57>	IN	9B4 73D3
					H43	CPU_D58#	FSB_D_L<58>	IN	9B4 73D3
73C3 906	IN	FSB_ADS_L	AD42	CPU_ADS#	H42	CPU_D59#	FSB_D_L<59>	IN	9B4 73D3
73C3 906	IN	FSB_BNR_L	AD43	CPU_BNR#	K41	CPU_D60#	FSB_D_L<60>	IN	9B4 73D3
73C3 906	IN	FSB_BREQ0_L	AE40	CPU_BR0#	J40	CPU_D61#	FSB_D_L<61>	IN	9B4 73D3
73C3		FSB_BREQ1_L	AL32	CPU_BR1#	H39	CPU_D62#	FSB_D_L<62>	IN	9B4 73D3
73C3 906	IN	FSB_DBSY_L	AD39	CPU_DBSY#	M43	CPU_D63#	FSB_D_L<63>	IN	9B4 73D3
73C3 906	IN	FSB_DRDY_L	AD41	CPU_DRDY#					
73C3 906	IN	FSB_HIT_L	AB42	CPU_HIT#	AA41	CPU_BPRI#	FSB_BPRI_L	OUT	9D6 73C3
73C3 906	IN	FSB_HITM_L	AD40	CPU_HITM#	AA40	CPU_DEFER#	FSB_DEFER_L	OUT	9D6 73C3
73C3 906	IN	FSB_LOCK_L	AC43	CPU_LOCK#					
73C3 906	OUT	FSB_TRDY_L	AE41	CPU_TRDY#					
					G42	BCLK_OUT_CPU_P	FSB_CLK_CPU_P	OUT	9B6 73B3
8C4	OUT	CPU_PECI_MCP	E41	CPU_PECI	G41	BCLK_OUT_CPU_N	FSB_CLK_CPU_N	OUT	9B6 73B3
73C3 62C8 41D4 9C5	OUT	CPU_PROCHOT_L	AJ41	CPU_PROCHOT#					
			AG43	CPU_THERMTRIP#	AL43	BCLK_OUT_ITP_P	FSB_CLK_ITP_P	OUT	12C3 73B3
			AH40	CPU_FERR#	AL42	BCLK_OUT_ITP_N	FSB_CLK_ITP_N	OUT	12C3 73B3
					AL41	BCLK_OUT_NB_P	FSB_CLK_MCP_P	73B3	
		(MCP_BSEL<2>)	F42	CPU_BSEL2	AK42	BCLK_OUT_NB_N	FSB_CLK_MCP_N	73B3	
		(MCP_BSEL<1>)	D42	CPU_BSEL1					
		(MCP_BSEL<0>)	F41	CPU_BSEL0					
					AK41	BCLK_IN_N			
					AJ40	BCLK_IN_P			
73C3 906	OUT	FSB_RS_L<0>	AC41	CPU_RS0#					
73C3 906	OUT	FSB_RS_L<1>	AB41	CPU_RS1#					
73C3 906	OUT	FSB_RS_L<2>	AC42	CPU_RS2#					
					AF41	CPU_A20M#	CPU_A20M_L	OUT	9C8 73C3
22C7	PP1V05_S0_MCP_PLL_FSB				AH39	CPU_IGNNE#	CPU_IGNNE_L	OUT	9C8 73C3
270 mA (A01)					AH42	CPU_INIT#	CPU_INIT_L	OUT	9D6 73C3
206 mA		AG27	+V_DLL_DLCELL_AVDD		AF42	CPU_INTR	CPU_INTR	OUT	9C8 73C3
20 mA		AH27	+V_PLL_MCLK		AG41	CPU_NMI	CPU_NMI	OUT	9B8 73C3
29 mA		AG28	+V_PLL_FSB		AH41	CPU_SMI#	CPU_SMI_L	OUT	9B8 73B3
15 mA		AH28	+V_PLL_CPU						
					AH43	CPU_PWRGD	CPU_PWRGD		
73B3	MCP_BCLK_VML_COMP_VDD	AM39	BCLK_VML_COMP_VDD		H38	CPU_RESET#	FSB_CPURST_L	OUT	9D6 12C2 73C3
73B3	MCP_BCLK_VML_COMP_GND	AM40	BCLK_VML_COMP_GND						
					AM33	CPU_SLP#	FSB_CPUSLP_L	OUT	9B2 73B3
73B3	MCP_CPU_COMP_VCC	AM43	CPU_COMP_VCC		AN33	CPU_DPSLP#	CPU_DPSLP_L	OUT	9B2 73B3
73B3	MCP_CPU_COMP_GND	AM42	CPU_COMP_GND		AM32	CPU_DPWR#	FSB_DPWR_L	OUT	9B2 73B3
					AG42	CPU_STPCLK#	CPU_STPCLK_L	OUT	9C8 73B3
					AN32	CPU_DPRSTP#	CPU_DPRSTP_L	OUT	9B2 62C7 73B3

22C8 21D3 13A2 7D7 =PP1V05_S0_MCP_FSB

R1410 54.9 1% 1/16W MF-LF 402
R1415 62 5% 1/16W MF-LF 402
R1416 62 5% 1/16W MF-LF 402

73B3 41C4 9C6 IN PM_THRMTRIP_L
73C3 9C8 IN CPU_FERR_L

NO STUFF
R1420 1K 5% 1/16W MF-LF 402
R1421 1K 5% 1/16W MF-LF 402
R1422 1K 5% 1/16W MF-LF 402

BB1 IN =MCP_BSEL<2>
BB1 IN =MCP_BSEL<1>
BB1 IN =MCP_BSEL<0>

R1430 49.9 1% 1/16W MF-LF 402
R1435 49.9 1% 1/16W MF-LF 402
R1431 49.9 1% 1/16W MF-LF 402
R1436 49.9 1% 1/16W MF-LF 402

Loop-back clock for delay matching.

=PP1V05_S0_MCP_FSB 7D7 13B7 21D3 22C8

NO STUFF
R1440 150 5% 1/16W MF-LF 402
9B2 12C7 73C3

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

SYNC MASTER=T18 MLB
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MEMORY PARTITION 0

MEM_A_DQ<63>	AL8	MDQ0_63	MDQS0_7_P	AL10	MEM_A_DQS_P<7>	26A5 74C3		
MEM_A_DQ<62>	AL9	MDQ0_62	MDQS0_7_N	AL11	MEM_A_DQS_N<7>	26A5 74C3		
MEM_A_DQ<61>	AP9	MDQ0_61	MDQS0_6_P	AR8	MEM_A_DQS_P<6>	26B7 74C3		
MEM_A_DQ<60>	AN9	MDQ0_60	MDQS0_6_N	AR9	MEM_A_DQS_N<6>	26B7 74C3		
MEM_A_DQ<59>	AL6	MDQ0_59	MDQS0_5_P	AW7	MEM_A_DQS_P<5>	26B5 74C3		
MEM_A_DQ<58>	AL7	MDQ0_58	MDQS0_5_N	AW8	MEM_A_DQS_N<5>	26B5 74C3		
MEM_A_DQ<57>	AN6	MDQ0_57	MDQS0_4_P	AP13	MEM_A_DQS_P<4>	26B7 74C3		
MEM_A_DQ<56>	AN7	MDQ0_56	MDQS0_4_N	AR13	MEM_A_DQS_N<4>	26B7 74C3		
MEM_A_DQ<55>	AR6	MDQ0_55	MDQS0_3_P	AV25	MEM_A_DQS_P<3>	26C4 74C3		
MEM_A_DQ<54>	AR7	MDQ0_54	MDQS0_3_N	AW25	MEM_A_DQS_N<3>	26C4 74C3		
MEM_A_DQ<53>	AV6	MDQ0_53	MDQS0_2_P	AU30	MEM_A_DQS_P<2>	26B2 74C3		
MEM_A_DQ<52>	AW5	MDQ0_52	MDQS0_2_N	AU29	MEM_A_DQS_N<2>	26C2 74C3		
MEM_A_DQ<51>	AN10	MDQ0_51	MDQS0_1_P	AT35	MEM_A_DQS_P<1>	26C4 74C3		
MEM_A_DQ<50>	AR5	MDQ0_50	MDQS0_1_N	AU35	MEM_A_DQS_N<1>	26C4 74C3		
MEM_A_DQ<49>	AU6	MDQ0_49	MDQS0_0_P	AU39	MEM_A_DQS_P<0>	26C2 74C3		
MEM_A_DQ<48>	AV5	MDQ0_48	MDQS0_0_N	AT39	MEM_A_DQS_N<0>	26D2 74C3		
MEM_A_DQ<47>	AU7	MDQ0_47						
MEM_A_DQ<46>	AU8	MDQ0_46						
MEM_A_DQ<45>	AW9	MDQ0_45						
MEM_A_DQ<44>	AP11	MDQ0_44						
MEM_A_DQ<43>	AW6	MDQ0_43						
MEM_A_DQ<42>	AY5	MDQ0_42	MRAS0#	AV17	MEM_A_RAS_L	OUT	26C5 74D3	
MEM_A_DQ<41>	AU9	MDQ0_41	MCAS0#	AP17	MEM_A_CAS_L	OUT	26C7 74D3	
MEM_A_DQ<40>	AV9	MDQ0_40	MWE0#	AR17	MEM_A_WE_L	OUT	26C7 74D3	
MEM_A_DQ<39>	AU11	MDQ0_39						
MEM_A_DQ<38>	AV11	MDQ0_38						
MEM_A_DQ<37>	AV13	MDQ0_37						
MEM_A_DQ<36>	AW13	MDQ0_36						
MEM_A_DQ<35>	AR11	MDQ0_35						
MEM_A_DQ<34>	AT11	MDQ0_34	MBA0_2	AP23	MEM_A_BA<2>	OUT	26C7 74D3	
MEM_A_DQ<33>	AR14	MDQ0_33	MBA0_1	AP19	MEM_A_BA<1>	OUT	26C5 74D3	
MEM_A_DQ<32>	AU13	MDQ0_32	MBA0_0	AW17	MEM_A_BA<0>	OUT	26C7 74D3	
MEM_A_DQ<31>	AR26	MDQ0_31						
MEM_A_DQ<30>	AU25	MDQ0_30						
MEM_A_DQ<29>	AT27	MDQ0_29						
MEM_A_DQ<28>	AU27	MDQ0_28						
MEM_A_DQ<27>	AP25	MDQ0_27	MA0_14	AR23	MEM_A_A<14>	OUT	26C5 74D3	
MEM_A_DQ<26>	AR25	MDQ0_26	MA0_13	AU15	MEM_A_A<13>	OUT	26C7 74D3	
MEM_A_DQ<25>	AP27	MDQ0_25	MA0_12	AN23	MEM_A_A<12>	OUT	26C7 74D3	
MEM_A_DQ<24>	AR27	MDQ0_24	MA0_11	AW21	MEM_A_A<11>	OUT	26C5 74D3	
MEM_A_DQ<23>	AP29	MDQ0_23	MA0_10	AN19	MEM_A_A<10>	OUT	26C7 74D3	
MEM_A_DQ<22>	AR29	MDQ0_22	MA0_9	AV21	MEM_A_A<9>	OUT	26C7 74D3	
MEM_A_DQ<21>	AP31	MDQ0_21	MA0_8	AR22	MEM_A_A<8>	OUT	26C7 74D3	
MEM_A_DQ<20>	AR31	MDQ0_20	MA0_7	AU21	MEM_A_A<7>	OUT	26C5 74D3	
MEM_A_DQ<19>	AV27	MDQ0_19	MA0_6	AP21	MEM_A_A<6>	OUT	26C5 74D3	
MEM_A_DQ<18>	AN29	MDQ0_18	MA0_5	AR21	MEM_A_A<5>	OUT	26C7 74D3	
MEM_A_DQ<17>	AV29	MDQ0_17	MA0_4	AN21	MEM_A_A<4>	OUT	26C5 74D3	
MEM_A_DQ<16>	AN31	MDQ0_16	MA0_3	AV19	MEM_A_A<3>	OUT	26C7 74D3	
MEM_A_DQ<15>	AU31	MDQ0_15	MA0_2	AU19	MEM_A_A<2>	OUT	26C5 74D3	
MEM_A_DQ<14>	AR33	MDQ0_14	MA0_1	AT19	MEM_A_A<1>	OUT	26C7 74D3	
MEM_A_DQ<13>	AV37	MDQ0_13	MA0_0	AR19	MEM_A_A<0>	OUT	26C5 74D3	
MEM_A_DQ<12>	AW37	MDQ0_12						
MEM_A_DQ<11>	AT31	MDQ0_11						
MEM_A_DQ<10>	AV31	MDQ0_10						
MEM_A_DQ<9>	AT37	MDQ0_9						
MEM_A_DQ<8>	AU37	MDQ0_8						
MEM_A_DQ<7>	AW39	MDQ0_7						
MEM_A_DQ<6>	AV39	MDQ0_6						
MEM_A_DQ<5>	AR37	MDQ0_5						
MEM_A_DQ<4>	AR38	MDQ0_4						
MEM_A_DQ<3>	AV38	MDQ0_3						
MEM_A_DQ<2>	AW38	MDQ0_2						
MEM_A_DQ<1>	AR35	MDQ0_1						
MEM_A_DQ<0>	AP35	MDQ0_0						
MEM_A_DM<7>	AN5	MDQM0_7						
MEM_A_DM<6>	AU5	MDQM0_6						
MEM_A_DM<5>	AR10	MDQM0_5						
MEM_A_DM<4>	AN13	MDQM0_4						
MEM_A_DM<3>	AN27	MDQM0_3						
MEM_A_DM<2>	AW29	MDQM0_2						
MEM_A_DM<1>	AV35	MDQM0_1						
MEM_A_DM<0>	AR34	MDQM0_0						

MEMORY CONTROL 0A

MCLK0A_2_P	AW33	TP_MEM_A_CLK2P			
MCLK0A_2_N	AV33	TP_MEM_A_CLK2N			
MCLK0A_1_P	BA24	MEM_A_CLK_P<1>	OUT	26C5 74D3	
MCLK0A_1_N	AY24	MEM_A_CLK_N<1>	OUT	26C5 74D3	
MCLK0A_0_P	BB20	MEM_A_CLK_P<0>	OUT	26C7 74D3	
MCLK0A_0_N	BC20	MEM_A_CLK_N<0>	OUT	26C7 74D3	
MCS0A_1#	AT15	MEM_A_CS_L<1>	OUT	26C7 74D3	
MCS0A_0#	AR18	MEM_A_CS_L<0>	OUT	26C5 74D3	
MODT0A_1	AP15	MEM_A_ODT<1>	OUT	26C5 74D3	
MODT0A_0	AV15	MEM_A_ODT<0>	OUT	26C5 74D3	
MCKE0A_1	AU23	MEM_A_CKE<1>	OUT	26D5 74D3	
MCKE0A_0	AT23	MEM_A_CKE<0>	OUT	26D7 74D3	

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MEMORY PARTITION 1

MEM_B_DQ<63>	AT4	MDQ1_63	MDQS1_7_P	AT2	MEM_B_DQS_P<7>	27A5 74A3		
MEM_B_DQ<62>	AT3	MDQ1_62	MDQS1_7_N	AT1	MEM_B_DQS_N<7>	27A5 74A3		
MEM_B_DQ<61>	AV2	MDQ1_61	MDQS1_6_P	AY2	MEM_B_DQS_P<6>	27B7 74A3		
MEM_B_DQ<60>	AV3	MDQ1_60	MDQS1_6_N	AY1	MEM_B_DQS_N<6>	27B7 74A3		
MEM_B_DQ<59>	AR4	MDQ1_59	MDQS1_5_P	BB6	MEM_B_DQS_P<5>	27B5 74A3		
MEM_B_DQ<58>	AR3	MDQ1_58	MDQS1_5_N	BA6	MEM_B_DQS_N<5>	27B5 74A3		
MEM_B_DQ<57>	AU2	MDQ1_57	MDQS1_4_P	BA10	MEM_B_DQS_P<4>	27B7 74A3		
MEM_B_DQ<56>	AU3	MDQ1_56	MDQS1_4_N	AY11	MEM_B_DQS_N<4>	27B7 74A3		
MEM_B_DQ<55>	AY4	MDQ1_55	MDQS1_3_P	BB33	MEM_B_DQS_P<3>	27B2 74A3		
MEM_B_DQ<54>	AY3	MDQ1_54	MDQS1_3_N	BA33	MEM_B_DQS_N<3>	27C2 74A3		
MEM_B_DQ<53>	BB3	MDQ1_53	MDQS1_2_P	BB37	MEM_B_DQS_P<2>	27C4 74A3		
MEM_B_DQ<52>	BC3	MDQ1_52	MDQS1_2_N	BA37	MEM_B_DQS_N<2>	27C4 74A3		
MEM_B_DQ<51>	AW4	MDQ1_51	MDQS1_1_P	BA43	MEM_B_DQS_P<1>	27C4 74A3		
MEM_B_DQ<50>	AW3	MDQ1_50	MDQS1_1_N	AY42	MEM_B_DQS_N<1>	27C4 74A3		
MEM_B_DQ<49>	BA3	MDQ1_49	MDQS1_0_P	AT42	MEM_B_DQS_P<0>	27C2 74A3		
MEM_B_DQ<48>	BB2	MDQ1_48	MDQS1_0_N	AT43	MEM_B_DQS_N<0>	27D2 74A3		
MEM_B_DQ<47>	BB5	MDQ1_47						
MEM_B_DQ<46>	BA5	MDQ1_46						
MEM_B_DQ<45>	BA8	MDQ1_45						
MEM_B_DQ<44>	BC8	MDQ1_44						
MEM_B_DQ<43>	BB4	MDQ1_43						
MEM_B_DQ<42>	BC4	MDQ1_42	MRAS1#	AW16	MEM_B_RAS_L	OUT	27C5 74B3	
MEM_B_DQ<41>	BA7	MDQ1_41	MCAS1#	BA15	MEM_B_CAS_L	OUT	27C7 74B3	
MEM_B_DQ<40>	AY8	MDQ1_40	MWE1#	BA16	MEM_B_WE_L	OUT	27C7 74B3	
MEM_B_DQ<39>	BA9	MDQ1_39						
MEM_B_DQ<38>	BB10	MDQ1_38						
MEM_B_DQ<37>	BB12	MDQ1_37						
MEM_B_DQ<36>	AW12	MDQ1_36						
MEM_B_DQ<35>	BB8	MDQ1_35						
MEM_B_DQ<34>	BB9	MDQ1_34	MBA1_2	BB29	MEM_B_BA<2>	OUT	27C7 74B3	
MEM_B_DQ<33>	AY12	MDQ1_33	MBA1_1	BB18	MEM_B_BA<1>	OUT	27C5 74B3	
MEM_B_DQ<32>	BA12	MDQ1_32	MBA1_0	BB17	MEM_B_BA<0>	OUT	27C7 74B3	
MEM_B_DQ<31>	BC32	MDQ1_31						
MEM_B_DQ<30>	AW32	MDQ1_30						
MEM_B_DQ<29>	BA35	MDQ1_29						
MEM_B_DQ<28>	AY36	MDQ1_28						
MEM_B_DQ<27>	BA32	MDQ1_27	MA1_14	BA29	MEM_B_A<14>	OUT	27C5 74B3	
MEM_B_DQ<26>	BB32	MDQ1_26	MA1_13	BA14	MEM_B_A<13>	OUT	27C7 74B3	
MEM_B_DQ<25>	BA34	MDQ1_25	MA1_12	AW28	MEM_B_A<12>	OUT	27C7 74B3	
MEM_B_DQ<24>	AY35	MDQ1_24	MA1_11	BC28	MEM_B_A<11>	OUT	27C5 74B3	
MEM_B_DQ<23>	BC36	MDQ1_23	MA1_10	BA17	MEM_B_A<10>	OUT	27C7 74B3	
MEM_B_DQ<22>	AW36	MDQ1_22	MA1_9	BB28	MEM_B_A<9>	OUT	27C7 74B3	
MEM_B_DQ<21>	BA39	MDQ1_21	MA1_8	AY28	MEM_B_A<8>	OUT	27C7 74B3	
MEM_B_DQ<20>	AY40	MDQ1_20	MA1_7	BA28	MEM_B_A<7>	OUT	27C5 74B3	
MEM_B_DQ<19>	BA36	MDQ1_19	MA1_6	AY27	MEM_B_A<6>	OUT	27C5 74B3	
MEM_B_DQ<18>	BB36	MDQ1_18	MA1_5	BA27	MEM_B_A<5>	OUT	27C7 74B3	
MEM_B_DQ<17>	BA38	MDQ1_17	MA1_4	BA26	MEM_B_A<4>	OUT	27C5 74B3	
MEM_B_DQ<16>	AY39	MDQ1_16	MA1_3	BB26	MEM_B_A<3>	OUT	27C7 74B3	
MEM_B_DQ<15>	BB40	MDQ1_15	MA1_2	BB25	MEM_B_A<2>	OUT	27C5 74B3	
MEM_B_DQ<14>	AW40	MDQ1_14	MA1_1	BB25	MEM_B_A<1>	OUT	27C7 74B3	
MEM_B_DQ<13>	AV42	MDQ1_13	MA1_0	BA18	MEM_B_A<0>	OUT	27C5 74B3	
MEM_B_DQ<12>	AV41	MDQ1_12						
MEM_B_DQ<11>	BA40	MDQ1_11						
MEM_B_DQ<10>	BC40	MDQ1_10						
MEM_B_DQ<9>	AW42	MDQ1_9						
MEM_B_DQ<8>	AW41	MDQ1_8						
MEM_B_DQ<7>	AT40	MDQ1_7						
MEM_B_DQ<6>	AT41	MDQ1_6						
MEM_B_DQ<5>	AP41	MDQ1_5						
MEM_B_DQ<4>	AN40	MDQ1_4						
MEM_B_DQ<3>	AU40	MDQ1_3						
MEM_B_DQ<2>	AU41	MDQ1_2						
MEM_B_DQ<1>	AR41	MDQ1_1						
MEM_B_DQ<0>	AP42	MDQ1_0						
MEM_B_DM<7>	AT5	MDQM1_7						
MEM_B_DM<6>	BA2	MDQM1_6						
MEM_B_DM<5>	AY7	MDQM1_5						
MEM_B_DM<4>	BA11	MDQM1_4						
MEM_B_DM<3>	BB34	MDQM1_3						
MEM_B_DM<2>	BB38	MDQM1_2						
MEM_B_DM<1>	AY43	MDQM1_1						
MEM_B_DM<0>	AR42	MDQM1_0						

MEMORY CONTROL 1A

MCLK1A_2_P	BA42	TP_MEM_B_CLK2P			
MCLK1A_2_N	BB42	TP_MEM_B_CLK2N			
MCLK1A_1_P	BB22	MEM_B_CLK_P<1>	OUT	27C5 74C3	
MCLK1A_1_N	BA22	MEM_B_CLK_N<1>	OUT	27C5 74C3	
MCLK1A_0_P	BA19	MEM_B_CLK_P<0>	OUT	27C7 74C3	
MCLK1A_0_N	AY19	MEM_B_CLK_N<0>	OUT	27C7 74C3	
MCS1A_1#	BB14	MEM_B_CS_L<1>	OUT	27C7 74B3	
MCS1A_0#	BB16	MEM_B_CS_L<0>	OUT	27C5 74B3	
MODT1A_1	BB13	MEM_B_ODT<1>	OUT	27C5 74B3	
MODT1A_0	AY15	MEM_B_ODT<0>	OUT	27C5 74B3	
MCKE1A_1	AY31	MEM_B_CKE<1>	OUT	27D5 74B3	
MCKE1A_0	BB30	MEM_B_CKE<0>	OUT	27D7 74B3	

SYNC_MASTER=T18_MLB SYNC_DATE=04/04/2008

PAGE TITLE
MCP Memory Interface

Apple Inc.

DRAWING NUMBER 051-7898
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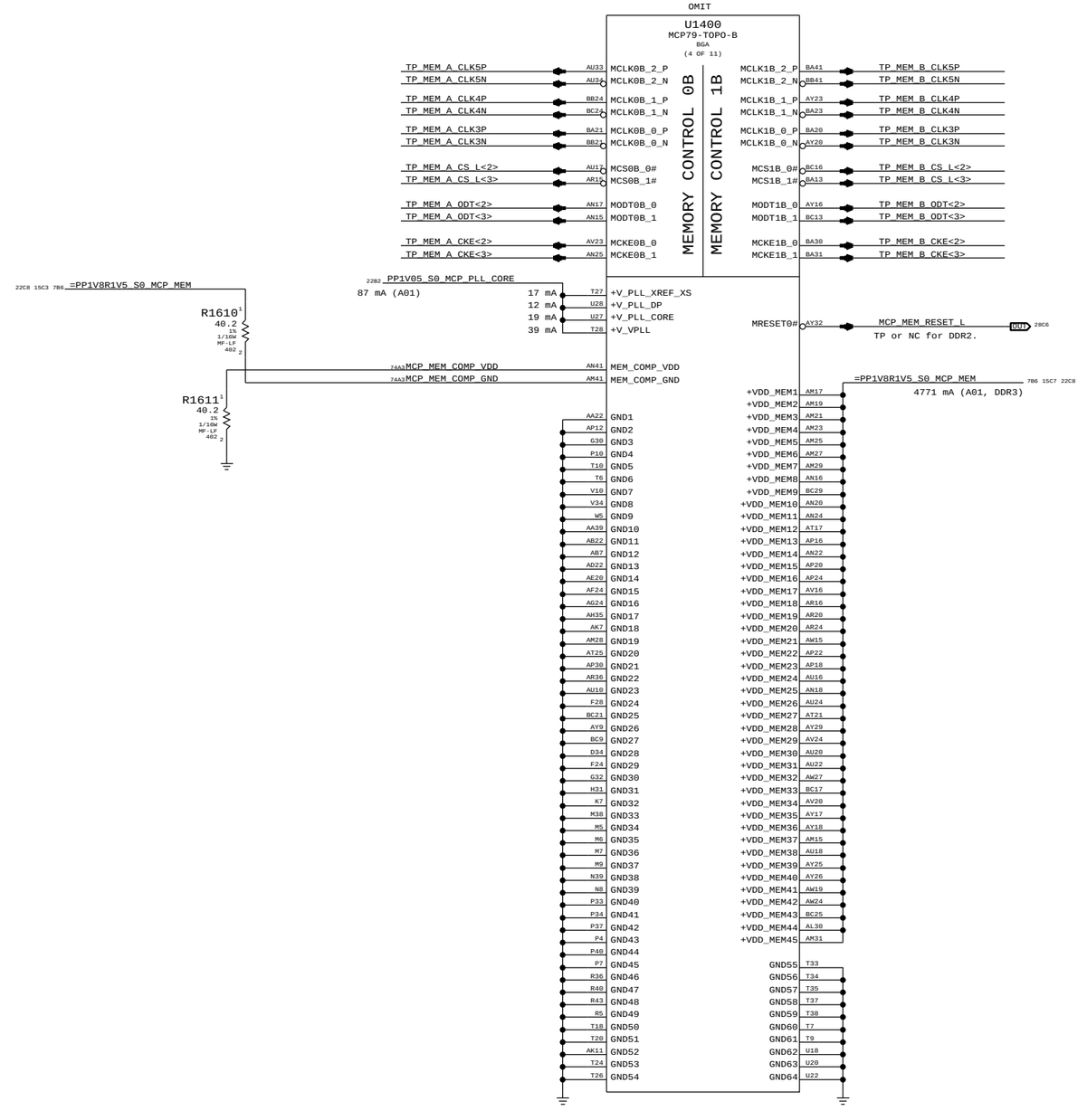

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PAGE TITLE: MCP Memory Misc

Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D

REVISION: C.0.0

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OMIT

U1400
MCP79-TOPO-B
BGA
(5 OF 11)

PCI EXPRESS

8D6	IN	=PEG_D2R_P<0>	F7	PE0_RX0_P	C5	PE0_TX0_P	=PEG_R2D_C_P<0>
8D6	IN	=PEG_D2R_N<0>	E7	PE0_RX0_N	D4	PE0_TX0_N	=PEG_R2D_C_N<0>
8D6	IN	=PEG_D2R_P<1>	D7	PE0_RX1_P	C4	PE0_TX1_P	=PEG_R2D_C_P<1>
8D6	IN	=PEG_D2R_N<1>	C7	PE0_RX1_N	B4	PE0_TX1_N	=PEG_R2D_C_N<1>
8D6	IN	=PEG_D2R_P<2>	E6	PE0_RX2_P	A4	PE0_TX2_P	=PEG_R2D_C_P<2>
8D6	IN	=PEG_D2R_N<2>	F6	PE0_RX2_N	A3	PE0_TX2_N	=PEG_R2D_C_N<2>
8D6	IN	=PEG_D2R_P<3>	E5	PE0_RX3_P	B3	PE0_TX3_P	=PEG_R2D_C_P<3>
8D6	IN	=PEG_D2R_N<3>	F5	PE0_RX3_N	B2	PE0_TX3_N	=PEG_R2D_C_N<3>
8D6	IN	=PEG_D2R_P<4>	E4	PE0_RX4_P	C1	PE0_TX4_P	=PEG_R2D_C_P<4>
8D6	IN	=PEG_D2R_N<4>	E3	PE0_RX4_N	D1	PE0_TX4_N	=PEG_R2D_C_N<4>
8D6	IN	=PEG_D2R_P<5>	C3	PE0_RX5_P	D2	PE0_TX5_P	=PEG_R2D_C_P<5>
8D6	IN	=PEG_D2R_N<5>	D3	PE0_RX5_N	E1	PE0_TX5_N	=PEG_R2D_C_N<5>
8D6	IN	=PEG_D2R_P<6>	G5	PE0_RX6_P	E2	PE0_TX6_P	=PEG_R2D_C_P<6>
8D6	IN	=PEG_D2R_N<6>	H5	PE0_RX6_N	F2	PE0_TX6_N	=PEG_R2D_C_N<6>
8D6	IN	=PEG_D2R_P<7>	J7	PE0_RX7_P	F3	PE0_TX7_P	=PEG_R2D_C_P<7>
8D6	IN	=PEG_D2R_N<7>	J6	PE0_RX7_N	F4	PE0_TX7_N	=PEG_R2D_C_N<7>
8D6	IN	=PEG_D2R_P<8>	J5	PE0_RX8_P	G3	PE0_TX8_P	=PEG_R2D_C_P<8>
8D6	IN	=PEG_D2R_N<8>	J4	PE0_RX8_N	H4	PE0_TX8_N	=PEG_R2D_C_N<8>
8D6	IN	=PEG_D2R_P<9>	L11	PE0_RX9_P	H3	PE0_TX9_P	=PEG_R2D_C_P<9>
8D6	IN	=PEG_D2R_N<9>	L10	PE0_RX9_N	H2	PE0_TX9_N	=PEG_R2D_C_N<9>
8D6	IN	=PEG_D2R_P<10>	L9	PE0_RX10_P	H1	PE0_TX10_P	=PEG_R2D_C_P<10>
8D6	IN	=PEG_D2R_N<10>	L8	PE0_RX10_N	J1	PE0_TX10_N	=PEG_R2D_C_N<10>
8D6	IN	=PEG_D2R_P<11>	L7	PE0_RX11_P	J2	PE0_TX11_P	=PEG_R2D_C_P<11>
8D6	IN	=PEG_D2R_N<11>	L6	PE0_RX11_N	J3	PE0_TX11_N	=PEG_R2D_C_N<11>
8D6	IN	=PEG_D2R_P<12>	N11	PE0_RX12_P	K2	PE0_TX12_P	=PEG_R2D_C_P<12>
8D6	IN	=PEG_D2R_N<12>	N10	PE0_RX12_N	K3	PE0_TX12_N	=PEG_R2D_C_N<12>
8D6	IN	=PEG_D2R_P<13>	N8	PE0_RX13_P	L4	PE0_TX13_P	=PEG_R2D_C_P<13>
8D6	IN	=PEG_D2R_N<13>	P8	PE0_RX13_N	L3	PE0_TX13_N	=PEG_R2D_C_N<13>
8D6	IN	=PEG_D2R_P<14>	N7	PE0_RX14_P	M4	PE0_TX14_P	=PEG_R2D_C_P<14>
8D6	IN	=PEG_D2R_N<14>	N6	PE0_RX14_N	M3	PE0_TX14_N	=PEG_R2D_C_N<14>
8D6	IN	=PEG_D2R_P<15>	N5	PE0_RX15_P	M2	PE0_TX15_P	=PEG_R2D_C_P<15>
8D6	IN	=PEG_D2R_N<15>	N4	PE0_RX15_N	M1	PE0_TX15_N	=PEG_R2D_C_N<15>

8D6	IN	PEG_PRSNT_L	C9	PE0_PRSNT_16# Int PU	E11	PE0_REFCLK_P	PEG_CLK100M_P 8D6
					D11	PE0_REFCLK_N	PEG_CLK100M_N 8D6
2907	IN	MINI_CLKREQ_L	D5	PEB_CLKREQ#/GPIO_49 Int PU	G11	PE1_REFCLK_P	PCIE_CLK100M_MINI_P 29C5 75D3
2907	IN	PCIE_MINI_PRSNT_L	D9	PEB_PRSNT# Int PU	F11	PE1_REFCLK_N	PCIE_CLK100M_MINI_N 29C5 75D3
35D3	IN	FW_CLKREQ_L	E8	PEC_CLKREQ#/GPIO_50 Int PU	J11	PE2_REFCLK_P	PCIE_CLK100M_FW_P 34C2
35D3 8C6	IN	PCIE_FW_PRSNT_L	C10	PEC_PRSNT# Int PU	J10	PE2_REFCLK_N	PCIE_CLK100M_FW_N 34C2
8D6	IN	EXCARD_CLKREQ_L	M15	PED_CLKREQ#/GPIO_51 Int PU	G13	PE3_REFCLK_P	PCIE_CLK100M_EXCARD_P 8D6
8D6	IN	PCIE_EXCARD_PRSNT_L	B10	PED_PRSNT# Int PU	F13	PE3_REFCLK_N	PCIE_CLK100M_EXCARD_N 8C6
		TP_PE4_CLKREQ_L	L16	PEE_CLKREQ#/GPIO_16 Int PU	J13	PE4_REFCLK_P	TP_PCIE_CLK100M_PE4P
		TP_PE4_PRSNT_L	L18	PEE_PRSNT#/GPIO_46 Int PU	H13	PE4_REFCLK_N	TP_PCIE_CLK100M_PE4N
57A4		AUD_IP_PERIPHERAL_DET	M16	PEF_CLKREQ#/GPIO_17 Int PU	L14	PE5_REFCLK_P	TP_PCIE_CLK100M_PE5P
8C4	OUT	GMUX_JTAG_TCK_L	M18	PEF_PRSNT#/GPIO_47 Int PU	K14	PE5_REFCLK_N	TP_PCIE_CLK100M_PE5N
38B7	OUT	CARDREADER_RESET	M17	PEG_CLKREQ#/GPIO_18 Int PU	N14	PE6_REFCLK_P	TP_PCIE_CLK100M_PE6P
8C4	IN	GMUX_JTAG_TDO	M19	PEG_PRSNT#/GPIO_48 Int PU	M14	PE6_REFCLK_N	TP_PCIE_CLK100M_PE6N
29C7 6D5	IN	PCIE_WAKE_L	F17	PE_WAKE# Int PU (S5)	K11	PEX_RST0#	PCIE_RESET_L OUT 24C4
75D3 29C7 6D5	IN	PCIE_MINI_D2R_P	K9	PE1_RX0_P	D8	PE1_TX0_P	PCIE_MINI_R2D_C_P OUT 29C5 75D3
75D3 29C7 6D5	IN	PCIE_MINI_D2R_N	J9	PE1_RX0_N	C8	PE1_TX0_N	PCIE_MINI_R2D_C_N OUT 29C5 75D3
75D3 34C1	IN	PCIE_FW_D2R_P	H9	PE1_RX1_P	B8	PE1_TX1_P	PCIE_FW_R2D_C_P OUT 34C1 75D3
75D3 34C1	IN	PCIE_FW_D2R_N	G9	PE1_RX1_N	A8	PE1_TX1_N	PCIE_FW_R2D_C_N OUT 34C1 75D3
8D6	IN	PCIE_EXCARD_D2R_P	F9	PE1_RX2_P	A7	PE1_TX2_P	PCIE_EXCARD_R2D_C_P OUT 8D6
8D6	IN	PCIE_EXCARD_D2R_N	E9	PE1_RX2_N	B7	PE1_TX2_N	PCIE_EXCARD_R2D_C_N OUT 8D6
		TP_PCIE_PE4_D2RP	H7	PE1_RX3_P	B6	PE1_TX3_P	TP_PCIE_PE4_R2D_CP
		TP_PCIE_PE4_D2RN	G7	PE1_RX3_N	C6	PE1_TX3_N	TP_PCIE_PE4_R2D_CN

7A6 =PP1V05_S0_MCP_PEX_DVDD0
57 mA (A01, DVDD0 & 1)

T17	+DVDD0_PEX1	
W19	+DVDD0_PEX2	
U17	+DVDD0_PEX3	
V19	+DVDD0_PEX4	
W16	+DVDD0_PEX5	
W17	+DVDD0_PEX6	
W18	+DVDD0_PEX7	
U16	+DVDD0_PEX8	

7A6 =PP1V05_S0_MCP_PEX_DVDD1

T19	+DVDD1_PEX1	
U19	+DVDD1_PEX2	

22C2 PP1V05_S0_MCP_PLL_PEX
84 mA (A01)

T16	+V_PLL_PEX	
A11	PEX_CLK_COMP	

75C3 MCP_PEX_CLK_COMP

NO STUFF
R1710
2.37K
1%
1/16W
MF-LF
402
PLACEMENT_NOTE=Place within 12.7mm of U1400

=PP1V05_S0_MCP_PEX_AVDD0 7A6
206 mA (A01, AVDD0 & 1)

Y12	+AVDD0_PEX1	
AA12	+AVDD0_PEX2	
AB12	+AVDD0_PEX3	
M12	+AVDD0_PEX4	
P12	+AVDD0_PEX5	
R12	+AVDD0_PEX6	
N12	+AVDD0_PEX7	
T12	+AVDD0_PEX8	
U12	+AVDD0_PEX9	
AC12	+AVDD0_PEX10	
AD12	+AVDD0_PEX11	
V12	+AVDD0_PEX12	
W12	+AVDD0_PEX13	

=PP1V05_S0_MCP_PEX_AVDD1 7A6

M13	+AVDD1_PEX1	
N13	+AVDD1_PEX2	
P13	+AVDD1_PEX3	

If PE0 interface is not used, ground DVDD0_PEX and AVDD0_PEX.
If PE1 interface is not used, ground DVDD1_PEX and AVDD1_PEX.

SYNC_MASTER=T18_MLB SYNC_DATE=04/04/2008

PAGE TITLE
MCP PCIe Interfaces

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D
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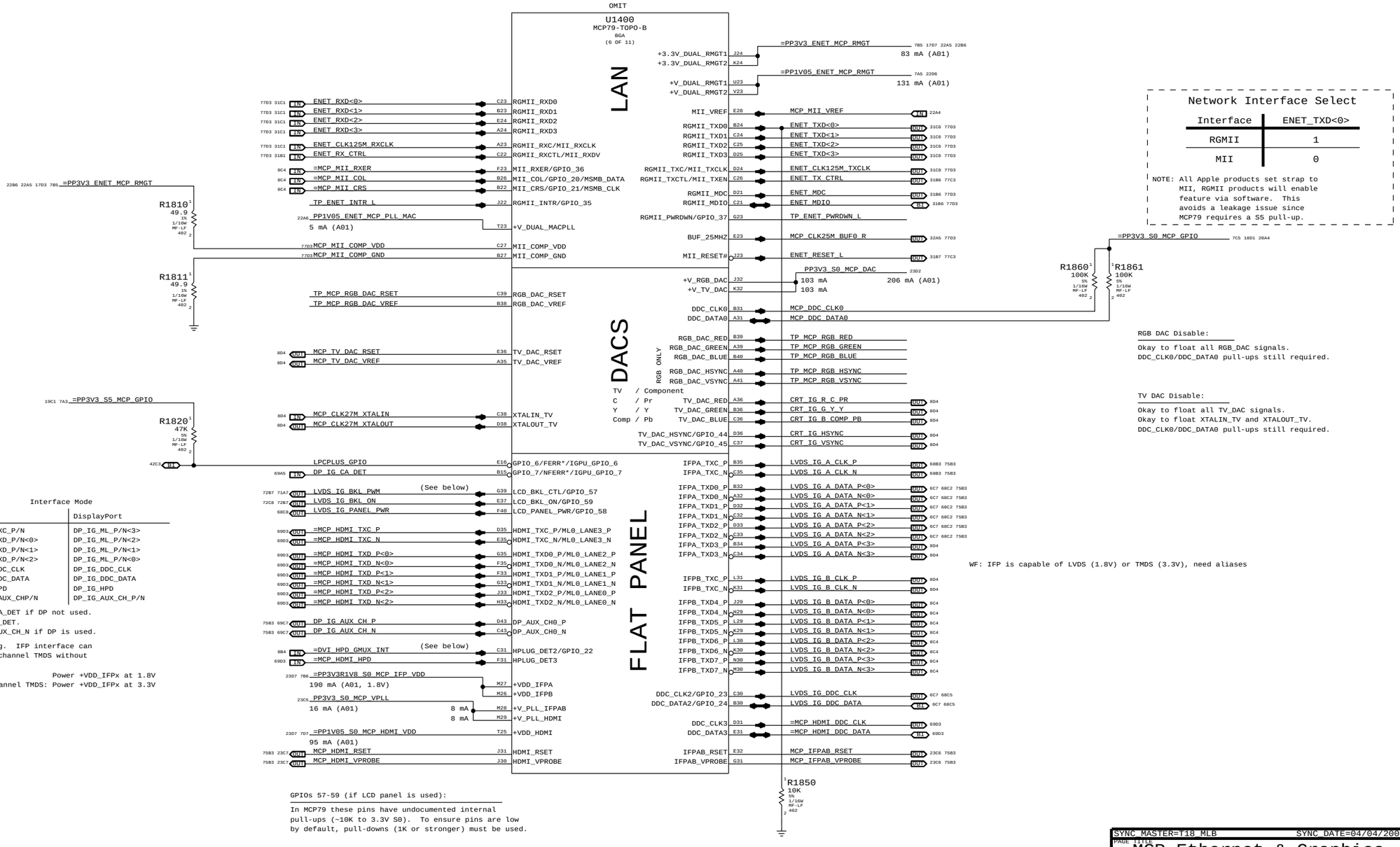

Interface Mode

MCP Signal	TMDS/HDMI	DisplayPort
=MCP_HDMI_TXC_P/N	TMDS_IG_TXC_P/N	DP_IG_ML_P/N<3>
=MCP_HDMI_TXD_P/N<0>	TMDS_IG_TXD_P/N<0>	DP_IG_ML_P/N<2>
=MCP_HDMI_TXD_P/N<1>	TMDS_IG_TXD_P/N<1>	DP_IG_ML_P/N<1>
=MCP_HDMI_TXD_P/N<2>	TMDS_IG_TXD_P/N<2>	DP_IG_ML_P/N<0>
=MCP_HDMI_DDC_CLK	TMDS_IG_DDC_CLK	DP_IG_DDC_CLK
=MCP_HDMI_DDC_DATA	TMDS_IG_DDC_DATA	DP_IG_DDC_DATA
=MCP_HDMI_HPD	TMDS_IG_HPD	DP_IG_HPD
DP_IG_AUX_CH_P/N	TP_DP_IG_AUX_CHP/N	DP_IG_AUX_CH_P/N

NOTE: 1M pull-down required on DP_IG_CA_DET if DP not used.
NOTE: 20K pull-down required on DP_HPD_DET.
NOTE: 1K pull-down required on DP_IG_AUX_CH_N if DP is used.

NOTE: HDMI port requires level-shifting. IFP interface can be used to provide HDMI or dual-channel TMDS without level-shifters.

LVDS: Power +VDD_IFPx at 1.8V
Dual-channel TMDS: Power +VDD_IFPx at 3.3V

GPIOs 57-59 (if LCD panel is used):

In MCP79 these pins have undocumented internal pull-ups (~10K to 3.3V S0). To ensure pins are low by default, pull-downs (1K or stronger) must be used.

=DVI_HPD_GMUX_INT:

Alias to DVI_HPD for systems using IFP for DVI.
Alias to GMUX_INT for systems with GMUX.
Alias to HPLUG_DET2 for other systems.
Pull-down (20k) required in all cases.

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PAGE TITLE: MCP Ethernet & Graphics

Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D
REVISION: C.0.0
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PAGE: 18 OF 109
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U1400
MCP79-TOPO-B
BGA
(7 OF 11)

PCI

76D3 18D2 PCI_REQ0_L	T2	PCI_REQ0#	
76D3 18D2 PCI_REQ1_L	V5	PCI_REQ1#/FANRPM2	
35D6 35C7 35C4 35A4 18D7 OUT FW_PWR_EN	T3	PCI_REQ2#/GPIO_40/RS232_DSR#	PCI_GNT2#/GPIO_41/RS232_DTR# R4 — GMUX_JTAG_TMS OUT 8C4
57D7 OUT AUD_IPHS_SWITCH_EN	U5	PCI_REQ3#/GPIO_38/RS232_CTS#	PCI_GNT3#/GPIO_39/RS232_RTS# U11 — GMUX_JTAG_TDI OUT 8C4
18D2 IN MCP_RS232_SIN_L	T4	PCI_REQ4#/GPIO_52/RS232_SIN#	PCI_GNT4#/GPIO_53/RS232_SOUT# P3 — MCP_RS232_SOUT_L OUT 18D2
76D3 12C3 B3 MCP_DEBUG<0>	AC3	PCI_AD0	PCI_CBE0# AA3 — TP_PCI_C_BE_L<0>
76D3 12C3 B2 MCP_DEBUG<1>	AE10	PCI_AD1	PCI_CBE1# AA6 — TP_PCI_C_BE_L<1>
76D3 12C3 A3 MCP_DEBUG<2>	AC4	PCI_AD2	PCI_CBE2# AA11 — TP_PCI_C_BE_L<2>
76D3 12C3 A2 MCP_DEBUG<3>	AE11	PCI_AD3	PCI_CBE3# W10 — TP_PCI_C_BE_L<3>
76D3 12C3 C3 MCP_DEBUG<4>	AB3	PCI_AD4	
76D3 12C3 C2 MCP_DEBUG<5>	AC6	PCI_AD5	PCI_DEVSEL# AA9 — TP_PCI_DEVSEL_L
76D3 12C3 B1 MCP_DEBUG<6>	AB2	PCI_AD6	PCI_FRAME# V4 — TP_PCI_FRAME_L
76D3 12C3 A1 MCP_DEBUG<7>	AC7	PCI_AD7	PCI_IRDY# AA10 — TP_PCI_IRDY_L
TP_PCI_AD<8>	AC8	PCI_AD8	PCI_PAR Y1 — TP_PCI_PAR
TP_PCI_AD<9>	AA2	PCI_AD9	PCI_PERR#/GPIO_43/RS232_DCD# AB9 — TP_PCI_PERR_L
TP_PCI_AD<10>	AC9	PCI_AD10	PCI_SERR# AA7 — TP_PCI_SERR_L
TP_PCI_AD<11>	AC10	PCI_AD11	PCI_STOP# V2 — TP_PCI_STOP_L
TP_PCI_AD<12>	AC11	PCI_AD12	PCI_PME#/GPIO_30 T1 — PM_LATRIGGER_L OUT 12C6
TP_PCI_AD<13>	AA1	PCI_AD13	Int PU (S5)
TP_PCI_AD<14>	AA5	PCI_AD14	
TP_PCI_AD<15>	Y5	PCI_AD15	PCI_RESET0# R10 — MEM_VTT_EN_R OUT 24C4
TP_PCI_AD<16>	W3	PCI_AD16	PCI_RESET1# R11 — TP_PCI_RESET1_L
TP_PCI_AD<17>	W6	PCI_AD17	
TP_PCI_AD<18>	W4	PCI_AD18	PCI_CLK0 R6 — TP_PCI_CLK0
TP_PCI_AD<19>	W7	PCI_AD19	PCI_CLK1 R7 — TP_PCI_CLK1
TP_PCI_AD<20>	V3	PCI_AD20	PCI_CLK2 R8 — 76C3 PCI_CLK33M_MCP_R
TP_PCI_AD<21>	W8	PCI_AD21	
TP_PCI_AD<22>	V2	PCI_AD22	R1910 22 5% 1/16W MF-LF 402
TP_PCI_AD<23>	W9	PCI_AD23	PCI_CLKIN R9 — 76C3 PCI_CLK33M_MCP
TP_PCI_AD<24>	U3	PCI_AD24	PLACEMENT_NOTE=Place close to pin R8
TP_PCI_AD<25>	W11	PCI_AD25	
TP_PCI_AD<26>	U2	PCI_AD26	
TP_PCI_AD<27>	U5	PCI_AD27	
TP_PCI_AD<28>	U1	PCI_AD28	
TP_PCI_AD<29>	U6	PCI_AD29	
TP_PCI_AD<30>	T5	PCI_AD30	
TP_PCI_AD<31>	U7	PCI_AD31	
TP_PCI_INTW_L	P2	PCI_INTW#	
TP_PCI_INTX_L	N3	PCI_INTX#	
TP_PCI_INTY_L	N2	PCI_INTY#	
TP_PCI_INTZ_L	N1	PCI_INTZ#	
TP_PCI_TRDY_L	Y3	PCI_TRDY#	
42D5 40C5 IN PM_CLKRUN_L	AD11	PCI_CLKRUN#/GPIO_42	
8C2 IN FW_PME_L	AE3	LPC_DRQ1#/GPIO_19 Int PU	
TP_LPC_DRQ0_L	AE1	LPC_DRQ0# Int PU	
42D3 40C8 B3 LPC_SERIRQ	AE6	LPC_SERIRQ Int PU	

LPC

LPC_FRAME# AD4	LPC_FRAME_R_L	R1960 22 5% 1/16W MF-LF 402	LPC_FRAME_L OUT 40C8 42D5 76C3
LPC_PWRDWN#/GPIO_54/EXT_NMI# AE12	LPC_PWRDWN_L		OUT 40C5 42D3
LPC_RESET0# AE5	LPC_RESET_L		OUT 24D4 76C3
LPC_AD0 AD3	LPC_AD_R<0>	R1950 22 5% 1/16W MF-LF 402	LPC_AD<0> B3 40C8 42D5 76C3
LPC_AD1 AD2	LPC_AD_R<1>	R1951 22 5% 1/16W MF-LF 402	LPC_AD<1> B3 40C8 42D5 76C3
LPC_AD2 AD1	LPC_AD_R<2>	R1952 22 5% 1/16W MF-LF 402	LPC_AD<2> B3 40C8 42D3 76C3
LPC_AD3 AD5	LPC_AD_R<3>	R1953 22 5% 1/16W MF-LF 402	LPC_AD<3> B3 40C8 42D3 76C3
LPC_CLK0 AE9	LPC_CLK33M_SMC_R		OUT 24B4 76C3

R1961 10K 5% 1/16W MF-LF 402

Strap for Boot ROM Selection (See HDA_SDOUT)

GND

U24	GND65	GND98	Y26
U26	GND66	GND99	Y27
U39	GND67	GND100	AB18
U4	GND68	GND101	H34
U8	GND69	GND102	AB20
V16	GND70	GND103	AB21
V17	GND71	GND104	AB23
V18	GND72	GND105	AB24
V20	GND73	GND106	AB25
V22	GND74	GND107	AB26
V24	GND75	GND108	AB27
V26	GND76	GND109	AB28
V27	GND77	GND110	AB34
V28	GND78	GND111	AB37
V33	GND79	GND112	AB4
V37	GND80	GND113	AB40
V4	GND81	GND114	AC22
V40	GND82	GND115	AC36
V7	GND83	GND116	AC40
W20	GND84	GND117	AB33
W22	GND85	GND118	AC5
W24	GND86	GND119	AD16
W36	GND87	GND120	AD17
W40	GND88	GND121	AD18
W43	GND89	GND122	AD19
Y16	GND90	GND123	AD20
Y17	GND91	GND124	AD24
Y18	GND92	GND125	AD25
Y19	GND93	GND126	AD26
Y20	GND94	GND127	AD27
Y22	GND95	GND128	AD28
Y24	GND96	GND129	AD33
Y25	GND97	GND130	AD34

20A4 17C1 7C5 =PP3V3_S0_MCP_GPIO

18D4 MCP_RS232_SOUT_L	R1989	8.2K	5% 1/16W MF-LF 402
76D3 18D7 PCI_REQ0_L	R1990	8.2K	5% 1/16W MF-LF 402
76D3 18D7 PCI_REQ1_L	R1991	8.2K	5% 1/16W MF-LF 402
35D6 35C7 35C4 35A4 18D7 FW_PWR_EN	R1992	8.2K	5% 1/16W MF-LF 402
18D7 MCP_RS232_SIN_L	R1994	8.2K	5% 1/16W MF-LF 402

SYNC MASTER=T18 MLB SYNC DATE=04/04/2008

PAGE TITLE: MCP PCI & LPC

Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D
REVISION: C.0.0
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PAGE: 19 OF 109
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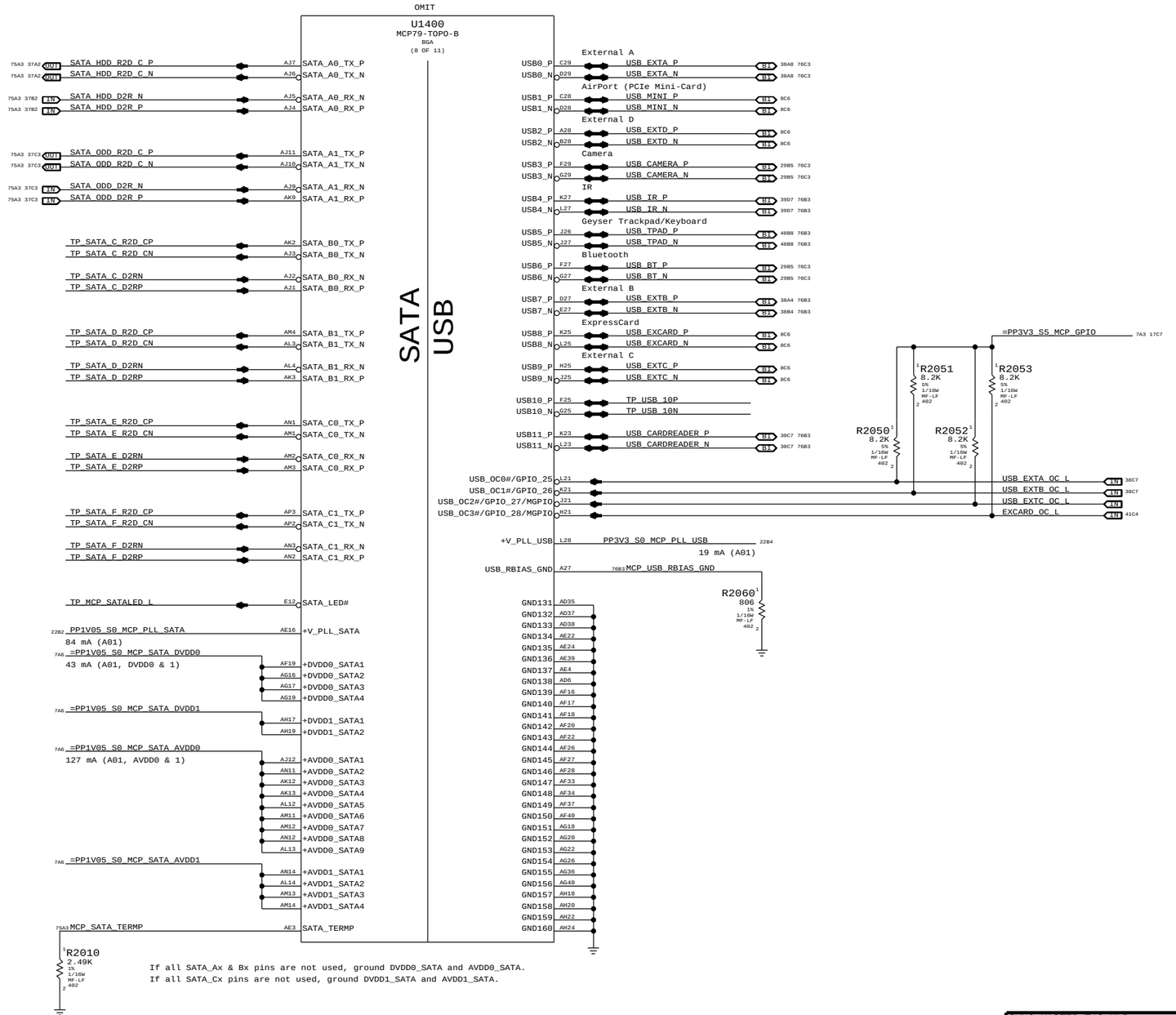

If all SATA_Ax & Bx pins are not used, ground DVDD0_SATA and AVDD0_SATA.
If all SATA_Cx pins are not used, ground DVDD1_SATA and AVDD1_SATA.

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SYNC_MASTER=T18_MLB	SYNC_DATE=04/04/2008
PAGE TITLE	MCP SATA & USB
Apple Inc.	DRAWING NUMBER 051-7898 · SIZE D
	REVISION C.0.0
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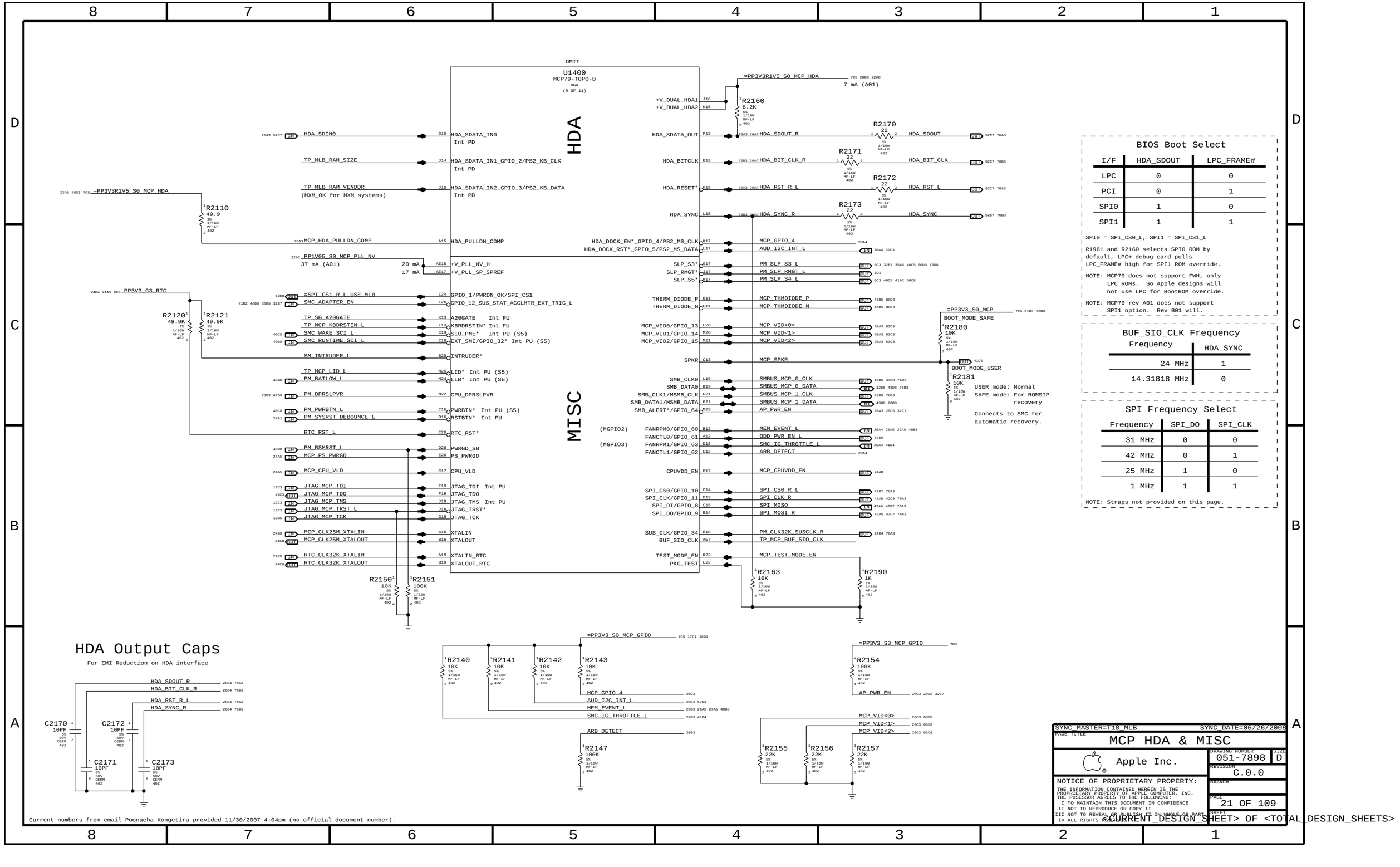
OMIT
U1400
MCP79-TOPO-B
BGA
(9 OF 11)
HDA
MISC
HDA_SDIN0
TP_MLB_RAM_SIZE
TP_MLB_RAM_VENDOR
(MXM_OK for MXM systems)
=PP3V3R1V5_S0_MCP_HDA
R2110 49.9
MCP_HDA_PULLDN_COMP
PP1V05_S0_MCP_PLL_NV
37 mA (A01)
20 mA
17 mA
PP3V3_G3_RTC
R2120 49.9K
R2121 49.9K
=SPI_CS1_R_L_USE_MLB
SMC_ADAPTER_EN
TP_SB_A20GATE
TP_MCP_KBDRSTIN_L
SMC_WAKE_SCI_L
SMC_RUNTIME_SCI_L
SM_INTRUDER_L
TP_MCP_LID_L
PM_BATLOW_L
PM_DPRSLPVR
PM_PWRBTN_L
PM_SYSRST_DEBOUNCE_L
RTC_RST_L
PM_RSMRST_L
MCP_PS_PWRGD
MCP_CPU_VLD
JTAG_MCP_TDI
JTAG_MCP_TDO
JTAG_MCP_TMS
JTAG_MCP_TRST_L
JTAG_MCP_TCK
MCP_CLK25M_XTALIN
MCP_CLK25M_XTALOUT
RTC_CLK32K_XTALIN
RTC_CLK32K_XTALOUT
R2150 10K
R2151 100K
HDA_SDATA_IN0
Int PD
HDA_SDATA_IN1_GPIO_2/PS2_KB_CLK
HDA_SDATA_IN2_GPIO_3/PS2_KB_DATA
HDA_PULLDN_COMP
+V_PLL_NV_H
+V_PLL_SP_SPREF
GPIO_1/PWRDN_OK/SPI_CS1
GPIO_12_SUS_STAT_ACCLMTR_EXT_TRIG_L
A20GATE Int PU
KBRDRSTIN* Int PU
SIO_PME* Int PU (S5)
EXT_SMI/GPIO_32* Int PU (S5)
INTRUDER*
LID* Int PU (S5)
LLB* Int PU (S5)
CPU_DPRSLPVR
PWRBTN* Int PU (S5)
RSTBTN* Int PU
RTC_RST*
PWRGD_SB
PS_PWRGD
CPU_VLD
JTAG_TDI Int PU
JTAG_TDO
JTAG_TMS Int PU
JTAG_TRST*
JTAG_TCK
XTALIN
XTALOUT
XTALIN_RTC
XTALOUT_RTC
=PP3V3R1V5_S0_MCP_HDA
7 mA (A01)
R2160 8.2K
HDA_SDATA_OUT
HDA_BITCLK
HDA_RESET*
HDA_SYNC
HDA_SDOUT_R
HDA_BIT_CLK_R
HDA_RST_R_L
HDA_SYNC_R
R2170 22
R2171 22
R2172 22
R2173 22
HDA_SDOUT
HDA_BIT_CLK
HDA_RST_L
HDA_SYNC
HDA_DOCK_EN*_GPIO_4/PS2_MS_CLK
HDA_DOCK_RST*_GPIO_5/PS2_MS_DATA
MCP_GPIO_4
AUD_I2C_INT_L
SLP_S3*
SLP_RMGT*
SLP_S5*
PM_SLP_S3_L
PM_SLP_RMGT_L
PM_SLP_S4_L
THERM_DIODE_P
THERM_DIODE_N
MCP_THMDIODE_P
MCP_THMDIODE_N
MCP_VID0/GPIO_13
MCP_VID1/GPIO_14
MCP_VID2/GPIO_15
MCP_VID<0>
MCP_VID<1>
MCP_VID<2>
SPKR
MCP_SPKR
SMB_CLK0
SMB_DATA0
SMB_CLK1/MSMB_CLK
SMB_DATA1/MSMB_DATA
SMB_ALERT*/GPIO_64
SMBUS_MCP_0_CLK
SMBUS_MCP_0_DATA
SMBUS_MCP_1_CLK
SMBUS_MCP_1_DATA
AP_PWR_EN
(MGPIO2)
(MGPIO3)
FANRPM0/GPIO_60
FANCTL0/GPIO_61
FANRPM1/GPIO_63
FANCTL1/GPIO_62
MEM_EVENT_L
ODD_PWR_EN_L
SMC_IG_THROTTLE_L
ARB_DETECT
CPUVDD_EN
MCP_CPUVDD_EN
SPI_CS0/GPIO_10
SPI_CLK/GPIO_11
SPI_DI/GPIO_8
SPI_DO/GPIO_9
SPI_CS0_R_L
SPI_CLK_R
SPI_MISO
SPI_MOSI_R
SUS_CLK/GPIO_34
BUF_SIO_CLK
PM_CLK32K_SUSCLK_R
TP_MCP_BUF_SIO_CLK
TEST_MODE_EN
PKG_TEST
MCP_TEST_MODE_EN
R2163 10K
R2190 1K
=PP3V3_S0_MCP
BOOT_MODE_SAFE
R2180 10K
BOOT_MODE_USER
R2181 10K
USER mode: Normal
SAFE mode: For ROMSIP recovery
Connects to SMC for automatic recovery.
BIOS Boot Select
I/F | HDA_SDOUT | LPC_FRAME#
LPC | 0 | 0
PCI | 0 | 1
SPI0 | 1 | 0
SPI1 | 1 | 1
SPI0 = SPI_CS0_L, SPI1 = SPI_CS1_L
R1961 and R2160 selects SPI0 ROM by default, LPC+ debug card pulls LPC_FRAME# high for SPI1 ROM override.
NOTE: MCP79 does not support FWH, only LPC ROMs. So Apple designs will not use LPC for BootROM override.
NOTE: MCP79 rev A01 does not support SPI1 option. Rev B01 will.
BUF_SIO_CLK Frequency
Frequency | HDA_SYNC
24 MHz | 1
14.31818 MHz | 0
SPI Frequency Select
Frequency | SPI_DO | SPI_CLK
31 MHz | 0 | 0
42 MHz | 0 | 1
25 MHz | 1 | 0
1 MHz | 1 | 1
NOTE: Straps not provided on this page.
HDA Output Caps
For EMI Reduction on HDA interface
HDA_SDOUT_R
HDA_BIT_CLK_R
HDA_RST_R_L
HDA_SYNC_R
C2170 10PF
C2172 10PF
C2171 10PF
C2173 10PF
=PP3V3_S0_MCP_GPIO
R2140 10K
R2141 10K
R2142 10K
R2143 10K
MCP_GPIO_4
AUD_I2C_INT_L
MEM_EVENT_L
SMC_IG_THROTTLE_L
ARB_DETECT
R2147 100K
=PP3V3_S3_MCP_GPIO
R2154 100K
AP_PWR_EN
R2155 22K
R2156 22K
R2157 22K
SYNC_MASTER=T18_MLB
SYNC_DATE=06/26/2008
PAGE TITLE
MCP HDA & MISC
Apple Inc.
DRAWING NUMBER 051-7898
SIZE D
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OMIT

U1400
MCP79-TOPO-B
BGA
(11 OF 11)

GND

AH26	GND161	GND253	AV40
AH33	GND162	GND254	BA1
AH34	GND163	GND255	BA4
AH37	GND164	GND256	AW31
AH38	GND165	GND257	AY6
AJ39	GND166	GND258	L35
AJ8	GND167	GND259	BC33
AK10	GND168	GND260	BC37
AK33	GND169	GND261	BC41
AK34	GND170	GND262	AY14
AK37	GND171	GND263	BC5
AK4	GND172	GND264	C2
AK40	GND173	GND265	D10
AL36	GND174	GND266	D14
AL40	GND175	GND267	D15
AL5	GND176	GND268	D18
AM10	GND177	GND269	D19
AM16	GND178	GND270	D22
AM18	GND179	GND271	D23
AM20	GND180	GND272	D26
AM22	GND181	GND273	D30
AM24	GND182	GND274	D37
AM26	GND183	GND275	D6
AM30	GND184	GND276	E13
AM34	GND185	GND277	E17
AM35	GND186	GND278	E21
AM37	GND187	GND279	E25
AM38	GND188	GND280	E29
AM5	GND189	GND281	E33
AM6	GND190	GND282	F12
AM7	GND191	GND283	F16
AM9	GND192	GND284	F32
AP26	GND193	GND285	F8
AN28	GND194	GND286	G10
AN30	GND195	GND287	G12
AN39	GND196	GND288	G14
AN4	GND197	GND289	G16
Y7	GND198	GND290	BC12
AP10	GND199	GND291	G22
AU26	GND200	GND292	G24
AP14	GND201	GND293	AW20
AU14	GND202	GND294	G34
AP28	GND203	GND295	G4
AP32	GND204	GND296	G43
AP34	GND205	GND297	G6
AP36	GND206	GND298	G8
AP37	GND207	GND299	H11
AP4	GND208	GND300	H15
AP40	GND209	GND301	AW35
AP7	GND210	GND302	H23
AW23	GND211	GND303	AN8
AR28	GND212	GND304	G40
AR32	GND213	GND305	J12
AR40	GND214	GND306	J8
AT10	GND215	GND307	K10
AR12	GND216	GND308	K12
AT13	GND217	GND309	K18
AT29	GND218	GND310	K26
AT33	GND219	GND311	K37
AT6	GND220	GND312	K4
AT7	GND221	GND313	K40
AT9	GND222	GND314	K8
AY21	GND223	GND315	AU1
AY22	GND224	GND316	L40
L12	GND225	GND317	L43
AU12	GND226	GND318	L5
AU28	GND227	GND319	M10
AP33	GND228	GND320	M34
AU32	GND229	GND321	M35
AR36	GND230	GND322	M37
AU36	GND231	GND323	Y28
AU38	GND232	GND324	Y33
AU4	GND233	GND325	Y34
G28	GND234	GND326	Y35
F20	GND235	GND327	Y37
AV28	GND236	GND328	Y38
AV32	GND237	GND329	AB17
AV36	GND238	GND330	AB16
AV4	GND239	GND331	AN26
AV7	GND240	GND332	AD7
AW11	GND241	GND333	M11
G20	GND242	GND334	AA4
AR43	GND243	GND335	AB19
AW43	GND244	GND336	AY13
AY10	GND245	GND337	P11
AV12	GND246	GND338	Y6
AY30	GND247	GND339	T11
AY33	GND248	GND340	V11
AY34	GND249	GND341	Y11
AY37	GND250	GND342	AH16
AY38	GND251	GND343	T22
AY41	GND252		

OMIT

U1400
MCP79-TOPO-B
BGA
(10 OF 11)

POWER

=PPVCORE_S0_MCP
22D8 7C6
23065 mA (A01, 1.2V)
16996 mA (A01, 1.0V)

AA25	+VDD_CORE1	+VTT_CPU1	R32	
AC23	+VDD_CORE2	+VTT_CPU2	AC32	
U25	+VDD_CORE3	+VTT_CPU3	E40	
AH12	+VDD_CORE4	+VTT_CPU4	J36	
AG10	+VDD_CORE5	+VTT_CPU5	N32	
AG5	+VDD_CORE6	+VTT_CPU6	T32	
Y21	+VDD_CORE7	+VTT_CPU7	U32	
Y23	+VDD_CORE8	+VTT_CPU8	V32	
AA16	+VDD_CORE9	+VTT_CPU9	W32	
AA26	+VDD_CORE10	+VTT_CPU10	P31	
AA27	+VDD_CORE11	+VTT_CPU11	AF32	
AA28	+VDD_CORE12	+VTT_CPU12	AE32	
AC16	+VDD_CORE13	+VTT_CPU13	AH32	
AC17	+VDD_CORE14	+VTT_CPU14	AJ32	
AC18	+VDD_CORE15	+VTT_CPU15	AK31	
AC19	+VDD_CORE16	+VTT_CPU16	AK32	
AC20	+VDD_CORE17	+VTT_CPU17	AD32	
AC21	+VDD_CORE18	+VTT_CPU18	AL31	
AA17	+VDD_CORE19	+VTT_CPU19	AB32	
AC24	+VDD_CORE20	+VTT_CPU20	B41	
AC25	+VDD_CORE21	+VTT_CPU21	B42	
AC26	+VDD_CORE22	+VTT_CPU22	C40	
AC27	+VDD_CORE23	+VTT_CPU23	C41	
AC28	+VDD_CORE24	+VTT_CPU24	C42	
AD21	+VDD_CORE25	+VTT_CPU25	D39	
AD23	+VDD_CORE26	+VTT_CPU26	D40	
W27	+VDD_CORE27	+VTT_CPU27	D41	
V25	+VDD_CORE28	+VTT_CPU28	E38	
AA18	+VDD_CORE29	+VTT_CPU29	E39	
AE19	+VDD_CORE30	+VTT_CPU30	F37	
AE21	+VDD_CORE31	+VTT_CPU31	F38	
AE23	+VDD_CORE32	+VTT_CPU32	F39	
AE25	+VDD_CORE33	+VTT_CPU33	G36	
AE26	+VDD_CORE34	+VTT_CPU34	G37	
AE27	+VDD_CORE35	+VTT_CPU35	G38	
AE28	+VDD_CORE36	+VTT_CPU36	H35	
AF10	+VDD_CORE37	+VTT_CPU37	H37	
AF11	+VDD_CORE38	+VTT_CPU38	J34	
AA19	+VDD_CORE39	+VTT_CPU39	J35	
AF2	+VDD_CORE40	+VTT_CPU40	K33	
AF21	+VDD_CORE41	+VTT_CPU41	K34	
AF23	+VDD_CORE42	+VTT_CPU42	K35	
AF25	+VDD_CORE43	+VTT_CPU43	L32	
AF3	+VDD_CORE44	+VTT_CPU44	L33	
AF4	+VDD_CORE45	+VTT_CPU45	L34	
AF7	+VDD_CORE46	+VTT_CPU46	M31	
AH23	+VDD_CORE47	+VTT_CPU47	M32	
AF9	+VDD_CORE48	+VTT_CPU48	M33	
AA28	+VDD_CORE49	+VTT_CPU49	N31	
AG11	+VDD_CORE50	+VTT_CPU50	P32	
AG12	+VDD_CORE51	+VTT_CPU51	Y32	
AG21	+VDD_CORE52	+VTT_CPU52	AA32	
AG23	+VDD_CORE53			
AG25	+VDD_CORE54	+VTT_CPUCLK	AG32	43 mA
AG3	+VDD_CORE55			
AG4	+VDD_CORE56			
AA21	+VDD_CORE57			
AG6	+VDD_CORE58			
AG7	+VDD_CORE59			
AG8	+VDD_CORE60			
AG9	+VDD_CORE61			
AH1	+VDD_CORE62			
AH10	+VDD_CORE63			
AH11	+VDD_CORE64			
W26	+VDD_CORE65			
AH2	+VDD_CORE66			
AA23	+VDD_CORE67			
W28	+VDD_CORE68			
AH25	+VDD_CORE69			
AH21	+VDD_CORE70	+3.3V_DUAL1	G18	16 mA
AH3	+VDD_CORE71	+3.3V_DUAL2	H19	
AH4	+VDD_CORE72	+3.3V_DUAL3	J20	
AH5	+VDD_CORE73	+3.3V_DUAL4	K20	
AH6	+VDD_CORE74			
AH7	+VDD_CORE75	+3.3V_DUAL_USB1	G26	250 mA
AH9	+VDD_CORE76	+3.3V_DUAL_USB2	H27	
AA24	+VDD_CORE77	+3.3V_DUAL_USB3	J28	
W21	+VDD_CORE78	+3.3V_DUAL_USB4	K28	
W23	+VDD_CORE79			
W25	+VDD_CORE80			
AF12	+VDD_CORE81			

=PP1V05_S0_MCP_FSB
7D7 13A2 13B7 22C8
1139 mA
1182 mA (A01)

=PP3V3_S0_MCP
7C5 20C2 22B8
450 mA (A01)

+3.3V_1	AD10	
+3.3V_2	AE8	
+3.3V_3	AB10	
+3.3V_4	AD9	
+3.3V_5	Y10	
+3.3V_6	AB11	
+3.3V_7	AA8	
+3.3V_8	Y9	

=PP3V3_S5_MCP
7A3 22B8
266 mA (A01)

=PP1V05_S5_MCP_VDD_AUXC
7B3 22D8
105 mA (A01)

+VDD_AUXC1	T21	
+VDD_AUXC2	U21	
+VDD_AUXC3	V21	

PP3V3_G3_RTC
24D4 20C8 6C9
10 uA (G3)
80 uA (S0)

A20	+VBAT	

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SYNC_MASTER=T18_MLB SYNC_DATE=04/04/2008

PAGE TITLE: MCP Power & Ground

Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D

REVISION: C.0.0

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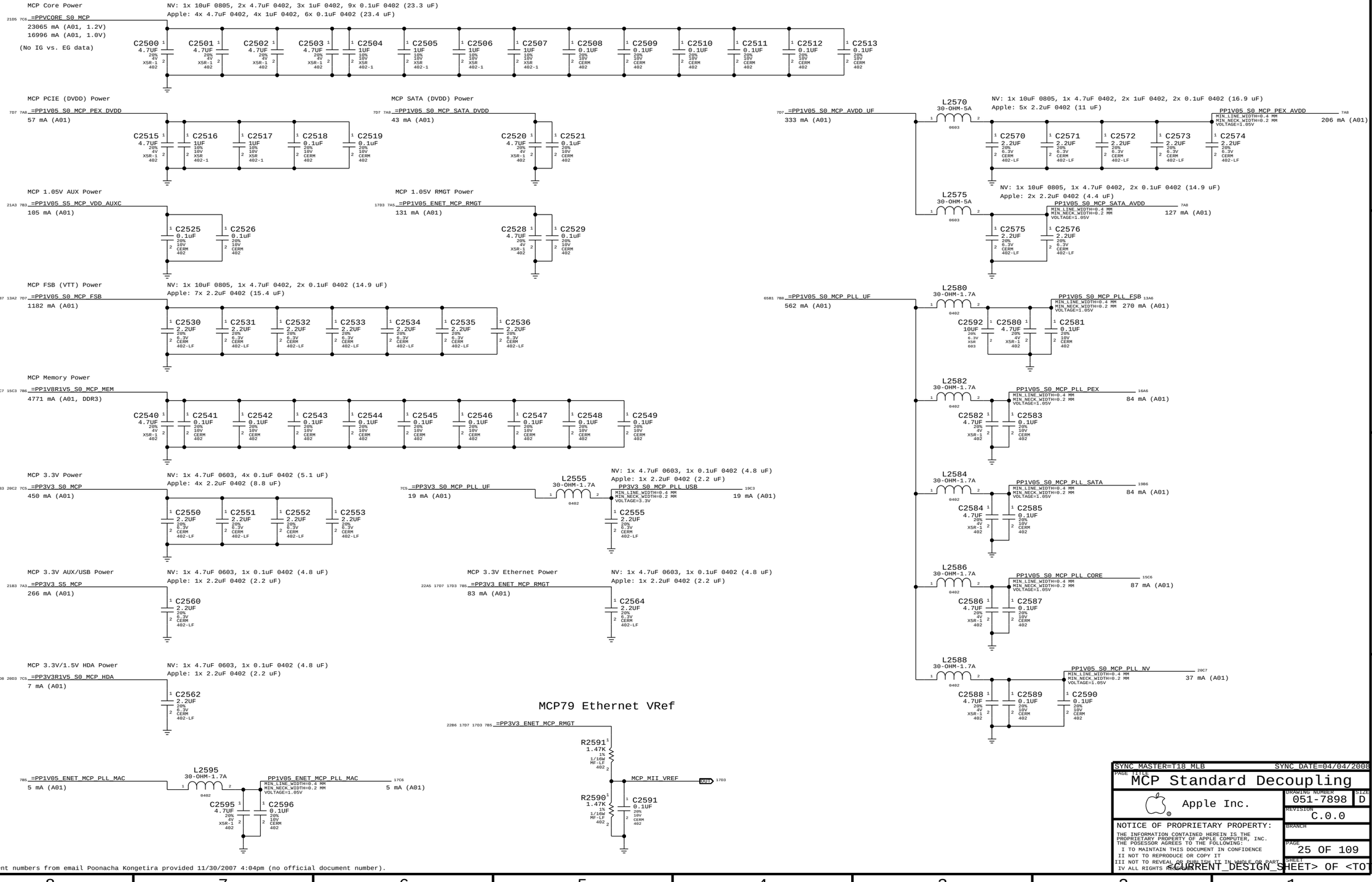
MCP Core Power
NV: 1x 10uF 0805, 2x 4.7uF 0402, 3x 1uF 0402, 9x 0.1uF 0402 (23.3 uF)
Apple: 4x 4.7uF 0402, 4x 1uF 0402, 6x 0.1uF 0402 (23.4 uF)
=PPVCORE_S0_MCP
23065 mA (A01, 1.2V)
16996 mA (A01, 1.0V)
(No IG vs. EG data)
C2500 4.7UF 20% 4V X5R-1 402
C2501 4.7UF 20% 4V X5R-1 402
C2502 4.7UF 20% 4V X5R-1 402
C2503 4.7UF 20% 4V X5R-1 402
C2504 1UF 10% 10V X5R 402-1
C2505 1UF 10% 10V X5R 402-1
C2506 1UF 10% 10V X5R 402-1
C2507 1UF 10% 10V X5R 402-1
C2508 0.1UF 20% 10V CERM 402
C2509 0.1UF 20% 10V CERM 402
C2510 0.1UF 20% 10V CERM 402
C2511 0.1UF 20% 10V CERM 402
C2512 0.1UF 20% 10V CERM 402
C2513 0.1UF 20% 10V CERM 402
MCP PCIE (DVDD) Power
=PP1V05_S0_MCP_PEX_DVDD
57 mA (A01)
C2515 4.7UF 20% 4V X5R-1 402
C2516 1UF 10% 10V X5R 402-1
C2517 1UF 10% 10V X5R 402-1
C2518 0.1UF 20% 10V CERM 402
C2519 0.1UF 20% 10V CERM 402
MCP SATA (DVDD) Power
=PP1V05_S0_MCP_SATA_DVDD
43 mA (A01)
C2520 4.7UF 20% 4V X5R-1 402
C2521 0.1UF 20% 10V CERM 402
MCP 1.05V AUX Power
=PP1V05_S5_MCP_VDD_AUXC
105 mA (A01)
C2525 0.1UF 20% 10V CERM 402
C2526 0.1UF 20% 10V CERM 402
MCP 1.05V RMGT Power
=PP1V05_ENET_MCP_RMGT
131 mA (A01)
C2528 4.7UF 20% 4V X5R-1 402
C2529 0.1UF 20% 10V CERM 402
MCP FSB (VTT) Power
NV: 1x 10uF 0805, 1x 4.7uF 0402, 2x 0.1uF 0402 (14.9 uF)
Apple: 7x 2.2uF 0402 (15.4 uF)
=PP1V05_S0_MCP_FSB
1182 mA (A01)
C2530 2.2UF 20% 6.3V CERM 402-LF
C2531 2.2UF 20% 6.3V CERM 402-LF
C2532 2.2UF 20% 6.3V CERM 402-LF
C2533 2.2UF 20% 6.3V CERM 402-LF
C2534 2.2UF 20% 6.3V CERM 402-LF
C2535 2.2UF 20% 6.3V CERM 402-LF
C2536 2.2UF 20% 6.3V CERM 402-LF
MCP Memory Power
=PP1V8R1V5_S0_MCP_MEM
4771 mA (A01, DDR3)
C2540 4.7UF 20% 4V X5R-1 402
C2541 0.1UF 20% 10V CERM 402
C2542 0.1UF 20% 10V CERM 402
C2543 0.1UF 20% 10V CERM 402
C2544 0.1UF 20% 10V CERM 402
C2545 0.1UF 20% 10V CERM 402
C2546 0.1UF 20% 10V CERM 402
C2547 0.1UF 20% 10V CERM 402
C2548 0.1UF 20% 10V CERM 402
C2549 0.1UF 20% 10V CERM 402
MCP 3.3V Power
NV: 1x 4.7uF 0603, 4x 0.1uF 0402 (5.1 uF)
Apple: 4x 2.2uF 0402 (8.8 uF)
=PP3V3_S0_MCP
450 mA (A01)
C2550 2.2UF 20% 6.3V CERM 402-LF
C2551 2.2UF 20% 6.3V CERM 402-LF
C2552 2.2UF 20% 6.3V CERM 402-LF
C2553 2.2UF 20% 6.3V CERM 402-LF
=PP3V3_S0_MCP_PLL_UF
19 mA (A01)
L2555 30-OHM-1.7A 0402
PP3V3_S0_MCP_PLL_USB
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
19 mA (A01)
C2555 2.2UF 20% 6.3V CERM 402-LF
MCP 3.3V AUX/USB Power
NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)
=PP3V3_S5_MCP
266 mA (A01)
C2560 2.2UF 20% 6.3V CERM 402-LF
MCP 3.3V Ethernet Power
NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)
=PP3V3_ENET_MCP_RMGT
83 mA (A01)
C2564 2.2UF 20% 6.3V CERM 402-LF
MCP 3.3V/1.5V HDA Power
NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)
=PP3V3R1V5_S0_MCP_HDA
7 mA (A01)
C2562 2.2UF 20% 6.3V CERM 402-LF
MCP79 Ethernet VRef
=PP3V3_ENET_MCP_RMGT
R2591 1.47K 1% 1/16W MF-LF 402
R2590 1.47K 1% 1/16W MF-LF 402
MCP_MII_VREF
OUT
C2591 0.1UF 20% 10V CERM 402
=PP1V05_ENET_MCP_PLL_MAC
5 mA (A01)
L2595 30-OHM-1.7A 0402
PP1V05_ENET_MCP_PLL_MAC
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
5 mA (A01)
C2595 4.7UF 20% 4V X5R-1 402
C2596 0.1UF 20% 10V CERM 402
=PP1V05_S0_MCP_AVDD_UF
333 mA (A01)
L2570 30-OHM-5A 0603
NV: 1x 10uF 0805, 1x 4.7uF 0402, 2x 1uF 0402, 2x 0.1uF 0402 (16.9 uF)
Apple: 5x 2.2uF 0402 (11 uF)
PP1V05_S0_MCP_PEX_AVDD
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
206 mA (A01)
C2570 2.2UF 20% 6.3V CERM 402-LF
C2571 2.2UF 20% 6.3V CERM 402-LF
C2572 2.2UF 20% 6.3V CERM 402-LF
C2573 2.2UF 20% 6.3V CERM 402-LF
C2574 2.2UF 20% 6.3V CERM 402-LF
L2575 30-OHM-5A 0603
NV: 1x 10uF 0805, 1x 4.7uF 0402, 2x 0.1uF 0402 (14.9 uF)
Apple: 2x 2.2uF 0402 (4.4 uF)
PP1V05_S0_MCP_SATA_AVDD
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
127 mA (A01)
C2575 2.2UF 20% 6.3V CERM 402-LF
C2576 2.2UF 20% 6.3V CERM 402-LF
=PP1V05_S0_MCP_PLL_UF
562 mA (A01)
L2580 30-OHM-1.7A 0402
PP1V05_S0_MCP_PLL_FSB
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
270 mA (A01)
C2592 10UF 20% 6.3V X5R 603
C2580 4.7UF 20% 4V X5R-1 402
C2581 0.1UF 20% 10V CERM 402
L2582 30-OHM-1.7A 0402
PP1V05_S0_MCP_PLL_PEX
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
84 mA (A01)
C2582 4.7UF 20% 4V X5R-1 402
C2583 0.1UF 20% 10V CERM 402
L2584 30-OHM-1.7A 0402
PP1V05_S0_MCP_PLL_SATA
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
84 mA (A01)
C2584 4.7UF 20% 4V X5R-2 402
C2585 0.1UF 20% 10V CERM 402
L2586 30-OHM-1.7A 0402
PP1V05_S0_MCP_PLL_CORE
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
87 mA (A01)
C2586 4.7UF 20% 4V X5R-2 402
C2587 0.1UF 20% 10V CERM 402
L2588 30-OHM-1.7A 0402
PP1V05_S0_MCP_PLL_NV
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
37 mA (A01)
C2588 4.7UF 20% 4V X5R-2 402
C2589 0.1UF 20% 10V CERM 402
C2590 0.1UF 20% 10V CERM 402
SYNC MASTER=T18 MLB
SYNC DATE=04/04/2008
PAGE TITLE
MCP Standard Decoupling
Apple Inc.
DRAWING NUMBER 051-7898
SIZE D
REVISION C.0.0
BRANCH
PAGE 25 OF 109
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>
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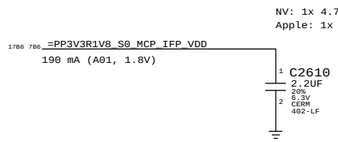
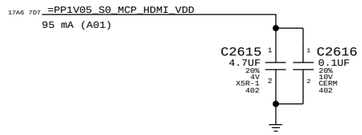
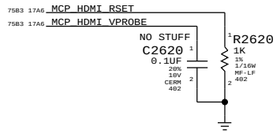
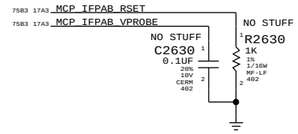
Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

WF: Checklist says 0-ohm resistor placeholder for ferrite bead.
NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)

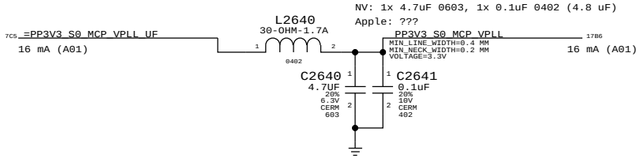




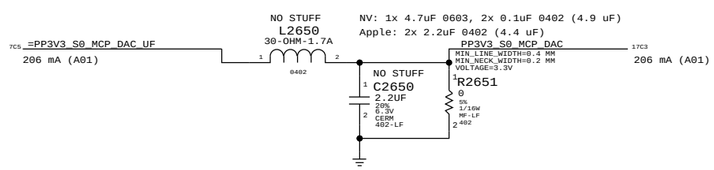




WF: Checklist says 0-ohm resistor placeholder for ferrite bead.
NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: ???



NO STUFF
NV: 1x 4.7uF 0603, 2x 0.1uF 0402 (4.9 uF)
Apple: 2x 2.2uF 0402 (4.4 uF)



SYNC FROM T18
REMOVE MCP 27MHZ CRYSTAL CRICUIT SINCE NOT SUPPORTING TV-OUT
REMOVE DAC TERMINATIONS R2665,C2665 AND R2670 TO R2672
NOSTUFF PP3V3_S0_MCP_DAC RAIL COMPONENTS (L2650 AND C2650)
CHANGE C2651 TO R2651 TO GND PP3V3_S0_MCP_DAC
REMOVE HDCP ROMS

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

SYNC_MASTER=T18_MLB SYNC_DATE=12/12/2007

PAGE TITLE: MCP Graphics Support

Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D
REVISION: C.0.0
BRANCH:
PAGE: 26 OF 109
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

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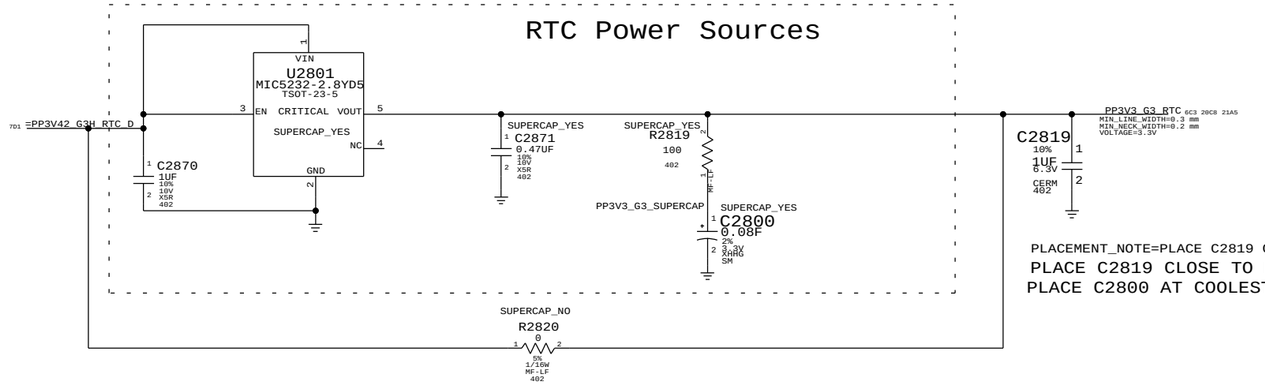
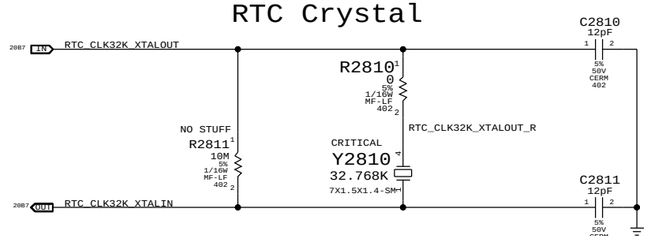
RTC Power Sources

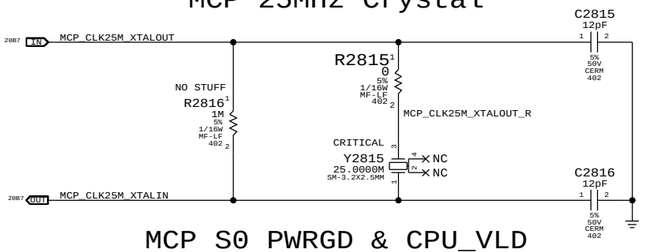


PLACEMENT_NOTE=PLACE C2819 CLOSE TO MCP79
PLACE C2819 CLOSE TO MCP79
PLACE C2800 AT COOLEST SPOT ON MLB

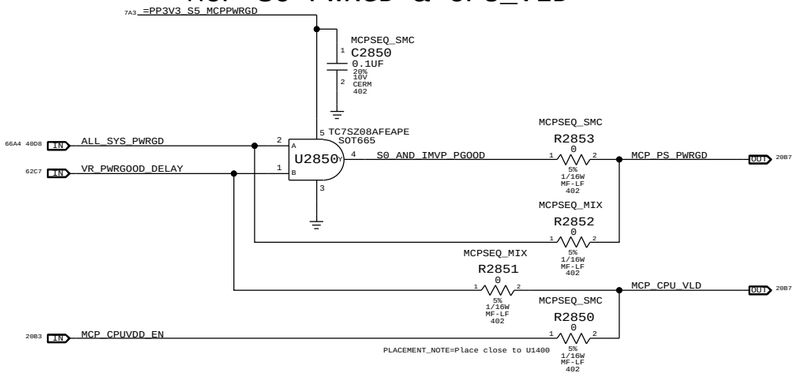
RTC Crystal



MCP 25MHz Crystal



MCP S0 PWRGD & CPU_VLD



MCPSEQ_SMC represents MCP79 'MLB' power sequencing connections, but results in MCP79 ROMSIP sequence happening after CPU powers up.

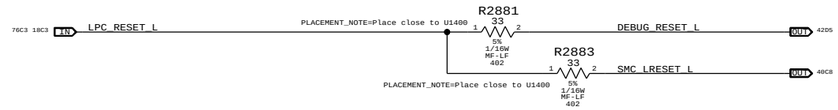
MCPSEQ_MIX is cross between MLB and internal power sequencing, which results in earlier ROMSIP and MCP FSB I/O interface initialization.

SMC 99ms delay from ALL_SYS_PWRGD to IMVP_VR_ON plus IMVP6 delay for VR_PWRGOOD_DELAY should guarantee CPU_VLD does not go high before CPUVDD_EN (which is 40-100ms after PS_PWRGD assertion).

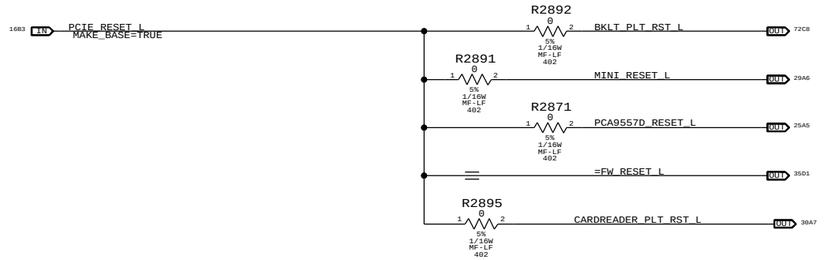
NOTE: If CPU_VLD deasserts during S0 MCP79 will take system to S5 immediately.

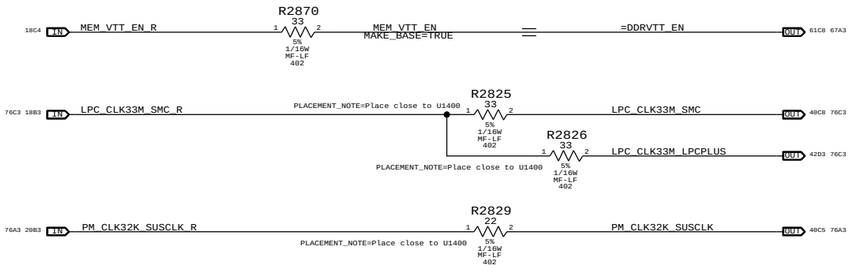
Platform Reset Connections

LPC Reset (Unbuffered)

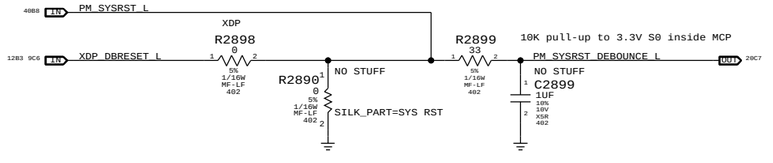


PCIE Reset (Unbuffered)





Reset Button



SYNC FROM T18
CHANGE RESET BUTTOM TO RESET PADS
REMOVE UNUSED PCIE RESET SIGNALS
REMOVE R2824 AND NET PCI_CLK33M_SLOT_A
CHANGE RTC COIN CELL TO LDO & SUPERCAP
ALIAS MEM_VTT_EN TO =DDRVTT_EN
CHANGE Y2810 AND U2850 TO SMALLER PARTS

SYNC MASTER=RAYMOND SYNC DATE=04/05/2008

PAGE TITLE
SB Misc

Apple Inc.

DRAWING NUMBER 051-7898
SIZE D
REVISION C.0.0
BRANCH
PAGE 28 OF 109
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

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Page Notes

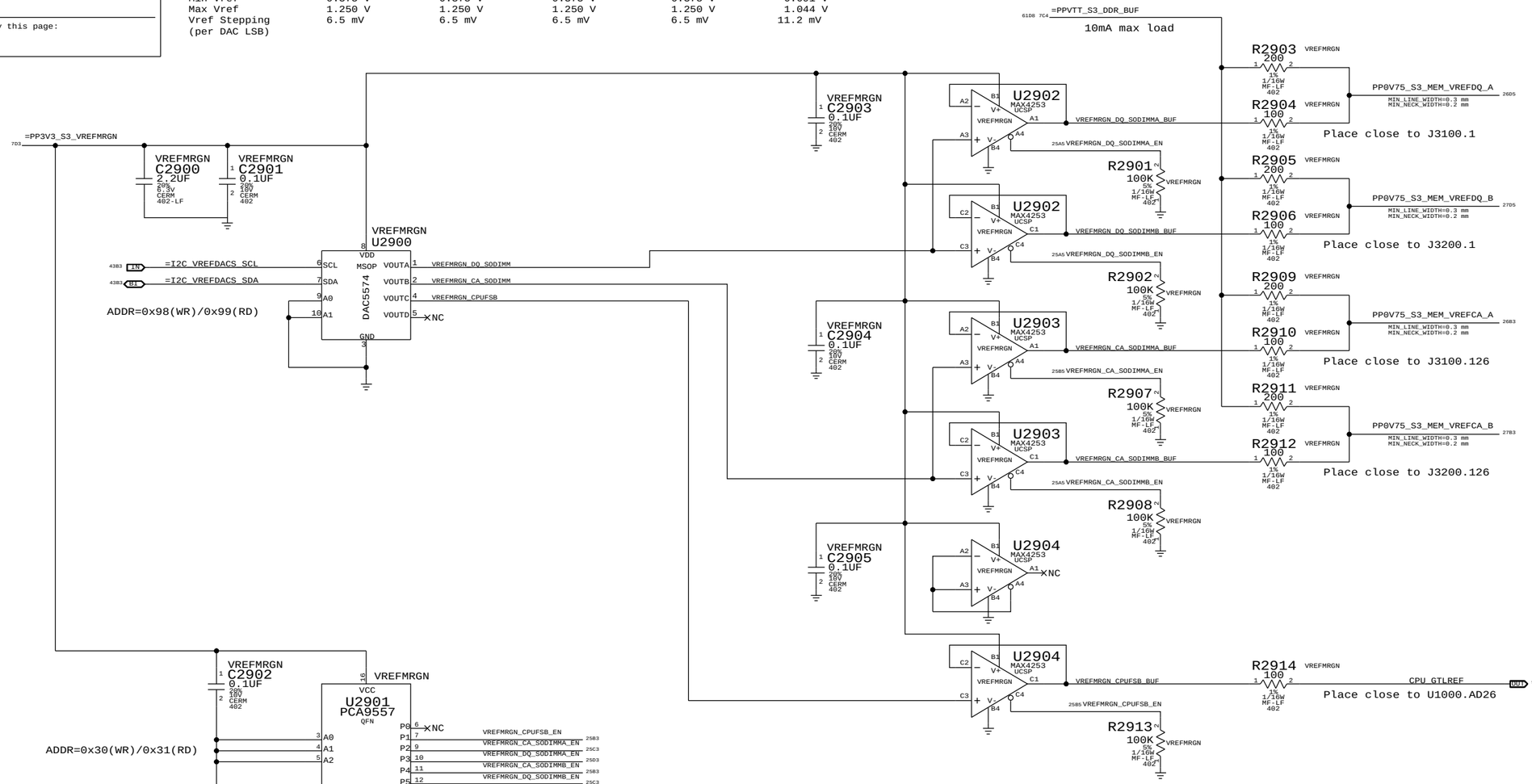
Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PP3V3_S5_VREFMRGN
- =PPVTT_S3_DDR_BUF

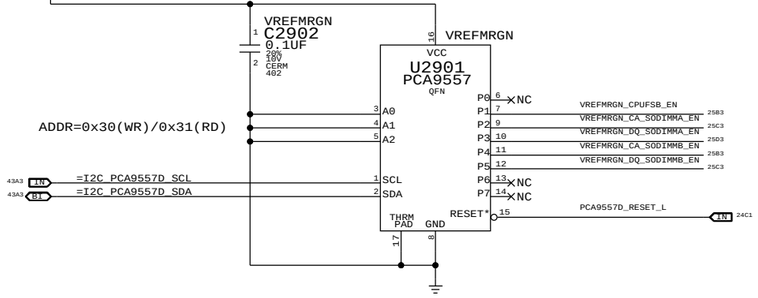
Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
VREFMRGN
NO_VREFMRGN

DAC channel	MEM A VREF DQ	MEM A VREF CA	MEM B VREF DQ	MEM B VREF CA	CPU FSB VREF
	A	B	A	B	C
Min DAC code	0x00	0x00	0x00	0x00	0x00
Max DAC code	0x87	0x87	0x87	0x87	0x55
Max sink I	-3.75 mA	-3.75 mA	-3.75 mA	-3.75 mA	-0.91 mA
Max source I	5 mA	5 mA	5 mA	5 mA	0.52 mA
Nominal Vref	0.75 V	0.75 V	0.75 V	0.75 V	0.70 V
Min Vref	0.375 V	0.375 V	0.375 V	0.375 V	0.091 V
Max Vref	1.250 V	1.250 V	1.250 V	1.250 V	1.044 V
Vref Stepping (per DAC LSB)	6.5 mV	6.5 mV	6.5 mV	6.5 mV	11.2 mV

SO-DIMM A and SO-DIMM B Vref settings should be margined separately
(i.e. not simultaneously) due to current limitation of TPS51116 regulator.





Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2903	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2905	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2909	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2911	CRITICAL	NO_VREFMRGN

SYNC_MASTER=BEN SYNC_DATE=03/31/2008

PAGE TITLE
FSB/DDR3 Vref Margining

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D
REVISION C.0.0
BRANCH
PAGE 29 OF 109
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

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Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_A
- =PP1V5_S3_MEM_A
- =PP0V75_S0_MEM_VTT_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

DDR3 DECOUPLING AND GROUND RETURN CAPS (CONNECTOR SIDE)

7D3 =PP1V5_S3_MEM_A

C3100 10UF 20% 6.3V X5R 603
C3101 10UF 20% 6.3V X5R 603
C3110 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL
C3111 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL
C3112 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL
C3113 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL
C3114 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL
C3115 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL
C3116 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL
C3117 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL

25D1 PP0V75_S3_MEM_VREFDQ_A

C3130 2.2UF 20% 6.3V CERM 402-LF
C3131 0.1UF 20% 10V CERM 402

J3100 F-RT-THB (SYMBOL 2 OF 2) DDR3-SODIMM-DUAL-M97-3

74D3 14A5 IN	MEM_A_CKE<0>	73	CKE0	CKE1	74	MEM_A_CKE<1>	IN 14A5 74D3
		75	VDD	VDD	76		
	NCX	77	NC	A15	78	MEM_A_A<15>	IN 8D2
74D3 14C5 IN	MEM_A_BA<2>	79	BA2	A14	80	MEM_A_A<14>	IN 14C5 74D3
		81	VDD	VDD	82		
74D3 14C5 IN	MEM_A_A<12>	83	A12/BC*	A11	84	MEM_A_A<11>	IN 14C5 74D3
74D3 14C5 IN	MEM_A_A<9>	85	A9	A7	86	MEM_A_A<7>	IN 14C5 74D3
		87	VDD	VDD	88		
74D3 14C5 IN	MEM_A_A<8>	89	A8	A6	90	MEM_A_A<6>	IN 14B5 74D3
74D3 14B5 IN	MEM_A_A<5>	91	A5	A4	92	MEM_A_A<4>	IN 14B5 74D3
		93	VDD	VDD	94		
74D3 14B5 IN	MEM_A_A<3>	95	A3	A2	96	MEM_A_A<2>	IN 14B5 74D3
74D3 14B5 IN	MEM_A_A<1>	97	A1	A0	98	MEM_A_A<0>	IN 14B5 74D3
		99	VDD	VDD	100		
74D3 14B5 IN	MEM_A_CLK_P<0>	101	CK0	CK1	102	MEM_A_CLK_P<1>	IN 14B5 74D3
74D3 14B5 IN	MEM_A_CLK_N<0>	103	CK0*	CK1*	104	MEM_A_CLK_N<1>	IN 14B5 74D3
		105	VDD	VDD	106		
74D3 14C5 IN	MEM_A_A<10>	107	A10/AP	BA1	108	MEM_A_BA<1>	IN 14C5 74D3
74D3 14C5 IN	MEM_A_BA<0>	109	BA0	RAS*	110	MEM_A_RAS_L	IN 14C5 74D3
		111	VDD	VDD	112		
74D3 14C5 IN	MEM_A_WE_L	113	WE*	S0*	114	MEM_A_CS_L<0>	IN 14B5 74D3
74D3 14C5 IN	MEM_A_CAS_L	115	CAS*	ODT0	116	MEM_A_ODT<0>	IN 14B5 74D3
		117	VDD	VDD	118		
74D3 14C5 IN	MEM_A_A<13>	119	A13	ODT1	120	MEM_A_ODT<1>	IN 14B5 74D3
74D3 14B5 IN	MEM_A_CS_L<1>	121	S1*	NC	122		
		123	VDD	VDD	124		
	NCX	125	TEST	VREFCA	126		
		127	VSS	VSS	128		
74D3 14C7 BI	MEM_A_DQ<32>	129	DQ32	DQ36	130	MEM_A_DQ<37>	BI 14C7 74D3
74D3 14C7 BI	MEM_A_DQ<33>	131	DQ33	DQ37	132	MEM_A_DQ<36>	BI 14C7 74D3
		133	VSS	VSS	134		
74C3 14B5 BI	MEM_A_DQS_N<4>	135	DQS4*	DM4	136	MEM_A_DM<4>	IN 14B7 74C3
74C3 14B5 BI	MEM_A_DQS_P<4>	137	DQS4	VSS	138		
		139	VSS	DQ38	140	MEM_A_DQ<35>	BI 14C7 74D3
74D3 14C7 BI	MEM_A_DQ<34>	141	DQ34	DQ39	142	MEM_A_DQ<39>	BI 14C7 74D3
74D3 14C7 BI	MEM_A_DQ<38>	143	DQ35	VSS	144		
		145	VSS	DQ44	146	MEM_A_DQ<40>	BI 14C7 74D3
74D3 14C7 BI	MEM_A_DQ<44>	147	DQ40	DQ45	148	MEM_A_DQ<41>	BI 14C7 74D3
74D3 14C7 BI	MEM_A_DQ<45>	149	DQ41	VSS	150		
		151	VSS	DQS5*	152	MEM_A_DQS_N<5>	BI 14D5 74C3
74C3 14B7 IN	MEM_A_DM<5>	153	DM5	DQS5	154	MEM_A_DQS_P<5>	BI 14D5 74C3
		155	VSS	VSS	156		
74D3 14D7 BI	MEM_A_DQ<47>	157	DQ42	DQ46	158	MEM_A_DQ<43>	BI 14C7 74D3
74D3 14D7 BI	MEM_A_DQ<46>	159	DQ43	DQ47	160	MEM_A_DQ<42>	BI 14C7 74D3
		161	VSS	VSS	162		
74D3 14D7 BI	MEM_A_DQ<49>	163	DQ48	DQ52	164	MEM_A_DQ<53>	BI 14D7 74D3
74D3 14D7 BI	MEM_A_DQ<52>	165	DQ49	DQ53	166	MEM_A_DQ<48>	BI 14D7 74D3
		167	VSS	VSS	168		
74C3 14D5 BI	MEM_A_DQS_N<6>	169	DQS6*	DM6	170	MEM_A_DM<6>	IN 14B7 74C3
74C3 14D5 BI	MEM_A_DQS_P<6>	171	DQS6	VSS	172		
		173	VSS	DQ54	174	MEM_A_DQ<55>	BI 14D7 74D3
74D3 14D7 BI	MEM_A_DQ<54>	175	DQ50	DQ55	176	MEM_A_DQ<50>	BI 14D7 74D3
74D3 14D7 BI	MEM_A_DQ<51>	177	DQ51	VSS	178		
		179	VSS	DQ60	180	MEM_A_DQ<57>	BI 14D7 74D3
74D3 14D7 BI	MEM_A_DQ<61>	181	DQ56	DQ61	182	MEM_A_DQ<56>	BI 14D7 74D3
74D3 14D7 BI	MEM_A_DQ<60>	183	DQ57	VSS	184		
		185	VSS	DQS7*	186	MEM_A_DQS_N<7>	BI 14D5 74C3
74C3 14B7 IN	MEM_A_DM<7>	187	DM7	DQS7	188	MEM_A_DQS_P<7>	BI 14D5 74C3
		189	VSS	VSS	190		
74D3 14D7 BI	MEM_A_DQ<58>	191	DQ58	DQ62	192	MEM_A_DQ<62>	BI 14D7 74D3
74D3 14D7 BI	MEM_A_DQ<59>	193	DQ59	DQ63	194	MEM_A_DQ<63>	BI 14D7 74D3
		195	VSS	VSS	196		
	MEM_A_SA<0>	197	SA0	EVENT*	198	MEM_EVENT_L	OUT 20A4 20B3 27A5 40B8
		199	VDDSPD	SDA	200	=I2C_SODIMMA_SDA	BI 43D6
	MEM_A_SA<1>	201	SA1	SCL	202	=I2C_SODIMMA_SCL	IN 43D6
		203	VTT	VTT	204		

KEY

J3100 F-RT-THB (SYMBOL 1 OF 2) DDR3-SODIMM-DUAL-M97-3

	1	VREFDQ	VSS	2	
	3	VSS	DQ4	4	MEM_A_DQ<4>	BI 14B7 74D3
74D3 14B7 BI MEM_A_DQ<0>	5	DQ0	DQ5	6	MEM_A_DQ<5>	BI 14B7 74D3
74D3 14B7 BI MEM_A_DQ<1>	7	DQ1	VSS	8		
	9	VSS	DQS0*	10	MEM_A_DQS_N<0>	BI 14D5 74C3
74D3 14A7 IN MEM_A_DM<0>	11	DM0	DQS0	12	MEM_A_DQS_P<0>	BI 14D5 74C3
	13	VSS	VSS	14		
74D3 14B7 BI MEM_A_DQ<6>	15	DQ2	DQ6	16	MEM_A_DQ<3>	BI 14B7 74D3
74D3 14B7 BI MEM_A_DQ<7>	17	DQ3	DQ7	18	MEM_A_DQ<2>	BI 14B7 74D3
	19	VSS	VSS	20		
74D3 14B7 BI MEM_A_DQ<8>	21	DQ8	DQ12	22	MEM_A_DQ<9>	BI 14B7 74D3
74D3 14B7 BI MEM_A_DQ<12>	23	DQ9	DQ13	24	MEM_A_DQ<13>	BI 14B7 74D3
	25	VSS	VSS	26		
74C3 14D5 BI MEM_A_DQS_N<1>	27	DQS1*	DM1	28	MEM_A_DM<1>	IN 14A7 74C3
74C3 14D5 BI MEM_A_DQS_P<1>	29	DQS1	RESET*	30	MEM_RESET_L	IN 27C2 28C5
	31	VSS	VSS	32		
74D3 14B7 BI MEM_A_DQ<10>	33	DQ10	DQ14	34	MEM_A_DQ<11>	BI 14B7 74D3
74D3 14B7 BI MEM_A_DQ<15>	35	DQ11	DQ15	36	MEM_A_DQ<14>	BI 14B7 74D3
	37	VSS	VSS	38		
74D3 14C7 BI MEM_A_DQ<25>	39	DQ16	DQ20	40	MEM_A_DQ<29>	BI 14C7 74D3
74D3 14C7 BI MEM_A_DQ<24>	41	DQ17	DQ21	42	MEM_A_DQ<28>	BI 14C7 74D3
	43	VSS	VSS	44		
74C3 14D5 BI MEM_A_DQS_N<3>	45	DQS2*	DM2	46	MEM_A_DM<3>	IN 14B7 74C3
74C3 14D5 BI MEM_A_DQS_P<3>	47	DQS2	VSS	48		
	49	VSS	DQ22	50	MEM_A_DQ<27>	BI 14C7 74D3
74D3 14C7 BI MEM_A_DQ<26>	51	DQ18	DQ23	52	MEM_A_DQ<31>	BI 14C7 74D3
74D3 14C7 BI MEM_A_DQ<30>	53	DQ19	VSS	54		
	55	VSS	DQ28	56	MEM_A_DQ<18>	BI 14B7 74D3
74D3 14C7 BI MEM_A_DQ<20>	57	DQ24	DQ29	58	MEM_A_DQ<17>	BI 14B7 74D3
74D3 14C7 BI MEM_A_DQ<21>	59	DQ25	VSS	60		
	61	VSS	DQS3*	62	MEM_A_DQS_N<2>	BI 14D5 74C3
74C3 14B7 IN MEM_A_DM<2>	63	DM3	DQS3	64	MEM_A_DQS_P<2>	BI 14D5 74C3
	65	VSS	VSS	66		
74D3 14C7 BI MEM_A_DQ<23>	67	DQ26	DQ30	68	MEM_A_DQ<19>	BI 14B7 74D3
74D3 14B7 BI MEM_A_DQ<16>	69	DQ27	DQ31	70	MEM_A_DQ<22>	BI 14C7 74D3
	71	VSS	VSS	72		

KEY

516-0201

CRITICAL

PP0V75_S3_MEM_VREFCA_A 25C1

C3135 2.2UF 20% 6.3V CERM 402-LF
C3136 0.1UF 20% 10V CERM 402

7C5 =PPSPD_S0_MEM_A

C3140 2.2UF 20% 6.3V CERM 402-LF
R3140 10K 5% 1/16W MF-LF 402
R3141 10K 5% 1/16W MF-LF 402

516-0201
SPD ADDR=0xA0(WR)/0xA1(RD)

C3150 2.2UF 20% 6.3V CERM 402-LF
C3151 2.2UF 20% 6.3V CERM 402-LF

=PP0V75_S0_MEM_VTT_A 7C7

"Factory" (top) slot

SYNC_MASTER=BEN SYNC_DATE=06/30/2008

PAGE TITLE: DDR3 SO-DIMM Connector A

Apple Inc.

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SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

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DDR3 DECOUPLING AND GROUND RETURN CAPS (CONNECTOR SIDE)

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_B
- =PP1V5_S3_MEM_B
- =PP0V75_S0_MEM_VTT_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:
(NONE)

7D3 =PP1V5_S3_MEM_B

C3200 10UF 20% 6.3V X5R 603
C3201 10UF 20% 6.3V X5R 603
C3210 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL
C3211 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL
C3212 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL
C3213 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL
C3214 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL
C3215 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL
C3216 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL
C3217 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL

25C1 PP0V75_S3_MEM_VREFDQ_B

C3230 2.2UF 20% 6.3V CERM 402-LF
C3231 0.1UF 20% 10V CERM 402

J3200 DDR3-SODIMM (2 OF 2) F-RT-BGA3

74B3 14A1	IN	MEM_B_CKE<0>	73 CKE0	CKE1 74	MEM_B_CKE<1> IN 14A1 74B3
			75 VDD	VDD 76	
			77 NC	A15 78	MEM_B_A<15> IN 8D2
74B3 14C1	IN	MEM_B_BA<2>	79 BA2	A14 80	MEM_B_A<14> IN 14C1 74B3
			81 VDD	VDD 82	
74B3 14C1	IN	MEM_B_A<12>	83 A12/BC*	A11 84	MEM_B_A<11> IN 14C1 74B3
74B3 14C1	IN	MEM_B_A<9>	85 A9	A7 86	MEM_B_A<7> IN 14C1 74B3
			87 VDD	VDD 88	
74B3 14C1	IN	MEM_B_A<8>	89 A8	A6 90	MEM_B_A<6> IN 14B1 74B3
74B3 14B1	IN	MEM_B_A<5>	91 A5	A4 92	MEM_B_A<4> IN 14B1 74B3
			93 VDD	VDD 94	
74B3 14B1	IN	MEM_B_A<3>	95 A3	A2 96	MEM_B_A<2> IN 14B1 74B3
74B3 14B1	IN	MEM_B_A<1>	97 A1	A0 98	MEM_B_A<0> IN 14B1 74B3
			99 VDD	VDD 100	
74C3 14B1	IN	MEM_B_CLK_P<0>	101 CK0	CK1 102	MEM_B_CLK_P<1> IN 14B1 74C3
74C3 14B1	IN	MEM_B_CLK_N<0>	103 CK0*	CK1* 104	MEM_B_CLK_N<1> IN 14B1 74C3
			105 VDD	VDD 106	
74B3 14C1	IN	MEM_B_A<10>	107 A10/AP	BA1 108	MEM_B_BA<1> IN 14C1 74B3
74B3 14C1	IN	MEM_B_BA<0>	109 BA0	RAS* 110	MEM_B_RAS_L IN 14C1 74B3
			111 VDD	VDD 112	
74B3 14C1	IN	MEM_B_WE_L	113 WE*	S0* 114	MEM_B_CS_L<0> IN 14B1 74B3
74B3 14C1	IN	MEM_B_CAS_L	115 CAS*	ODT0 116	MEM_B_ODT<0> IN 14B1 74B3
			117 VDD	VDD 118	
74B3 14C1	IN	MEM_B_A<13>	119 A13	ODT1 120	MEM_B_ODT<1> IN 14B1 74B3
74B3 14B1	IN	MEM_B_CS_L<1>	121 S1*	NC 122	
			123 VDD	VDD 124	
			125 TEST	VREFCA 126	
			127 VSS	VSS 128	
74B3 14C2	BI	MEM_B_DQ<37>	129 DQ32	DQ36 130	MEM_B_DQ<36> BI 14C3 74B3
74B3 14C2	BI	MEM_B_DQ<32>	131 DQ33	DQ37 132	MEM_B_DQ<33> BI 14C3 74B3
			133 VSS	VSS 134	
74A3 14D1	BI	MEM_B_DQS_N<4>	135 DQS4*	DM4 136	MEM_B_DM<4> IN 14B3 74B3
74A3 14D1	BI	MEM_B_DQS_P<4>	137 DQS4	VSS 138	
74B3 14C2	BI	MEM_B_DQ<35>	141 DQ34	DQ38 140	MEM_B_DQ<38> BI 14C3 74B3
74B3 14C2	BI	MEM_B_DQ<39>	143 DQ35	DQ39 142	MEM_B_DQ<34> BI 14C3 74B3
			145 VSS	VSS 144	
74B3 14C2	BI	MEM_B_DQ<45>	147 DQ40	DQ44 146	MEM_B_DQ<40> BI 14C3 74B3
74B3 14C2	BI	MEM_B_DQ<41>	149 DQ41	DQ45 148	MEM_B_DQ<44> BI 14C3 74B3
			151 VSS	VSS 150	
74B3 14B3	IN	MEM_B_DM<5>	153 DM5	DQS5* 152	MEM_B_DQS_N<5> BI 14D1 74A3
			155 VSS	DQS5 154	MEM_B_DQS_P<5> BI 14D1 74A3
74B3 14D2	BI	MEM_B_DQ<46>	157 DQ42	VSS 156	
74B3 14D2	BI	MEM_B_DQ<47>	159 DQ43	DQ46 158	MEM_B_DQ<42> BI 14C3 74B3
			161 VSS	DQ47 160	MEM_B_DQ<43> BI 14C3 74B3
74B3 14D2	BI	MEM_B_DQ<53>	163 DQ48	VSS 162	
74B3 14D2	BI	MEM_B_DQ<49>	165 DQ49	DQ52 164	MEM_B_DQ<52> BI 14D3 74B3
			167 VSS	DQ53 166	MEM_B_DQ<48> BI 14D3 74B3
74A3 14D1	BI	MEM_B_DQS_N<6>	169 DQS6*	VSS 168	
74A3 14D1	BI	MEM_B_DQS_P<6>	171 DQS6	DM6 170	MEM_B_DM<6> IN 14B3 74B3
			173 VSS	VSS 172	
74B3 14D2	BI	MEM_B_DQ<55>	175 DQ50	DQ54 174	MEM_B_DQ<51> BI 14D3 74B3
74B3 14D2	BI	MEM_B_DQ<54>	177 DQ51	DQ55 176	MEM_B_DQ<50> BI 14D3 74B3
			179 VSS	VSS 178	
74B3 14D2	BI	MEM_B_DQ<56>	181 DQ56	DQ60 180	MEM_B_DQ<63> BI 14D3 74B3
74B3 14D2	BI	MEM_B_DQ<58>	183 DQ57	DQ61 182	MEM_B_DQ<59> BI 14D3 74B3
			185 VSS	VSS 184	
74B3 14B3	IN	MEM_B_DM<7>	187 DM7	DQS7* 186	MEM_B_DQS_N<7> BI 14D1 74A3
			189 VSS	DQS7 188	MEM_B_DQS_P<7> BI 14D1 74A3
74B3 14D2	BI	MEM_B_DQ<61>	191 DQ58	VSS 190	
74B3 14D2	BI	MEM_B_DQ<60>	193 DQ59	DQ62 192	MEM_B_DQ<62> BI 14D3 74B3
			195 VSS	DQ63 194	MEM_B_DQ<57> BI 14D3 74B3
		MEM_B_SA<0>	197 SA0	VSS 196	
			199 VDDSPD	EVENT* 198	MEM_EVENT_L OUT 20A4 20B3 26A5 40B8
		MEM_B_SA<1>	201 SA1	SDA 200	=I2C_SODIMMB_SDA BI 43C6
			203 VTT	SCL 202	=I2C_SODIMMB_SCL IN 43C6
			MTG PINS	VTT 204	=PP0V75_S0_MEM_VTT_B 7C7
			205 MTG PIN	MTG PIN 206	
			207 MTG PIN	MTG PIN 208	
			209 MTG PIN	MTG PIN 210	
			211 MTG PIN	MTG PIN 212	

7C5 =PPSPD_S0_MEM_B

R3240 10K 5% 1/16W MF-LF 402
C3240 2.2UF 20% 6.3V CERM 402-LF
R3241 10K 5% 1/16W MF-LF 402

C3235 2.2UF 20% 6.3V CERM 402-LF
C3236 0.1UF 20% 10V CERM 402
C3250 2.2UF 20% 6.3V CERM 402-LF
C3251 2.2UF 20% 6.3V CERM 402-LF

516S0706
SPD ADDR=0xA2(WR)/0xA3(RD)

J3200 DDR3-SODIMM (1 OF 2) F-RT-BGA3

			1 VREFDQ	VSS 2	
			3 VSS	DQ4 4	MEM_B_DQ<4> BI 14B3 74B3
74B3 14B3	BI	MEM_B_DQ<1>	5 DQ0	DQ5 6	MEM_B_DQ<5> BI 14B3 74B3
74B3 14B3	BI	MEM_B_DQ<0>	7 DQ1	VSS 8	
			9 VSS	DQS0* 10	MEM_B_DQS_N<0> BI 14D1 74A3
74B3 14A3	IN	MEM_B_DM<0>	11 DM0	DQS0 12	MEM_B_DQS_P<0> BI 14D1 74A3
			13 VSS	VSS 14	
74B3 14B3	BI	MEM_B_DQ<3>	15 DQ2	DQ6 16	MEM_B_DQ<7> BI 14B3 74B3
74B3 14B3	BI	MEM_B_DQ<6>	17 DQ3	DQ7 18	MEM_B_DQ<2> BI 14B3 74B3
			19 VSS	VSS 20	
74B3 14B3	BI	MEM_B_DQ<13>	21 DQ8	DQ12 22	MEM_B_DQ<12> BI 14B3 74B3
74B3 14B3	BI	MEM_B_DQ<14>	23 DQ9	DQ13 24	MEM_B_DQ<9> BI 14B3 74B3
			25 VSS	VSS 26	
74A3 14D1	BI	MEM_B_DQS_N<1>	27 DQS1*	DM1 28	MEM_B_DM<1> IN 14A3 74B3
74A3 14D1	BI	MEM_B_DQS_P<1>	29 DQS1	RESET* 30	MEM_RESET_L IN 26C2 28C5
			31 VSS	VSS 32	
74B3 14B3	BI	MEM_B_DQ<15>	33 DQ10	DQ14 34	MEM_B_DQ<8> BI 14B3 74B3
74B3 14B3	BI	MEM_B_DQ<10>	35 DQ11	DQ15 36	MEM_B_DQ<11> BI 14B3 74B3
			37 VSS	VSS 38	
74B3 14C3	BI	MEM_B_DQ<20>	39 DQ16	DQ20 40	MEM_B_DQ<16> BI 14B3 74B3
74B3 14B3	BI	MEM_B_DQ<17>	41 DQ17	DQ21 42	MEM_B_DQ<21> BI 14C3 74B3
			43 VSS	VSS 44	
74A3 14D1	BI	MEM_B_DQS_N<2>	45 DQS2*	DM2 46	MEM_B_DM<2> IN 14B3 74B3
74A3 14D1	BI	MEM_B_DQS_P<2>	47 DQS2	VSS 48	
			49 VSS	DQ22 50	MEM_B_DQ<18> BI 14B3 74B3
74B3 14C3	BI	MEM_B_DQ<22>	51 DQ18	DQ23 52	MEM_B_DQ<23> BI 14C3 74B3
74B3 14B3	BI	MEM_B_DQ<19>	53 DQ19	VSS 54	
			55 VSS	DQ28 56	MEM_B_DQ<29> BI 14C3 74B3
74B3 14C3	BI	MEM_B_DQ<24>	57 DQ24	DQ29 58	MEM_B_DQ<25> BI 14C3 74B3
74B3 14C3	BI	MEM_B_DQ<28>	59 DQ25	VSS 60	
			61 VSS	DQS3* 62	MEM_B_DQS_N<3> BI 14D1 74A3
74B3 14B3	IN	MEM_B_DM<3>	63 DM3	DQS3 64	MEM_B_DQS_P<3> BI 14D1 74A3
			65 VSS	VSS 66	
74B3 14C3	BI	MEM_B_DQ<26>	67 DQ26	DQ30 68	MEM_B_DQ<30> BI 14C3 74B3
74B3 14C3	BI	MEM_B_DQ<31>	69 DQ27	DQ31 70	MEM_B_DQ<27> BI 14C3 74B3
			71 VSS	VSS 72	

516S0706

DDR3 GROUND RETURN CAPS (MCP SIDE)

7B6 =PP1V5_S0_MEM_MCP

C3222 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL
C3223 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL
C3224 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL
C3225 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL
C3226 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL
C3227 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL
C3228 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL
C3229 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL

"Expansion" (bottom) slot

SYNC_MASTER=BEN SYNC_DATE=05/09/2008
PAGE TITLE: DDR3 SO-DIMM Connector B

Apple Inc.

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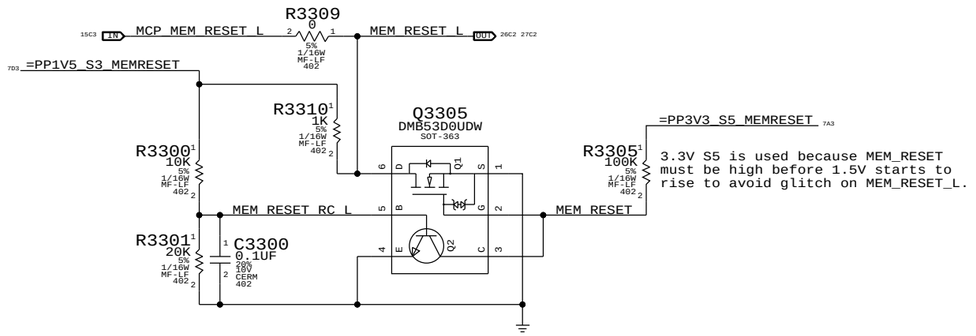
DDR3 RESET Support

Required becaues MCP79 does not meet DDR3 spec power-up reset timing requirement.



SYNC_MASTER=T18_MLB SYNC_DATE=04/04/2008

PAGE TITLE: DDR3 Support

Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D

REVISION: C.0.0

BRANCH:

PAGE: 33 OF 109

SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

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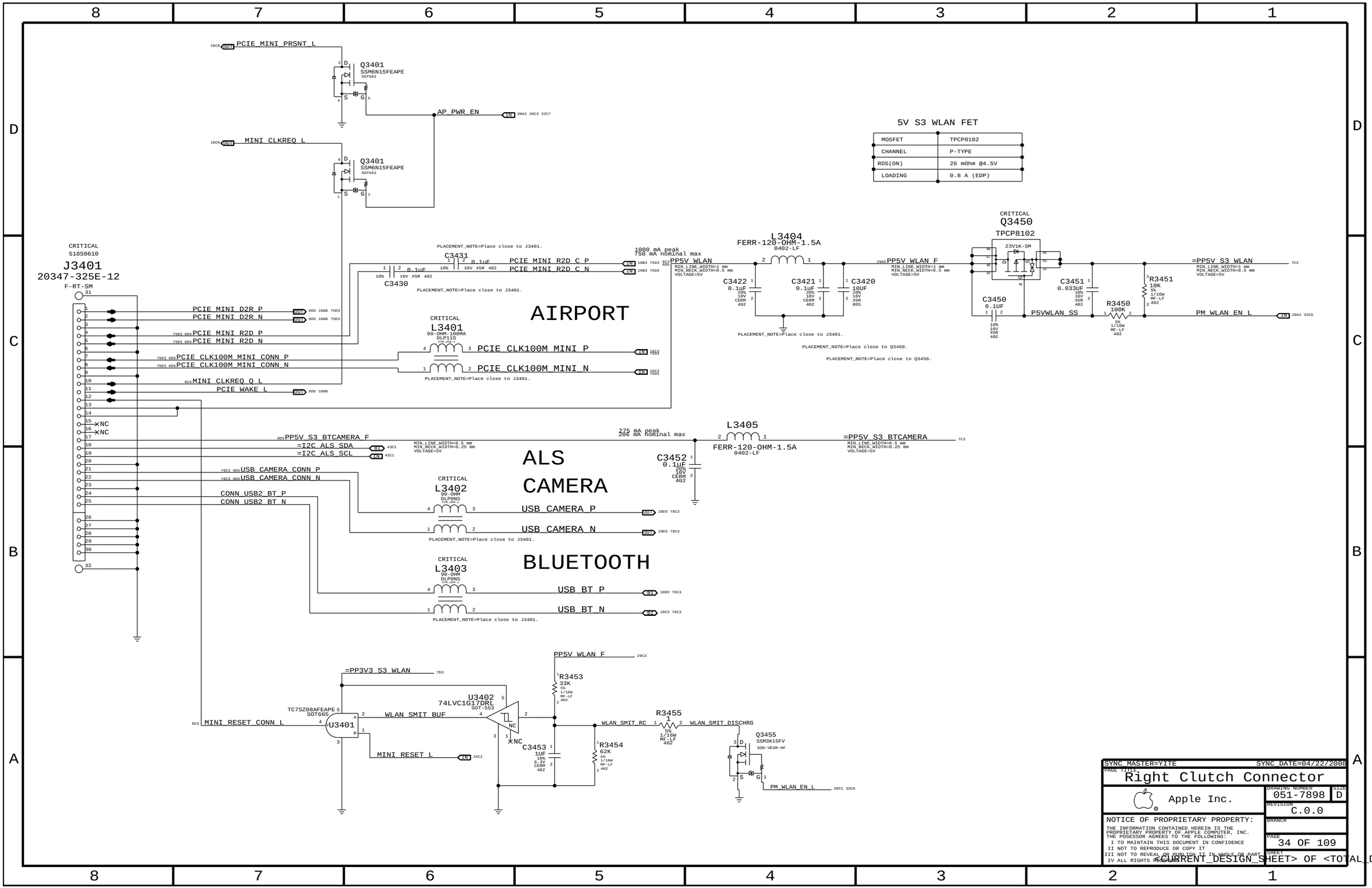

SYNC_MASTER=YITE SYNC_DATE=04/22/2008

PAGE TITLE: Right Clutch Connector

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D

REVISION C.0.0

BRANCH

PAGE 34 OF 109

SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

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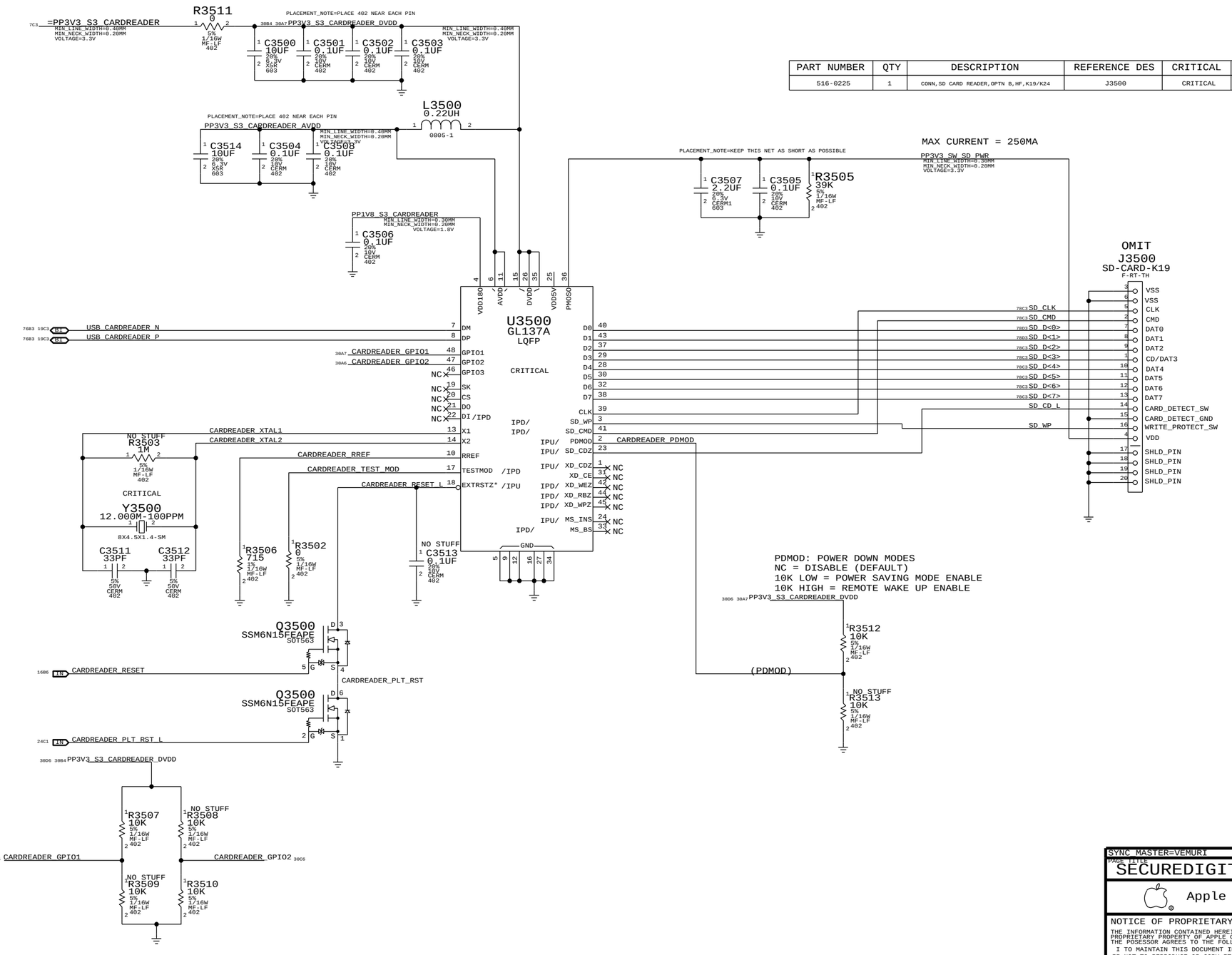
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
516-0225	1	CONN,SD CARD READER,OPTN B,HF,K19/K24	J3500	CRITICAL	



SYNC_MASTER=VEMURI SYNC_DATE=01/30/2009

PAGE TITLE: SECUREDIGITAL CARD READER

Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D

REVISION: C.0.0

BRANCH:

PAGE: 35 OF 109

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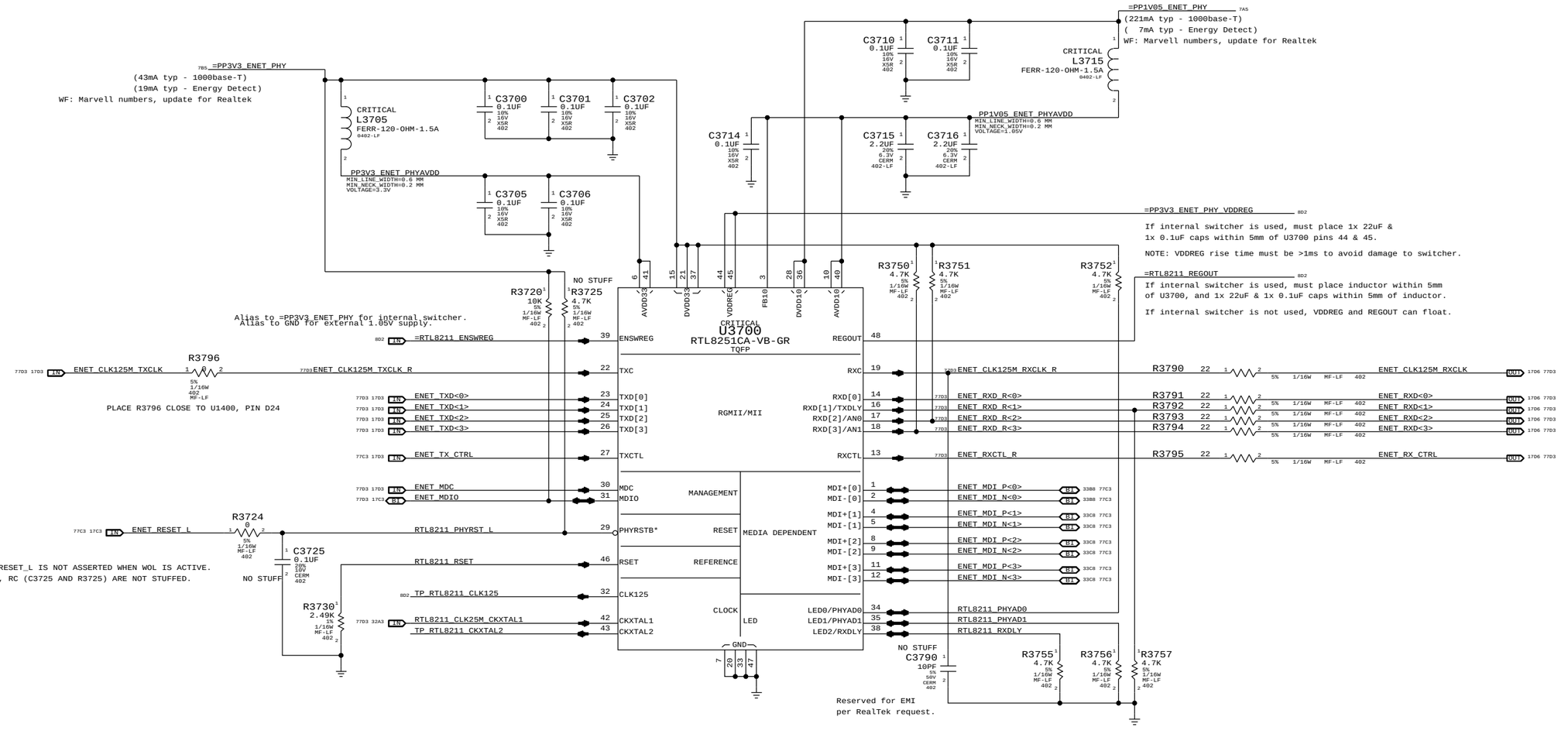

Configuration Settings:

PHYAD = 01 (PHY Address 00001)
AN[1:0] = 11 (Full auto-negotiation)
RXDLY = 0 (RXCLK transitions with data)
TXDLY = 0 (No TXCLK Delay)

SYNC_MASTER=SUMA SYNC_DATE=05/23/2008

PAGE TITLE: Ethernet PHY (RTL8211CL)

Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D
REVISION: C.0.0
BRANCH:
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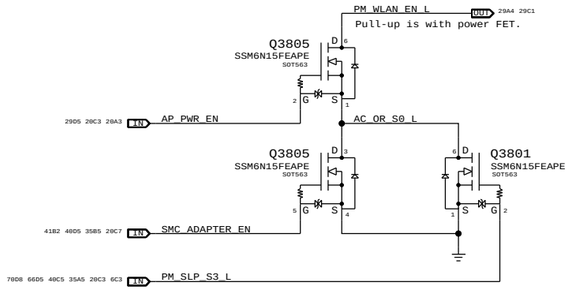
WLAN Enable Generation

"WLAN" = ("S3" && "AP_PWR_EN" && ("AC" || "S0"))

NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.

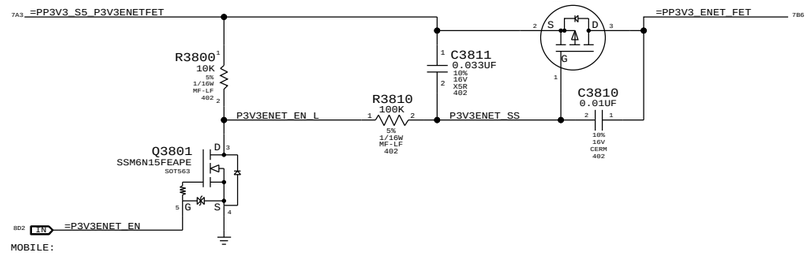


3.3V ENET FET

@ 2.5V Vgs:
Rds(on) = 90mOhm max
I(max) = 1.7A (85C)

CRITICAL

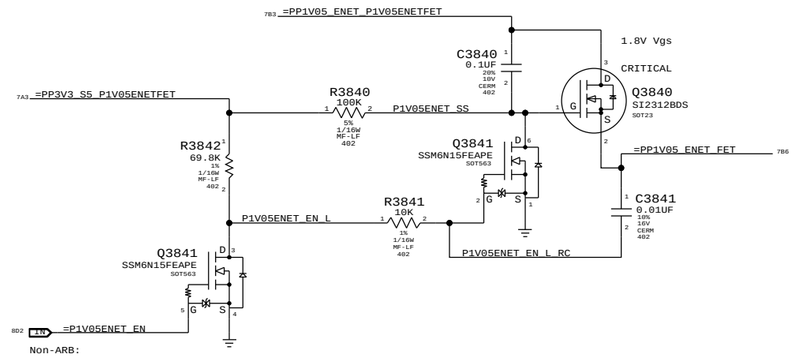
Q3810
NTR4101P
SOT-23-HF



MOBILE:

Recommend aliasing PM_SLP_RMGT_L and =P3V3ENET_EN. Nets separated on ARB for alternate power options.

1.05V ENET FET



Non-ARB:

Recommend aliasing PM_SLP_RMGT_L and =P1V05ENET_EN. Nets separated on ARB for alternate power options.

RTL8211 25MHz Clock

NOTE: MCP79 can provide 25MHz clock, but clock runs whenever RMGT rails are powered.
Designs must ensure PHY is powered whenever RMGT rails are, or use separate crystal.

PLACEMENT_NOTE=Place close to U1400

SYNC MASTER=SUMA SYNC DATE=07/07/2008

PAGE TITLE
Ethernet & AirPort Support

Apple Inc.

DRAWING NUMBER 051-7898
SIZE D
REVISION C.0.0
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PAGE 38 OF 109
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

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- COPY THIS PAGE FROM K36 CSA.39

PLACE ONE CAP EACH NEAR PINS 3 AND 4 OF T3901 AND T3902

ENET_CONN_CTAP

C3900 0.1UF 10% 16V X5R 402
C3901 0.1UF 10% 16V X5R 402
C3902 0.1UF 10% 16V X5R 402
C3903 0.1UF 10% 16V X5R 402

CRITICAL
T3901
SM
TX
TLA-6T213HF
RX

CRITICAL
T3902
SM
TX
TLA-6T213HF
RX

77C3 31B3 B1 ENET_MDI_P<1>
77C3 31B3 B1 ENET_MDI_N<1>
77C3 31B3 B1 ENET_MDI_P<3>
77C3 31B3 B1 ENET_MDI_N<3>
77C3 31B3 B1 ENET_MDI_N<2>
77C3 31B3 B1 ENET_MDI_P<2>
77C3 31B3 B1 ENET_MDI_N<0>
77C3 31B3 B1 ENET_MDI_P<0>

77C3 ENET_MDI_TRAN_P<1>
77C3 ENET_MDI_TRAN_N<1>
77C3 ENET_MDI_TRAN_P<3>
77C3 ENET_MDI_TRAN_N<3>
77C3 ENET_MDI_TRAN_N<2>
77C3 ENET_MDI_TRAN_P<2>
77C3 ENET_MDI_TRAN_N<0>
77C3 ENET_MDI_TRAN_P<0>

ENET_CENTER_TAP<1> R3903 75 1% 1/16W MF-LF 402
ENET_CENTER_TAP<3> R3902 75 1% 1/16W MF-LF 402
ENET_CENTER_TAP<2> R3901 75 1% 1/16W MF-LF 402
ENET_CENTER_TAP<0> R3900 75 1% 1/16W MF-LF 402

C3911 10PF 5% 50V CERM 402-1 CRITICAL
C3912 10PF 5% 50V CERM 402-1 CRITICAL
C3913 10PF 5% 50V CERM 402-1 CRITICAL
C3914 10PF 5% 50V CERM 402-1 CRITICAL
C3915 10PF 5% 50V CERM 402-1 CRITICAL
C3916 10PF 5% 50V CERM 402-1 CRITICAL
C3917 10PF 5% 50V CERM 402-1 CRITICAL
C3918 10PF 5% 50V CERM 402-1 CRITICAL

PLACEMENT_NOTE=PLACE C3911-C3918 ON MDI LINES WITHOUT ANY STUBS

ENET_BOB_SMITH_CAP
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.25MM

CRITICAL
C3910 1000PF 10% 2KV CERM 1206

ETHERNET CONNECTOR

CRITICAL
J3900
RJ45-M97-3
F-RT-TH

514-0636

SYNC MASTER=SUMA SYNC DATE=04/04/2008

PAGE TITLE
ETHERNET CONNECTOR

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D
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PAGE 39 OF 109
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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0558	1	RES,0.68 OHM,1%,0402,SMD	R4100	CRITICAL	

OMIT
R4100
0
5%
1/10W
MF-LF
402

35D3 7A1 =PP1V0_FW_FWPHY
135 mA
PP1V0_FW_R

L4110
120-OHM-0.3A-EMI
0402-LF
PP1V0_FW_FWPHY_AVDD
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.0V

110 mA Digital Core
C4100 1UF 10% 6.3V CERM 402
C4101 1UF 10% 6.3V CERM 402
C4102 1UF 10% 6.3V CERM 402
C4103 1UF 10% 6.3V CERM 402
C4104 1UF 10% 6.3V CERM 402
C4105 1UF 10% 6.3V CERM 402
C4106 1UF 10% 6.3V CERM 402

25 mA PCIe SerDes
C4110 1UF 10% 6.3V CERM 402
C4111 1UF 10% 6.3V CERM 402

7 mA I/O
C4120 1UF 10% 6.3V CERM 402
C4121 1UF 10% 6.3V CERM 402
C4122 1UF 10% 6.3V CERM 402
C4123 1UF 10% 6.3V CERM 402
C4124 1UF 10% 6.3V CERM 402

=PP3V3_FW_FWPHY
781 34B1 35D8 36B6 36D5
138 mA

L4130
120-OHM-0.3A-EMI
0402-LF

114 mA FireWire PHY
PP3V3_FW_FWPHY_VDDA
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
C4130 1UF 10% 6.3V CERM 402
C4131 1UF 10% 6.3V CERM 402
C4132 1UF 10% 6.3V CERM 402

L4135
120-OHM-0.3A-EMI
0402-LF

17 mA PCIe SerDes
PP3V3_FW_FWPHY_VP25
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
C4135 1UF 10% 6.3V CERM 402
C4136 1UF 10% 6.3V CERM 402

0 mA VReg PWR
C4141 0.1UF 20% 16V CERM 402
C4140 1UF 10% 6.3V CERM 402

VDD10 VDD33 VDDH VP VP25 VREG_PWR

CRITICAL
U4100
FW643E
BGA

NC ATBUSB B13
NC ATBUSH A13
NC ATBUSN A11
=FW_PHY_DS0 DS0 (IPD) NT-19 F12
=FW_PHY_DS1 DS1 (IPD) NT-20 E12
=FW_PHY_DS2 DS2 (IPD) NT-21 E13

PCIE_RXD0N N8 75D3 PCIE_FW_R2D_N
PCIE_RXD0P N7 75D3 PCIE_FW_R2D_P
PCIE_TXD0N N5 75D3 PCIE_FW_D2R_C_N
PCIE_TXD0P N6 75D3 PCIE_FW_D2R_C_P

PLACEMENT_NOTE=Place C4170 close to U1400
PLACEMENT_NOTE=Place C4171 close to U1400
C4170 0.1UF 10% 16V X5R 402 PCIE_FW_R2D_C_N IN 16B3 75D3
C4171 0.1UF 10% 16V X5R 402 PCIE_FW_R2D_C_P IN 16B3 75D3
C4175 0.1UF 10% 16V X5R 402 PCIE_FW_D2R_N OUT 16B6 75D3
C4176 0.1UF 10% 16V X5R 402 PCIE_FW_D2R_P OUT 16B6 75D3
PLACEMENT_NOTE=Place C4175 close to U4000
PLACEMENT_NOTE=Place C4176 close to U4000

PCI EXPRESS PHY
REFCLKN N9 PCIE_CLK100M_FW_N IN 16C3
REFCLKP N10 PCIE_CLK100M_FW_P IN 16C3

TEST CONTROLLER
NT-4 (IPU) TCK M4 TP_FW643_TCK
NT-3 (IPU) TDI N2 TP_FW643_TDI
(IPU) TDO M1 TP_FW643_TDO
NT-1 (IPU) TMS M3 TP_FW643_TMS
NT-2 (IPU) TRST* N1 FW643_TRST_L

1394 PHY

FIXME!!! - TYPO IN SYMBOL REGCTL
POWER MANAGEMENT
NT-10 (IPD) WAKE* C2 =FW_PME_L OUT 8C2 35C8
REGCLT D13 FW643_REGCTL
VAUX_DETECT E1 FW643_VAUX_DETECT
NT-12 (IPD) VAUX_DISABLE D2 TP_FW643_VAUX_ENABLE
NT-13 (OD) CLKREQN L2 =FW_CLKREQ_L OUT 35C4

=PP3V3_FW_FWPHY
781 34D2 35D8 36B6 36D5
FW643_LDO
R4165 10K 5% 1/10W MF-LF 402
R4166 10K 5% 1/10W MF-LF 402
R4164 10K 5% 1/10W MF-LF 402

SCIF
NT-16 (IPD) SCIFCLK G2 TP_FW643_SCIFCLK
NT-14 (IPD) SCIFDAIN G1 TP_FW643_SCIFDAIN
NT-17 SCIFDOUT H1 TP_FW643_SCIFDOUT
NT-15 (IPD) SCIFMC F2 TP_FW643_SCIFMC

SERIAL EEPROM CONTROLLER
NT-7 SCL N12 FW643_SCL
NT-6 SDA M11 TP_FW643_SDA

CHIP RESET
NT-5 PERST* N4 FW_RESET_L IN 35C1
R4163 10K 5% 1/10W MF-LF 402

36C4 =PPVP_FW_PHY_CPS
R4160 200K 1% 1/10W MF-LF 402
C4150 22PF 5% 50V CERM 402
C4151 22PF 5% 50V CERM 402
FW_CLK24P576M_XO
CRITICAL
Y4150 24.576MHZ SM-3.2X2.5MM
NC
NC
R4150 412 1% 1/10W MF-LF 402
R4161 2.94K 1% 1/10W MF-LF 402
R4170 191 1% 1/10W MF-LF 402
R4162 470K 5% 1/10W MF-LF 402
C4162 0.33UF 10% 6.3V CERM-X5R 402

FW_P0_TPA_N B8 TPA0N
FW_P0_TPA_P A8 TPA0P
FW_P1_TPA_N B5 TPA1N
FW_P1_TPA_P A5 TPA1P
FW_P2_TPA_N B3 TPA2N
FW_P2_TPA_P A3 TPA2P
FW_P0_TPB_N B9 TPB0N
FW_P0_TPB_P A9 TPB0P
FW_P1_TPB_N B6 TPB1N
FW_P1_TPB_P A6 TPB1P
FW_P2_TPB_N B4 TPB2N
FW_P2_TPB_P A4 TPB2P
FW_P0_TPBIAS B7 TPBIAS0
FW_P1_TPBIAS C3 TPBIAS1
FW_P2_TPBIAS A2 TPBIAS2
FW643_R0 B11 R0
FW643_TPCPS B10 TPCPS

TP_FW643_NAND_TREE K1 NAND_TREE NT-OUT
FW643_REXT L8 REXT
FW_CLK24P576M_XO_R F13 XO
FW_CLK24P576M_XI G13 XI NT-9

NOTE: NT-xx notes show NAND tree order.

TP_FW643_SE M13 SE (IPD)
TP_FW643_SM N13 SM (IPD)
TP_FW643_MODE_A J2 MODE_A (IPD) NT-18
TP_FW643_CE L13 CE (IPD)
TP_FW643_FW620_L D12 FW620* (IPU)
TP_FW643_JASI_EN D1 JASI_EN (IPD) NT-11
TP_FW643_AVREG A10 AVREG
TP_FW643_VBUF H13 VBUF
FW643_PU_RST_L K13 FW_RESET* (IPU) NT-8
TP_FW643_OCR10_CTL J12 OCR_CTL_V10
NC OCR_CTL_V12 (Reserved) J13

MISCELLANEOUS

VSS VREG_VSS

SYNC_MASTER=K19_MLB	SYNC_DATE=11/02/2008
PAGE TITLE	FireWire LLC/PHY (FW643)
Apple Inc.	DRAWING NUMBER 051-7898 SIZE D
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Page Notes

Power aliases required by this page:
- =PPBUS_S5_FWPWRSW (system supply for bus power)
- =PP3V3_FW_LATEVG_ACTIVE
- =PPVP_FW_SUMNODE (power passthru summation node)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:

3.3V FW FET

@ 2.5V Vgs:
Rds(on) = 90mOhm max
I(max) = 1.7A (85C)

=PP3V3_S0_P3V3FWFET
R4290 10K 5% 1/16W MF-LF 402
P3V3FW_EN_L
R4291 100K 5% 1/16W MF-LF 402
Q4290 SSM6N15FEAPE SOT563
FW_PWR_EN
C4290 0.033UF 10% 16V X5R 402
CRITICAL Q4291 NTR4101P SOT-23-HF
C4291 0.01UF 10% 16V CERM 402
P3V3FW_SS
=PP3V3_FW_FET

1.05V FW FET

=PP1V05_FW_P1V05FWFET
C4296 0.1UF 20% 16V CERM 402
=PP3V3_S0_P1V05FWFET
R4297 220K 5% 1/16W MF-LF 402
P1V05FW_SS
CRITICAL Q4295 SI2312BDS SOT23
Q4293 SSM6N15FEAPE SOT563
=PP1V0_FW_FET
=PP3V3_S5_P1V05FWFET
R4295 10K 5% 1/16W MF-LF 402
R4296 100K 5% 1/16W MF-LF 402
C4295 0.068UF 10% 16V CERM 402
P1V05_FW_EN_L
P1V05_FW_EN_L_RC
Q4293 SSM6N15FEAPE SOT563
FW_PWR_EN

=PP3V3_FW_FWPHY
R4277 10K 5% 1/16W MF-LF 402
FWPHY_WAKE_YES
R4276 100K 5% 1/16W MF-LF 402
FW_WAKE
FW_PLUG_DET_L
CRITICAL Q4276 DMB53D0UV SOT-563
=FW_PME_L
CRITICAL Q4276 DMB53D0UV SOT-563
FWPHY_WAKE_YES

PCIE_FW_PRSNT
MAKE_BASE=TRUE
Q4264 SSM6N15FEAPE SOT563
FW_CLKREQ_L
Q4264 SSM6N15FEAPE SOT563
FW_PWR_EN
=FW_CLKREQ_L
FW_CLKREQ_PHY_L
MAKE_BASE=TRUE

=PP3V3_S0_FWPWRCTL
R4281 100K 5% 1/16W MF-LF 402
R4280 10K 1% 1/16W MF-LF 402
=PP1V0_FW_FWPHY
C4281 1UF 10% 6.3V CERM 402
P1V0_FW_RC
CRITICAL Q4299 DMB53D0UV SOT-563
P1V0_RESET_GATE
R4283 10K 5% 1/16W MF-LF 402
=FW_RESET_L
CRITICAL Q4299 DMB53D0UV SOT-563
FW_RESET_L
PP1V05_FW PGOOD/FW_RESET_L

FireWire Port Power Switch

CRITICAL Q4260 FDC638P_G SM
=PPBUS_S5_FWPWRSW
PPBUS_FW_FWPWRSW_F
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V
CRITICAL F4260 1.1A-24V MINISMDC110H24
PPBUS_FW_FWPWRSW_D
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V
CRITICAL D4260 SM CRS08-1.5A-30V
=PPBUS_S5_FW_FET

Late-VG Event Detection

CRITICAL Q4262 DMB54D0UV SOT-563
R4265 10K 1% 1/16W MF-LF 402
LATEVG_FAULT_EVENT_PNP
NOSTUFF R4263 100 1% 1/16W MF-LF 402
LATEVG_FAULT_EVENT
LATEVG_RETRY_RC
C4263 1UF 10% 10V X5R 402
NOSTUFF
R4260 300K 5% 1/16W MF-LF 402
C4260 0.1UF 10% 25V X5R 402
FWPWR_EN_L_DIV
R4261 470K 5% 1/16W MF-LF 402
FWPWR_EN_L
Q4261 2N7002DW-X-G SOT-363
Q4261 2N7002DW-X-G SOT-363
SMC_ADAPTER_EN
PM_SLP_S3_L
Enables port power when machine is running or on AC.

=PP3V3_FW_LATEVG_ACTIVE
=PP2V4_FW_LATEVG
R4211 10K 5% 1/16W MF-LF 402
R4212 10K 1% 1/16W MF-LF 402
C4210 0.1UF 10% 16V CERM 402
U4210 LMC7211 SM-HF
FWLATEGV_3V_REF
LATEVG_EVENT
P2V4_FWLATEVG_RC
C4211 100PF 5% 50V CERM 402
R4213 80.6K 1% 1/16W MF-LF 402
R4210 200K 1% 1/16W MF-LF 402
FWLATEVG Hysteresis:
3.08V when port power is on
2.91V when late Vg event and port power is off

=PP1V1_FWPWRCTL
R4275 1K 5% 1/16W MF-LF 402
FW_PWR_EN_L
R4270 330K 5% 1/16W MF-LF 402
CRITICAL Q4270 BC847CDXV6TXG SOT563
FW_DET_MIRROR
FW_P1_TPBIAS_R
R4272 1K 5% 1/16W MF-LF 402
R4271 56K 5% 1/16W MF-LF 402
FW_PLUG_DET
CRITICAL Q4270 BC847CDXV6TXG SOT563
FW_DET_EMIT
R4273 12K 5% 1/16W MF-LF 402
C4270 0.1UF 10% 16V X5R 402
=PP3V3_S0_FWPWRCTL
R4274 100K 5% 1/16W MF-LF 402
FW_PLUG_DET_L
CRITICAL Q4275 DMB53D0UV SOT-563
CRITICAL Q4275 DMB53D0UV SOT-563
FW_PWR_EN
FW_P1_TPBIAS

SYNC_MASTER=YUN_K19_MLB	SYNC_DATE=12/22/2008
PAGE TITLE	FireWire Port Power
Apple Inc.	DRAWING NUMBER: 051-7898 SIZE: D
	REVISION: C.0.0
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Page Notes

Power aliases required by this page:

- =PPVP_FW_PORT1
- =PP3V3_FW_LATEVG

- =GND_CHASSIS_FW_PORT1
- =GND_CHASSIS_FW_EMI_R

Signal aliases required by this page:
(NONE)

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:
(NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

FireWire PHY Config Straps

Configures PHY for:

- 1-port Portable Power Class (0)

- Port "1" Bilingual (1394B)

3686 35D8 34D2 34B1 7B1 =PP3V3_FW_FWPHY

R4382 10K 1% 1/16W MF-LF 402

R4380 10K 1% 1/16W MF-LF 402

FWPHY_DS0 MAKE_BASE=TRUE =FW_PHY_DS0 34C6

FWPHY_DS2 MAKE_BASE=TRUE =FW_PHY_DS2 34C6

FWPHY_DS1 MAKE_BASE=TRUE =FW_PHY_DS1 34C6

R4381 10K 1% 1/16W MF-LF 402

34B6 FW_P0_TPBIAS = NC_FW0_TPBIAS MAKE_BASE=TRUE

34B6 FW_P2_TPBIAS = NC_FW2_TPBIAS MAKE_BASE=TRUE

78D3 34C6 FW_P0_TPA_N = NC_FW0_TPAN MAKE_BASE=TRUE

78D3 34B6 FW_P0_TPA_P = NC_FW0_TPAP MAKE_BASE=TRUE

34B6 FW_P2_TPA_N = NC_FW2_TPAN MAKE_BASE=TRUE

34B6 FW_P2_TPA_P = NC_FW2_TPAP MAKE_BASE=TRUE

78D3 34B6 FW_P0_TPB_N = NC_FW0_TPBN MAKE_BASE=TRUE

78D3 34B6 FW_P0_TPB_P = NC_FW0_TPBP MAKE_BASE=TRUE

34B6 FW_P2_TPB_N = NC_FW2_TPBN MAKE_BASE=TRUE

34B6 FW_P2_TPB_P = NC_FW2_TPBP MAKE_BASE=TRUE

Termination

Place close to FireWire PHY

35A4 3486 FW_P1_TPBIAS

TI PHYs require 1uF even though FW spec calls out 0.33uF

C4360 0.33UF 10% 6.3V CERM-X5R 402

SIGNAL_MODEL=EMPTY SIGNAL_MODEL=EMPTY

R4360 56.2 1% 1/16W MF-LF 402

R4361 56.2 1% 1/16W MF-LF 402

78D3 3486 FW_P1_TPA_P = FW_PORT1_TPA_P MAKE_BASE=TRUE 36B5

78D3 3486 FW_P1_TPA_N = FW_PORT1_TPA_N MAKE_BASE=TRUE 36B5

78D3 3486 FW_P1_TPB_P = FW_PORT1_TPB_P MAKE_BASE=TRUE 36B5

78D3 3486 FW_P1_TPB_N = FW_PORT1_TPB_N MAKE_BASE=TRUE 36B5

SIGNAL_MODEL=EMPTY SIGNAL_MODEL=EMPTY

R4362 56.2 1% 1/16W MF-LF 402

R4363 56.2 1% 1/16W MF-LF 402

FW_PORT1_TPB_C

C4364 220pF 5% 25V CERM 402

R4364 4.99K 1% 1/16W MF-LF 402

7B1 =PPVP_FW_PHY_CPS_FET

Q4300 BSS8402DW (SOT-363) (SYM-VER1)

PPVP_FW_CPS MIN_LINE_WIDTH=0.4 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=12.6V MAKE_BASE=TRUE =PPVP_FW_PHY_CPS 34B7

R4311 470K 5% 1/16W MF-LF 402

CPS_EN_L_DIV

R4312 330K 5% 1/16W MF-LF 402

CPS_EN_L

Q4300 BSS8402DW SOT-363 (SYM-VER1)

3686 35D8 34D2 34B1 7B1 =PP3V3_FW_FWPHY

"Snapback" & "Late VG" Protection

36A5 35A8 PP2V4_FW_LATEVG

DP4310 BAV99DW-X-G SOT-363 CRITICAL

C4311 0.01uF 10% 50V X7R 402

DP4310 BAV99DW-X-G SOT-363

C4310 0.01uF 10% 50V X7R 402

36B7 FW_PORT1_TPB_N

36B7 FW_PORT1_TPB_P

36B7 FW_PORT1_TPA_N

36B7 FW_PORT1_TPA_P

DP4311 BAV99DW-X-G SOT-363

C4312 0.01uF 10% 50V X7R 402

CRITICAL DP4311 BAV99DW-X-G SOT-363

C4313 0.01uF 10% 50V X7R 402

PLACEMENT_NOTE=Place C4319 close to connector pin 5.

C4319 0.1uF 10% 50V X7R 603-1

R4319 1M 5% 1/16W MF-LF 402

Cable Power

7B1 =PPVP_FW_PORT1

CRITICAL L4310 FERR-250-OHM SM

Note: Trace PPVP_FW_PORT1 must handle up to 5A

PPVP_FW_PORT1_F MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=33V

C4314 0.01UF 10% 50V X7R 402

PORT 1

BILINGUAL

CRITICAL J4310 1394B-M97 F-RT-TH

(FW_PORT1_BREF)

NC

(GND_FW_PORT1_VG)

FW_PORT1_AREF

TPB- TPB(R) TPB+ TPBR<R> TPB<R> VP NC/NC VG TPA- TPA+ TPA<R> TPA<R> TPA(R) CHASSIS GND

OUTPUT

INPUT

AREF needs to be isolated from all local grounds per 1394b spec

When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue)

BREF should be hard-connected to logic ground for speed signaling and connection

514S0605

Late-VG Protection Power

7A3 =PP3V3_FW_LATEVG

R4390 332 1% 1/10W MF-LF 402

PP2V4_FW_LATEVG MIN_LINE_WIDTH=0.38 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=2.4V 35A8 36C5

CRITICAL D4390 MMBZ5227BLT1H SOT23

ESD and late-VG rail for snap-back diodes (Common to all ports)

PP2V4_FWLATEVG needs to be biased to at least 2.1V for FW signal integrity and should be biased to 2.4V for margin

R4390 should be 390 Ohms max for a 3.3V rail

SYNC_MASTER=K19_MLB SYNC_DATE=11/02/2008

PAGE TITLE: FireWire Ports

Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D

REVISION: C.0.0

BRANCH:

PAGE: 43 OF 109

SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

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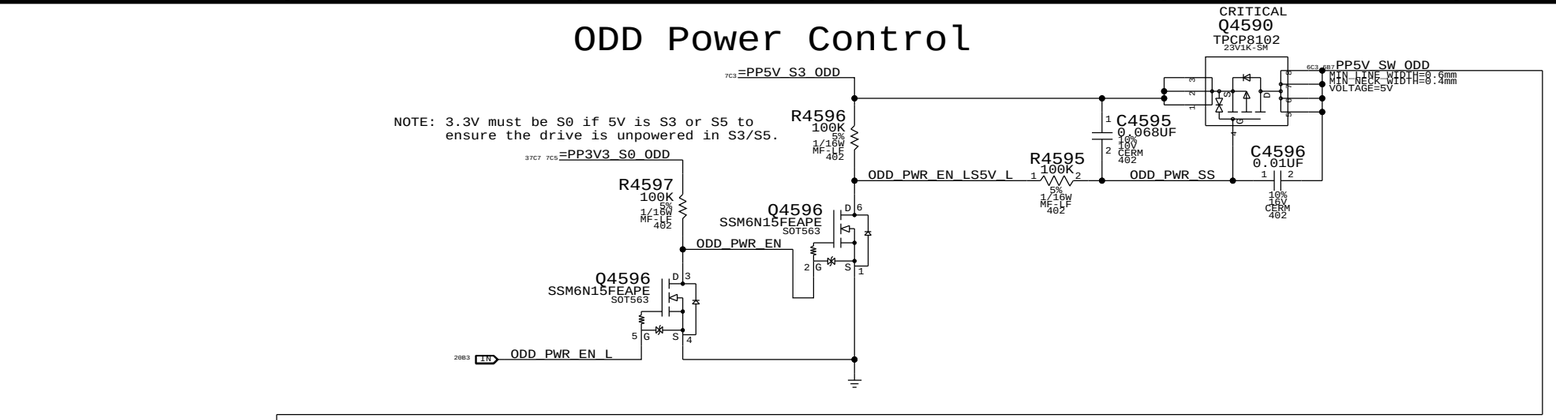
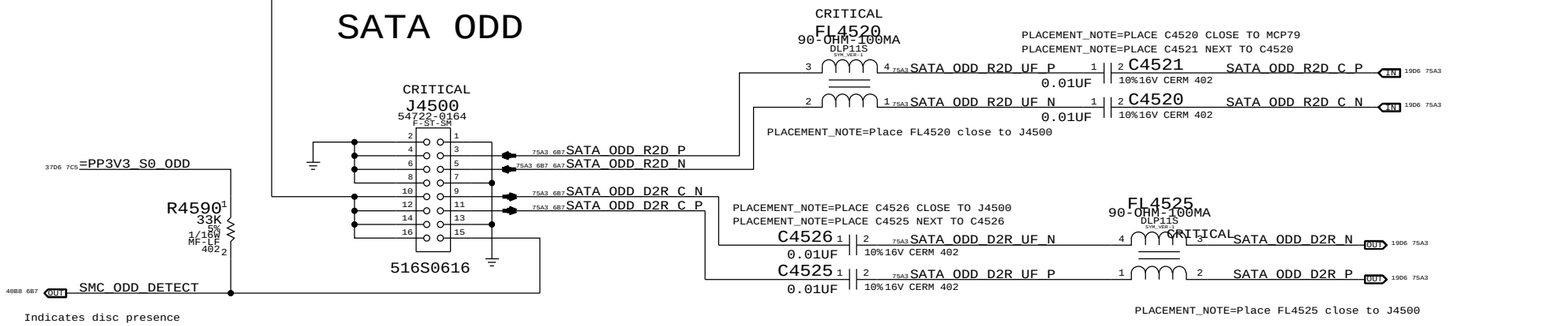
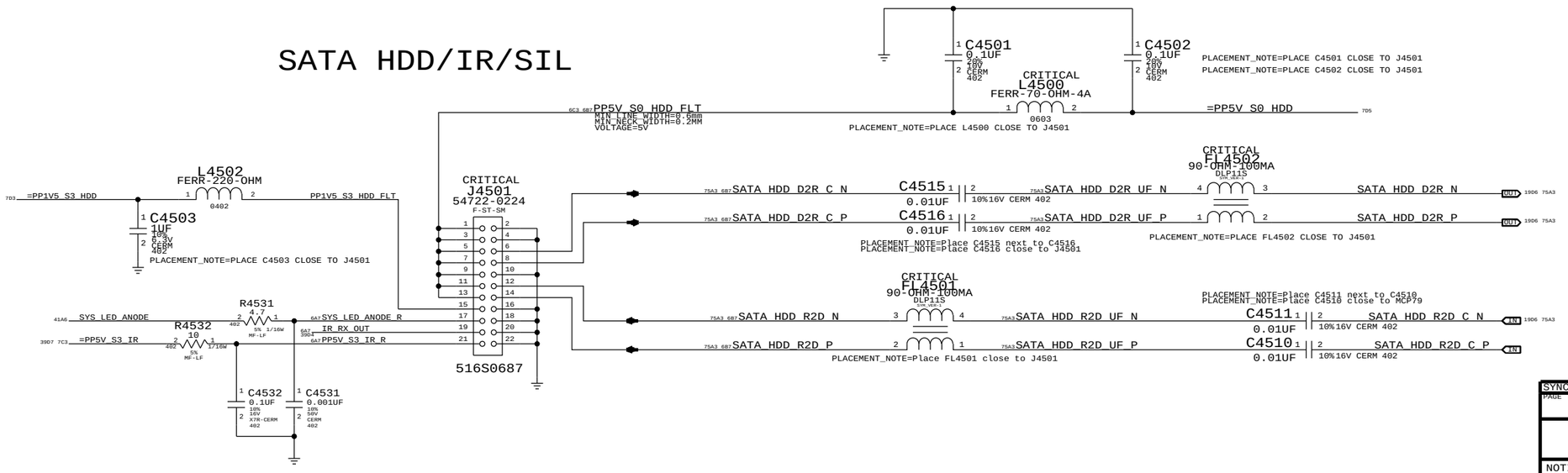
ODD Power Control



SATA ODD



SATA HDD/IR/SIL



SYNC MASTER=K19 MLB SYNC DATE=12/04/2008

PAGE TITLE

SATA Connectors

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D

REVISION C.0.0

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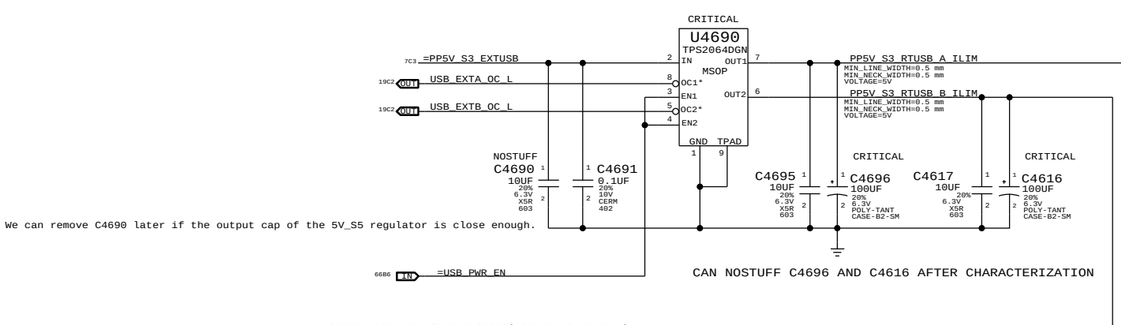
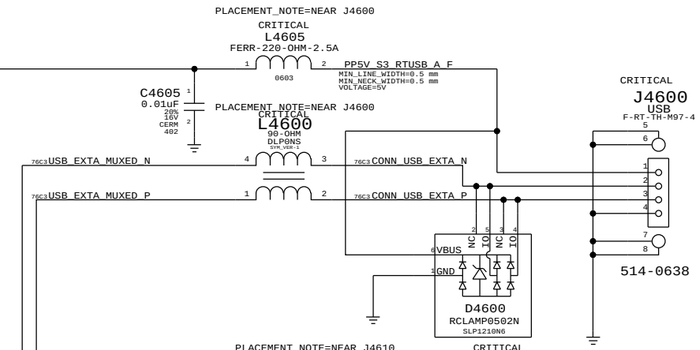
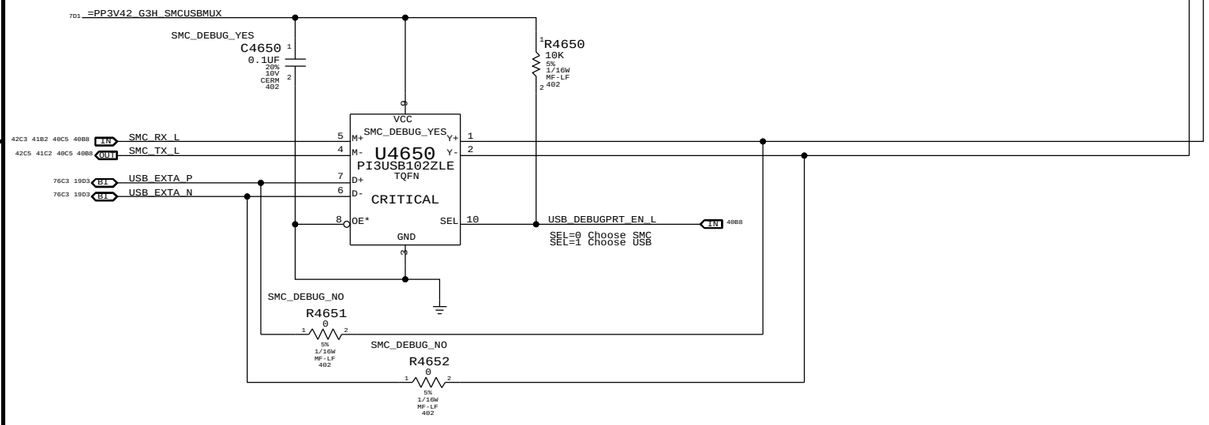
Port Power Switch



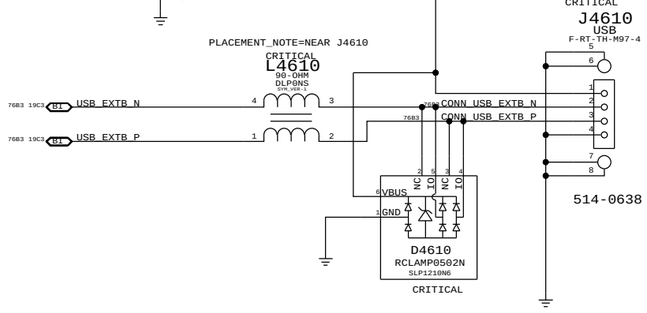
USB PORT A (FRONT PORT)



USB/SMC Debug Mux



USB PORT B (BACK PORT)



SYNC_MASTER=YUAN.MA SYNC_DATE=01/18/2008

PAGE TITLE: External USB Connectors

Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D

REVISION: C.0.0

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PAGE: 46 OF 109

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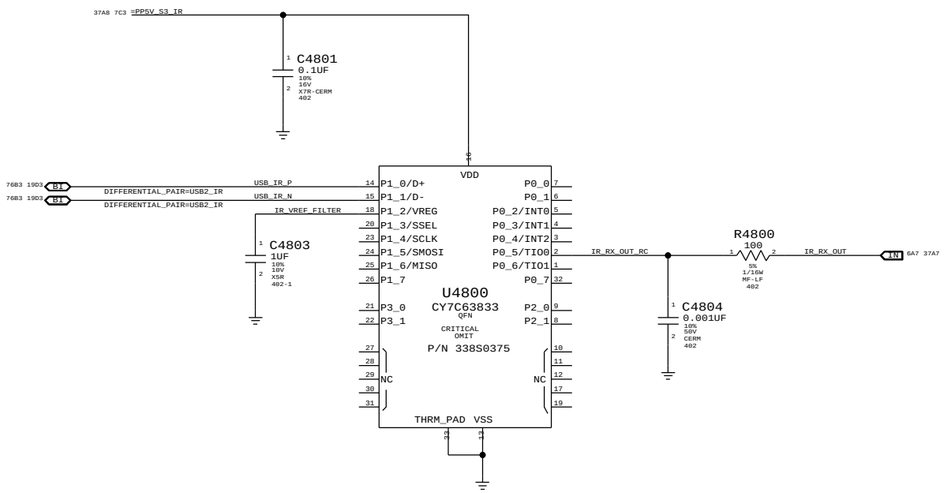

CYPRESS 'ENCORE II' USB CONTROLLER

SYNC_MASTER=YUAN.MA SYNC_DATE=05/28/2008

PAGE TITLE

Front Flex Support

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D

REVISION C.0.0

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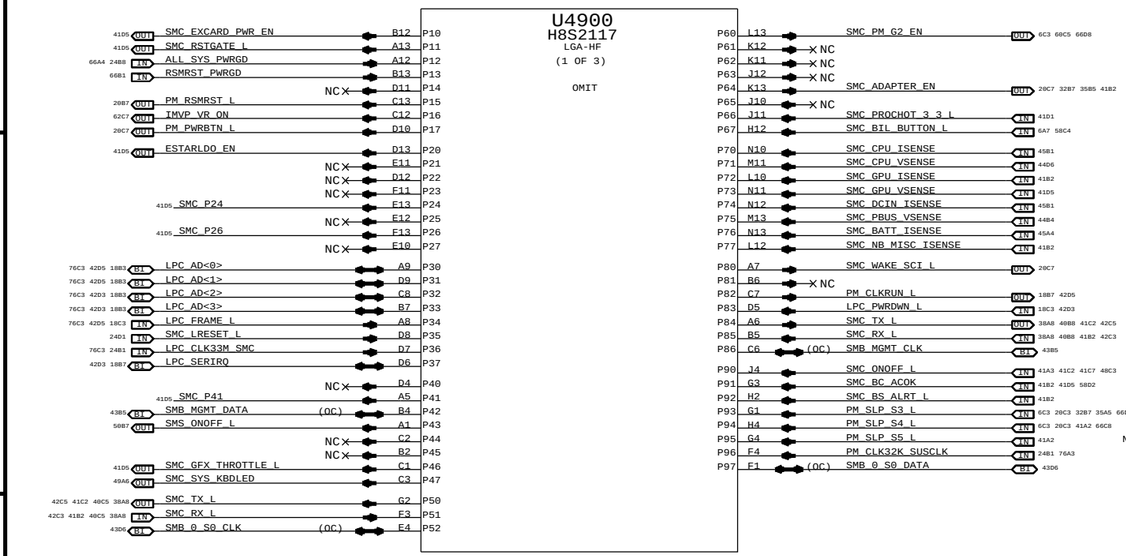
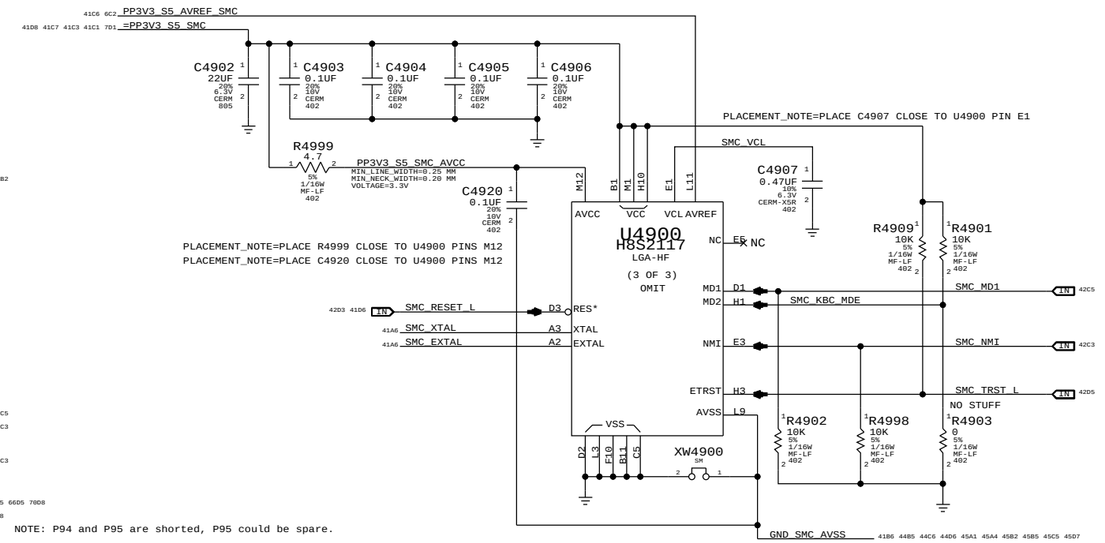
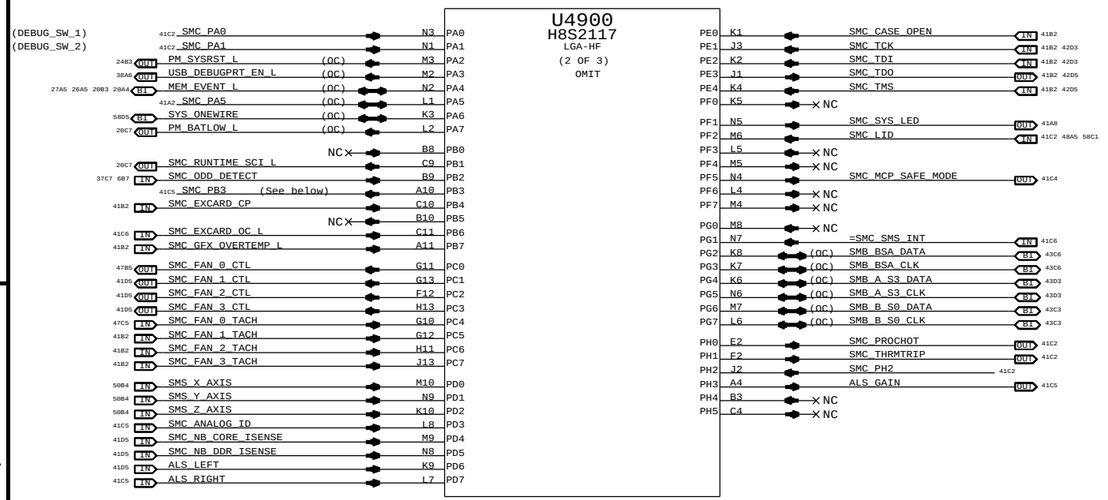
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.





NOTE: P94 and P95 are shorted, P95 could be spare.



(DEBUG_SW_1)
(DEBUG_SW_2)

SMC_PB3:

SMC_IG_THROTTLE_L for MG systems.
Otherwise, TP/NC okay (was ISENSE_CAL_EN)

NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

SYNC_MASTER=T18_MLB	SYNC_DATE=06/26/2008
PAGE TITLE: SMC	
Apple Inc.	DRAWING NUMBER: 051-7898 SIZE: D
	REVISION: C.0.0
	BRANCH:
	PAGE: 49 OF 109
	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

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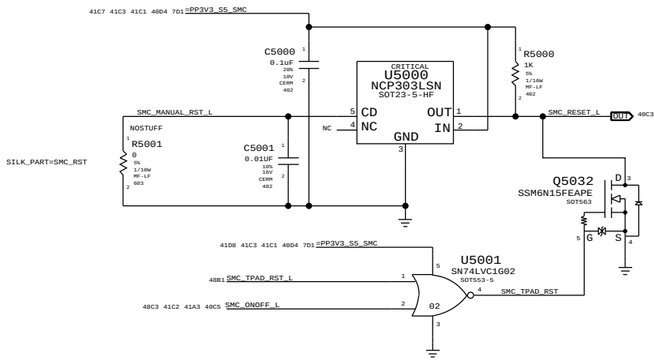
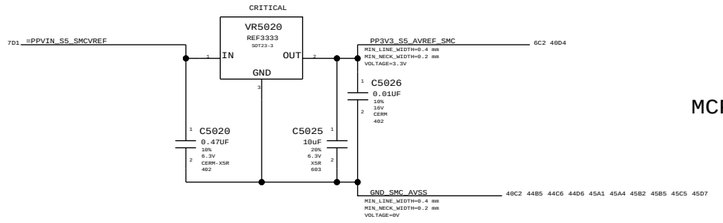
SMC Reset "Button" / Brownout Detect

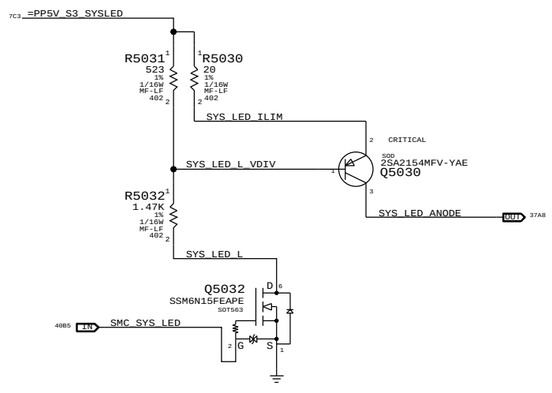


SMC AVREF Supply

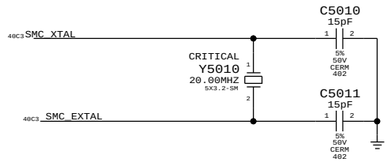


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1381	353S1912		ALL	ISL60002-33, INTERSIL

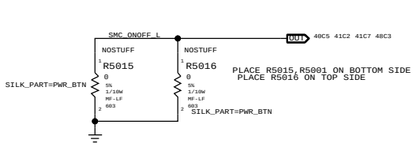
System (Sleep) LED Circuit



SMC Crystal Circuit

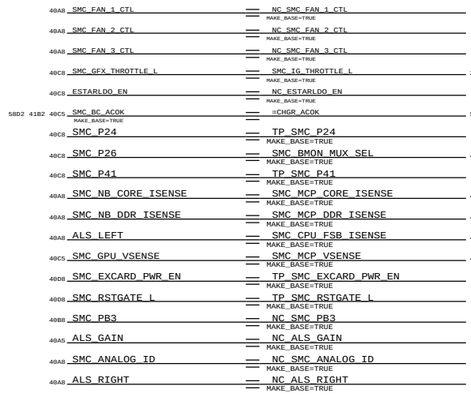


Debug Power "Button"

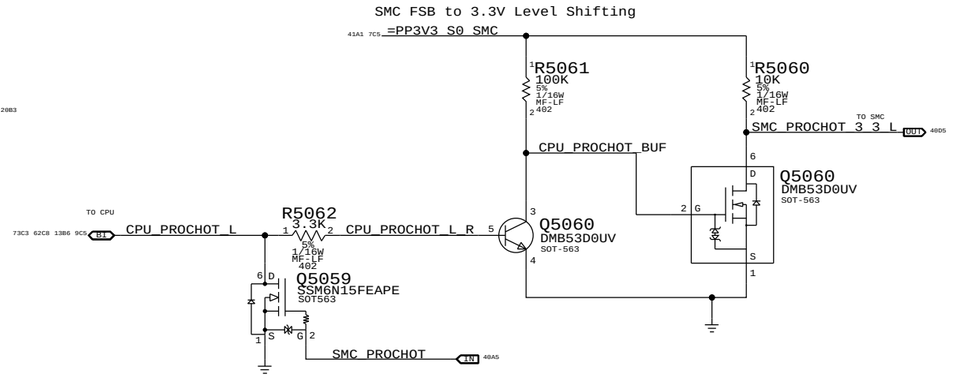


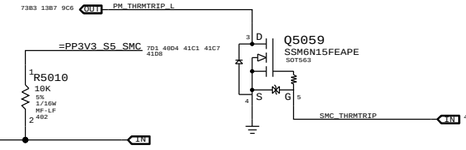
MCP_SAFE_MODE SIGNAL TO SUPPORT ROM FAILURE OVERRIDE

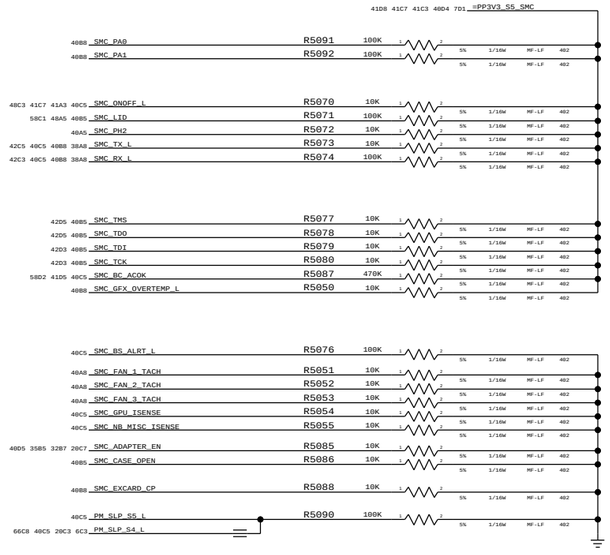
RADAR 5925345



SMC FSB to 3.3V Level Shifting







SYNC_MASTER=YUAN.MA	SYNC_DATE=05/28/2008
PAGE TITLE: SMC Support	
Apple Inc.	DRAWING NUMBER: 051-7898 SIZE: D
	REVISION: C.0.0
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	PAGE: 50 OF 109
	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

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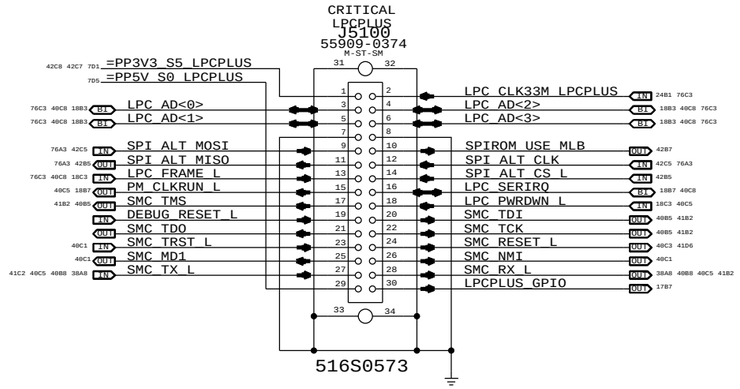
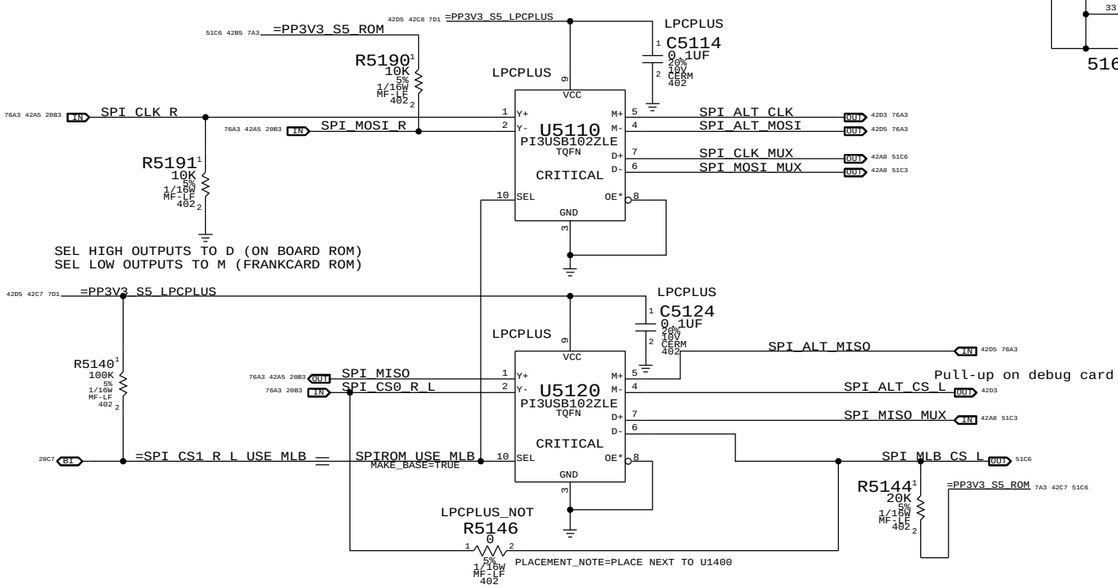
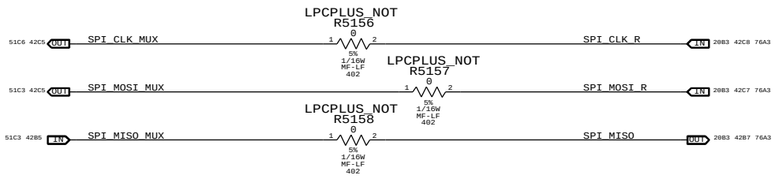
LPC+SPI Connector



Alternate SPI ROM Support



SPI MUX BYPASS



SYNC_MASTER=CHANGZHANG SYNC_DATE=05/09/2008

PAGE TITLE: LPC+SPI Debug Connector

Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D

REVISION: C.0.0

BRANCH:

PAGE: 51 OF 109

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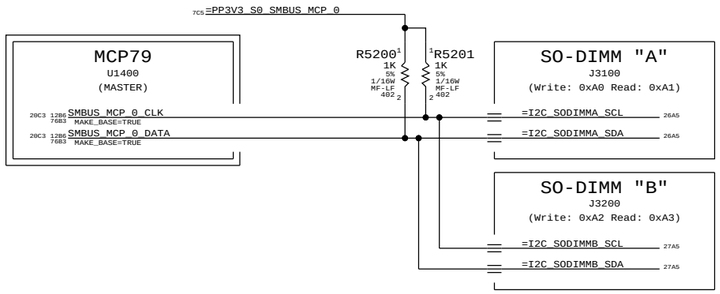
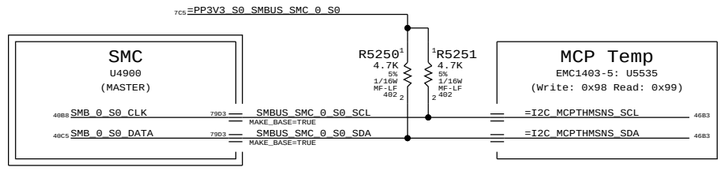
MCP79 SMBUS "0" CONNECTIONS



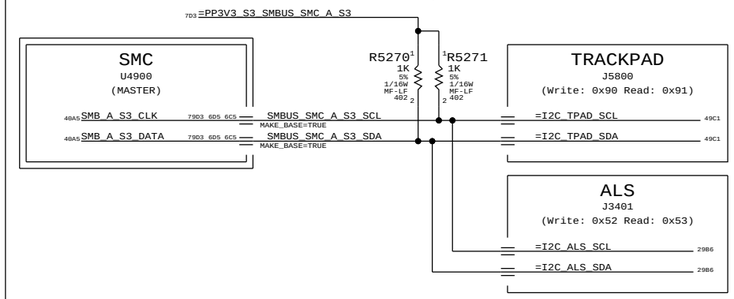
MCP79 SMBUS "1" CONNECTIONS

SMC "0" SMBus Connections

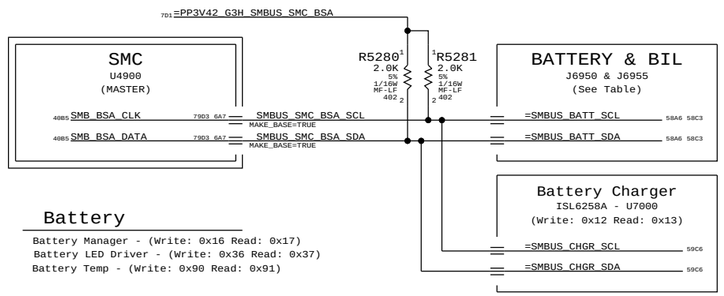


SMC "A" SMBus Connections

NOTE: SMC RMT bus remains powered and may be active in S3 state



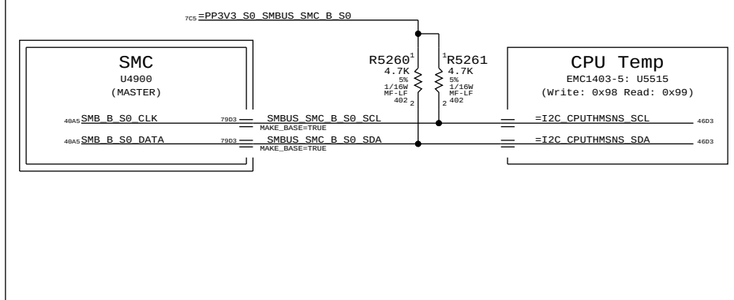
SMC "Battery A" SMBus Connections



Battery

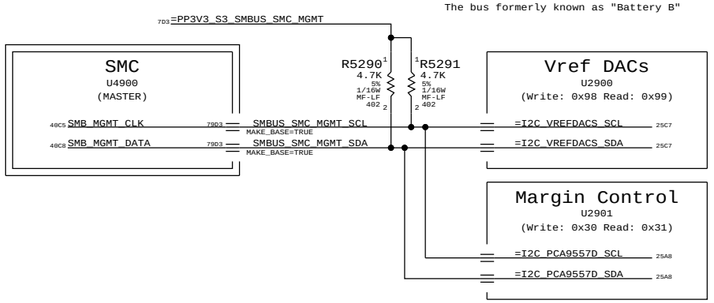
Battery Manager - (Write: 0x16 Read: 0x17)
Battery LED Driver - (Write: 0x36 Read: 0x37)
Battery Temp - (Write: 0x90 Read: 0x91)

SMC "B" SMBus Connections



SMC "Management" SMBus Connections

The bus formerly known as "Battery B"



SYNC MASTER=BEN SYNC DATE=04/21/2008

PAGE TITLE

K24 SMBUS CONNECTIONS

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D
REVISION C.0.0
BRANCH
PAGE 52 OF 109
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

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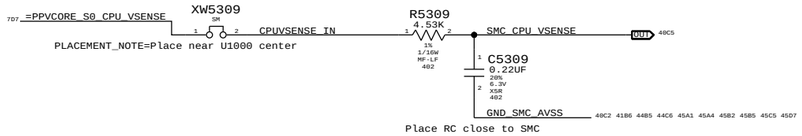
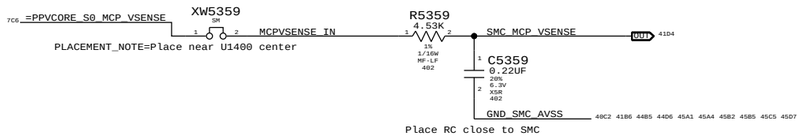
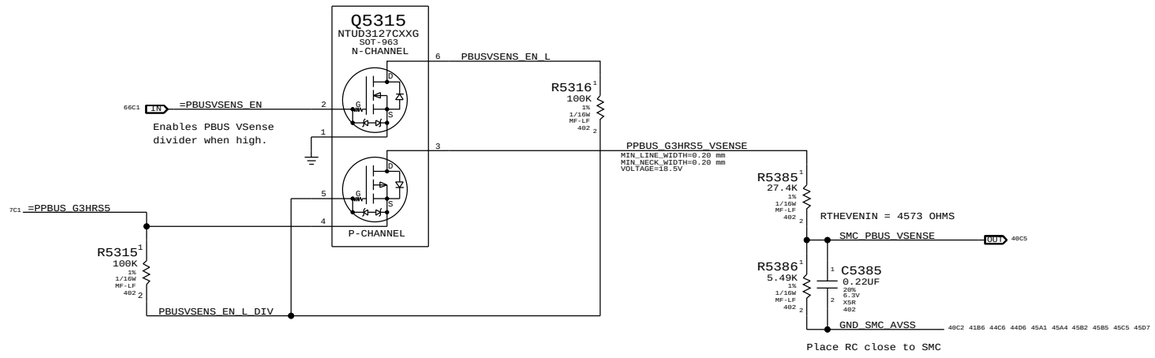
CPU Voltage Sense / Filter



MCP Voltage Sense / Filter



PBUS VOLTAGE SENSE ENABLE & FILTER



SYNC MASTER=YUNWU SYNC DATE=02/04/2008

PAGE TITLE

VOLTAGE SENSING

Apple Inc.

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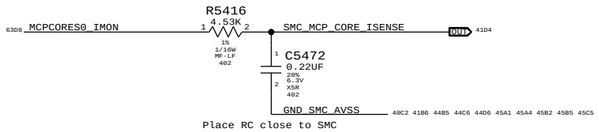
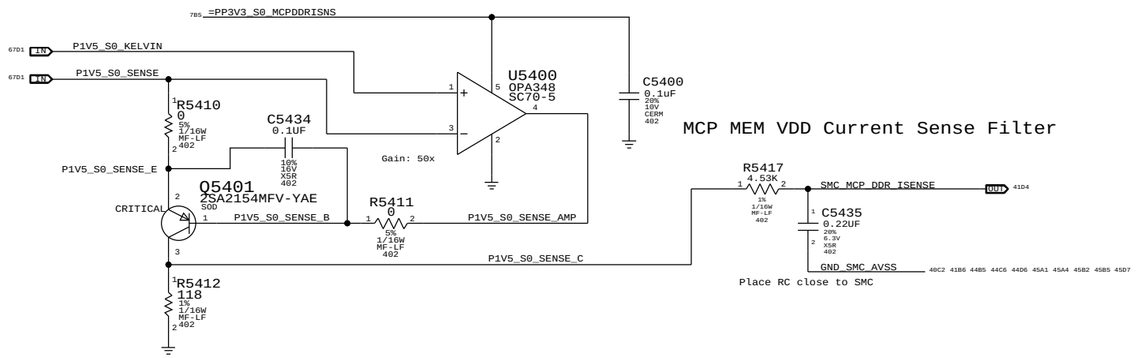
MCP VCore Current Sense Filter

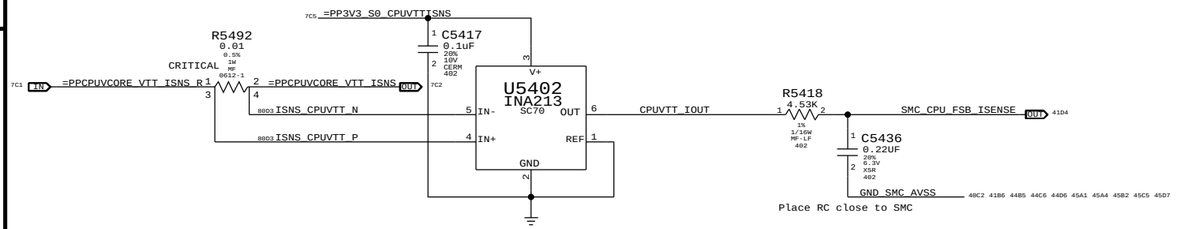


MCP MEM VDD Current Sense

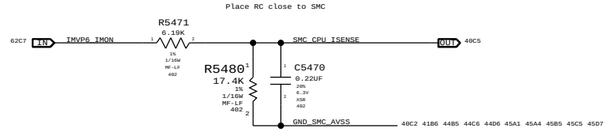


MCP MEM VDD Current Sense Filter

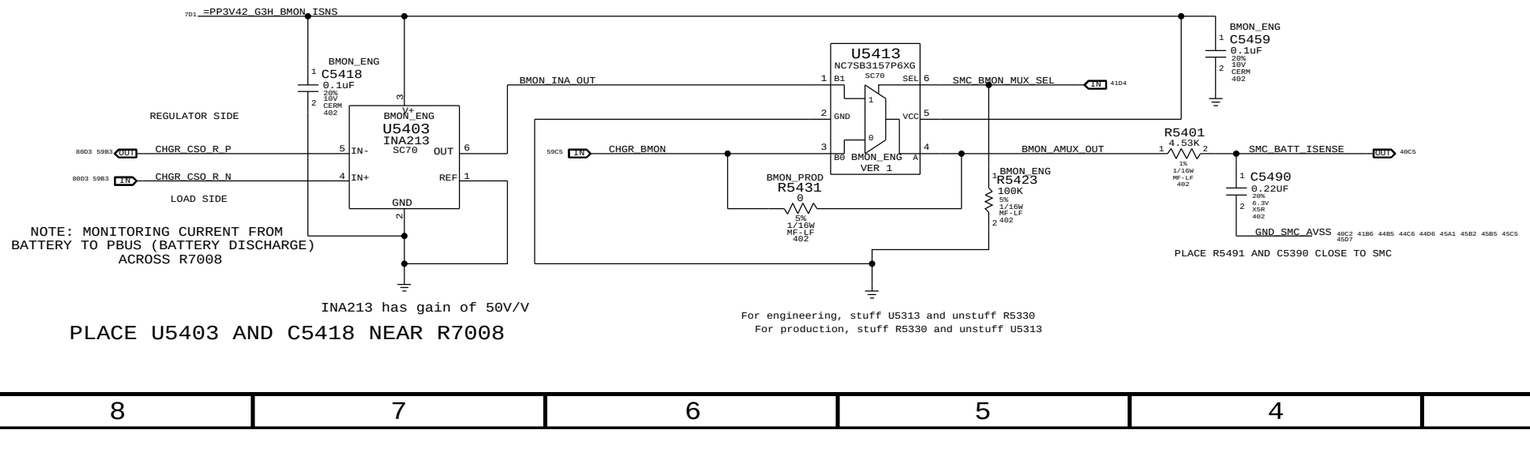
CPU 1.05V AND CPU VCORE HIGH SIDE CURRENT SENSE



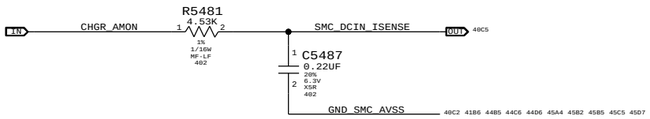
CPU VCore Load Side Current Sense / Filter



BMON CURRENT SENSE



DC-IN (AMON) CURRENT SENSE



SYNC_MASTER=YUNWU SYNC_DATE=12/17/2008

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Current Sensing

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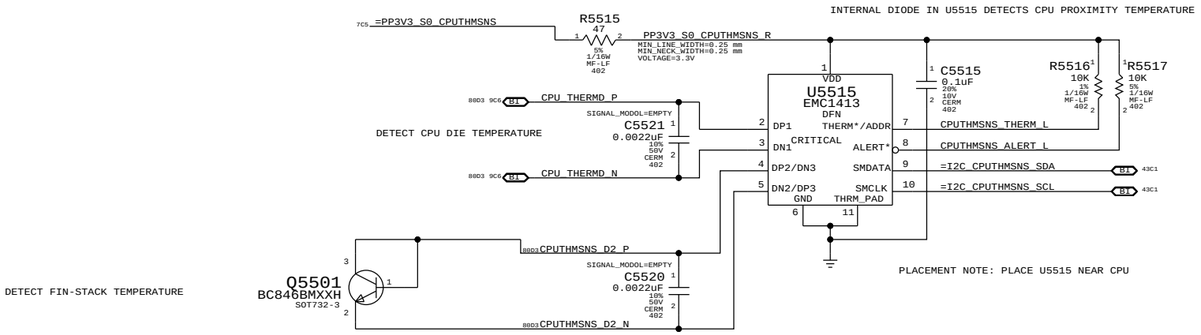
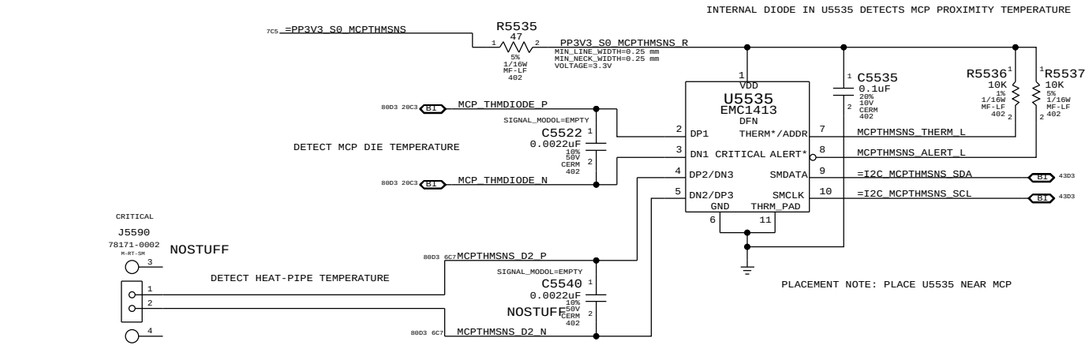
CPU T-Diode Thermal Sensor



MCP T-Diode Thermal Sensor



REPLACED 518S0521 WITH 518S0519

SYNC_MASTER=YUNWU SYNC_DATE=03/20/2008

PAGE TITLE: Thermal Sensors

Apple Inc.

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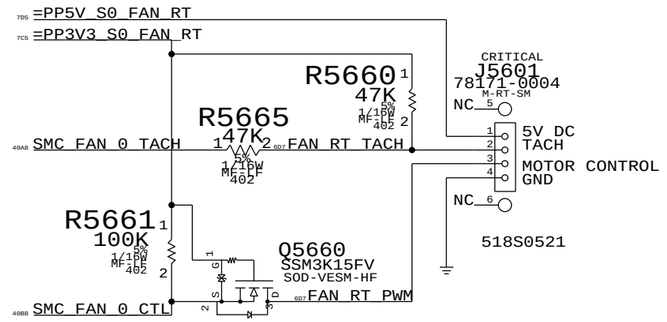

SYNC_MASTER=CHANGZHANG SYNC_DATE=01/18/2008

PAGE TITLE

Fan

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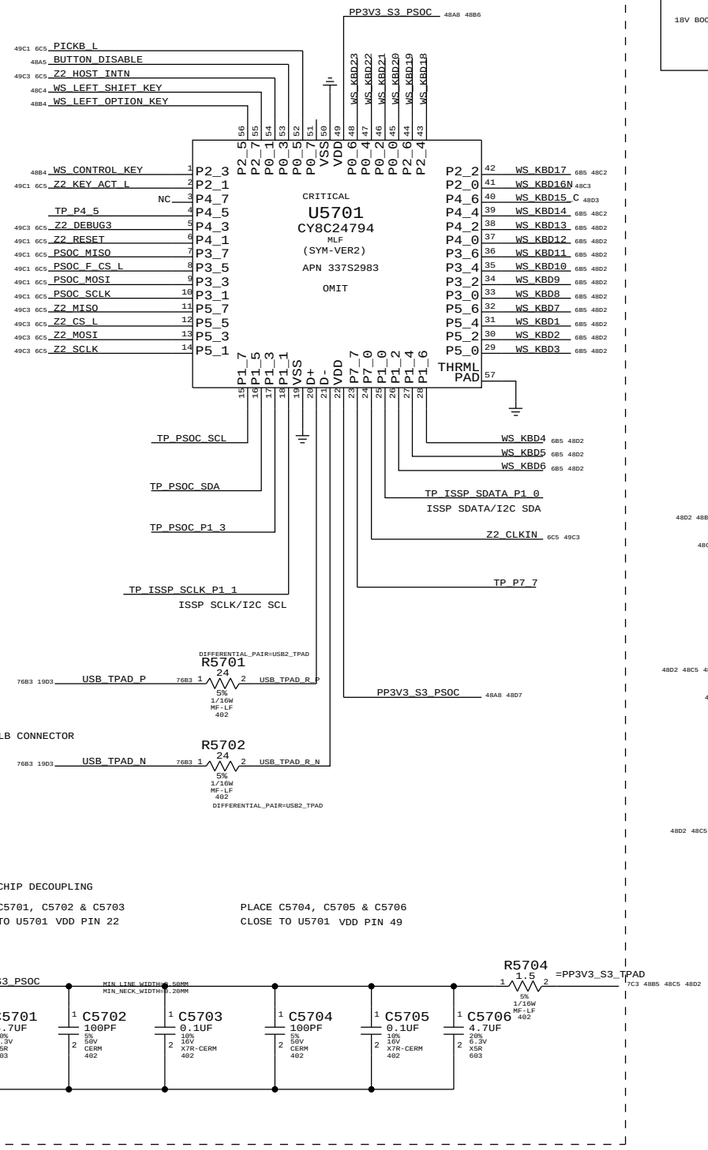
PSOC USB CONTROLLER

USB INTERFACES TO MLB
SPI HOST TO Z2

TRACKPAD PICK BUTTONS
KEYBOARD SCANNER



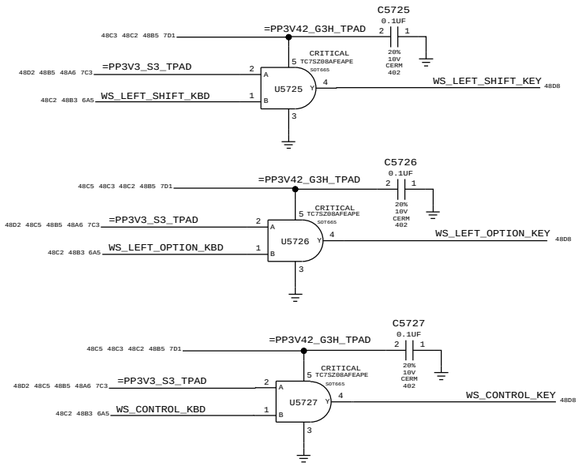
U5701 CHIP DECOUPLING

PLACE C5701, C5702 & C5703
CLOSE TO U5701 VDD PIN 22

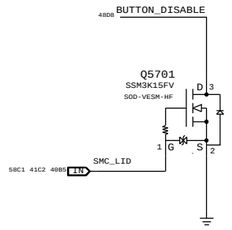
PLACE C5704, C5705 & C5706
CLOSE TO U5701 VDD PIN 49

IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA	2.55 KOHM	0.0255 V	0.255E-6 W
		80UA		0.204 V	16.32E-6 W
3V3 LDO	VDD	60MA MAX	10 OHM	0.6 V	36E-3 W
	VOUT	60MA MAX	0.2 OHM	0.012 V	0.72E-3 W
PSOC	VDD	8MA (TYP)	1.5 OHM	0.012 V	96E-6 W
		14MA (MAX)		0.021 V	294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

ISOLATION CIRCUIT



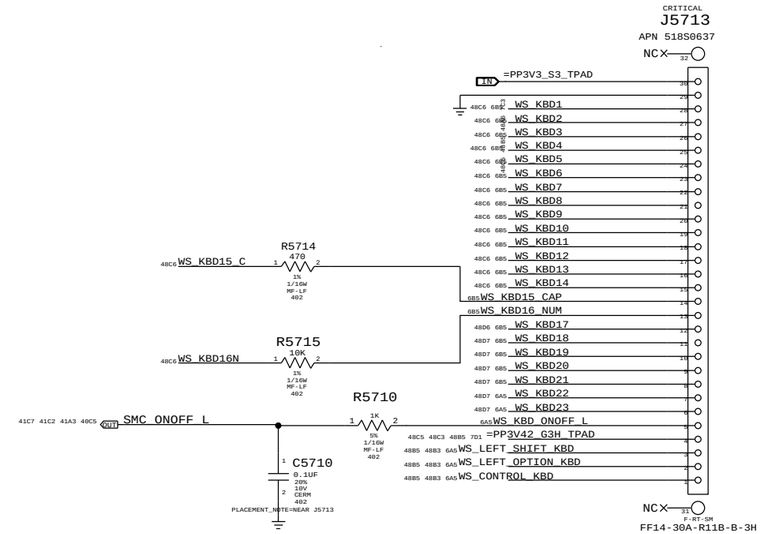
TPAD BUTTONS DISABLE



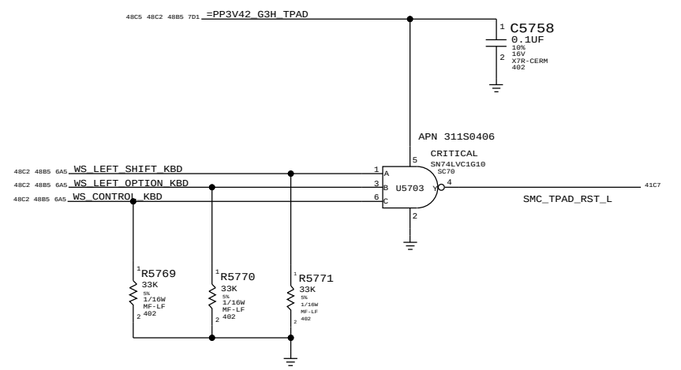
PLACE THESE COMPONENTS CLOSE TO J5800
THIS ASSUMES THERE'S A PP3V42_G3H PULL UP ON MLB

THE TPAD BUTTONS WILL BE DISABLE
WHEN THE LID IS CLOSED
LID OPEN => SMC_LID_LC ~ 3.42V
LID CLOSE => SMC_LID_LC < 0.50V

KEYBOARD CONNECTOR



SMC_MANUAL_RESET LOGIC



Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
311S0406	311S0447		ALL	NXP PART AS ALTERNATE

SYNC_MASTER=YUAN.MA SYNC_DATE=04/22/2008

PAGE TITLE
WELLSPRING 1

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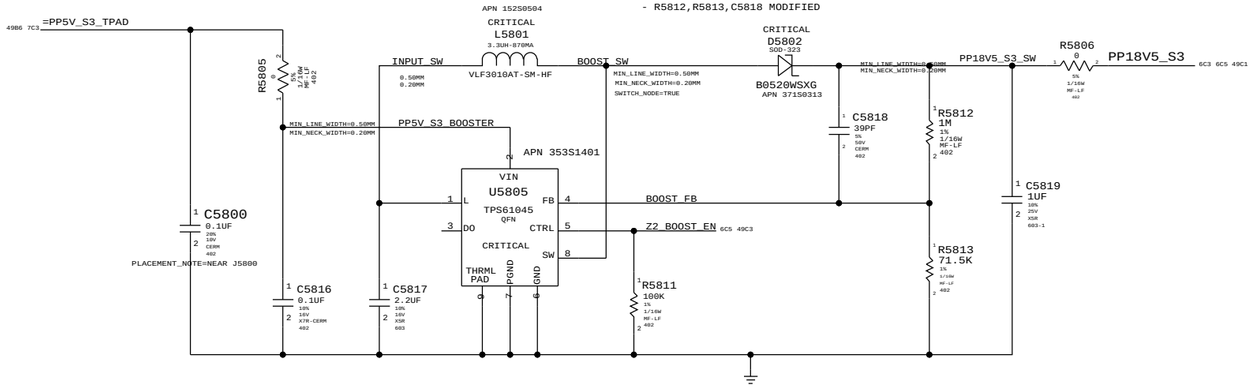
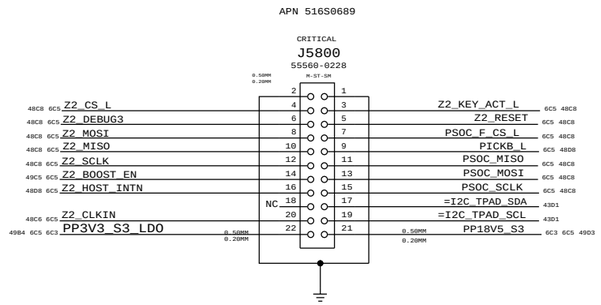
BOOSTER +18.5VDC FOR SENSORS

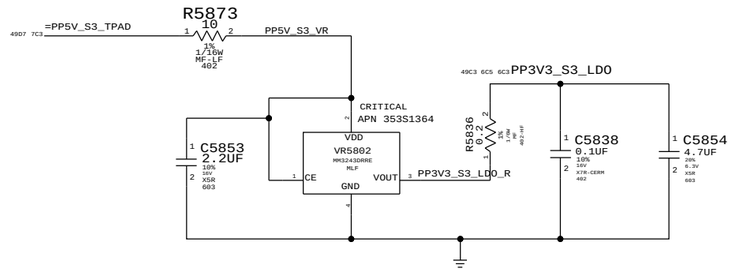
BOOSTER DESIGN CONSIDERATION:
- POWER CONSUMPTION
- DROOP LINE REGULATION
- RIPPLE TO MEET ERS
- 100-300 KHZ CLEAN SPECTRUM
- STARTUP TIME LESS THAN 2MS
- R5812,R5813,C5818 MODIFIED



IPD FLEX CONNECTOR



3V3 LDO FOR IPD



KEYBOARD BACKLIGHT DRIVNG AND DETECTION

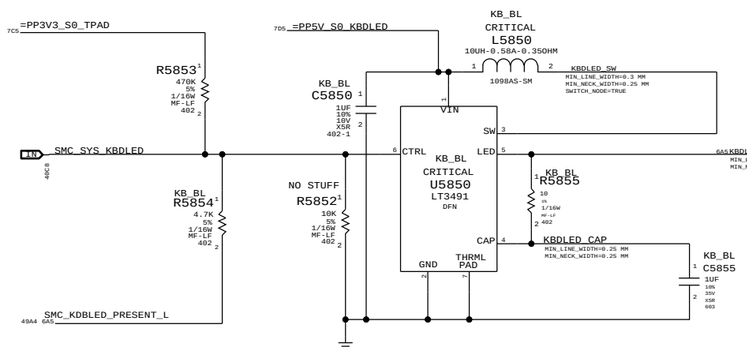
To detect Keyboard backlight, SMC will tristate SMC_SYS_KBDLED:

LOW = keyboard backlight present

HIGH= keyboard backlight not present

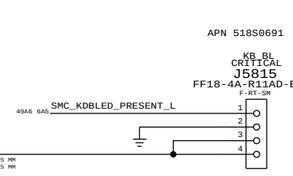
BOM OPTION: KBDLED_YES
TURNED ON FOR BEST MLB CONFIG

R5853 ALWAYS PRESENT



APN 518S0691

J5815 pin 1 is grounded on keyboard backlight flex



KBD BACKLIGHT CONNECTOR

SYNC_MASTER=YUAN.MA	SYNC_DATE=05/09/2008
PAGE TITLE: WELLSPRING 2	
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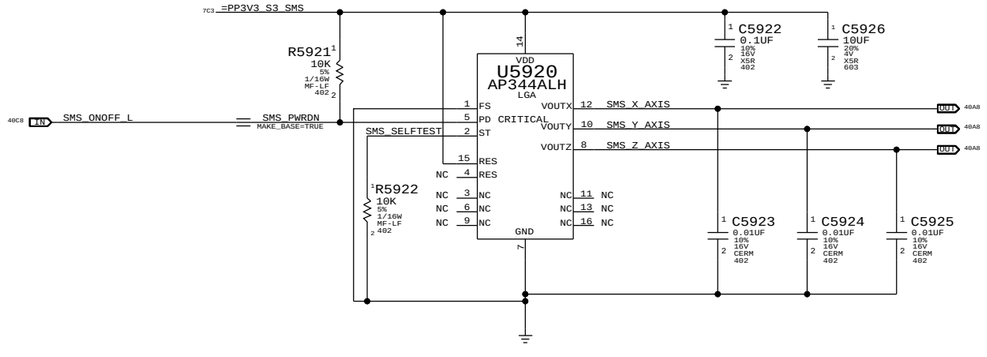
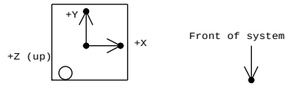
Analog SMS

R5921 PULLS UP SMS_PWRDN TO TURN OFF SMS WHEN PIN IS NOT BEING DRIVEN BY SMC



Desired orientation when placed on board top-side:



Circle indicates pin 1 location when placed in correct orientation

SYNC_MASTER=YUNWU SYNC_DATE=06/26/2008

PAGE TITLE: SMS

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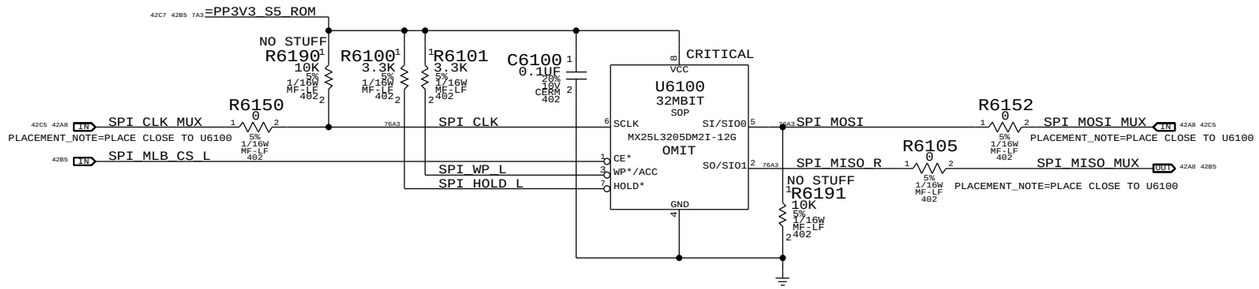

MCP79 SPI Frequency Select

Frequency	SPI_MOSI	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

25MHz is selected with R5190 and R5191
Any of the 4 frequencies can be selected
with R6190, R6191, R5190 and R5191

SYNC_MASTER=CHANGZHANG SYNC_DATE=05/02/2008

PAGE TITLE
SPI ROM

Apple Inc.

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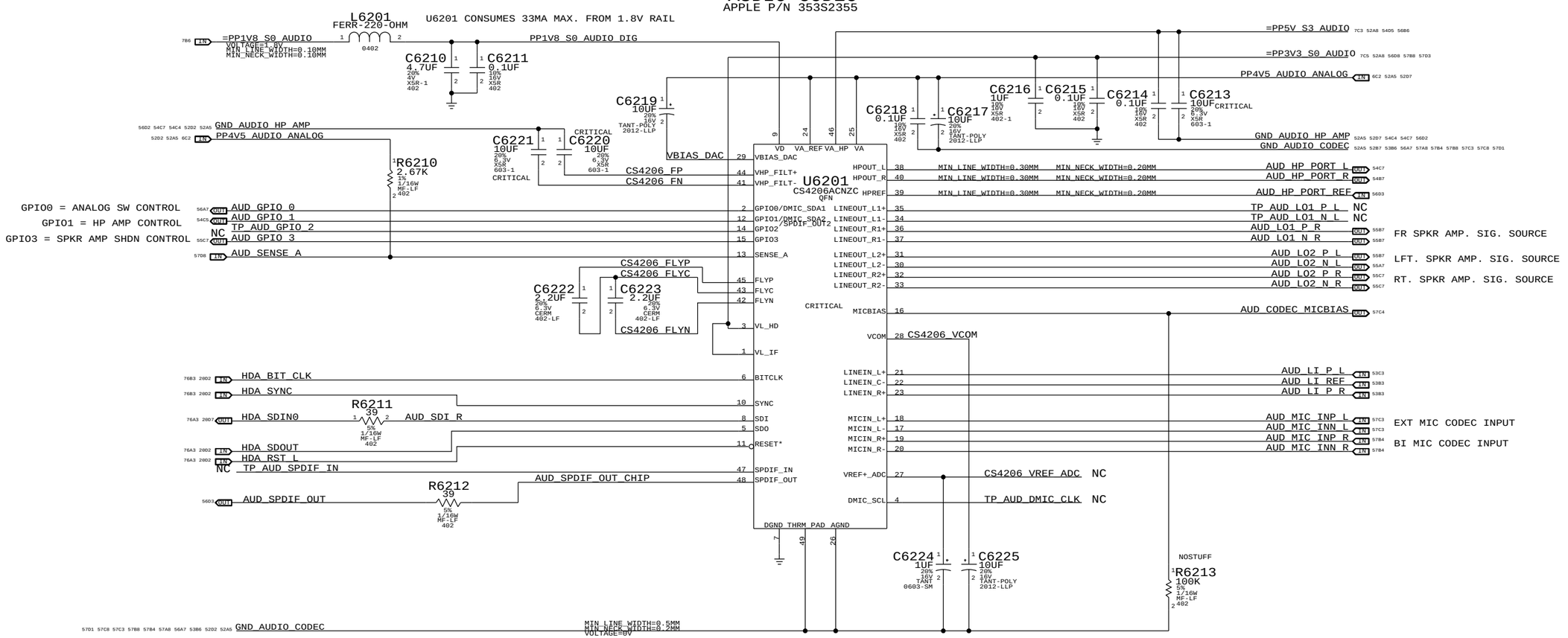
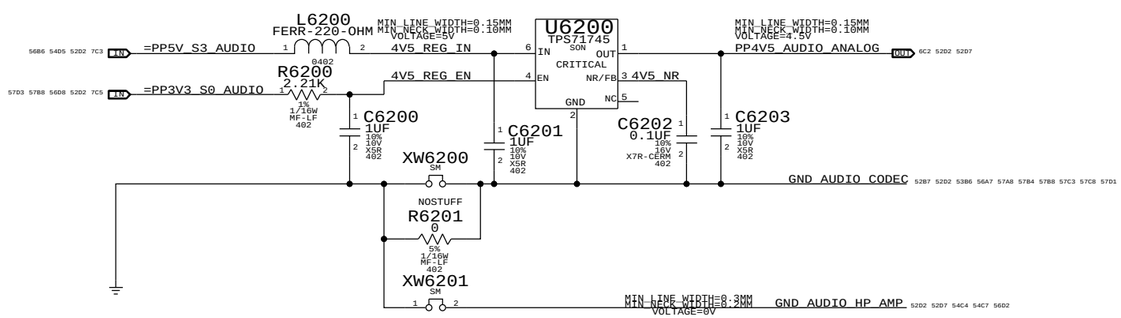
AUDIO CODEC
APPLE P/N 353S2355



4.5V POWER SUPPLY FOR CODEC
APPLE P/N 353S2456



NOTES ON CODEC I/O

DIFF FSINPUT= 2.45VRMS
SE FSINPUT= 1.22VRMS
DAC1 FSOUTPUT= 1.34VRMS
DAC2/3 FSOUTPUTDIFF= 2.67VRMS
DAC2/3 FSOUTPUTSE= 1.34VRMS

SYNC_MASTER=AUDIO SYNC_DATE=03/04/2009

PAGE TITLE: AUDIO: CODEC/REGULATOR

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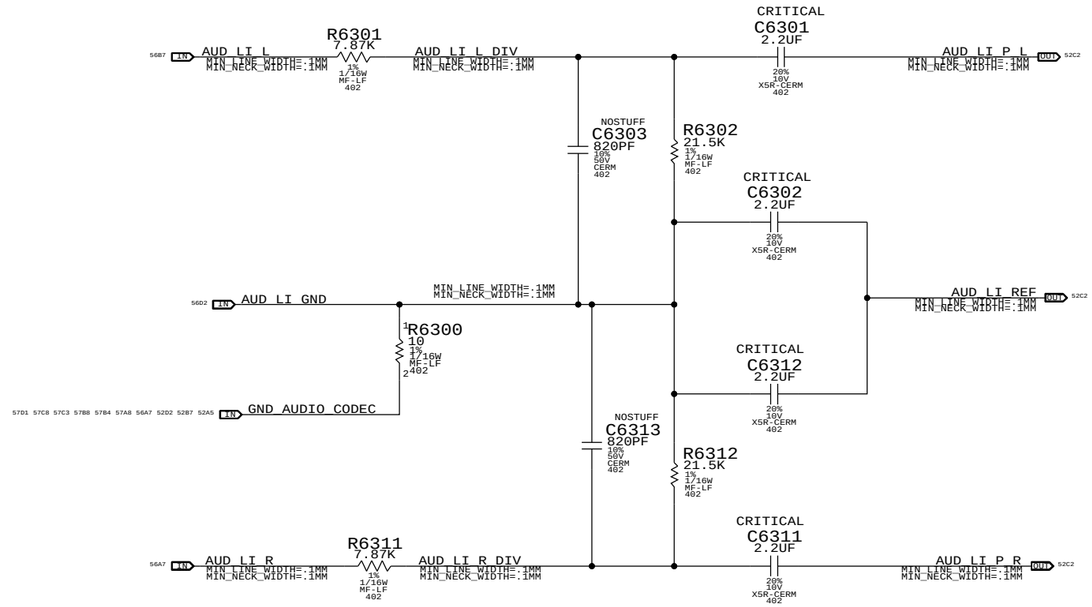
LINE INPUT VOLTAGE DIVIDER

CODEC RIN = 20K OHMS
NET RIN = 10.36K OHMS (INCLUDING PULL-DOWNS AT ANALOG SWITCH COM PINS)
FC_HP = 3.6 HZ
FC_LP = 43KHZ
VIN = 2VRMS, CODEC VIN = 1.14 VRMS



SYNC_MASTER=AUDIO SYNC_DATE=01/31/2009

PAGE TITLE

AUDIO: LINE INPUT FILTER

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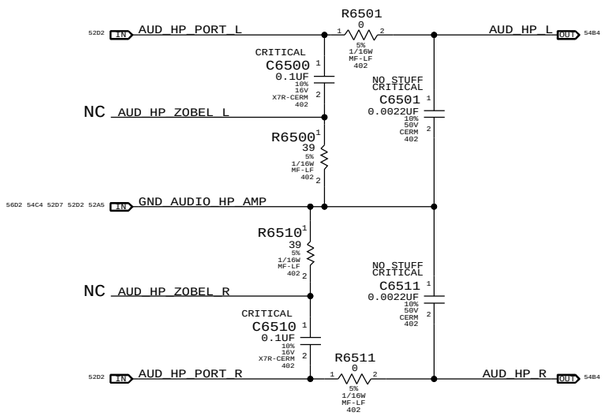
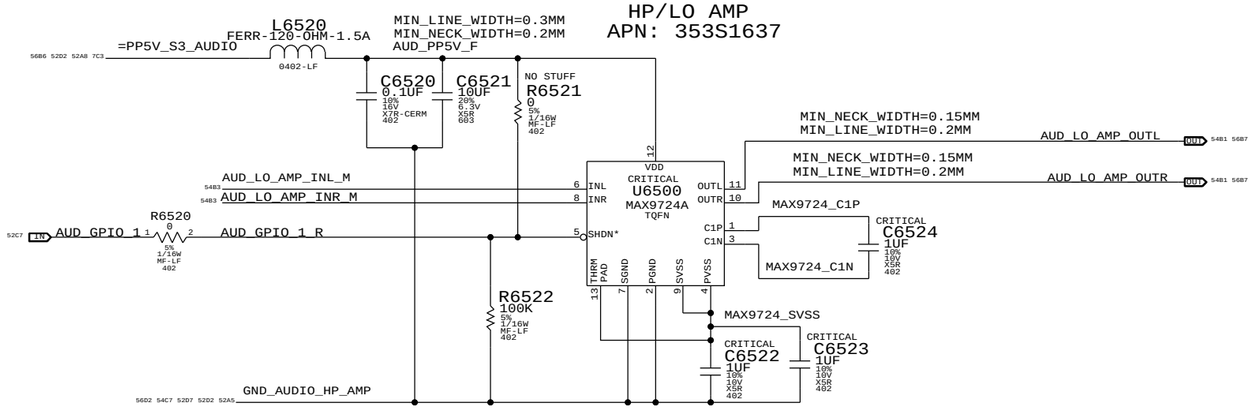
ZOBEL NETWORK & 1ST ORDER DAC FILTER PLACEHOLDER

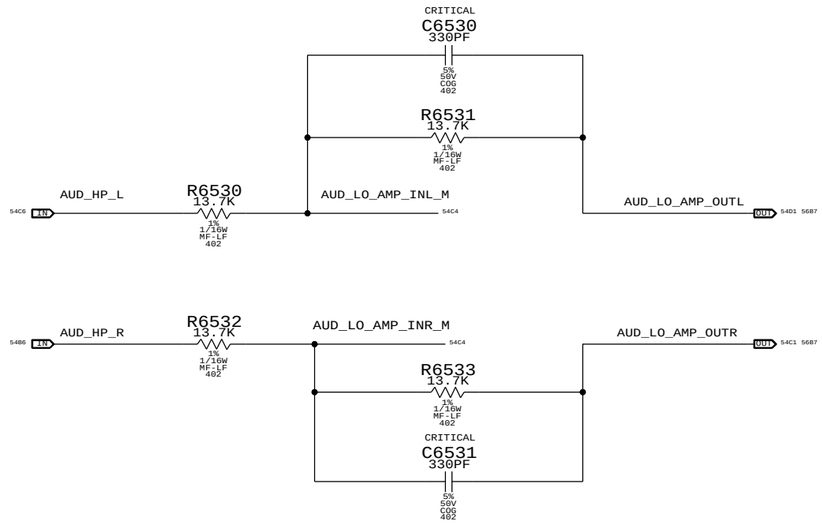


FOR PROTO2, STUFF R6521 AND NO STUFF R6520 AND R6522 UNTIL
RE-TASKABLE IO SW SUPPORT AVAILABLE (FORCES IO INTO OUTPUT MODE).

HP/LO AMP
APN: 353S1637



MAX9724 GAIN/FILTER COMPONENTS
AV_PB = -1V/V, FC_LPF = 35.2KHZ



SYNC_MASTER=AUDIO SYNC_DATE=02/03/2009

PAGE TITLE
AUDIO: HEADPHONE FILTER

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D
REVISION C.0.0
BRANCH
PAGE 65 OF 109
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

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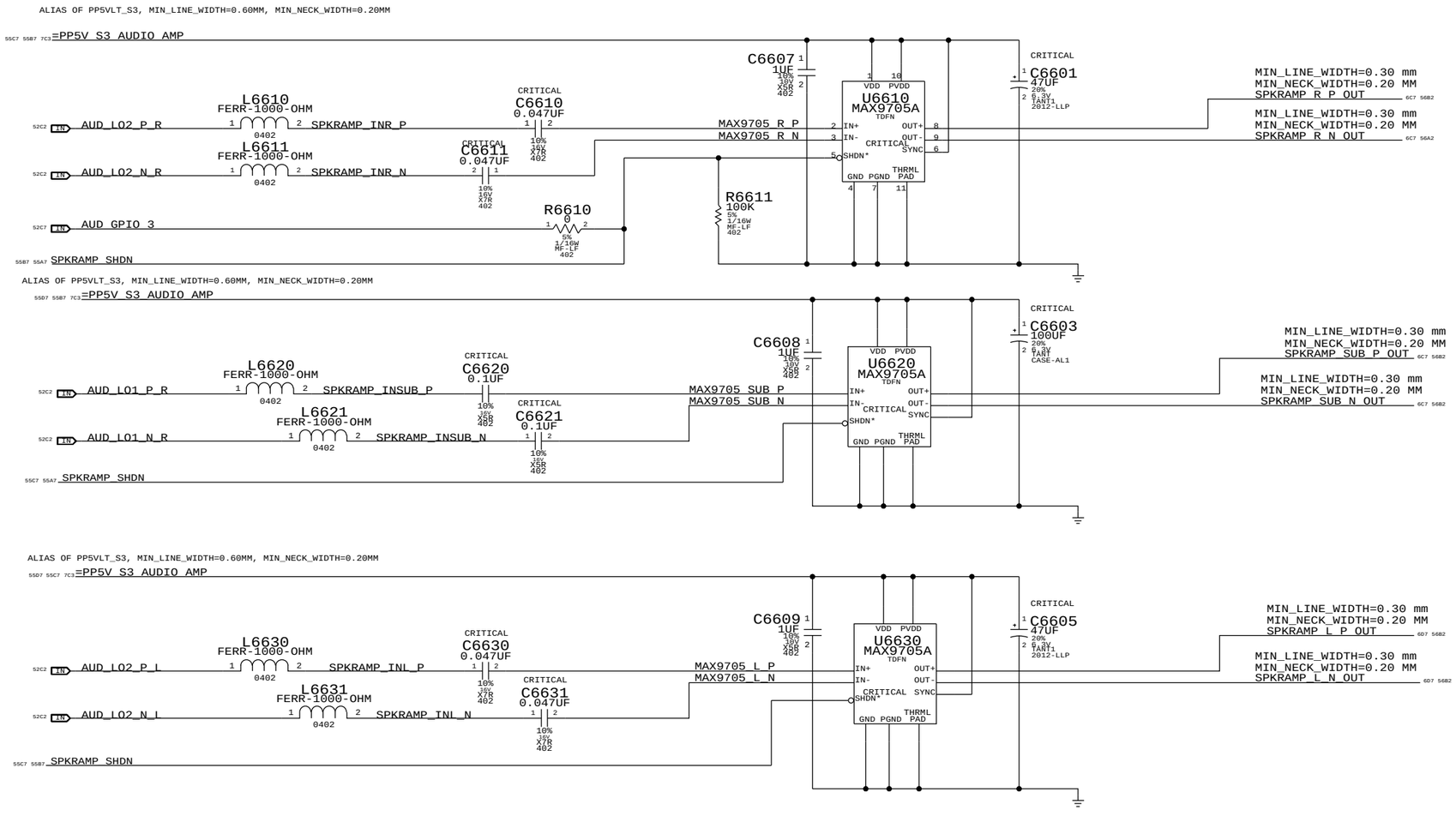
SATELLITE & SUB TWEETER AMPLIFIER

APN:353S2524

SATELLITE	169 HZ < FC < 282 HZ
SUB	80 HZ < FC < 132 HZ
GAIN	6DB



SYNC_MASTER=AUDIO SYNC_DATE=12/18/2008

PAGE TITLE

AUDIO: SPEAKER AMP

Apple Inc.

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PAGE 66 OF 109

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AUDIO JACK: LI/LO/HP CONNECTOR, SPDIF TX

=PP3V3_S0_AUDIO

APN:514-0671
J6700
SPDIF-TXRX-K24
F-RT-TH
CRITICAL
MIC 6
DETECT 5
SWITCH 2
LEFT 1
RIGHT 3
GND 4
AUDIO

A - VIN 7
B - VCC 8
C - GND 9
OPERATING VOLTAGE 3.3
POF

SHELL 10 11 12 13
SHIELD PINS

C6700 1UF 10% 6.3V CERM 402

AUD_SPDIF_OUT

L6701 FERR-1000-OHM 0402 — HS_MIC_HI
L6702 FERR-1000-OHM 0402 — HS_MIC_LO
L6706 CRITICAL FERR-220-OHM 0402 — AUD_HP_PORT_REF
CRITICAL L6703 FERR-120-OHM-1.5A 0402-LF — AUD_CONN_GND
CRITICAL L6704 FERR-220-OHM 0402 — AUD_CONN_L
CRITICAL L6705 FERR-220-OHM 0402 — AUD_CONN_R

AUD_CONNJ1_MIC
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
AUD_CONNJ1_SLEEVE
AUD_CONNJ1_SLEEVEDET
AUD_CONNJ1_TIPDET
AUD_CONNJ1_TIP
AUD_CONNJ1_RING

CRITICAL DZ6701 6.8V-100PF 402
CRITICAL DZ6704 6.8V-100PF 402
CRITICAL DZ6705 6.8V-100PF 402
CRITICAL DZ6703 6.8V-100PF 402
CRITICAL DZ6700 6.8V-100PF 402

R6700 10K 5% 1/10W MF-LF 402 — AUD_J1_SLEEVEDET_R
R6701 4.7 5% 1/10W MF-LF 402 — AUD_J1_TIPDET_R
C6701 100PF 5% 50V CERM 402

XW6700 SM — GND_AUDIO_HP_AMP
XW6701 SM — AUD_LI_GND
AUD_CONN_GND

GND_CHASSIS_AUDIO_JACK
CHASSIS_GND_STITCHES
XW6710 SM
XW6711 SM
R6760 0 5% 1/10W MF-LF 402

NOSTUFF R6723 0 5% 1/10W MF-LF 402
NOSTUFF R6722 0 5% 1/10W MF-LF 402
NOSTUFF R6725 0 5% 1/10W MF-LF 402
=PP3V42_G3H_AUDIO

R6724 0 5% 1/10W MF-LF 402
=PP5V_S3_AUDIO
PP_MAX14504_VCC
C6710 1UF 10% 10V X5R 402
NOSTUFF R6726 0 5% 1/10W MF-LF 402

APN: 353S2536

U6700 MAX14504 WLP CRITICAL
VCC A3
C4 NC1
C1 NC2
A4 NO1
A1 NO2
C2 CB
A2 NEG
COM1 B4
COM2 B1
EN* B2
GND B3 C3

SWITCH_CP
C6711 0.0033UF 10% 50V CERM 402

AUD_LO_AMP_OUTL — R6716 0 5% 1/10W MF-LF 402 — AUD_LO_AMP_OUTL_SWITCH
AUD_LO_AMP_OUTR — R6717 0 5% 1/10W MF-LF 402 — AUD_LO_AMP_OUTR_SWITCH
AUD_LI_L — R6718 0 5% 1/10W MF-LF 402 — AUD_LI_L_SWITCH
AUD_LI_R — R6719 0 5% 1/10W MF-LF 402 — AUD_LI_R_SWITCH
AUD_GPIO_0 — R6720 0 5% 1/10W MF-LF 402 — AUD_SWITCH_CTRL
R6721 100K 5% 1/16W MF-LF 402
AUD_CONN_GND — R6715 0 5% 1/10W MF-LF 402 — AUD_SWITCH_GND
GND_STUFFING_OPTIONS_FOR_CMOS_SWITCH
GND_AUDIO_CODEC — R6714 0 5% 1/10W MF-LF 402
NOSTUFF R6727 0 5% 1/10W MF-LF 402

MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.15MM
R6712 24K 5% 1/10W MF-LF 402
R6713 24K 5% 1/16W MF-LF 402

ANALOG AUDIO IO SWITCH

GPIO0 = 0 AND GPIO1 = 1 --> HP PATH SELECTED
GPIO0 = 1 AND GPIO1 = 0 --> LI PATH SELECTED

MIC CONNECTOR

APN:518S0520
CRITICAL J6701 78171-0003 M-RT-SM
BI_MIC_LO
BI_MIC_SHIELD
BI_MIC_HI

SPEAKER CONNECTOR

APN:518S0519
CRITICAL J6702 78171-0002 M-RT-SM
SPKRAMP_L_P_OUT
SPKRAMP_L_N_OUT
SPKRAMP_SUB_P_OUT
C6760 33PF 5% 50V CERM 402
C6761 33PF 5% 50V CERM 402
SPKRAMP_SUB_N_OUT
SPKRAMP_R_P_OUT
C6762 33PF 5% 50V CERM 402
C6763 33PF 5% 50V CERM 402
SPKRAMP_R_N_OUT
CRITICAL J6703 78171-0004 M-RT-SM
APN:518S0521
C6760 - C6763 ARE FOR FILTERING POTENTIAL FSB NOISE COUPLED ON SPKR LINES

SYNC_MASTER=AUDIO
SYNC_DATE=03/20/2009
PAGE TITLE: AUDIO: JACK
Apple Inc.
DRAWING NUMBER: 051-7898
SIZE: D
REVISION: C.0.0
BRANCH:
PAGE: 67 OF 109
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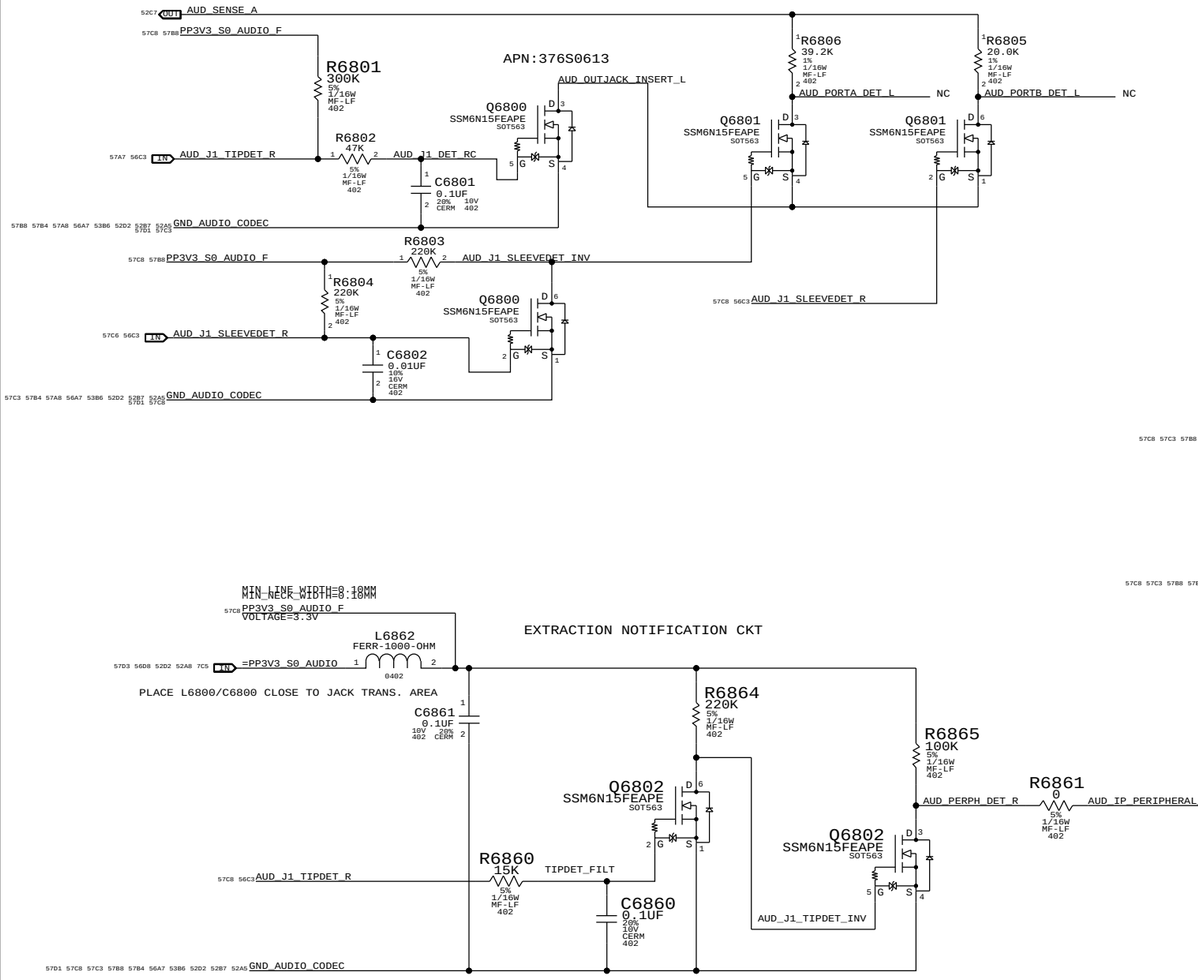
CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP/LINE OUT	0X02 (2)	0X02 (2)	0X09 (9,A)	GPIO_0 AND GPIO_1	0X09 (A)
LINE IN	0X05 (5)	0X05 (5)	0X0C (12)	GPIO_0 AND GPIO_1	0X09 (A)AND UI ELEMENT
SATELLITES	0X04 (4)	0X04 (4)	0X0B (11)	GPIO_3	N/A
SUB	0X03 (3)	0X03 (03)	0X0A (10)	GPIO_3	N/A
SPDIF OUT	N/A	0X08 (8)	0X10 (16)	N/A	0X0D (B)

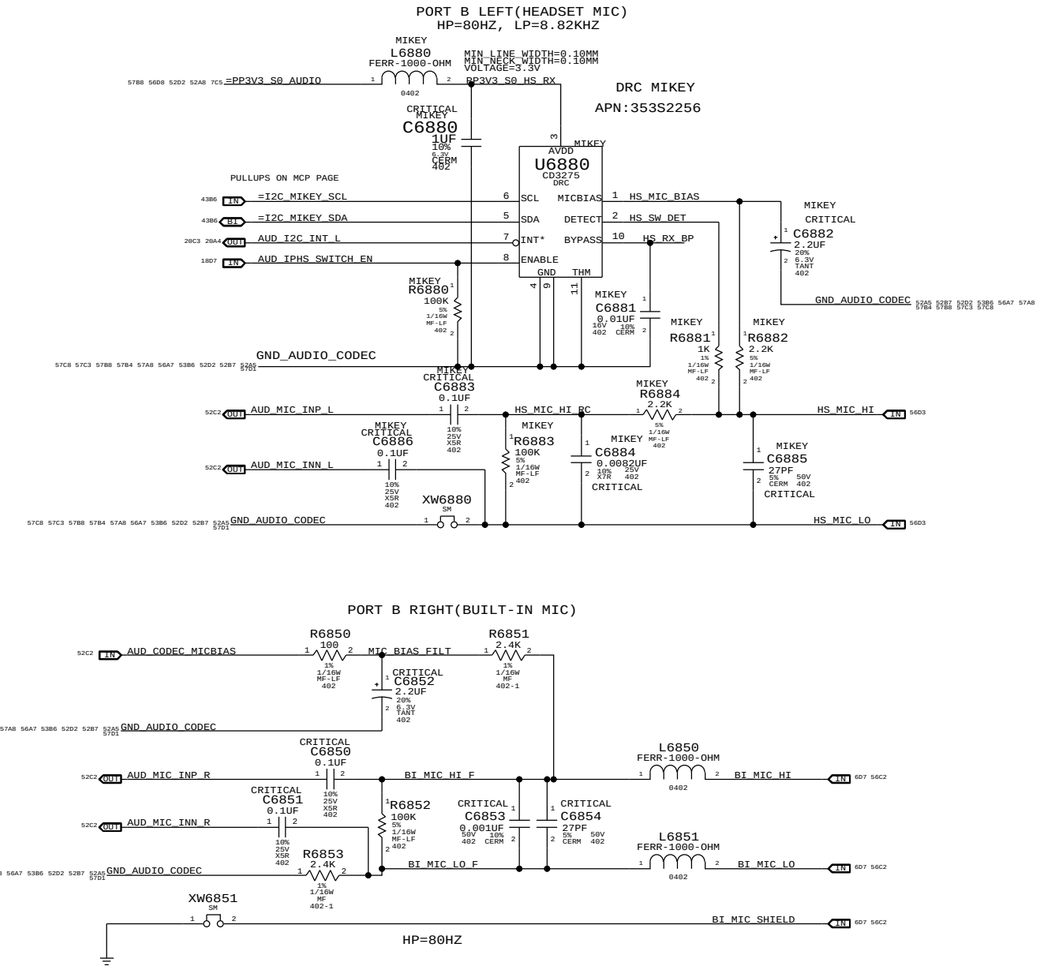
CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
BUILT-IN MIC	0X06 (6)	0X0D (13,B,RIGHT)	MIC_BIAS (80%)	N/A
HEADSET MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	MIKEY	MIKEY

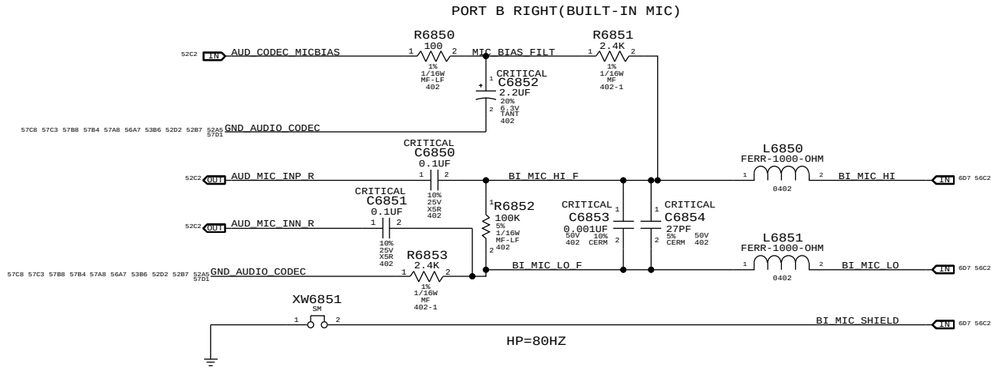
PORT A DETECT (HEADPHONES) PORT B DETECT(SPDIF DELEGATE)



PORT B LEFT(HEADSET MIC)
HP=80HZ, LP=8.82KHZ



PORT B RIGHT(BUILT-IN MIC)



EXTRACTION NOTIFICATION CKT

SYNC_MASTER=AUDIO	SYNC_DATE=03/20/2009
PAGE TITLE	AUDIO: JACK TRANSLATORS
Apple Inc.	DRAWING NUMBER 051-7898 SIZE D
	REVISION C.0.0
	BRANCH
	PAGE 68 OF 109
	SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

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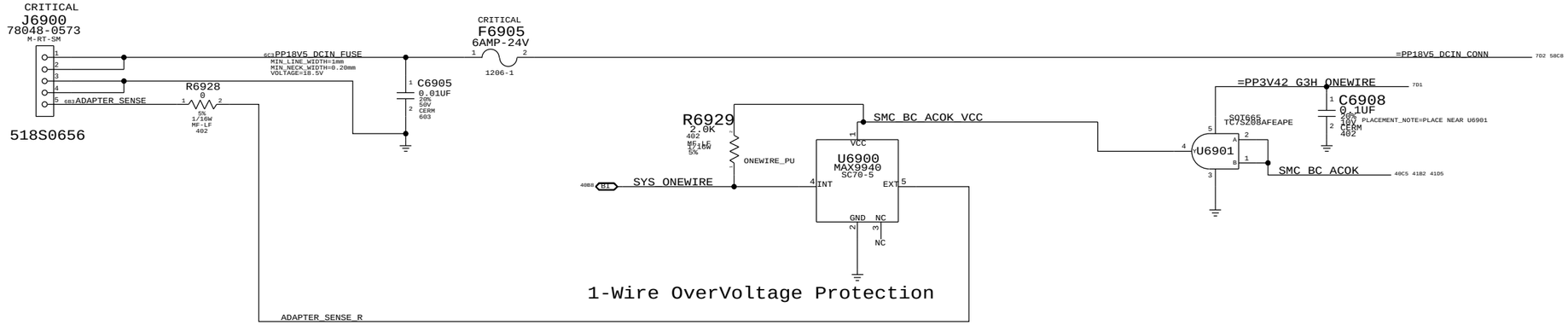
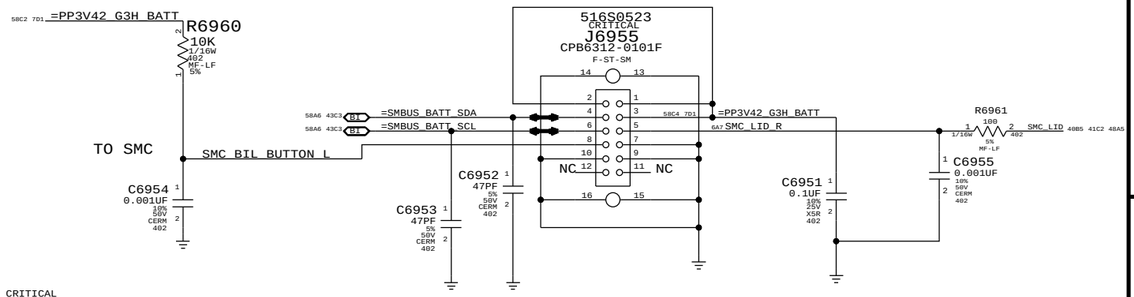
MagSafe DC Power Jack

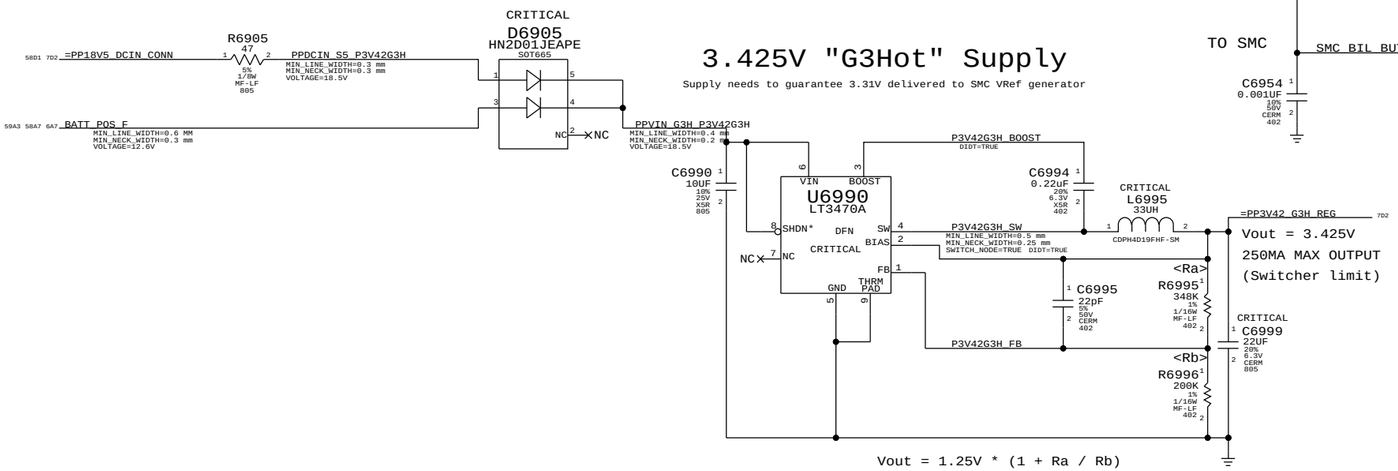


BIL CONNECTOR

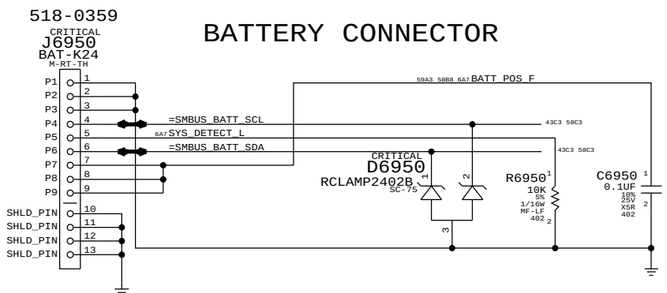


3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator



BATTERY CONNECTOR



SYNC_MASTER=YUNWU	SYNC_DATE=12/11/2008
PAGE TITLE: DC-In & Battery Connectors	
Apple Inc.	DRAWING NUMBER: 051-7898 SIZE: D
	REVISION: C.0.0
	BRANCH:
	PAGE: 69 OF 109
	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

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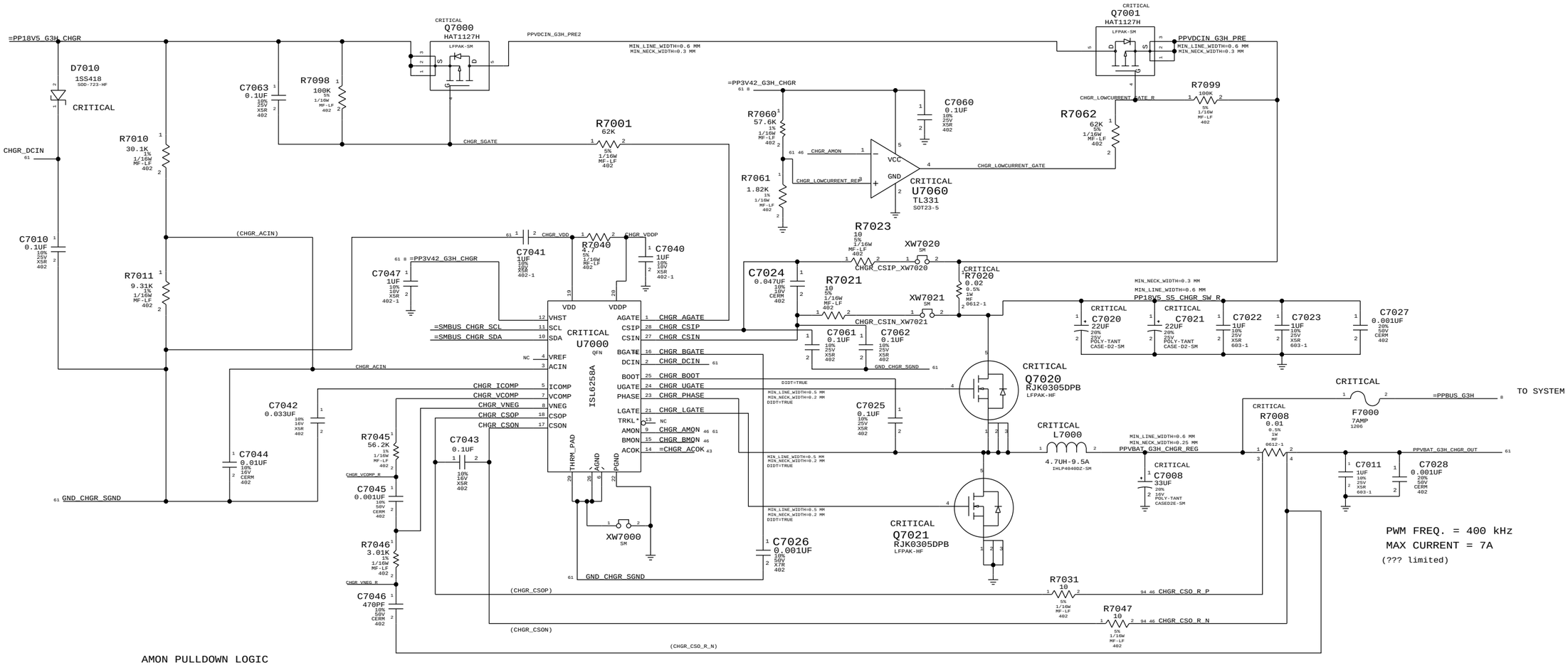
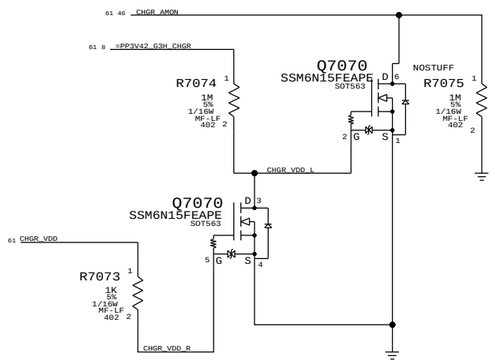
PBUS SUPPLY / BATTERY CHARGER

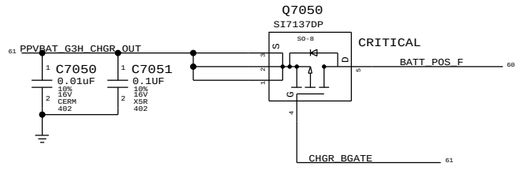


PWM FREQ. = 400 kHz
MAX CURRENT = 7A
(??? limited)

AMON PULLDOWN LOGIC



BATTERY CHARGE LIMITING FETS



SYNC_MASTER=K24_MLB SYNC_DATE=05/20/2009

PAGE TITLE: PBUS Supply/Battery Charger

Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D
REVISION: C.0.0
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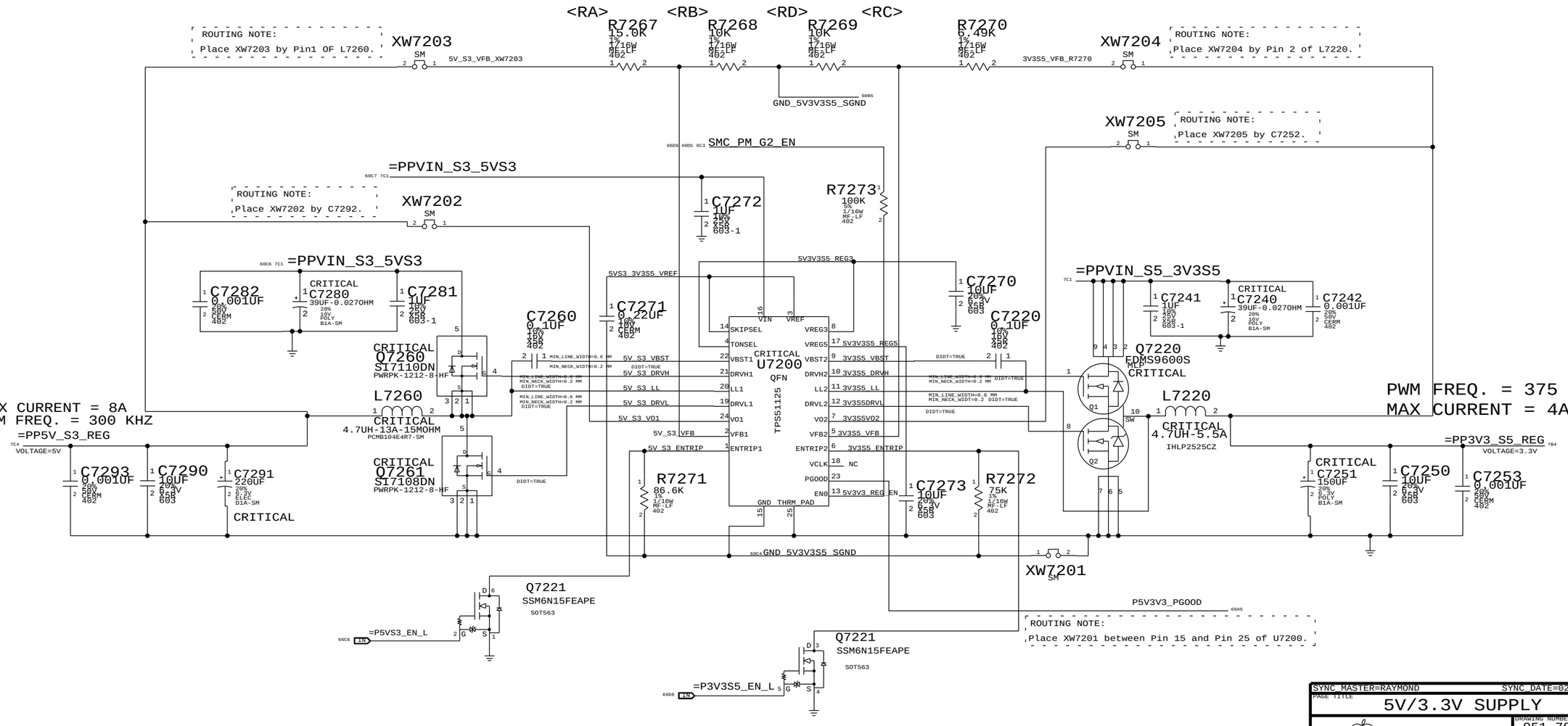
5V_S3/3.3V_S5 POWER SUPPLY

VOUT = (2 * RA / RB) + 2

VOUT = (2 * RC / RD) + 2



SYNC_MASTER=RAYMOND	SYNC_DATE=02/08/2008
PAGE TITLE	5V/3.3V SUPPLY
Apple Inc.	DRAWING NUMBER 051-7898 · SIZE D
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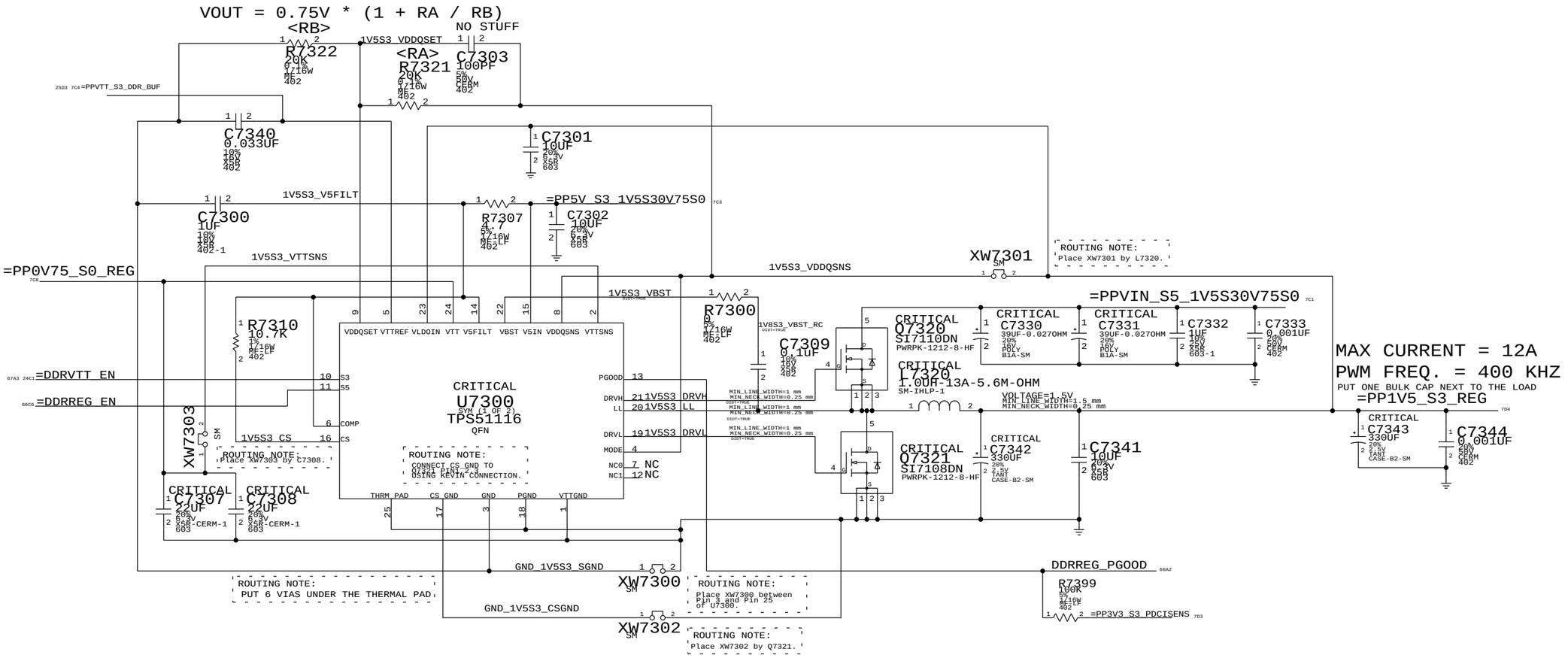
	PAGE 72 OF 109
	SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

1.5V/0.75V(DDR3) POWER SUPPLY



STATE	PM_SLP_S4_L	PM_SLP_S3_L	PP1V5_S3	PP0V75_S0
S0	HIGH	HIGH	1.5V	0.75V
S3	HIGH	LOW	1.5V	0.0V
S5/G3HOT	LOW	LOW	0.0V	0.0V

SYNC_MASTER=RAYMOND SYNC_DATE=01/31/2008

PAGE TITLE: 1.5V/0.75V DDR3 SUPPLY

Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D

REVISION: C.0.0

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PAGE: 73 OF 109

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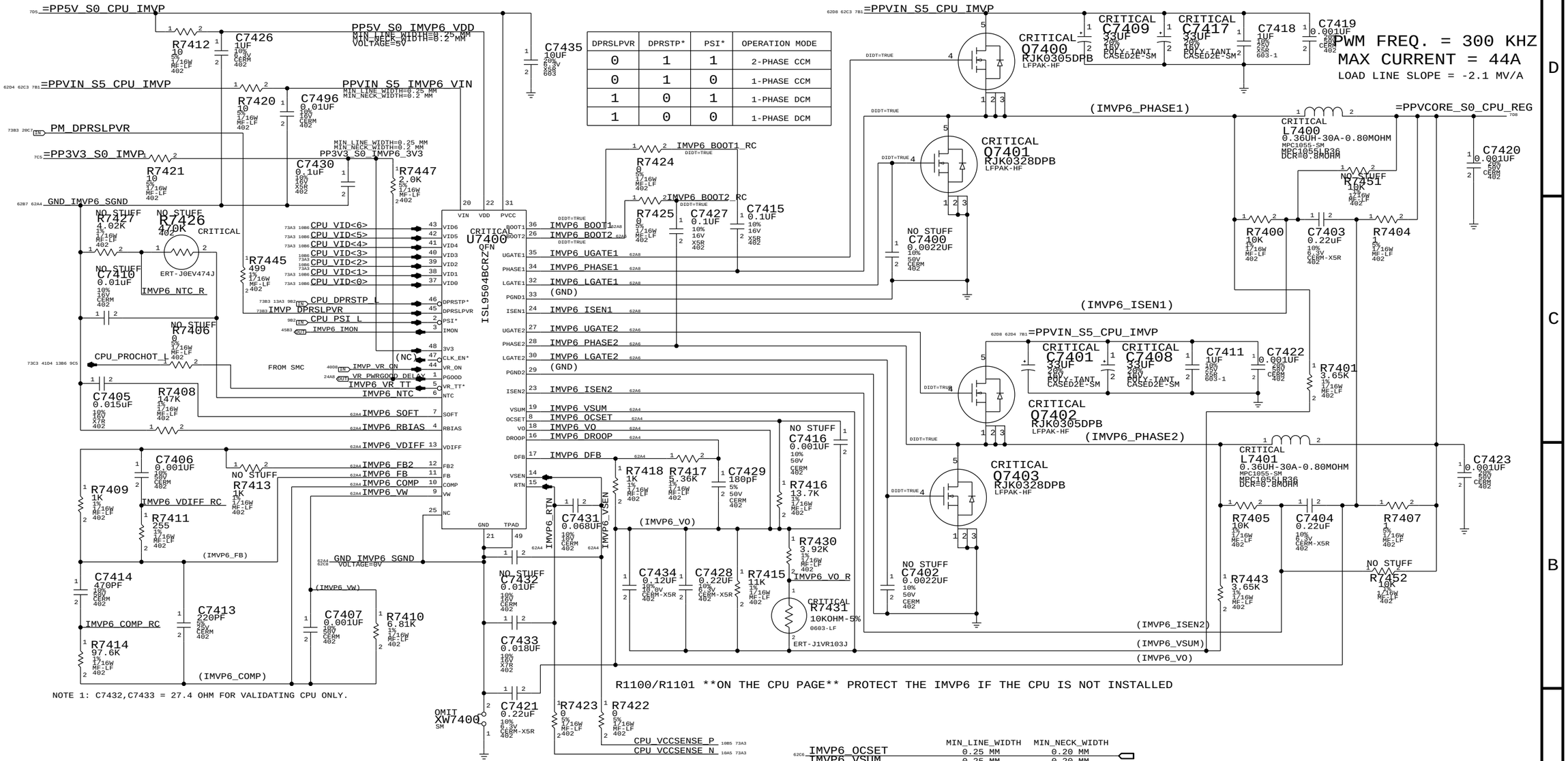

DPRSLPVR	DPRSTP*	PSI*	OPERATION MODE
0	1	1	2-PHASE CCM
0	1	0	1-PHASE CCM
1	0	1	1-PHASE DCM
1	0	0	1-PHASE DCM

PWM FREQ. = 300 KHZ
MAX CURRENT = 44A
LOAD LINE SLOPE = -2.1 MV/A

NOTE 1: C7432,C7433 = 27.4 OHM FOR VALIDATING CPU ONLY.

R1100/R1101 **ON THE CPU PAGE** PROTECT THE IMVP6 IF THE CPU IS NOT INSTALLED

IMVP6 CPU VCORE REGULATOR

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE1	1.5 MM	0.25 MM
IMVP6_BOOT1	0.25 MM	0.25 MM
IMVP6_UGATE1	1.5 MM	0.25 MM
IMVP6_LGATE1	1.5 MM	0.25 MM
IMVP6_ISEN1	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE2	0.25 MM	0.25 MM
IMVP6_BOOT2	0.25 MM	0.25 MM
IMVP6_UGATE2	0.25 MM	0.25 MM
IMVP6_LGATE2	0.25 MM	0.25 MM
IMVP6_ISEN2	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_OCSET	0.25 MM	0.20 MM
IMVP6_VSUM	0.25 MM	0.20 MM
GND_IMVP6_SGND	0.50 MM	0.20 MM
IMVP6_VO	0.25 MM	0.20 MM
IMVP6_DROOP	0.25 MM	0.20 MM
IMVP6_DFB	0.25 MM	0.20 MM
IMVP6_SOFT	0.25 MM	0.20 MM
IMVP6_RBIAS	0.25 MM	0.20 MM
IMVP6_VDIFF	0.25 MM	0.20 MM
IMVP6_FB2	0.25 MM	0.20 MM
IMVP6_FB	0.25 MM	0.20 MM
IMVP6_COMP	0.25 MM	0.20 MM
IMVP6_VW	0.25 MM	0.25 MM
IMVP6_RTN	0.25 MM	0.25 MM
IMVP6_VSEN	0.25 MM	0.25 MM

SYNC_MASTER=RAYMOND SYNC_DATE=01/31/2008

PAGE TITLE: IMVP6 CPU VCore Regulator

Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D
REVISION: C.0.0
BRANCH:
PAGE: 74 OF 109
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

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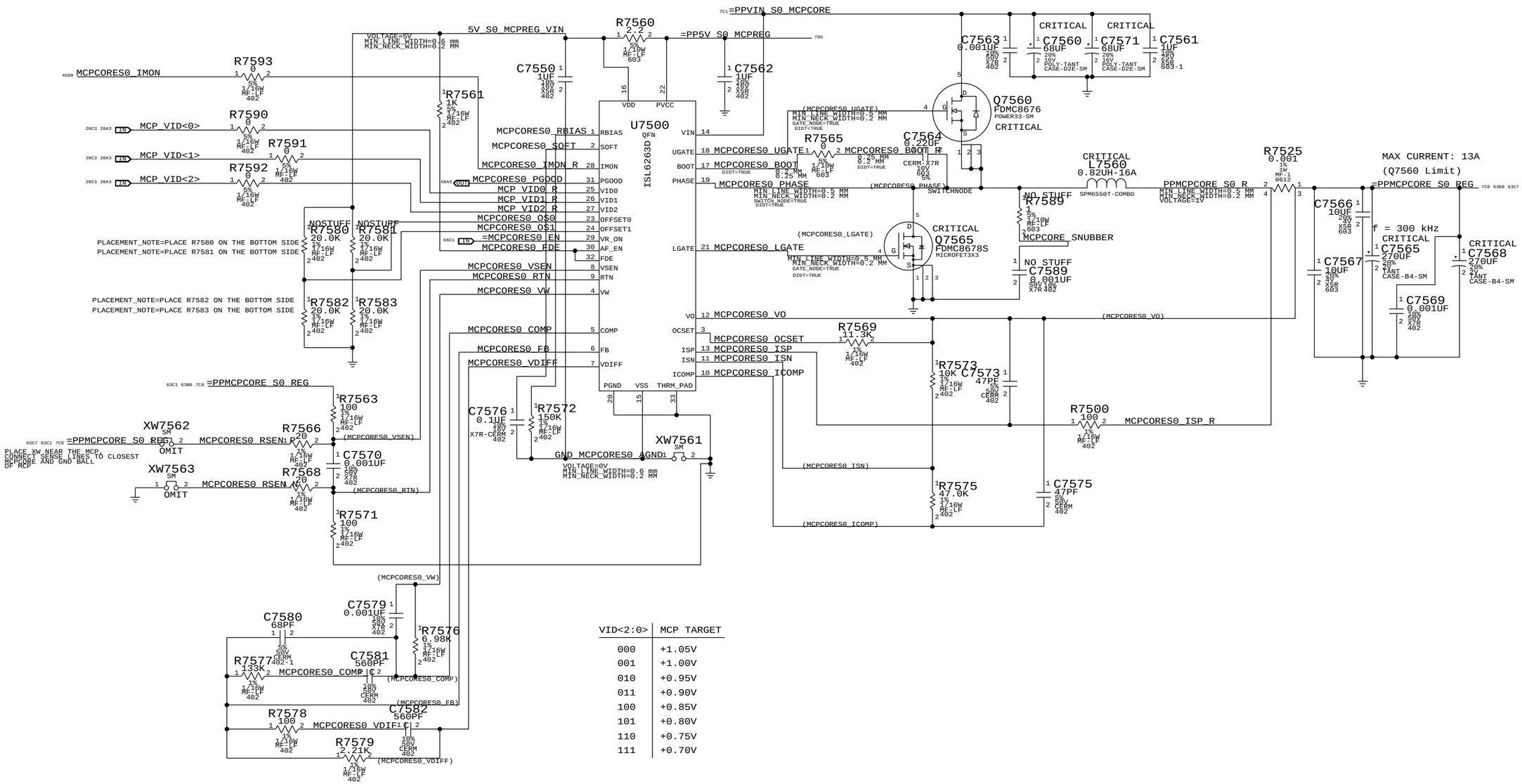
MCP VCORE POWER SUPPLY



VID<2:0>	MCP TARGET
000	+1.05V
001	+1.00V
010	+0.95V
011	+0.90V
100	+0.85V
101	+0.80V
110	+0.75V
111	+0.70V

SYNC MASTER=K19_MLB SYNC DATE=12/10/2008

PAGE TITLE: MCP CORE REGULATOR

Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D

REVISION: C.0.0

BRANCH:

PAGE: 75 OF 109

SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

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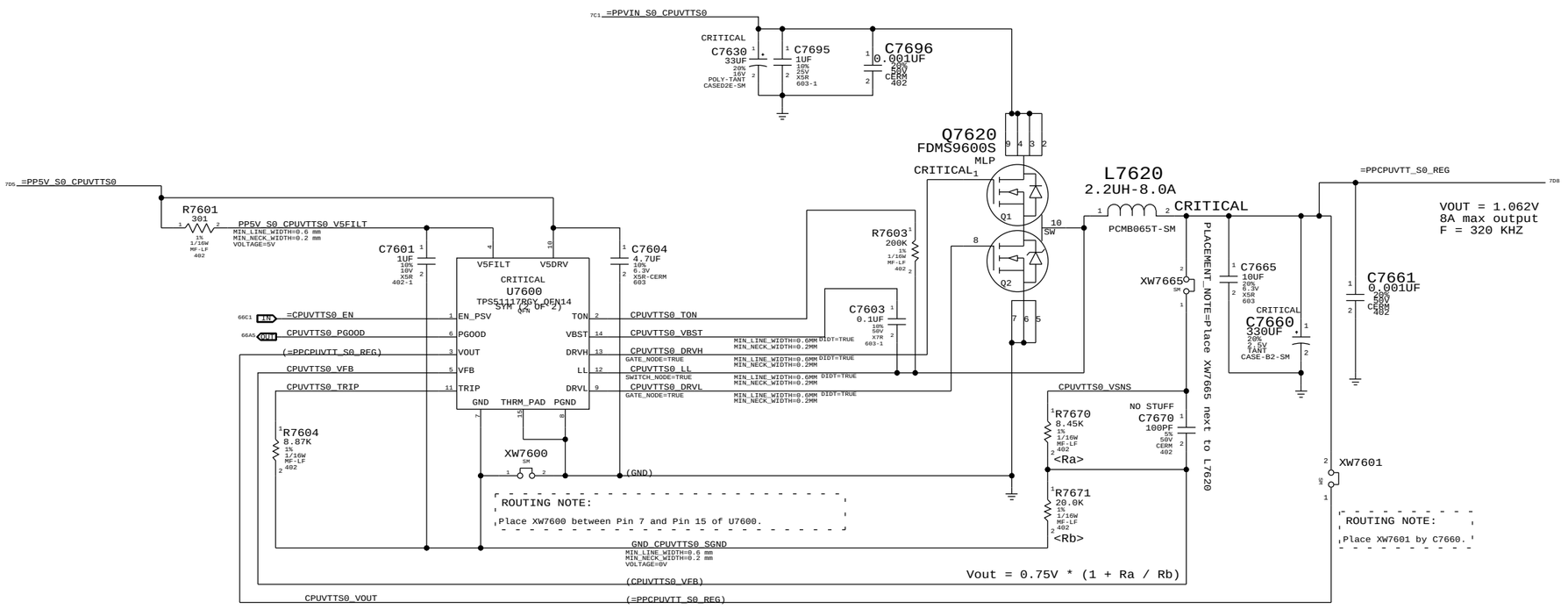
CPUVTT POWER SUPPLY



SYNC_MASTER=RAYMOND SYNC_DATE=02/08/2008

PAGE TITLE
CPU VTT(1.05V) SUPPLY

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D
REVISION C.0.0
BRANCH
PAGE 76 OF 109
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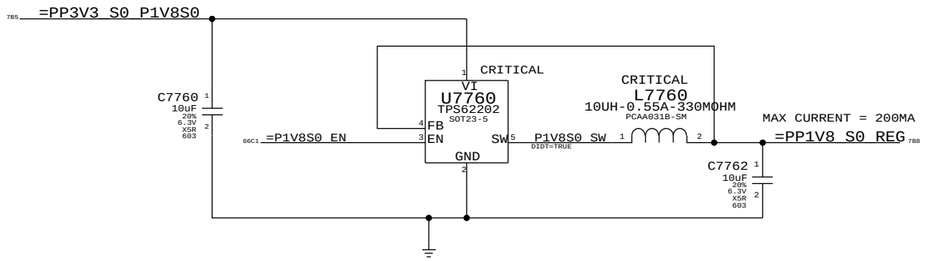
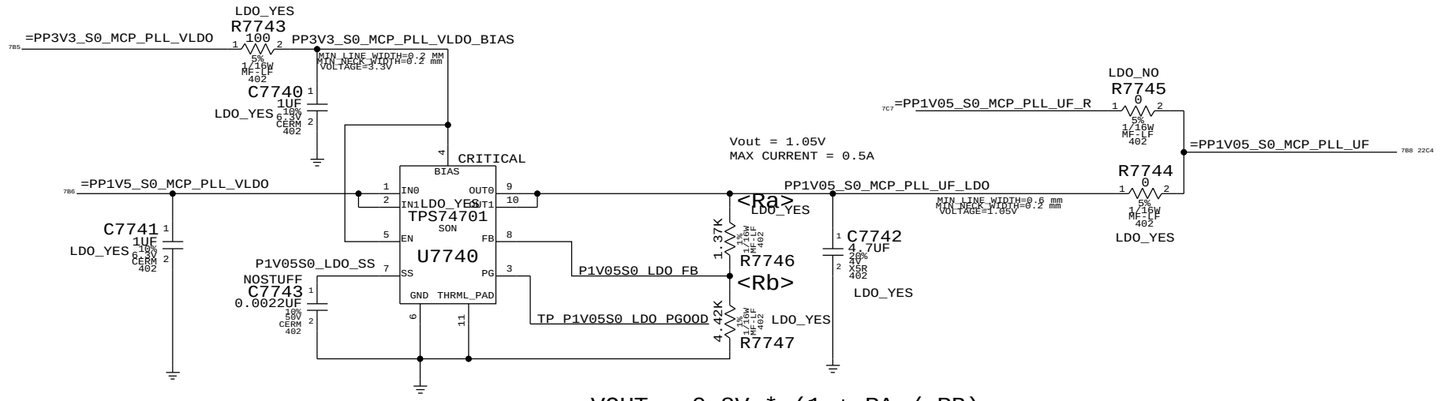
1.8V S0 SWITCHER

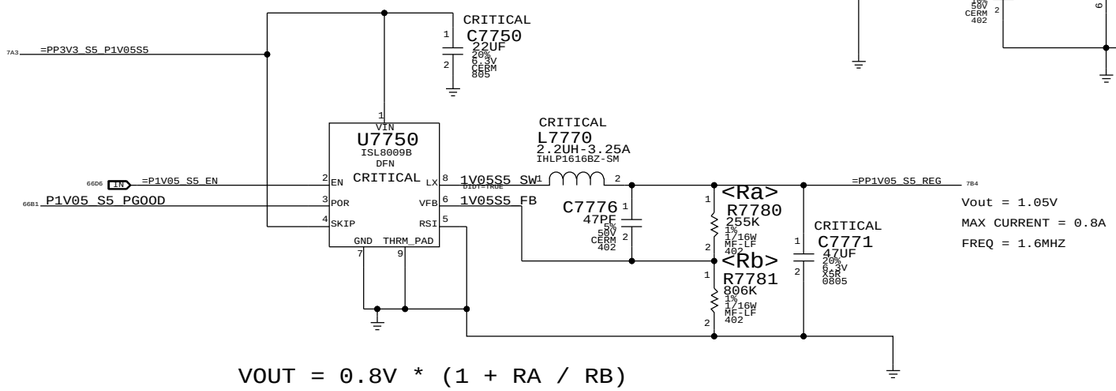


1.05V S0 PLL LDO



VOUT = 0.8V * (1 + RA / RB)

MCP 1.05V S5 (AUXC) SUPPLY



VOUT = 0.8V * (1 + RA / RB)

SYNC_MASTER=RAYMOND SYNC_DATE=01/23/2008

PAGE TITLE

MISC POWER SUPPLIES

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D

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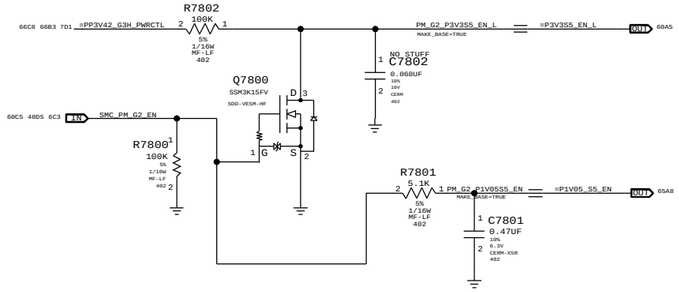
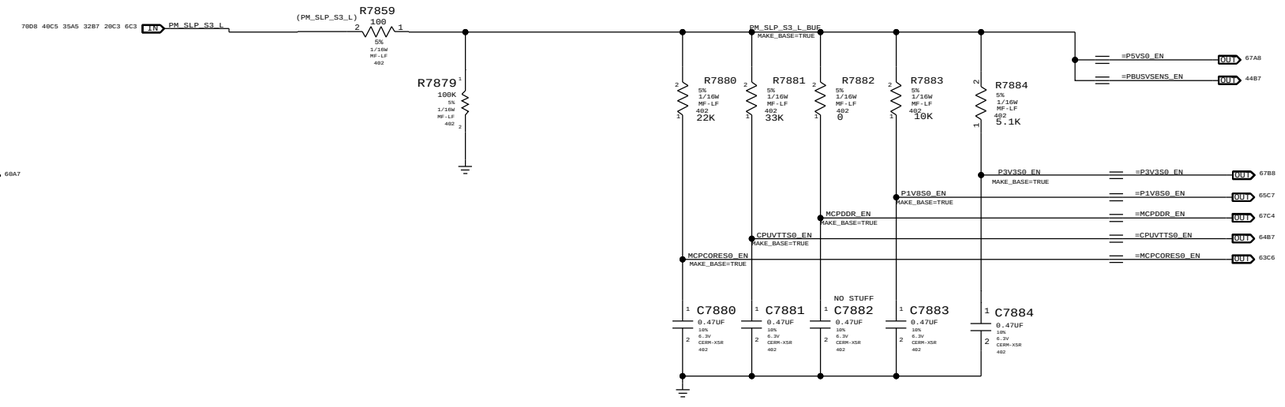
3.3V 1.05V S5 ENABLE



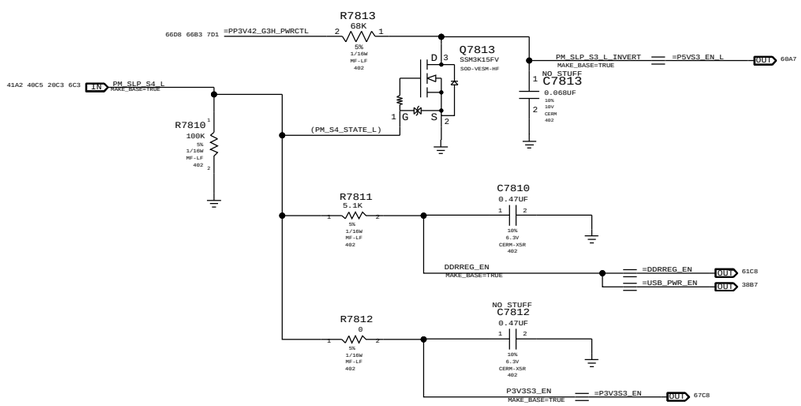
Power Control Signals

State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

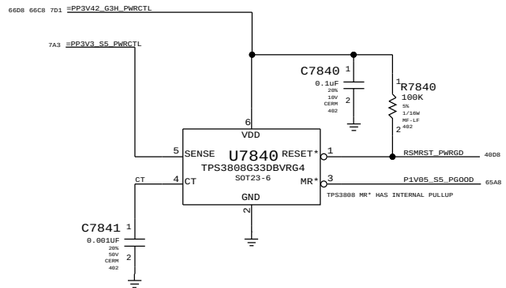
3.3V_S0, 1.8V_S0 ENABLE
MCPDDR, CPUVTT,MCPCORES0 ENABLE
1.5V S0 AND 1.05V S0 ENABLE



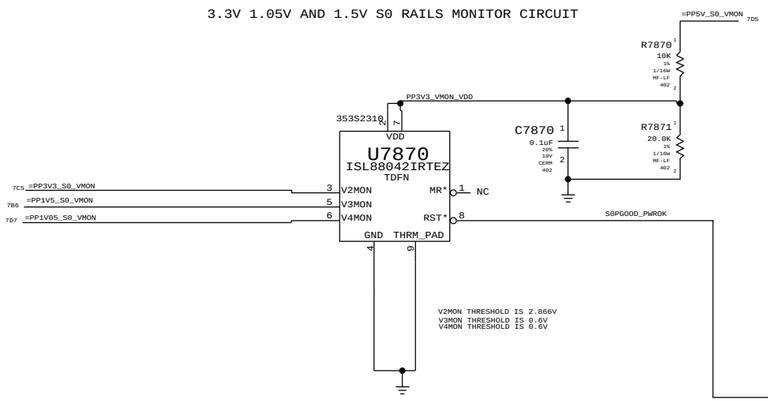
S3 ENABLE



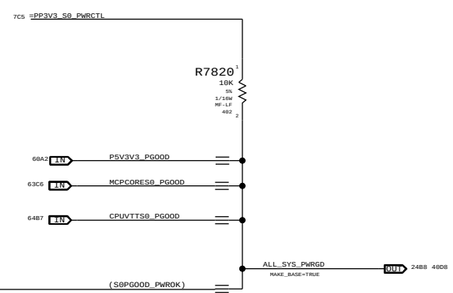
VOLTAGE MONITOR



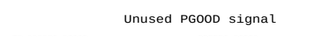
3.3V 1.05V AND 1.5V S0 RAILS MONITOR CIRCUIT



OTHER S0 RAILS PGOOD



Unused PGOOD signal



SYNC_MASTER=YUAN.MA SYNC_DATE=12/11/2008

PAGE TITLE

POWER SEQUENCING

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D

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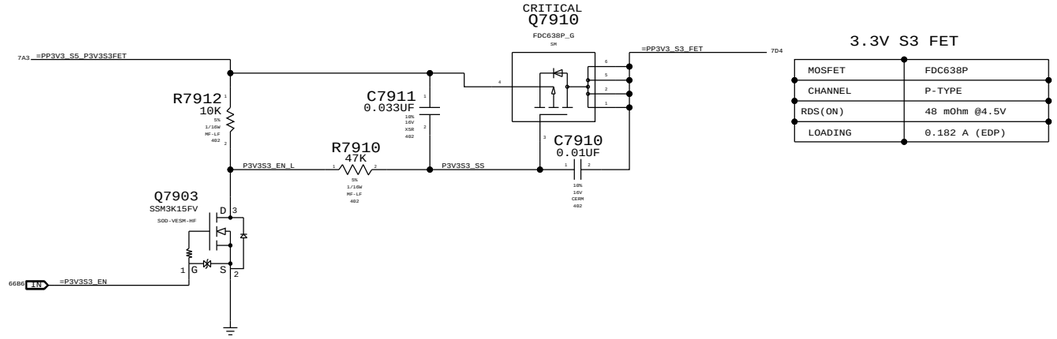
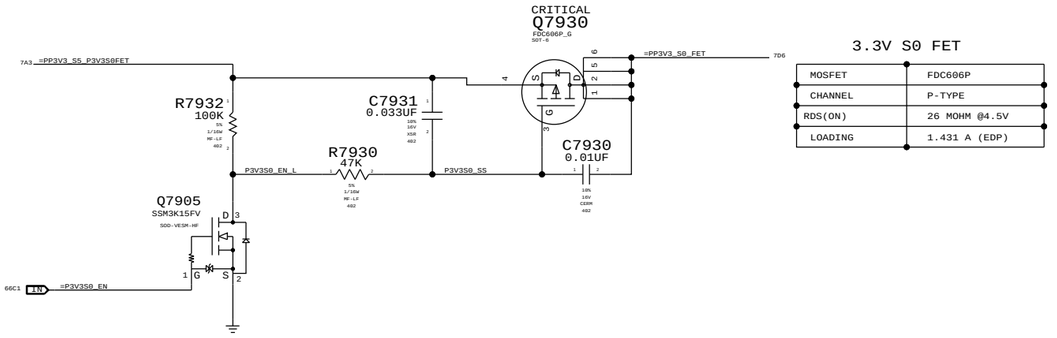
3.3V S3 FET



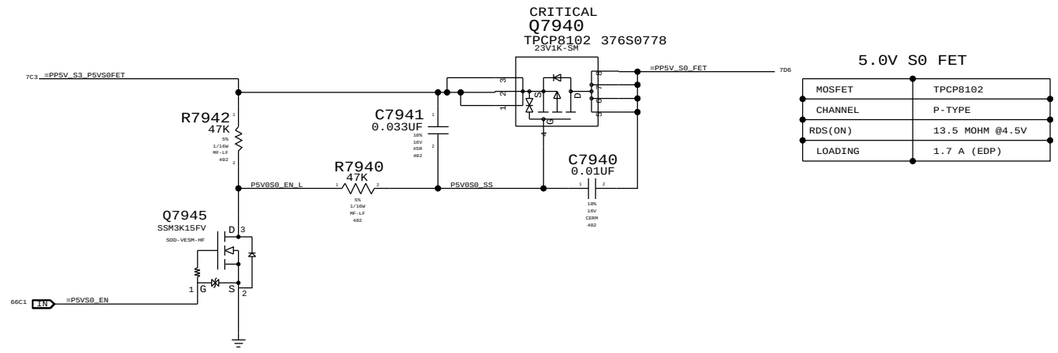
3.3V S3 FET	
MOSFET	FDC638P
CHANNEL	P-TYPE
RDS(ON)	48 mOhm @4.5V
LOADING	0.182 A (EDP)

3.3V S0 FET



3.3V S0 FET	
MOSFET	FDC606P
CHANNEL	P-TYPE
RDS(ON)	26 MOHM @4.5V
LOADING	1.431 A (EDP)

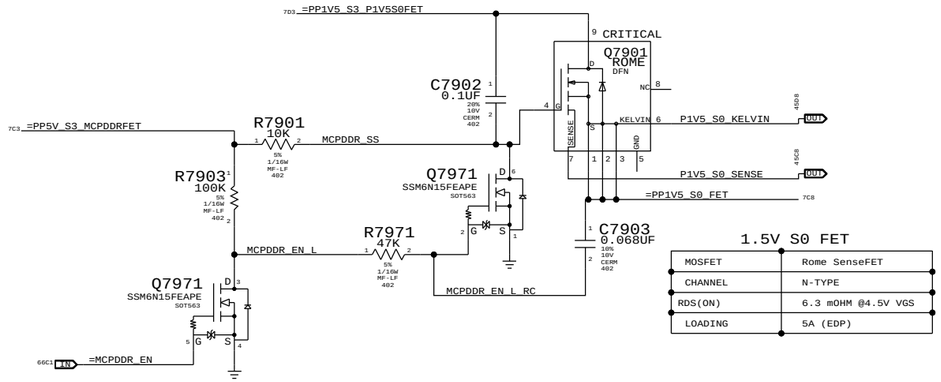
5.0V S0 FET



5.0V S0 FET	
MOSFET	TPCP8102
CHANNEL	P-TYPE
RDS(ON)	13.5 MOHM @4.5V
LOADING	1.7 A (EDP)

1.5V S0 FET

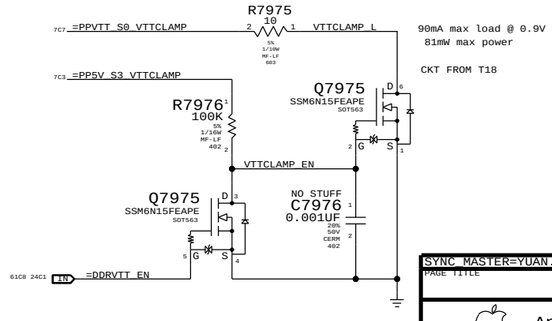
(1.5V S0 FET FOR DDR3 MEM, MCP79 AND CPU)



1.5V S0 FET	
MOSFET	Rome SenseFET
CHANNEL	N-TYPE
RDS(ON)	6.3 mOHM @4.5V VGS
LOADING	5A (EDP)

MCP79 DDRVTT FET

MCP79 DDR PAD LEAKAGE IS HIGH ENOUGH THAT
NVIDIA RECOMMENDS UNPOWERING DURING SLEEP.
IN ORDER TO SUPPORT UNPOWERING RAIL, HARDWARE
MUST GUARANTEE MEM_CKE SIGNALS ARE LOW
BEFORE RAIL IS TURNED OFF, AND REMAINS LOW
UNTIL AFTER RAIL TURNS BACK ON OR DIMMS
WILL EXIT SELF-REFRESH PREMATURELY.
MEM_VTT_EN OUTPUT FROM MCP79 USED TO ENABLE CLAMP
ON VTT RAIL, WHICH PULLS ALL CKE SIGNALS
LOW THROUGH VTT TERMINATION RESISTORS.



SYNC_MASTER=YUAN.MA SYNC_DATE=12/11/2008

PAGE TITLE: POWER FETS

Apple Inc.

DRAWING NUMBER: 051-7898 SIZE: D
REVISION: C.0.0
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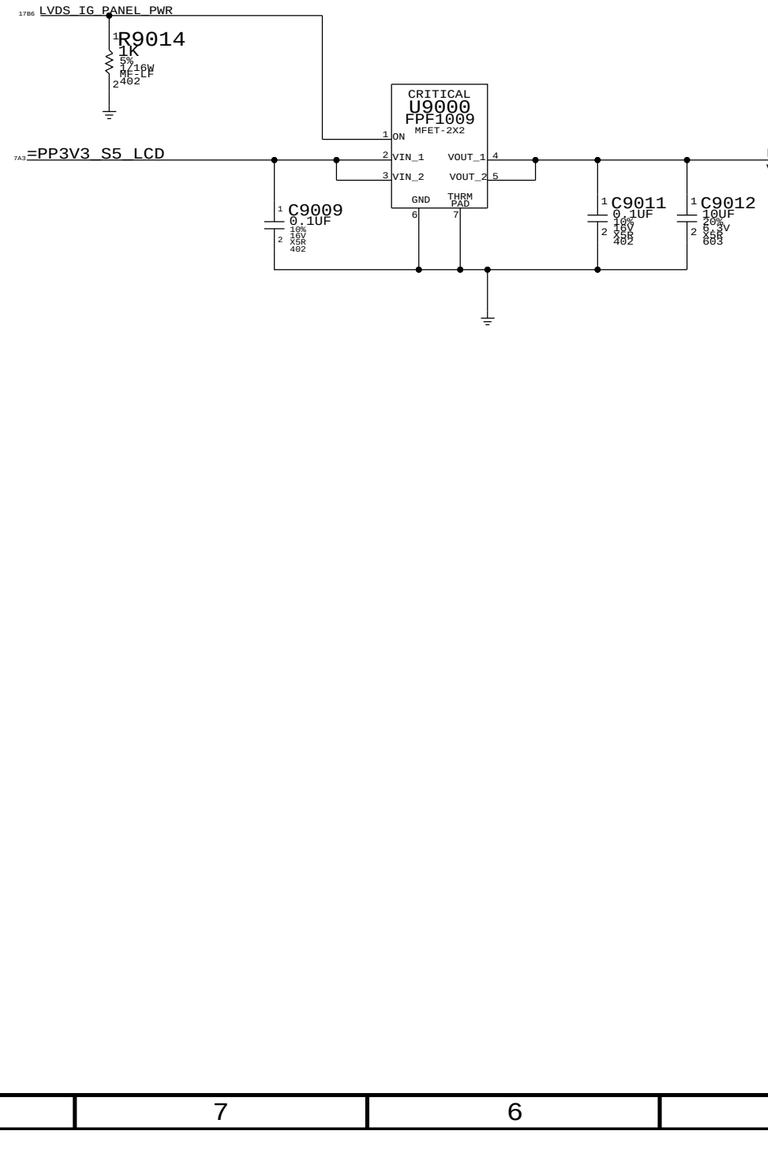
CHECK IF LVDS_IG_PANEL_PWR GLITCHES ON POWER UP



SYNC_MASTER=NMARTIN SYNC_DATE=04/04/2008

PAGE TITLE

LVDS CONNECTOR

Apple Inc.

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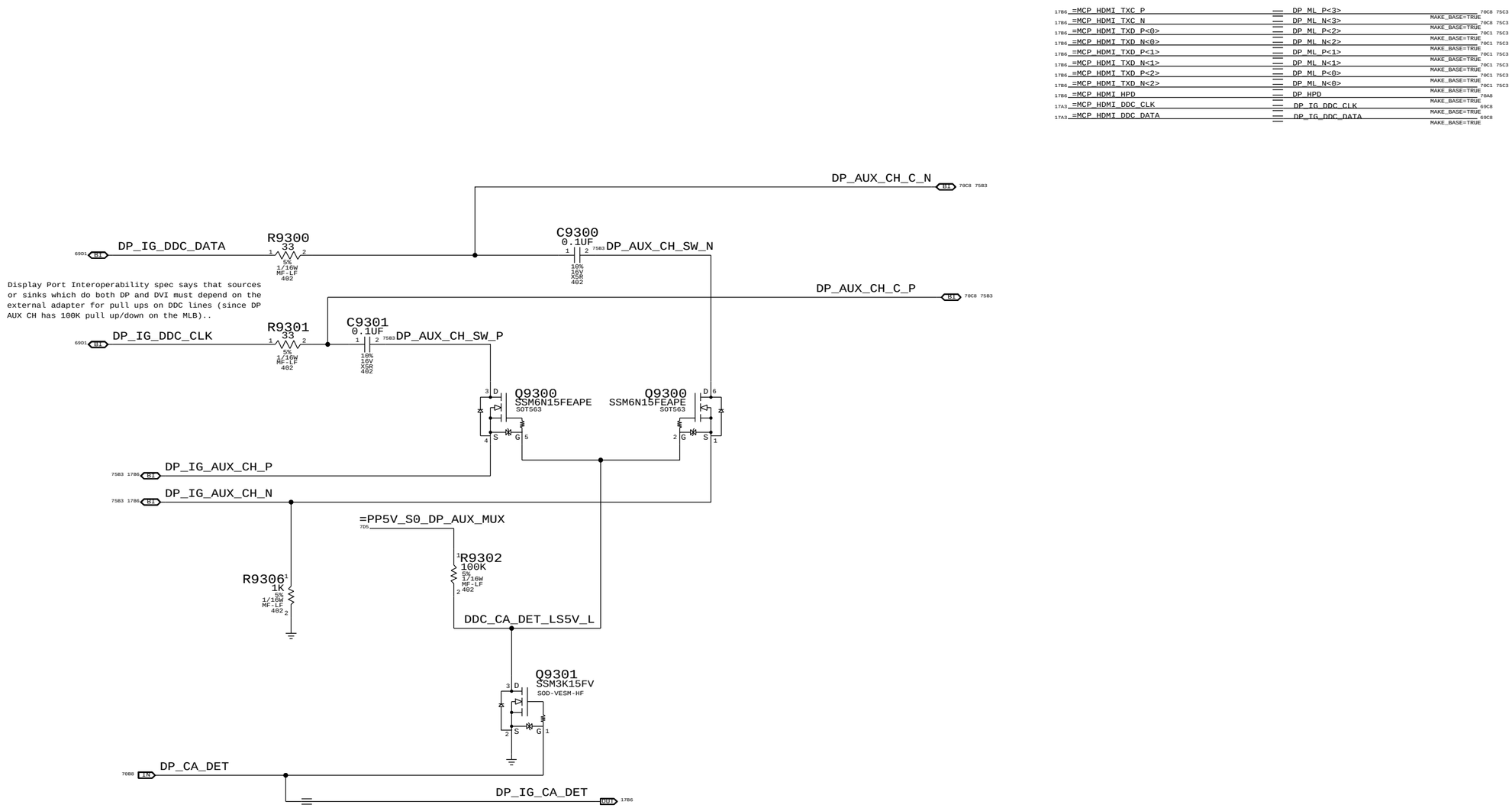

SYNC_MASTER=AMASON SYNC_DATE=04/18/2008

PAGE TITLE
DISPLAYPORT SUPPORT

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D

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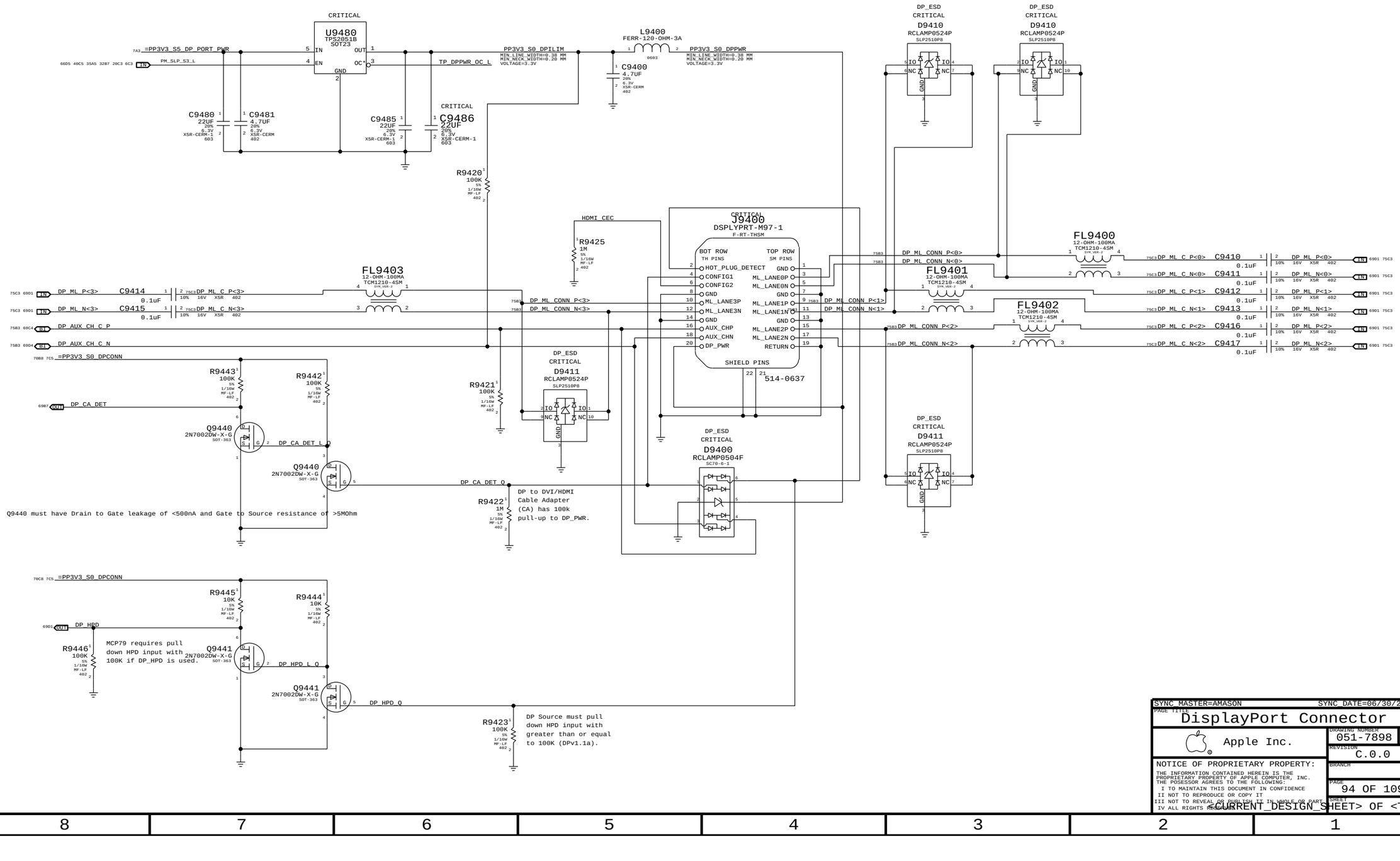
Port Power Switch



SYNC_MASTER=AMASON SYNC_DATE=06/30/2008

PAGE TITLE

DisplayPort Connector

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*L9701, D9701, C9796, C9797, C9799, C9712 AND C9713 SHOULD ALL BE PLACED NEAR EACHOTHER.
*PPVOUT_S0_LCDBKLT_SW SHOULD BE KEPT AS SHORT AS POSSIBLE.
* LVDS_IG_BKL_PWM SHOULD BE AWAY FROM BOOST CIRCUIT

BKLT_VLDO_EN_L
NO STUFF
Q9701
NTUD3127CXXG
SOT-963
N-CHANNEL
P-CHANNEL
NO STUFF R9701 0 5% 1/16W MF-LF 402
BKLT_EN_R
BKLT_EN 71B6
NO STUFF R9735 100K 1% 1/16W MF-LF 402
=PP5V_S0_BKL 7D5
MIN_LINE_WIDTH=0.4 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=5V
NO STUFF R9702 0 5% 1/16W MF-LF 402
BKLT_PROD R9700 0 5% 1/16W MF-LF 402
72C3 71B7 PPBUS_S0_LCDBKLT_PWR
CRITICAL C9712 10UF 10% 25V X5R 805
C9713 0.1UF 10% 25V X5R 402
BKL_SWGND 71B5 71C2
CRITICAL L9701 22UH-2.5A IHLP2525CZ-SM
PPVIN_BKL
MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.375 MM VOLTAGE=6V
PPBUS_S0_LCDBKLT_PWR_SW
MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.375 MM VOLTAGE=5V SWITCH_NODE=TRUE
R9703 0 5% 1/16W MF-LF 402
PPVIN_BKL_R
CRITICAL D9701 SOD-123 RB160M-40
PPVOUT_S0_LCDBKLT 6C3 6C7 68B2
MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.375 MM VOLTAGE=50V
C9796 200PF 5% 100V CERM 1206
C9799 2.2UF 10% 100V X7R 1210
C9797 2.2UF 10% 100V X7R 1210
BKL_SWGND 71B5 71C5
BKL_VLDO
785 =PP3V3_S0_BKL_VDDIO
R9716 100K 5% 1/16W MF-LF 402
C9714 0.01UF 10% 16V CERM 402
C9710 1UF 10% 25V X5R 603-1
C9711 0.1UF 10% 16V X5R 402
NO STUFF R9714 100K 5% 1/16W MF-LF 402
U9701 LLP LP8543SQX
VDDIO VLDO VIN
CRITICAL
NC
ALSO
ALSI
ADR
IF_SEL
SCLK
SDA
PWM
FAULT
EN
SW
FB
OUT1 OUT2 OUT3 OUT4 OUT5 OUT6 OUT7
BKL_ISEN1 BKL_ISEN2 BKL_ISEN3 BKL_ISEN4 BKL_ISEN5 BKL_ISEN6
NC
GND_SW GND_S GND_L THRM PAD
IF_SEL=1 FOR SMBUS
IF_SEL=0 FOR I2C
BKL_IF_SEL
OMIT
43B6 =I2C_BKL_1_SCL R9753 0 5% 1/16W MF-LF 402
BKL_SCL
43B6 =I2C_BKL_1_SDA R9757 0 5% 1/16W MF-LF 402
BKL_SDA
LVDS_IG_BKL_PWM_RC
TP_BKL_FAULT
71D3 BKLT_EN
72C3 71C7 PPBUS_S0_LCDBKLT_PWR
R9731 301K 1% 1/16W MF-LF 402
C9723 0.1UF 10% 25V X5R 402 NO STUFF
R9715 100K 1% 1/16W MF-LF 402
BKL_SWGND HIGH CURRENT
NEED 2 VIAS
XW9700 SM
71C5 71C7 BKL_SWGND
PLACEMENT_NOTE=SW9700 PLACE NEAR C9712 C9713
72B7 17B6 IN LVDS_IG_BKL_PWM
R9704 0 5% 1/16W MF-LF 402
NO STUFF C9704 33PF 5% 50V CERM 402
R9704 SHOULD BE 47K IF RC FILTER IS USED
XW9710 SM
BKL_SGND
MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.20 mm
R9717 0 5% 1/16W MF-LF 402 BKLT_PROD
LED_RETURN_1 OUT 6C7 68B3
R9718 0 5% 1/16W MF-LF 402 BKLT_PROD
LED_RETURN_2 OUT 6C7 68B3
R9719 0 5% 1/16W MF-LF 402 BKLT_PROD
LED_RETURN_3 OUT 6C7 68B3
R9720 0 5% 1/16W MF-LF 402 BKLT_PROD
LED_RETURN_4 OUT 6B7 68B3
R9721 0 5% 1/16W MF-LF 402 BKLT_PROD
LED_RETURN_5 OUT 6B7 68B3
R9722 0 5% 1/16W MF-LF 402 BKLT_PROD
LED_RETURN_6 OUT 6B7 68B3

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
103S0198	6	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SM	R9717,R9718,R9719,R9720,R9721,R9722		BKLT_ENG
116S0005	1	RES,1/16W,0.1 OHM,1%,0402,SM	R9700		BKLT_ENG

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S2670	1	IC,LP8543,WHT LED BKLT CTRLR,QFN24,PROD	U9701	CRITICAL	

SYNC_MASTER=KIRAN SYNC_DATE=12/05/2008
PAGE TITLE
LCD BACKLIGHT DRIVER

Apple Inc.

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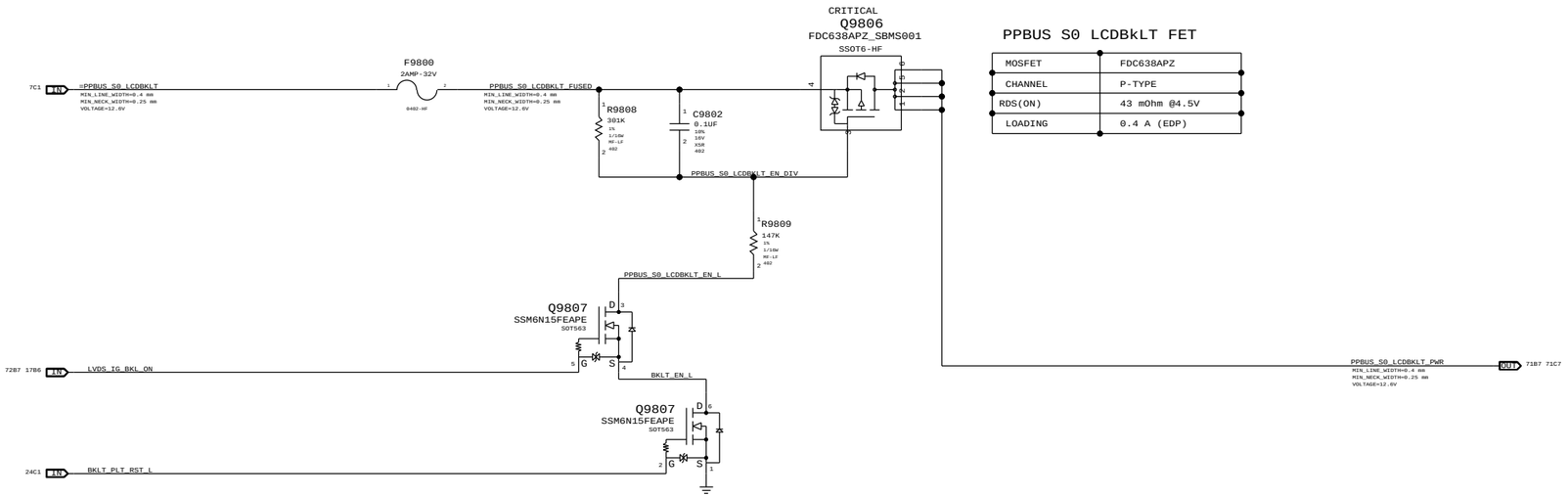

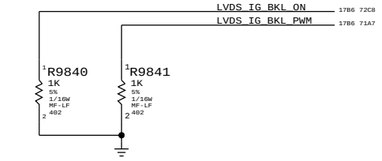

MCP HAS INTERNAL 10K PULL-UP FOR THESE SIGNALS

SYNC_MASTER=YITE SYNC_DATE=06/30/2008

PAGE TITLE

LCD Backlight Support

Apple Inc.

DRAWING NUMBER 051-7898 SIZE D

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FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=2x_DIELECTRIC	?
FSB_DSTB	*	=3x_DIELECTRIC	?
FSB_ADDR	*	=STANDARD	?
FSB_ADSTB	*	=2x_DIELECTRIC	?
FSB_1X	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_DSTB	TOP,BOTTOM	=5x_DIELECTRIC	?
FSB_ADDR	TOP,BOTTOM	=3x_DIELECTRIC	?
FSB_ADSTB	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_1X	TOP,BOTTOM	=3x_DIELECTRIC	?

All 4x/2x/1x FSB signals with impedance requirements are 50-ohm single-ended.

FSB 4X signals / groups shown in signal table on right.
Signals within each 4x group should be matched within 5 ps of strobe.
DSTB# complementary pairs should be matched within 1 ps of each other, all DSTB#s matched to +/- 300 ps.
Spacing is 2x dielectric between DATA#, DINV# signals, with 3x dielectric spacing to the DSTB#s.
DSTB# complementary pairs are spaced normally and are NOT routed as differential pairs.

FSB 2X signals / groups shown in signal table on right.
Signals within each 2x group should be matched within 20 ps. ADTSB#s should be matched +/- 300 ps.
Spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to ADSTB#.

FSB 1X signals shown in signal table on right.
Signals within each 1x group should be matched to CPU clock, +0/-1000 mils.

Design Guide recommends each strobe/signal group is routed on the same layer.
Intel Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Intel Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
SOURCE: Santa Rosa Platform DG, Rev 1.5 (#22294), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	25 MIL	?
CPU_GTLREF	*	25 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?

SR DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

MCP FSB COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_FSB_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.4

FSB Clock Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.5

CPU / FSB Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FSB 4X Signal Groups	FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB_D_L<15..0>	9C4 13D3
	FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB_DINV_L<0>	9C4 13D6
	FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<0>	9C4 13D6
	FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<0>	9C4 13D6
	FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB_D_L<31..16>	9B4 9C4 13C3 13D3
	FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB_DINV_L<1>	9B4 13D6
	FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<1>	9B4 13D6
	FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<1>	9B4 13D6
	FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB_D_L<47..32>	9C2 13B3 13C3
	FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB_DINV_L<2>	9C2 13D6
	FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<2>	9C2 13D6
	FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<2>	9C2 13D6
	FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB_D_L<63..48>	9B2 9C2 13B3
	FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB_DINV_L<3>	9B2 13D6
	FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<3>	9B2 13D6
	FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<3>	9B2 13D6
FSB 2X Signals	FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB_A_L<16..3>	9D8 13C6 13D6
	FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB_REQ_L<4..0>	9D8 13B6
	FSB_ADSTB0	FSB_50S	FSB_ADSTB	FSB_ADSTB_L<0>	9D8 13B6
	FSB_ADDR_GROUP1	FSB_50S	FSB_ADDR	FSB_A_L<35..17>	9C8 9D8 13C6
	FSB_ADSTB1	FSB_50S	FSB_ADSTB	FSB_ADSTB_L<1>	9C8 13B6
FSB 1X Signals	FSB_1X	FSB_50S	FSB_1X	FSB_ADS_L	9D6 13B6
	FSB_RREQ0_L	FSB_50S	FSB_1X	FSB_BREQ0_L	9D6 13B6
	FSB_RREQ1_L	FSB_50S	FSB_1X	FSB_BREQ1_L	13B6
	FSB_1X	FSB_50S	FSB_1X	FSB_BNR_L	9D6 13B6
	FSB_1X	FSB_50S	FSB_1X	FSB_BPRI_L	9D6 13B3
	FSB_1X	FSB_50S	FSB_1X	FSB_DBSY_L	9D6 13B6
	FSB_1X	FSB_50S	FSB_1X	FSB_DEFER_L	9D6 13B3
	FSB_1X	FSB_50S	FSB_1X	FSB_DRDY_L	9D6 13B6
	FSB_1X	FSB_50S	FSB_1X	FSB_HIT_L	9D6 13B6
	FSB_1X	FSB_50S	FSB_1X	FSB_HITM_L	9D6 13B6
	FSB_1X	FSB_50S	FSB_1X	FSB_LOCK_L	9D6 13B6
	FSB_CPURST_L	FSB_50S	FSB_1X	FSB_CPURST_L	9D6 12C2 13A3
	FSB_1X	FSB_50S	FSB_1X	FSB_RS_L<2..0>	9D6 13A6
	FSB_1X	FSB_50S	FSB_1X	FSB_TRDY_L	9D6 13B6
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_A20M_L	9C8 13A3
	CPU_BSEL	CPU_50S	CPU_AGTL	CPU_BSEL<2..0>	8B2 9B4
	CPU_FERR_L	CPU_50S	CPU_8MIL	CPU_FERR_L	9C8 13B7
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_IGNNE_L	9C8 13A3
	CPU_INIT_L	CPU_50S	CPU_AGTL	CPU_INIT_L	9D6 13A3
	CPU_ASYNC_P	CPU_50S	CPU_AGTL	CPU_INTR	9C8 13A3
	CPU_ASYNC_P	CPU_50S	CPU_AGTL	CPU_NMI	9B8 13A3
	CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU_PROCHOT_L	9C5 13B6 41D4 62C8
	CPU_PWRGD	CPU_50S	CPU_AGTL	CPU_PWRGD	9B2 12C7 13A3
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_SMI_L	9B8 13A3
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_STPCLK_L	9C8 13A3
	PM_THRMTRIP_L	CPU_50S	CPU_8MIL	PM_THRMTRIP_L	9C6 13B7 41C4
	FSB_CPUSLP_L	CPU_50S	CPU_AGTL	FSB_CPUSLP_L	9B2 13A3
	CPU_EROM_SB	CPU_50S	CPU_AGTL	CPU_DPSLP_L	9B2 13A3
	CPU_DPRSTP_L	CPU_50S	CPU_AGTL	CPU_DPRSTP_L	9B2 13A3 62C7
	CPU_ASYNC	CPU_50S	CPU_AGTL	FSB_DPWR_L	9B2 13A3
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_BCLK_VML_COMP_VDD	13A6
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_BCLK_VML_COMP_GND	13A6
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_CPU_COMP_VCC	13A6
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_CPU_COMP_GND	13A6
	FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_P	9B6 13B3
	FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_N	9B6 13B3
	FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB_CLK_ITP_P	12C3 13B3
	FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB_CLK_ITP_N	12C3 13B3
	FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB_CLK_MCP_P	13A4
	FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB_CLK_MCP_N	13A4
	CPU_IERR_L	CPU_50S		CPU_IERR_L	9D6
	PM_DPRSLPVR	CPU_50S	CPU_AGTL	PM_DPRSLPVR	20C7 62D8
	(See above)	CPU_50S	CPU_AGTL	IMVP_DPRSLPVR	62C7
	CPU_GTLREF	CPU_50S	CPU_GTLREF	CPU_GTLREF	9B4 25B1
	CPU_COMP	CPU_50S	CPU_COMP	CPU_COMP<3>	9B3
	CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<2>	9B3
	CPU_COMP	CPU_50S	CPU_COMP	CPU_COMP<1>	9B3
	CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<0>	9B3
	XDP_TDI	CPU_50S	CPU_ITP	XDP_TDI	9B6 9C6 12B3
	XDP_TDO	CPU_50S	CPU_ITP	XDP_TDO	9B6 9C6 12B3
	XDP_TMS	CPU_50S	CPU_ITP	XDP_TMS	9B6 9C6 12B3
	XDP_TCK	CPU_50S	CPU_ITP	XDP_TCK	9A6 9C6 12B6
	XDP_TRST_L	CPU_50S	CPU_ITP	XDP_TRST_L	9A6 9C6 12B3
	XDP_BPM_L	CPU_50S	CPU_ITP	XDP_BPM_L<4..0>	9C6 12C6
	XDP_BPM_L5	CPU_50S	CPU_ITP	XDP_BPM_L<5>	9C5 12C6
	(FSB_CPURST_L)	CPU_50S	CPU_ITP	XDP_CPURST_L	12C4
		CPU_50S	CPU_8MIL	CPU_VID<6..0>	10B6 62C7
		CPU_50S	CPU_8MIL	IMVP6_VID<6..0>	
	CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	10B5 62A5
	CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	10A5 62A5
	(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_P	
	(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_N	

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PAGE TITLE
CPU/FSB Constraints

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_40S_VDD	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_70D_VDD	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MIL	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

Need to support MEM_*-style wildcards!

DDR2:
DQ signals should be matched within 20 ps of associated DQS pair.
DQS intra-pair matching should be within 1 ps, no inter-pair matching requirement.
All DQS pairs should be matched within 100 ps of clocks.
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 140 ps.
A/BA/cmd signals should be matched within 75 ps, no CLK matching requirement.
All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).
DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

DDR3:
DQ signals should be matched within 5 ps of associated DQS pair.
DQS intra-pair matching should be within 1 ps, inter-pair matching shoulw be within 180 ps
No DQS to clock matching requirement.
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 2 ps.
A/BA/cmd signals should be matched within 5 ps of CLK pairs.
All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).
DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3
SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

MCP MEM COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MEM_COMP	*	Y	7 MIL	7 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_MEM_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3.4

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MEM_A_CLK	MEM_70D_VDD	MEM_CLK	MEM_A_CLK_P<5..0>	14B5 26C5 26C7
MEM_A_CLK	MEM_70D_VDD	MEM_CLK	MEM_A_CLK_N<5..0>	14B5 26C5 26C7
MEM_A_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_A_CKE<3..0>	14A5 26D5 26D7
MEM_A_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_A_CS_L<3..0>	14B5 26C5 26C7
MEM_A_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_A_ODT<3..0>	14B5 26C5
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_A<14..0>	14B5 14C5 26C5 26C7
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_BA<2..0>	14C5 26C5 26C7
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_RAS_L	14C5 26C5
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_CAS_L	14C5 26C7
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_WE_L	14C5 26C7
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_A_DQ<7..0>	14B7 26C2 26C4 26D2 26D4
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_A_DQ<15..8>	14B7 26C2 26C4
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_A_DQ<23..16>	14B7 14C7 26B2 26B4 26C2 26C4
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_A_DQ<31..24>	14C7 26C2 26C4
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_A_DQ<39..32>	14C7 26B5 26B7 26C5 26C7
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_A_DQ<47..40>	14C7 14D7 26B5 26B7
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_A_DQ<55..48>	14D7 26B5 26B7
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_A_DQ<63..56>	14D7 26A5 26A7 26B5 26B7
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_A_DM<0>	14A7 26C4
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_A_DM<1>	14A7 26C2
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_A_DM<2>	14B7 26B4
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_A_DM<3>	14B7 26C2
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_A_DM<4>	14B7 26B5
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_A_DM<5>	14B7 26B7
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_A_DM<6>	14B7 26B5
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_A_DM<7>	14B7 26A7
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM_A_DQS_P<0>	14D5 26C2
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM_A_DQS_N<0>	14D5 26D2
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM_A_DQS_P<1>	14D5 26C4
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM_A_DQS_N<1>	14D5 26C4
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM_A_DQS_P<2>	14D5 26B2
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM_A_DQS_N<2>	14D5 26C2
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM_A_DQS_P<3>	14D5 26C4
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM_A_DQS_N<3>	14D5 26C4
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM_A_DQS_P<4>	14D5 26B7
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM_A_DQS_N<4>	14D5 26B7
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM_A_DQS_P<5>	14D5 26B5
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM_A_DQS_N<5>	14D5 26B5
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM_A_DQS_P<6>	14D5 26B7
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM_A_DQS_N<6>	14D5 26B7
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM_A_DQS_P<7>	14D5 26A5
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM_A_DQS_N<7>	14D5 26A5
MEM_B_CLK	MEM_70D_VDD	MEM_CLK	MEM_B_CLK_P<5..0>	14B1 27C5 27C7
MEM_B_CLK	MEM_70D_VDD	MEM_CLK	MEM_B_CLK_N<5..0>	14B1 27C5 27C7
MEM_B_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_B_CKE<3..0>	14A1 27D5 27D7
MEM_B_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_B_CS_L<3..0>	14B1 27C5 27C7
MEM_B_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_B_ODT<3..0>	14B1 27C5
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_A<14..0>	14B1 14C1 27C5 27C7
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_BA<2..0>	14C1 27C5 27C7
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_RAS_L	14C1 27C5
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_CAS_L	14C1 27C7
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_WE_L	14C1 27C7
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_B_DQ<7..0>	14B3 27C2 27C4 27D2 27D4
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_B_DQ<15..8>	14B3 27C2 27C4
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_B_DQ<23..16>	14B3 14C3 27C2 27C4
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_B_DQ<31..24>	14C3 27B2 27B4 27C2 27C4
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_B_DQ<39..32>	14C3 27B5 27B7 27C5 27C7
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_B_DQ<47..40>	14C3 14D3 27B5 27B7
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_B_DQ<55..48>	14D3 27B5 27B7
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_B_DQ<63..56>	14D3 27A5 27A7 27B5 27B7
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_B_DM<0>	14A3 27C4
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_B_DM<1>	14A3 27C2
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_B_DM<2>	14B3 27C2
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_B_DM<3>	14B3 27B4
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_B_DM<4>	14B3 27B5
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_B_DM<5>	14B3 27B7
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_B_DM<6>	14B3 27B5
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_B_DM<7>	14B3 27A7
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM_B_DQS_P<0>	14D1 27C2
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM_B_DQS_N<0>	14D1 27D2
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM_B_DQS_P<1>	14D1 27C4
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM_B_DQS_N<1>	14D1 27C4
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM_B_DQS_P<2>	14D1 27C4
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM_B_DQS_N<2>	14D1 27C4
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM_B_DQS_P<3>	14D1 27B2
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM_B_DQS_N<3>	14D1 27C2
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM_B_DQS_P<4>	14D1 27B7
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM_B_DQS_N<4>	14D1 27B7
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM_B_DQS_P<5>	14D1 27B5
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM_B_DQS_N<5>	14D1 27B5
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM_B_DQS_P<6>	14D1 27B7
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM_B_DQS_N<6>	14D1 27B7
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM_B_DQS_P<7>	14D1 27A5
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM_B_DQS_N<7>	14D1 27A5
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP_VDD	15C6
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP_GND	15C6

SYNC_MASTER=T18_MLB SYNC_DATE=01/04/2008
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PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?
MCP_PEX_COMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.4

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
MCP_DV_COMP	*	Y	20 MIL	20 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DIsplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
SATA_90D_HDD	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=4x_DIELECTRIC	?
SATA_TERMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=3x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.7.1.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	PCIE_90D	PCIE	PCIE_MINI_R2D_P	6D5 29C7
	PCIE_90D	PCIE	PCIE_MINI_R2D_N	6D5 29C7
PCIE_MINI_R2D	PCIE_90D	PCIE	PCIE_MINI_R2D_C_P	16B3 29C5
	PCIE_90D	PCIE	PCIE_MINI_R2D_C_N	16B3 29C5
PCIE_MINI_D2R	PCIE_90D	PCIE	PCIE_MINI_D2R_P	6D5 16B6 29C7
	PCIE_90D	PCIE	PCIE_MINI_D2R_N	6D5 16B6 29C7
	PCIE_90D	PCIE	PCIE_FW_R2D_P	34C3
	PCIE_90D	PCIE	PCIE_FW_R2D_N	34C3
PCIE_FW_R2D	PCIE_90D	PCIE	PCIE_FW_R2D_C_P	16B3 34C1
	PCIE_90D	PCIE	PCIE_FW_R2D_C_N	16B3 34C1
PCIE_FW_D2R	PCIE_90D	PCIE	PCIE_FW_D2R_P	16B6 34C1
	PCIE_90D	PCIE	PCIE_FW_D2R_N	16B6 34C1
	PCIE_90D	PCIE	PCIE_FW_D2R_C_P	34C3
	PCIE_90D	PCIE	PCIE_FW_D2R_C_N	34C3
MCP_PE1_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_P	16C3 29C5
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_N	16C3 29C5
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_CONN_P	6D5 29C7
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_CONN_N	6D5 29C7
MCP_PE4_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FC_P	
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FC_N	
MCP_PEX_CLK_COMP		MCP_PEX_COMP	MCP_PEX_CLK_COMP	16A6
TMDS_IG_TXC	DP_100D	DISPLAYPORT	TMDS_IG_TXC_P	
TMDS_IG_TXC	DP_100D	DISPLAYPORT	TMDS_IG_TXC_N	
TMDS_IG_TXD	DP_100D	DISPLAYPORT	TMDS_IG_TXD_P<2..0>	
TMDS_IG_TXD	DP_100D	DISPLAYPORT	TMDS_IG_TXD_N<2..0>	
DP_ML	DP_100D	DISPLAYPORT	DP_ML_P<3..0>	69D1 70C1 70C8
	DP_100D	DISPLAYPORT	DP_ML_C_P<3..0>	70C2 70C7
DP_ML	DP_100D	DISPLAYPORT	DP_ML_N<3..0>	69D1 70C1 70C8
	DP_100D	DISPLAYPORT	DP_ML_C_N<3..0>	70C2 70C7
DP_AUX_CH	DP_100D	DISPLAYPORT	DP_IG_AUX_CH_P	17B6 69C7
	DP_100D	DISPLAYPORT	DP_IG_AUX_CH_N	17B6 69C7
	DP_100D	DISPLAYPORT	DP_AUX_CH_SW_P	69C6
	DP_100D	DISPLAYPORT	DP_AUX_CH_SW_N	69C5
	DP_100D	DISPLAYPORT	DP_AUX_CH_C_P	69C4 70C8
	DP_100D	DISPLAYPORT	DP_AUX_CH_C_N	69D4 70C8
MCP_HDMI_RSET	MCP_DV_COMP		MCP_HDMI_RSET	17A6 23C7
MCP_HDMI_VPROBE	MCP_DV_COMP		MCP_HDMI_VPROBE	17A6 23C7
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS_IG_A_CLK_P	17B3 68B3
	LVDS_100D	LVDS	LVDS_IG_A_CLK_F_P	6C7 68C2
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS_IG_A_CLK_N	17B3 68B3
	LVDS_100D	LVDS	LVDS_IG_A_CLK_F_N	6C7 68C2
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS_IG_A_DATA_P<2..0>	6C7 17B3 68C2
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS_IG_A_DATA_N<2..0>	6C7 17B3 68C2
16:8 DP_ML	DP_100D	DISPLAYPORT	DP_ML_CONN_P<3..0>	70C3 70C4 70C5
16:8	DP_100D	DISPLAYPORT	DP_ML_CONN_N<3..0>	70C3 70C4 70C5
MCP_IFPAB_RSET	MCP_DV_COMP		MCP_IFPAB_RSET	17A3 23C6
MCP_IFPAB_VPROBE			MCP_IFPAB_VPROBE	17A3 23C6
SATA_HDD_R2D	SATA_90D_HDD	SATA	SATA_HDD_R2D_C_P	19D6 37A2
	SATA_90D_HDD	SATA	SATA_HDD_R2D_C_N	19D6 37A2
	SATA_90D_HDD	SATA	SATA_HDD_R2D_P	6B7 37A5
	SATA_90D_HDD	SATA	SATA_HDD_R2D_N	6B7 37A5
	SATA_90D_HDD	SATA	SATA_HDD_R2D_UF_P	37A4
	SATA_90D_HDD	SATA	SATA_HDD_R2D_UF_N	37A4
SATA_HDD_D2R	SATA_90D_HDD	SATA	SATA_HDD_D2R_P	19D6 37B2
	SATA_90D_HDD	SATA	SATA_HDD_D2R_N	19D6 37B2
	SATA_90D_HDD	SATA	SATA_HDD_D2R_C_P	6B7 37B5
	SATA_90D_HDD	SATA	SATA_HDD_D2R_C_N	6B7 37B5
	SATA_90D_HDD	SATA	SATA_HDD_D2R_UF_P	37B4
	SATA_90D_HDD	SATA	SATA_HDD_D2R_UF_N	37B4
SATA_ODD_R2D	SATA_100D	SATA	SATA_ODD_R2D_C_P	19D6 37C3
	SATA_100D	SATA	SATA_ODD_R2D_C_N	19D6 37C3
	SATA_100D	SATA	SATA_ODD_R2D_P	6B7 37C6
	SATA_100D	SATA	SATA_ODD_R2D_N	6A7 6B7 37C6
	SATA_100D	SATA	SATA_ODD_R2D_UF_P	37C4
	SATA_100D	SATA	SATA_ODD_R2D_UF_N	37C4
SATA_ODD_D2R	SATA_100D	SATA	SATA_ODD_D2R_P	19D6 37C3
	SATA_100D	SATA	SATA_ODD_D2R_N	19D6 37C3
	SATA_100D	SATA	SATA_ODD_D2R_C_P	6B7 37C6
	SATA_100D	SATA	SATA_ODD_D2R_C_N	6B7 37C6
	SATA_100D	SATA	SATA_ODD_D2R_UF_P	37C4
	SATA_100D	SATA	SATA_ODD_D2R_UF_N	37C4
MCP_SATA_TERMP		SATA_TERMP	MCP_SATA_TERMP	19A6

SYNC_MASTER=T18_MLB SYNC_DATE=01/04/2008

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PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_5SS	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCI_5SS	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=STANDARD	?
CLK_PCI	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.8.

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_5SS	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_5SS	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.9.1.

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_USB_RBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.10.1.

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_5SS	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.11.1.

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_5SS	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?
MCP_HDA_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.12.1.

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_5SS	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.13.

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_5SS	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.14.

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
MCP_DEBUG	PCI_5SS	PCI	MCP_DEBUG<7..0> 12C3 18D7
PCI_AD	PCI_5SS	PCI	PCI_AD<23..8>
PCI_AD24	PCI_5SS	PCI	PCI_AD<24>
PCI_AD	PCI_5SS	PCI	PCI_AD<31..25>
PCI_AD	PCI_5SS	PCI	PCI_PAR
PCI_C_BE_L	PCI_5SS	PCI	PCI_C_BE_L<3..0>
PCI_CNTL	PCI_5SS	PCI	PCI_IRDY_L
PCI_CNTL	PCI_5SS	PCI	PCI_DEVSEL_L
PCI_CNTL	PCI_5SS	PCI	PCI_PERR_L
PCI_CNTL	PCI_5SS	PCI	PCI_SERR_L
PCI_CNTL	PCI_5SS	PCI	PCI_STOP_L
PCI_CNTL	PCI_5SS	PCI	PCI_TRDY_L
PCI_CNTL	PCI_5SS	PCI	PCI_FRAME_L
PCI_REQ0_L	PCI_5SS	PCI	PCI_REQ0_L 18D2 18D7
PCI_GNT0_L	PCI_5SS	PCI	PCI_GNT0_L
PCI_REQ1_L	PCI_5SS	PCI	PCI_REQ1_L 18D2 18D7
PCI_GNT1_L	PCI_5SS	PCI	PCI_GNT1_L
PCI_INTW_L	PCI_5SS	PCI	PCI_INTW_L
PCI_INTX_L	PCI_5SS	PCI	PCI_INTX_L
PCI_INTY_L	PCI_5SS	PCI	PCI_INTY_L
PCI_INTZ_L	PCI_5SS	PCI	PCI_INTZ_L
MCP_PCI_CLK2	CLK_PCI_5SS	CLK_PCI	PCI_CLK33M_MCP_R 18C5
	CLK_PCI_5SS	CLK_PCI	PCI_CLK33M_MCP 18C5
LPC_AD	LPC_5SS	LPC	LPC_AD<3..0> 18B3 40C8 42D3 42D5
LPC_FRAME_L	LPC_5SS	LPC	LPC_FRAME_L 18C3 40C8 42D5
LPC_RESET_L	LPC_5SS	LPC	LPC_RESET_L 18C3 24D4
MCP_LPC_CLK0	CLK_LPC_5SS	CLK_LPC	LPC_CLK33M_SMC_R 18B3 24B4
	CLK_LPC_5SS	CLK_LPC	LPC_CLK33M_SMC 24B1 40C8
	CLK_LPC_5SS	CLK_LPC	LPC_CLK33M_LPCPLUS 24B1 42D3
USB_EXTA	USB_90D	USB	USB_EXTA_P 19D3 38A8
	USB_90D	USB	USB_EXTA_N 19D3 38A8
	USB_90D	USB	USB_EXTA_MUXED_P 38C4
	USB_90D	USB	USB_EXTA_MUXED_N 38C4
	USB_90D	USB	CONN_USB_EXTA_P 38C3
	USB_90D	USB	CONN_USB_EXTA_N 38C3
USB_CAMERA	USB_90D	USB	USB_CAMERA_P 19D3 29B5
	USB_90D	USB	USB_CAMERA_N 19D3 29B5
	USB_90D	USB	USB_CAMERA_CONN_P 6D5 29B7
	USB_90D	USB	USB_CAMERA_CONN_N 6D5 29B7
USB_BT	USB_90D	USB	USB_BT_P 19D3 29B5
	USB_90D	USB	USB_BT_N 19C3 29B5
	USB_90D	USB	CONN_USB2_BT_P 6D5 29B7
	USB_90D	USB	CONN_USB2_BT_N 6D5 29B7
USB_TPAD	USB_90D	USB	USB_TPAD_P 19D3 48B8
	USB_90D	USB	USB_TPAD_N 19D3 48B8
	USB_90D	USB	USB_TPAD_R_P 48B7
	USB_90D	USB	USB_TPAD_R_N 48B7
USB_IR	USB_90D	USB	USB_IR_P 19D3 39D7
	USB_90D	USB	USB_IR_N 19D3 39D7
USB_EXTB	USB_90D	USB	USB_EXTB_P 19C3 38A4
	USB_90D	USB	USB_EXTB_N 19C3 38B4
	USB_90D	USB	CONN_USB_EXTB_P 38B3
	USB_90D	USB	CONN_USB_EXTB_N 38B3
USB_SD	USB_90D	USB	USB_CARDREADER_P 19C3 30C7
	USB_90D	USB	USB_CARDREADER_N 19C3 30C7
MCP_USB_RBIAS	MCP_USB_RBIAS		MCP_USB_RBIAS_GND 19C4
SMBUS_MCP_0_CLK	SMB_5SS	SMB	SMBUS_MCP_0_CLK 12B6 20C3 43D8
SMBUS_MCP_0_DATA	SMB_5SS	SMB	SMBUS_MCP_0_DATA 12B6 20C3 43D8
SMBUS_MCP_1_CLK	SMB_5SS	SMB	SMBUS_MCP_1_CLK 20C3 43B8
SMBUS_MCP_1_DATA	SMB_5SS	SMB	SMBUS_MCP_1_DATA 20C3 43B8
HDA_BIT_CLK	HDA_5SS	HDA	HDA_BIT_CLK 20D2 52C7
	HDA_5SS	HDA	HDA_BIT_CLK_R 20A7 20D4
HDA_SYNC	HDA_5SS	HDA	HDA_SYNC 20D2 52C7
	HDA_5SS	HDA	HDA_SYNC_R 20A7 20D4
HDA_RST_L	HDA_5SS	HDA	HDA_RST_R_L 20A7 20D4
	HDA_5SS	HDA	HDA_RST_L 20D2 52C7
HDA_SDIN0	HDA_5SS	HDA	HDA_SDIN0 20D7 52C7
	HDA_5SS	HDA	HDA_SDIN_CODEC
HDA_SDOUT	HDA_5SS	HDA	HDA_SDOUT 20D2 52C7
	HDA_5SS	HDA	HDA_SDOUT_R 20A7 20D4
MCP_HDA_PULLDN_COMP		MCP_HDA_COMP	MCP_HDA_PULLDN_COMP 20C7
MCP_SUS_CLK	CLK_SLOW_5SS	CLK_SLOW	PM_CLK32K_SUSCLK_R 20B3 24B4
	CLK_SLOW_5SS	CLK_SLOW	PM_CLK32K_SUSCLK 24B1 40C5
SPI_CLK	SPI_5SS	SPI	SPI_CLK_R 20B3 42A5 42C8
	SPI_5SS	SPI	SPI_CLK 51C5
	SPI_5SS	SPI	SPI_ALT_CLK 42C5 42D3
SPI_MOSI	SPI_5SS	SPI	SPI_MOSI_R 20B3 42A5 42C7
	SPI_5SS	SPI	SPI_MOSI 51C4
	SPI_5SS	SPI	SPI_ALT_MOSI 42C5 42D5
SPI_MISO	SPI_5SS	SPI	SPI_MISO 20B3 42A5 42B7
	SPI_5SS	SPI	SPI_MISO_R 51C4
	SPI_5SS	SPI	SPI_ALT_MISO 42B5 42D5
SPI_CS0	SPI_5SS	SPI	SPI_CS0_R_L 20B3 42B7
	SPI_5SS	SPI	SPI_CS0_L
	SPI_5SS	SPI	SPI_CS1_R_L
	SPI_5SS	SPI	SPI_CS1_R_L_USE_MLB

SYNC_MASTER=T18_MLB SYNC_DATE=12/14/2007

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DRAWING NUMBER: 051-7898 SIZE: D

REVISION: C.0.0

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MCP RGMII (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MII_COMP	*	=STANDARD	7.5 MIL	7.5 MIL	=STANDARD	=STANDARD	=STANDARD
ENET_MII_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_BUF0_CLK	*	=3:1_SPACING	?
ENET_MII	*	12 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Sections 2.7.2 & 2.7.4

88E1116R (Ethernet PHY) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_MDI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	25 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Section 2.7.4

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MCP_MII_COMP	MCP_MII_COMP		MCP_MII_COMP_VDD	17C6
MCP_MII_COMP	MCP_MII_COMP		MCP_MII_COMP_GND	17C6
MCP_CLK25M_BUF0	ENET_MII_55S	MCP_BUF0_CLK	MCP_CLK25M_BUF0_R	17C3 32A5
	ENET_MII_55S	MCP_BUF0_CLK	RTL8211_CLK25M_CKXTAL1	31B6 32A3
ENET_INTR_L	ENET_MII_55S	ENET_MII	ENET_INTR_L	
ENET_MDIO	ENET_MII_55S	ENET_MII	ENET_MDIO	17C3 31B6
ENET_MDC	ENET_MII_55S	ENET_MII	ENET_MDC	17D3 31B6
ENET_PWRDWN_L	ENET_MII_55S	ENET_MII	ENET_PWRDWN_L	
	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK_R	31C4
ENET_RXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK	17D6 31C1
	ENET_MII_55S	ENET_MII	ENET_RXD_R<3..0>	31C4
ENET_RXD	ENET_MII_55S	ENET_MII	ENET_RXD<0>	17D6 31C1
ENET_RXD_STRAP	ENET_MII_55S	ENET_MII	ENET_RXD<3..1>	17D6 31C1
ENET_RXD	ENET_MII_55S	ENET_MII	ENET_RX_CTRL	17D6 31B1
	ENET_MII_55S	ENET_MII	ENET_RXCTL_R	31B4
	ENET_MII_55S	ENET_MII	ENET_CLK125M_TXCLK_R	31C6
ENET_TXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_TXCLK	17D3 31C8
ENET_TXD0	ENET_MII_55S	ENET_MII	ENET_TXD<0>	17D3 31C6
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TXD<3..1>	17D3 31C6
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TX_CTRL	17D3 31B6
	ENET_MII_55S	ENET_MII	ENET_RESET_L	17C3 31B7
ENET_MDI	ENET_MDI_100D	ENET_MDI	ENET_MDI_P<3..0>	31B3 33B8 33C8
	ENET_MDI_100D	ENET_MDI	ENET_MDI_N<3..0>	31B3 33B8 33C8
	ENET_MDI_100D	ENET_MDI	ENET_MDI_TRAN_P<3..0>	33B4 33C4 33C5
	ENET_MDI_100D	ENET_MDI	ENET_MDI_TRAN_N<3..0>	33B4 33C4 33C5

SYNC_MASTER=T18_MLB SYNC_DATE=03/19/2008

PAGE TITLE: Ethernet Constraints

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DRAWING NUMBER: 051-7898 SIZE: D

REVISION: C.0.0

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FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

SD CARD INTERFACE CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SD_SSS	*	=SS_OHM_SE	=SS_OHM_SE	=SS_OHM_SE	=SS_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SD_INTERFACE	*	=3X_DIELECTRIC	?

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
FW_P0_TPA	FW_110D	FW_TP	FW_P0_TPA_P	34B6 36C4
FW_P0_TPA	FW_110D	FW_TP	FW_P0_TPA_N	34C6 36C4
FW_P0_TPB	FW_110D	FW_TP	FW_P0_TPB_P	34B6 36C4
FW_P0_TPB	FW_110D	FW_TP	FW_P0_TPB_N	34B6 36C4
FW_P1_TPA	FW_110D	FW_TP	FW_P1_TPA_P	34B6 36BB
FW_P1_TPA	FW_110D	FW_TP	FW_P1_TPA_N	34B6 36BB
FW_P1_TPB	FW_110D	FW_TP	FW_P1_TPB_P	34B6 36BB
FW_P1_TPB	FW_110D	FW_TP	FW_P1_TPB_N	34B6 36BB
Port 2 Not Used				

SD CARD NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
I23 SD_DATA	SD_SSS	SD_INTERFACE	SD_D<0>	30C2
I24 SD_DATA	SD_SSS	SD_INTERFACE	SD_D<1>	30C2
I25 SD_DATA	SD_SSS	SD_INTERFACE	SD_D<2>	30C2
I26 SD_DATA	SD_SSS	SD_INTERFACE	SD_D<3>	30C2
I27 SD_DATA	SD_SSS	SD_INTERFACE	SD_D<4>	30C2
I28 SD_DATA	SD_SSS	SD_INTERFACE	SD_D<5>	30C2
I29 SD_DATA	SD_SSS	SD_INTERFACE	SD_D<6>	30C2
I30 SD_DATA	SD_SSS	SD_INTERFACE	SD_D<7>	30C2
I32 SD_CLK	SD_SSS	SD_INTERFACE	SD_CLK	30C2
I33 SD_CMD	SD_SSS	SD_INTERFACE	SD_CMD	30C2

SYNC_MASTER=K19 MLB SYNC_DATE=12/01/2008

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SMBUS_SMC_A_S3_SCL	SMB_5SS	SMB	SMBUS_SMC_A_S3_SCL	6C5 6D5 43D2
SMBUS_SMC_A_S3_SDA	SMB_5SS	SMB	SMBUS_SMC_A_S3_SDA	6C5 6D5 43D2
SMBUS_SMC_B_S0_SCL	SMB_5SS	SMB	SMBUS_SMC_B_S0_SCL	43C2
SMBUS_SMC_B_S0_SDA	SMB_5SS	SMB	SMBUS_SMC_B_S0_SDA	43C2
SMBUS_SMC_0_S0_SCL	SMB_5SS	SMB	SMBUS_SMC_0_S0_SCL	43D5
SMBUS_SMC_0_S0_SDA	SMB_5SS	SMB	SMBUS_SMC_0_S0_SDA	43D5
SMBUS_SMC_BSA_SCL	SMB_5SS	SMB	SMBUS_SMC_BSA_SCL	6A7 43C5
SMBUS_SMC_BSA_SDA	SMB_5SS	SMB	SMBUS_SMC_BSA_SDA	6A7 43C5
SMBUS_SMC_MGMT_SCL	SMB_5SS	SMB	SMBUS_SMC_MGMT_SCL	43B5
SMBUS_SMC_MGMT_SDA	SMB_5SS	SMB	SMBUS_SMC_MGMT_SDA	43B5

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P
	1TO1_DIFFPAIR		CHGR_CSI_N
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P
	1TO1_DIFFPAIR		CHGR_CSO_N

SYNC_MASTER=T18_MLB SYNC_DATE=01/04/2008

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SMC Constraints

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

K24 SENSOR NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	DIFFPAIR		CHGR_CSO_R_P	45A8 59B3
	DIFFPAIR		CHGR_CSO_R_N	45A8 59B3
	DIFFPAIR		CPUTHMSNS_D2_P	46C5
	DIFFPAIR		CPUTHMSNS_D2_N	46C5
	DIFFPAIR		CPU_THERMD_P	9C6 46D5
	DIFFPAIR		CPU_THERMD_N	9C6 46D5
	DIFFPAIR		ISNS_CPUVTT_P	45B7
	DIFFPAIR		ISNS_CPUVTT_N	45B7
	DIFFPAIR		ISNS_P1V5S0MCP_P	
	DIFFPAIR		ISNS_P1V5S0MCP_N	
	DIFFPAIR		ISNS_PVCORES0MCP_P	
	DIFFPAIR		ISNS_PVCORES0MCP_N	
	DIFFPAIR		MCPTHMSNS_D2_P	6C7 46B5
	DIFFPAIR		MCPTHMSNS_D2_N	6C7 46B5
	DIFFPAIR		MCP_THMDIODE_P	20C3 46B5
	DIFFPAIR		MCP_THMDIODE_N	20C3 46B5

SYNC_MASTER=M97_MLB

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K24 SPECIAL CONSTRAINTS

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K24 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL OR MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA_P1MM	MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	0.100MM	30 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.115 MM	0.115 MM			
50_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.100 MM			
40_OHM_SE	*	Y	0.126 MM	0.100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.310 MM	0.310 MM			
27P4_OHM_SE	*	Y	0.222 MM	0.222 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.151 MM	0.100 MM	=STANDARD	0.224 MM	0.224 MM
70_OHM_DIFF	TOP,BOTTOM	Y	0.185 MM	0.100 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.095 MM	0.095 MM		0.234 MM	0.234 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.112 MM	0.112 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.075 MM	0.075 MM		0.244 MM	0.244 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.091 MM	0.091 MM		0.230 MM	0.230 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.075 MM	0.075 MM		0.330 MM	0.330 MM
110_OHM_DIFF	TOP,BOTTOM	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?
BGA_P3MM	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	TOP,BOTTOM	0.140 MM	?
3X_DIELECTRIC	TOP,BOTTOM	0.210 MM	?
4X_DIELECTRIC	TOP,BOTTOM	0.280 MM	?
5X_DIELECTRIC	TOP,BOTTOM	0.350 MM	?
2X_DIELECTRIC	-	0.126 MM	?
3X_DIELECTRIC	-	0.189 MM	?
4X_DIELECTRIC	-	0.252 MM	?
5X_DIELECTRIC	-	0.315 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA_P1MM	BGA_P1MM
MEM_CLK	*	BGA_P1MM	BGA_P2MM
CLK_FSB	*	BGA_P1MM	BGA_P2MM
CLK_LPC	*	BGA_P1MM	BGA_P2MM
CLK_PCI	*	BGA_P1MM	BGA_P2MM
CLK_PCIE	*	BGA_P1MM	BGA_P2MM
CLK_SLOW	*	BGA_P1MM	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA_P1MM	BGA_P3MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_40S	BGA_P1MM	STANDARD
MEM_40S_VDD	BGA_P1MM	STANDARD

SYNC MASTER=M97 MLB

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K24 RULE DEFINITIONS

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