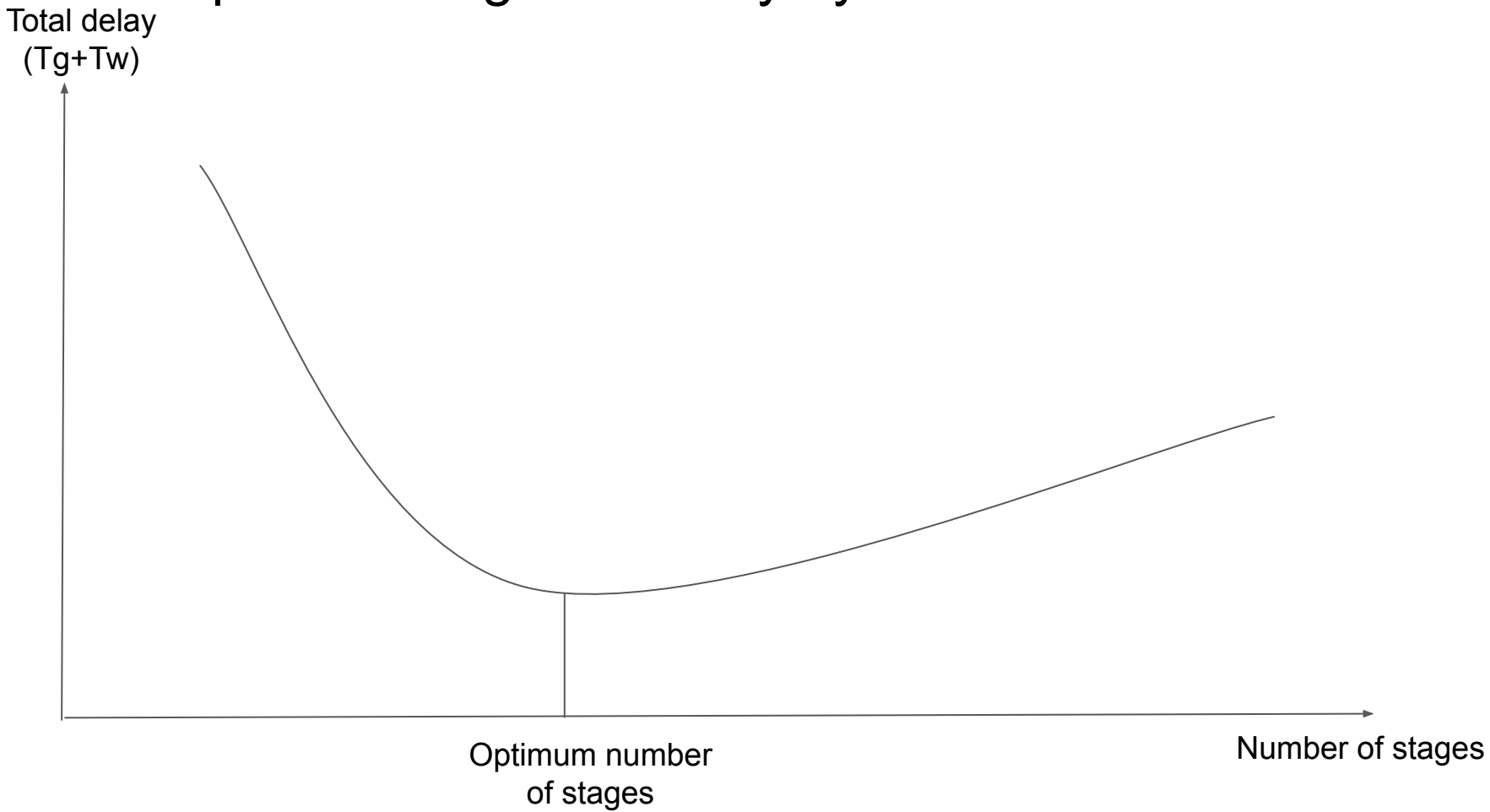
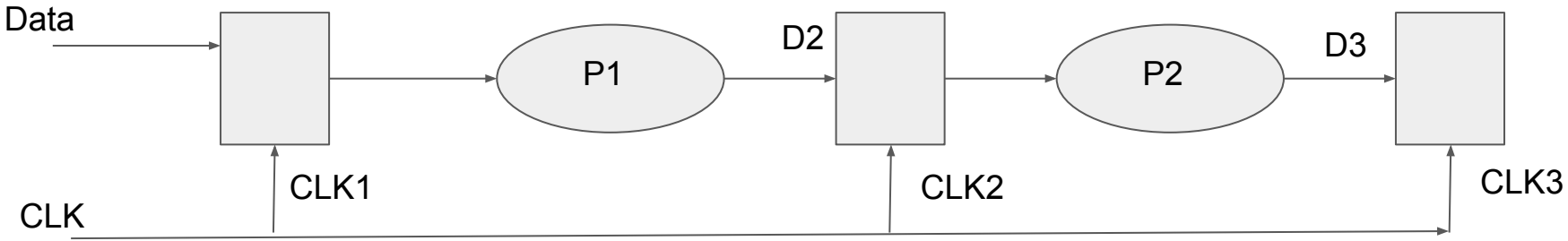
Delay

- Gate delay Tg = f(input slew, output load)
  - The higher input slew, load, the higher gate delay
  - Load is Cequ = equivalent capacitance of the parasitics and cell loads
  - Improve gate delay:
    - Optimize Cin of next stages by using small load cells while preserving timing
    - Matching Cequ and driver's strength -> save power
    - Using low Vt type cells ->
      - High leakage but possible lower short circuit power (internal cell power)
      - Only for critical paths
- Wire Delay:
  - Simple formula: Elmore delay = Tpd = $\sum R(n-i)Ci$
  - Improve wire delay:
    - Reducing R and/or C:
      - For long wires, resistance dominates -> reduce R first by increasing wire width
      - Too long wires -> buffer insertion -> cut total delay to half or even ⅓, ¼.

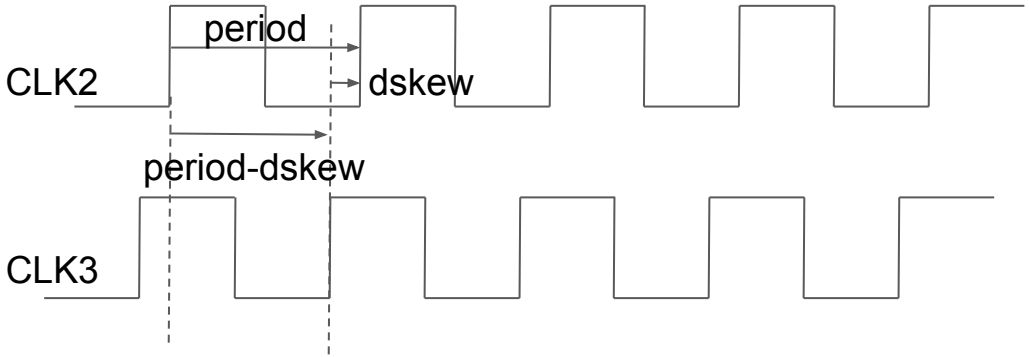
Optimize long wire delay by buffer insertion



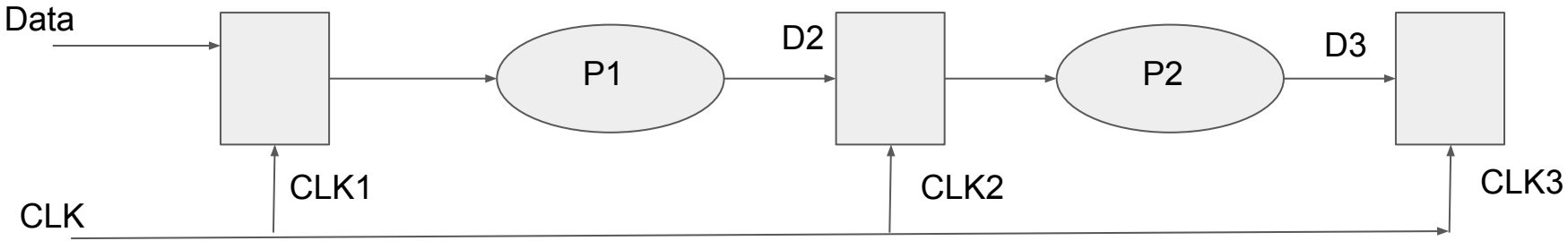
CLOCK SKEW



Td2 = Tclk1 + Tck2q + Tp1
Tclk2 = Tclk + skew2
Tclk3 = Tclk + skew2 - dskew, dskew>0 -> CLK3 is earlier than CLK2
Td3 = Tclk + skew2 + Tck2q + Tp2
The clock skew between CLK2 and CLK3 makes the path P2 more critical



CLOCK SKEW



- What causes clock skew?
  - CTS
- Consequences of clock skew
  - Reduced performance
  - Failed functional
- How to reduce clock skew?
  - Clock spines
  - Clock mesh
  - Htree
  - …

Power

Total Power = Pswitch + Pshort_circuit + Pleakage

- $P_{switch} = aCV^2f$ (C=Cequ of load), a = switching activity
  -
- $P_{short\_circuit}$ ~ slew, frequency
  - Use strong cells (large width or low Vt)
- $P_{leakage}$:
  - Use weak cells (min width or high Vt)

Depending upon which application that which type of power will dominate -> corresponding optimization

Signal Integrity

How to fix:

- Driver optimization: driver strength needs to match load, not too strong neither too weak.
- Buffer insertion: For long wire, even very big driver is not enough
- Crosstalk:
  a. Increase space to reduce coupling cap
  b. Add shielding for critical nets
  c. Increase strength of the drivers of the victim nets
  d. Decrease strength of the drivers of the aggressor nets
- Using NDR (Non Default Rule)

Questions

1. Clock skew:
   a. What is clock skew? Is it important? Why?
   b. What causes clock skew? How to reduce the clock skew?
   c. Is global clock skew or local clock skew important? Why?
2. Why is transition time measured from 10 to 90%?
3. Does improving gate delay also reduce wire delay?
4. What is the plus/minus of increasing the transistor width?
5. What are the components of power dissipation in a design? Which one is the most important?
6. What is crosstalk? When does crosstalk become significant? How to avoid/reduce crosstalk?