LSI Design

Final review

HCMC University of Technology

Final review

- 1. Which statement below is NOT CORRECT about CMOS technology?
  - A. CMOS uses both types of MOSFETs: pMOS and nMOS
  - B. CMOS circuits are composed of pull-up and pull-down networks.
  - C. We can implement all logic circuits using CMOS.
  - D. Logic gates can be created only by using CMOS

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2. When do we run Timing analysis?

A. After RTL design and after physical design
B. After synthesis, after DFT and during and after physical design.
C. After DFT and physical design.
D. After physical design.

3. What is used to determine the success of a functional verification?

A. Implemented all the test cases
B. Implemented all verification/test methodologies
C. Achieved required rate for functional coverage.
D. Implemented all test cases by modeling software and emulators

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4. Which step below might change the gate netlist?

A. RTL design.
B. DFT.
C. Functional verification
D. Static timing analysis.

5. When the netlist is changed, which step below needs to be done to qualify that the functions stays the same?

A. Timing verification.
B. Physical verification.
C. Equivalence check.
D. Design for test.

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6. Minimum time during which the inputs need to stay unchanged so that the output can achieve the correct logic is?

A. Longest path delay.

B. Shortest path delay.

C. Latest arrival time.

D. Longest path delay - shortest path delay.

7. To reduce power, we can

A. Reduce the voltage of the logic that runs at lower frequency

B. Turn off the blocks that are not needed when the circuit operates in a certain mode.

C. Turn off the clock to the flipflops that are not needed when the circuit operates in a certain mode.

D. All above

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8. Which methodology below can be used to synchronize the signals from clkA domain to clkB domain?

A. Use a flipflop in clkB domain.

B. Use 2 flipflops in series in clkB domain without any logic between them to latch the signal from clkA domain

C. Use 2 flipflops in parallel in clkB domain to latch the signal from clkA domain, then compare these 2 values.

D. All above are wrong.

9. What is the purpose of DFT - Design for testability?

A. To test the circuit during the design process

B. To test the circuit during the system integration

C. Discover functional failures after fabrication

D. Discover defects of the circuit after fabrication

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10. Which vector below is the minimum test vector to check stuck-at-fault of a NAND gate

A. {0, 1}, {1, 0}, {1, 1}

B. {0, 0}, {0, 1}, {1, 0}, {1, 1}

C. {1, 0}, {1, 1}

D. {1, 1}

11. In Verilog, which assignment below is used to describe a sequential circuit in always @ (edge sensitive)

A. Continuous assignment.

B. Blocking assignment.

C. Non-blocking assignment.

D. B and C.

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12. Which factor(s) below influence(s) the cost of DFT?

A. Complexity of the design

B. Frequency target of the design

C. A and B are correct.

D. A and B are wrong.

13. What is the requirement of Critical Path Slack to meet the frequency target?

A. >= 0.

B. <= clock period.

C. <= 0.

D. < 0.