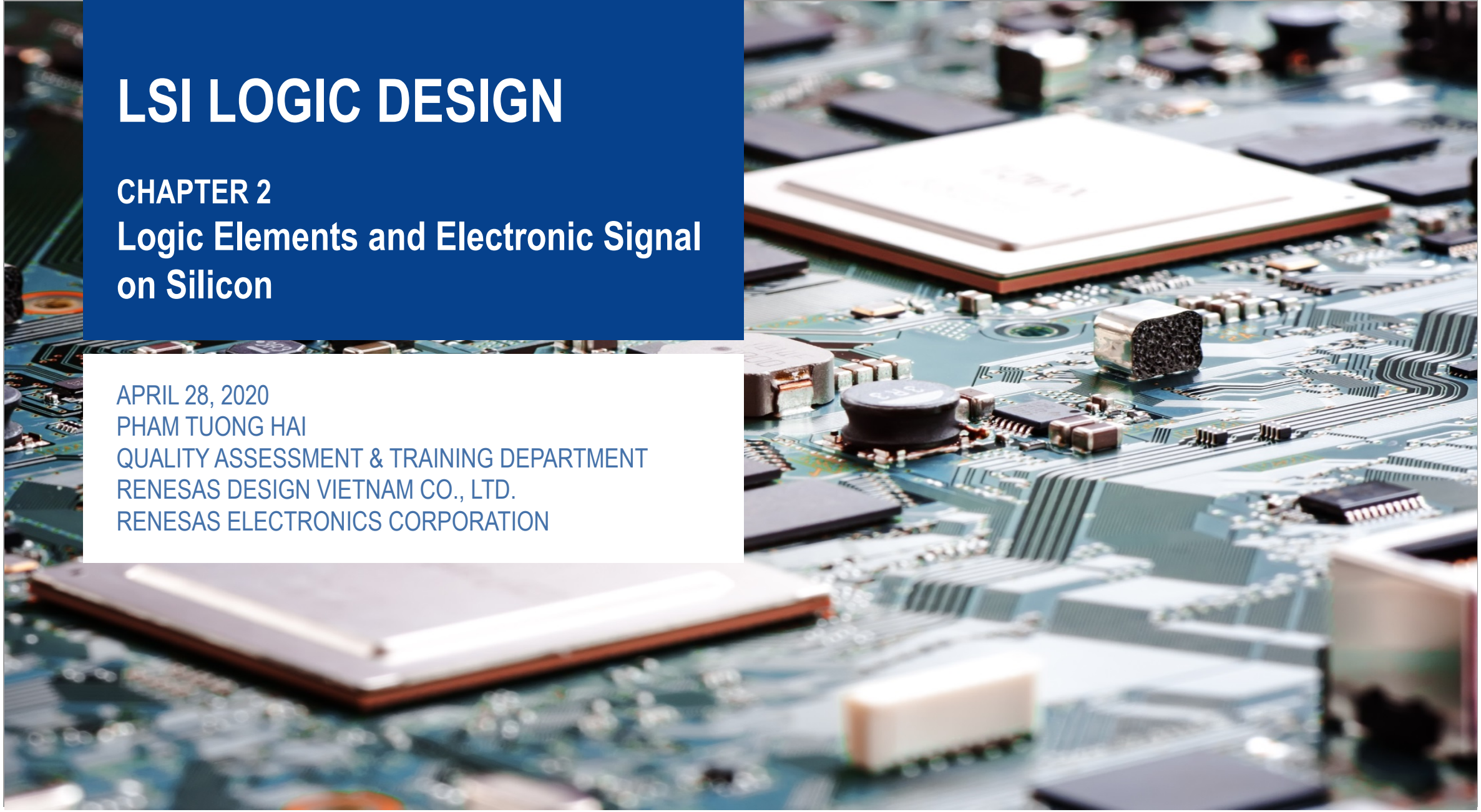
LSI LOGIC DESIGN

CHAPTER 2
Logic Elements and Electronic Signal on Silicon



APRIL 28, 2020
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RENESAS ELECTRONICS CORPORATION

CHAPTER 2. Logic Elements and Electronic Signal on Silicon

2.1. Digital Logic and CMOS Circuit.

2.2. Logic Gate on Silicon.

2.3. Electronic Signal Propagation on Silicon.

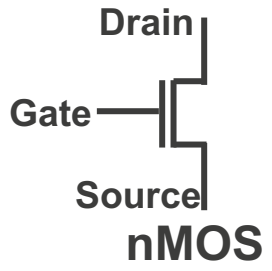
2.4. Problem with Electronic Signal.

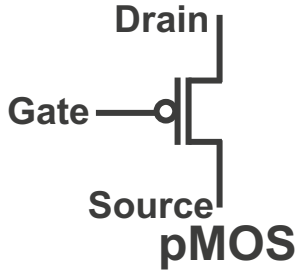
2.1 Digital Logic and CMOS Circuit

Devices Implemented in LSI

○ MOS Transistor

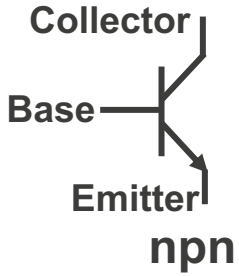
Broadly used owing to the properties of high-speed, low-voltage, and high-integration.

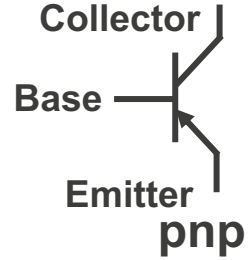




○ Bipolar Transistor

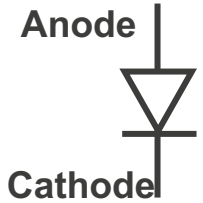
Used in RF and analog applications owing to its high-drive-ability.

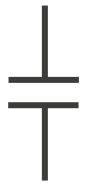




○ Other devices

Diode, resistors, capacitors etc.





MOS: Metal Oxide Semiconductor

What is Semiconductor?

A semiconductor is a material that behaves between a conductor and an insulator.

At room temperature, semiconductor has higher electric conductivity than an insulator, but lower than a conductor.

At very low temperatures, pure or intrinsic semiconductors behave like insulators.

At higher temperatures or under light, pure or intrinsic semiconductors can become conductive.

The addition of impurities to a pure semiconductor can also increase its conductivity.

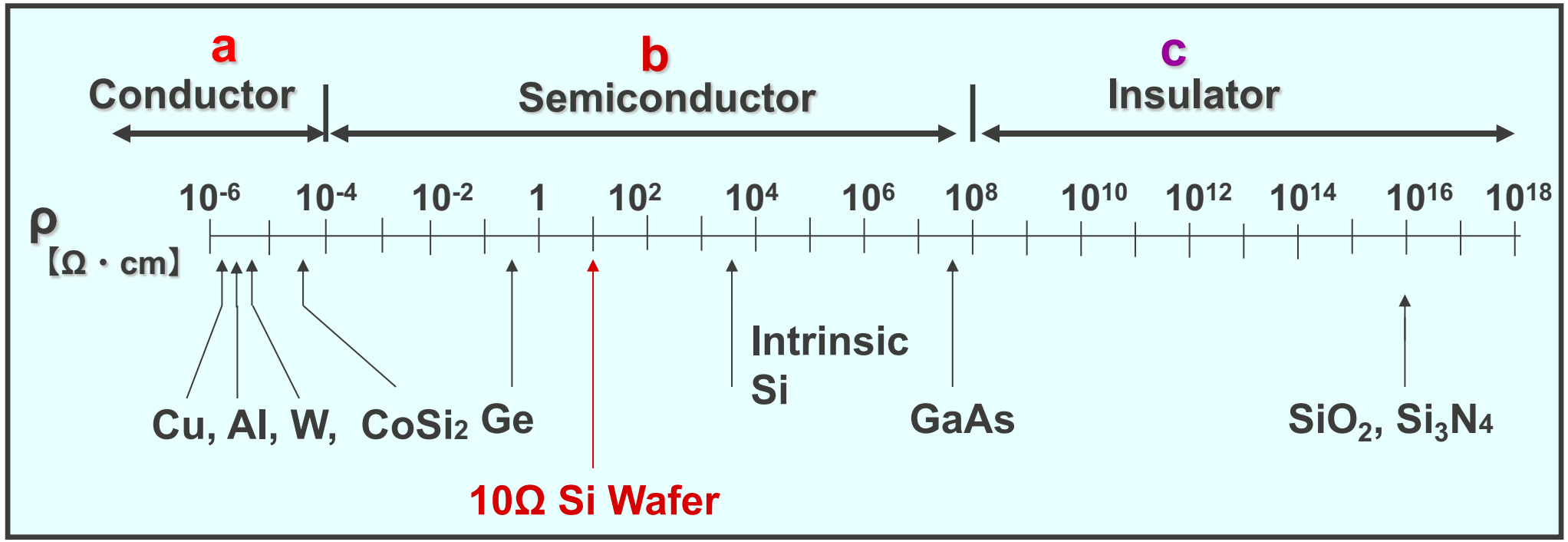
What is Semiconductor?

a) Conductor (Cu, Al) electron free from atomic bound

b) Semiconductor (Si, Ge, GaAs) electron loosely bounded to atom

c) Insulator (SiO_2, SiN) electron tightly bounded to atom

Materials are grouped by 3 types in electrical resistivity



Intrinsic and Extrinsic Semiconductor

Intrinsic semiconductor

A perfect semiconductor which has no impurities

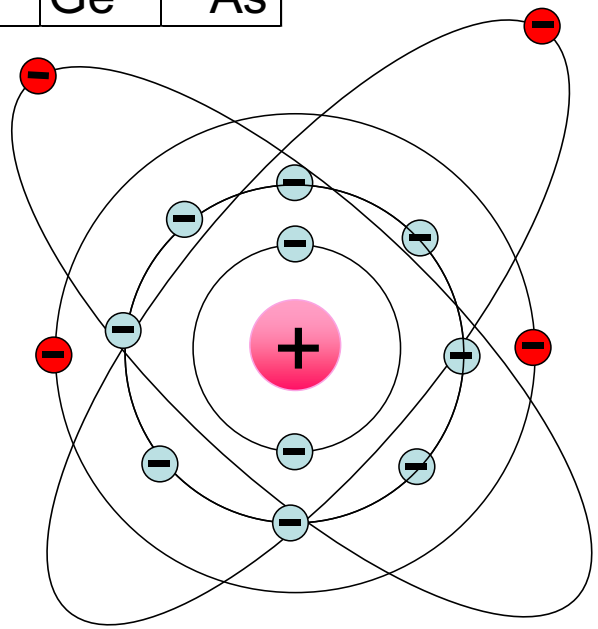
Its characteristics comes from the semiconductor itself

Extrinsic semiconductor

A semiconductor to which impurity is doped

Some part of its characteristics comes from the doped impurity

Group	III	IV	V
	5 B	6 C	7 N
	13 Al	14 Si	15 P
	31 Ga	32 Ge	33 As

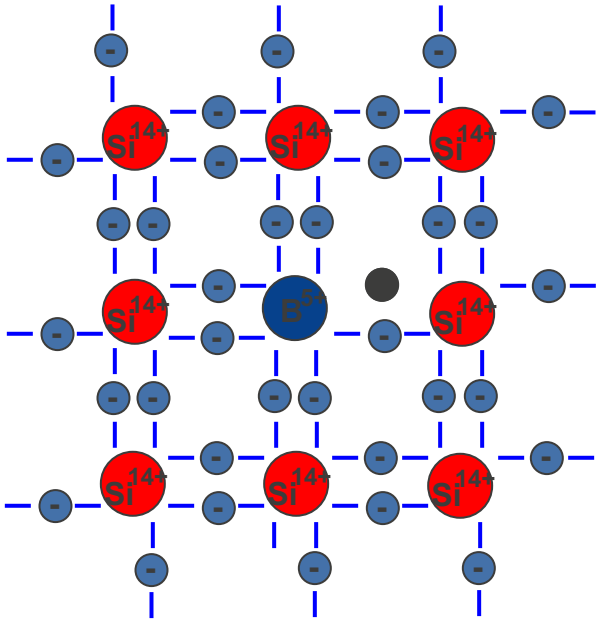


P-type Silicon - Acceptor

It is very easy for an electron from a nearby **Silicon** to **Silicon** bond to fall into this hole and effectively move the hole away from the **Boron** atom

Since the **Boron** atom will accept an electron, **Boron** and the other elements of Group III (**B**, **Ga**) are referred to as **acceptors**

Silicon with acceptor is called as **P-type Silicon**, since “positive” holes are generated and contribute a current flow

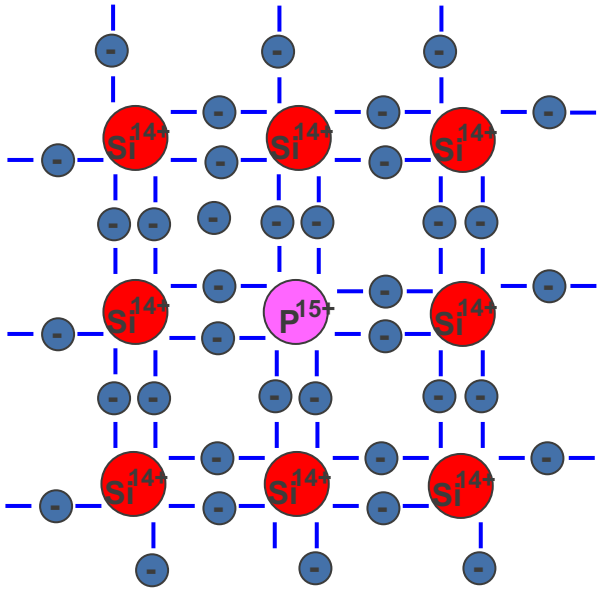


N-type Silicon - Donor

If a Group V atom, such as **Phosphorus**, is introduced into the **Silicon** lattice, it will have an extra electron which may easily break away, becoming a conduction electron

The **Phosphorus** is referred to a **donor**, since it donates an electron to the conduction band.
Other donor is **As**

Silicon with donor is called as **N-type Silicon**, since “negative” electrons are generated and contribute the current flow

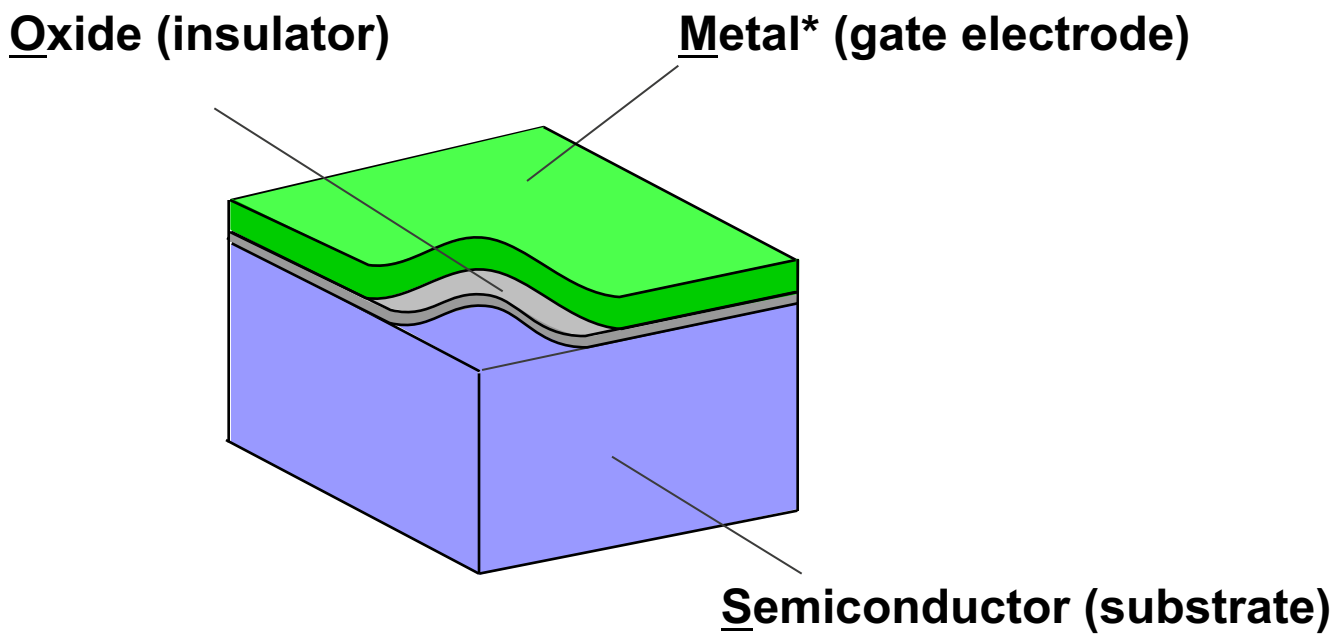


Properties of Silicon and Silicon Oxide

TABLE 2.1 Physical Properties of Si and SiO_2 at Room Temperature (300 K)

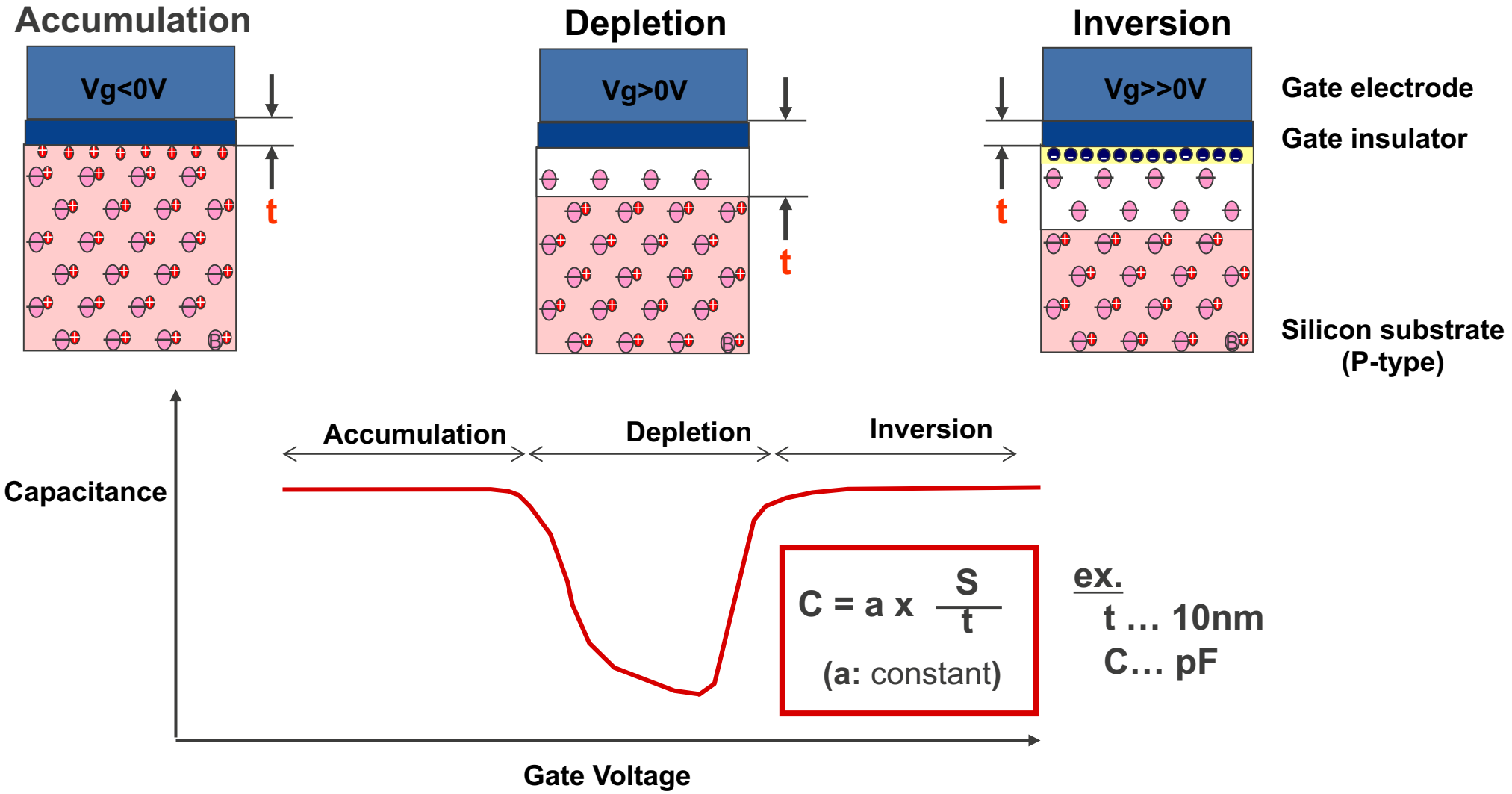
Property	Si	SiO_2
Atomic/molecular weight	28.09	60.08
Atoms or molecules/cm^3	5.0×10^{22}	2.3×10^{22}
Density (g/cm^3)	2.33	2.27
Crystal structure	Diamond	Amorphous
Lattice constant (Å)	5.43	—
Energy gap (eV)	1.12	8–9
Dielectric constant	11.7	3.9
Intrinsic carrier concentration (cm^{-3})	1.4×10^{10}	—
Carrier mobility (cm^2/V-s)	Electron: 1430	—
	Hole: 470	—
Effective density of states (cm^{-3})	Conduction band, N_c: 3.2×10^{19}	—
	Valence band, N_v: 1.8×10^{19}	—
Breakdown field (V/cm)	3×10^5	$>10^7$
Melting point (°C)	1415	1600–1700
Thermal conductivity (W/cm-°C)	1.5	0.014
Specific heat (J/g-°C)	0.7	1.0
Thermal diffusivity (cm^2/s)	0.9	0.006
Thermal expansion coefficient ($°C^{-1}$)	2.5×10^{-6}	0.5×10^{-6}

MOS Capacitor



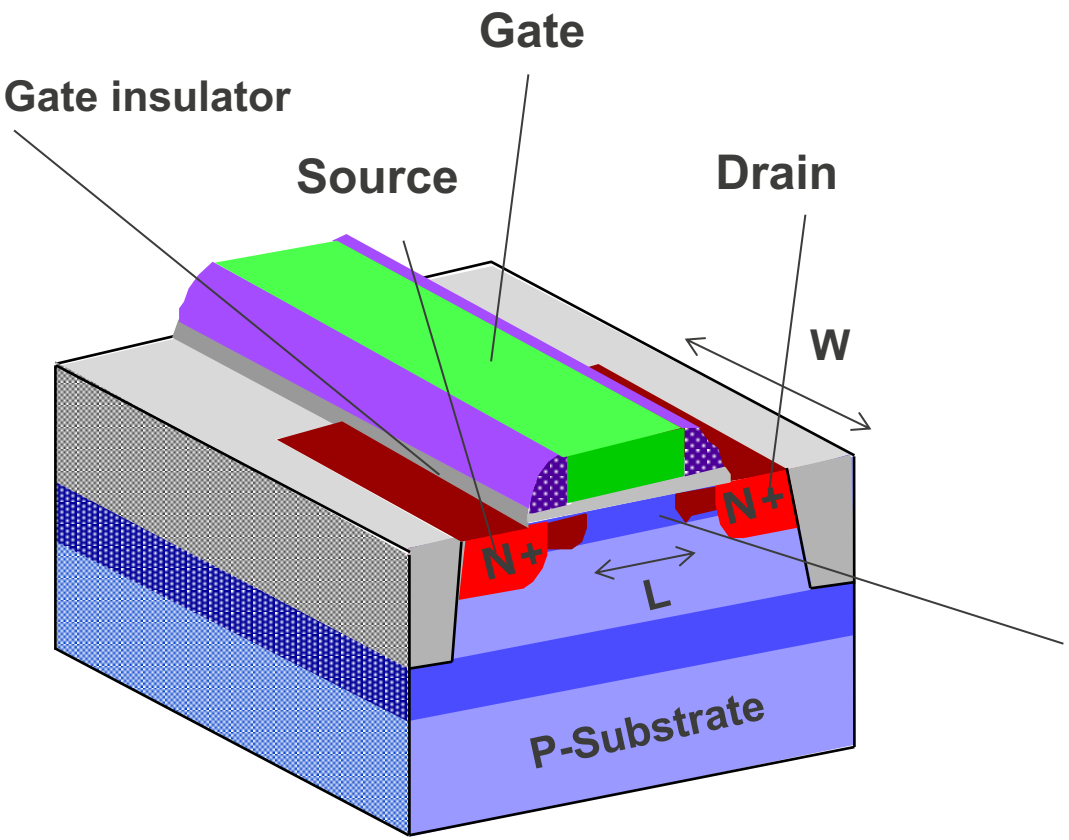
** actual metal or heavily doped polysilicon*

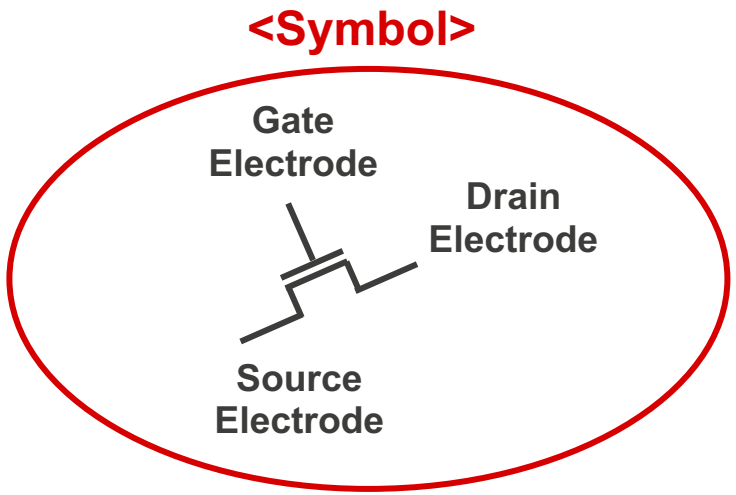
Behavior of MOS Capacitor



MOSFET

*** Focusing on n-channel transistor ***





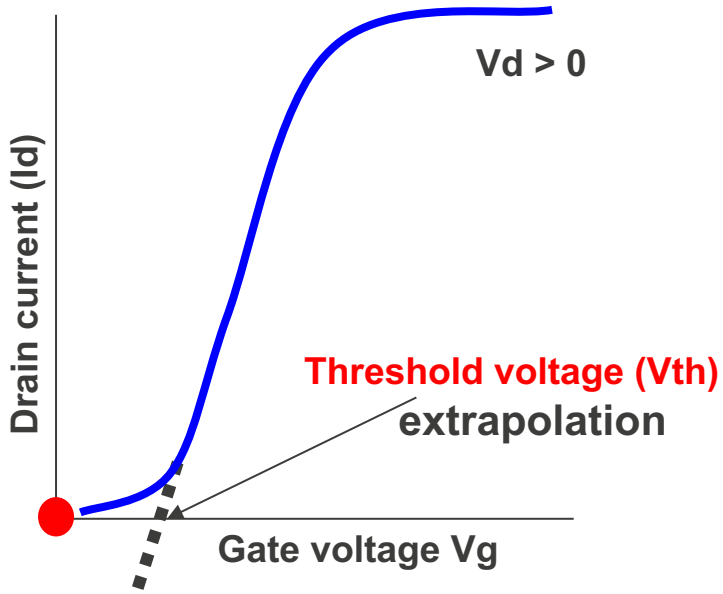
Channel

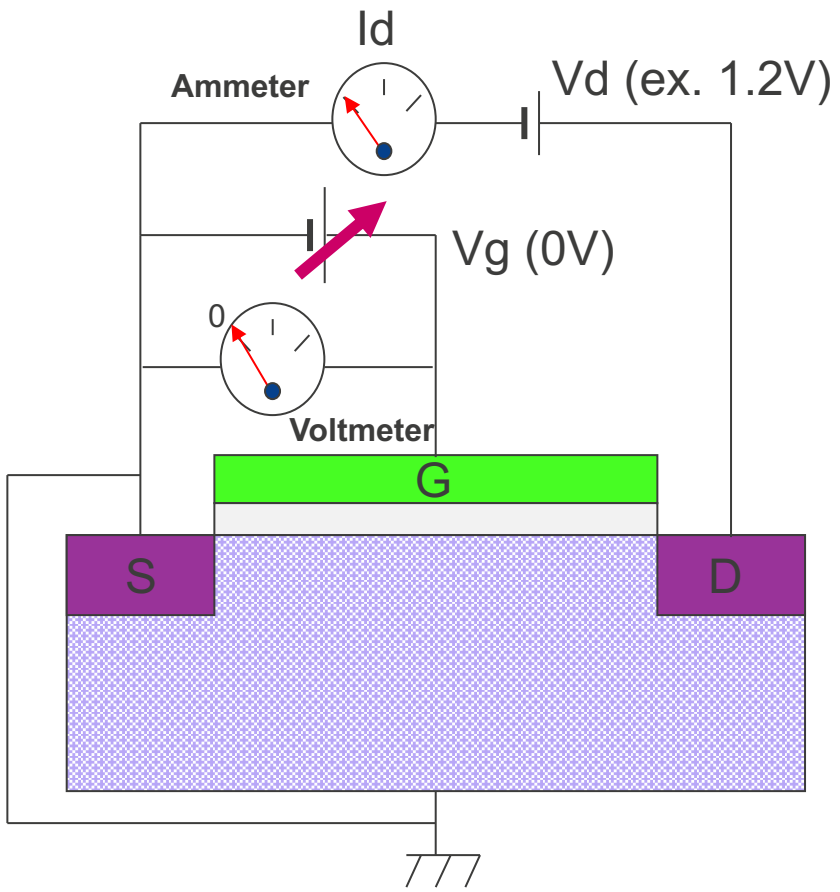
N+: heavily doped silicon
= low resistive electrode

L: channel length
W: channel width
FET: Field Effect Transistor

Operation of N-channel MOSFET (1)

- Gate characteristics



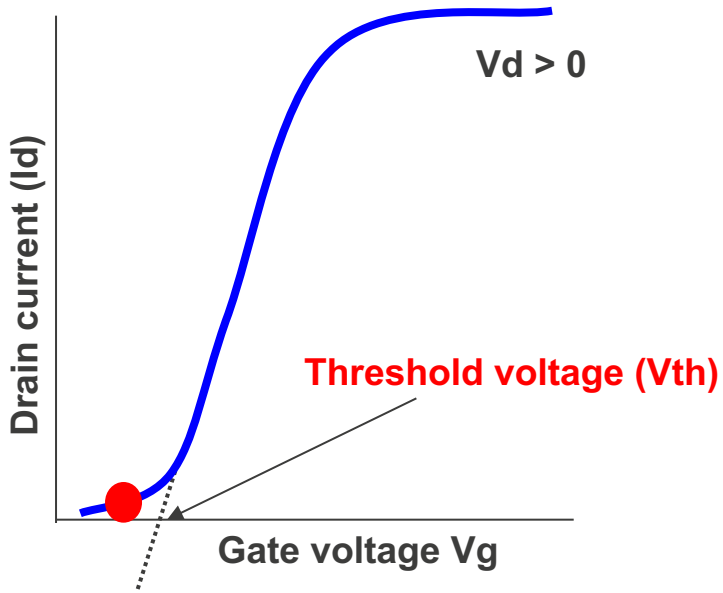


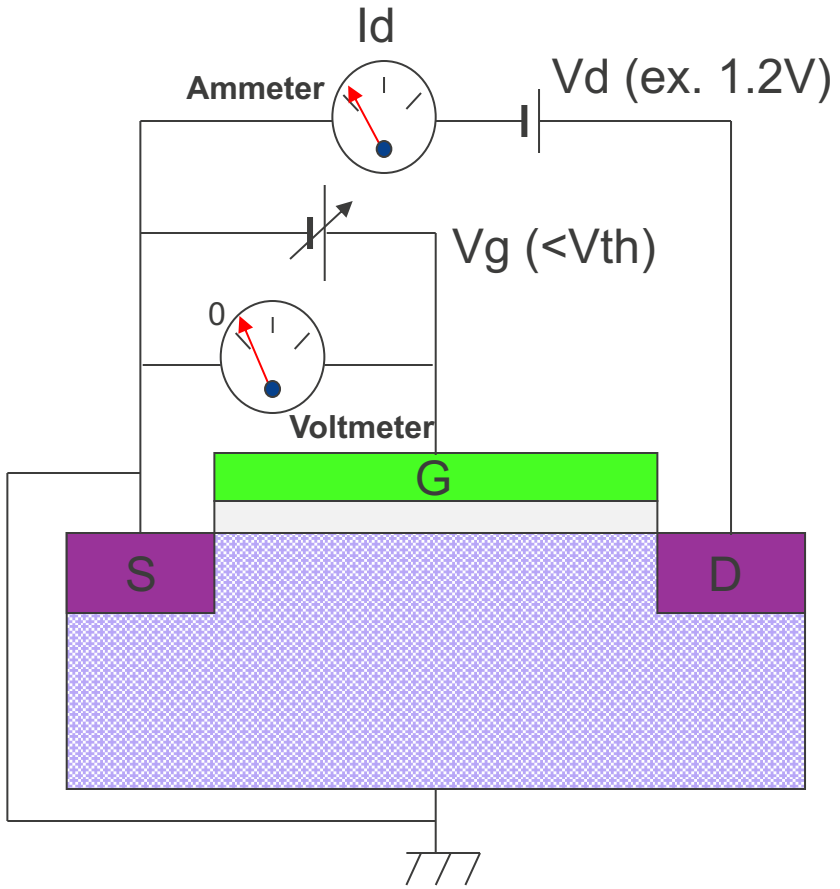
Sub-threshold region **(0≤Vg≤Vth)**

Id = 0 (nearly)

Operation of N-channel MOSFET (2)

- Gate characteristics

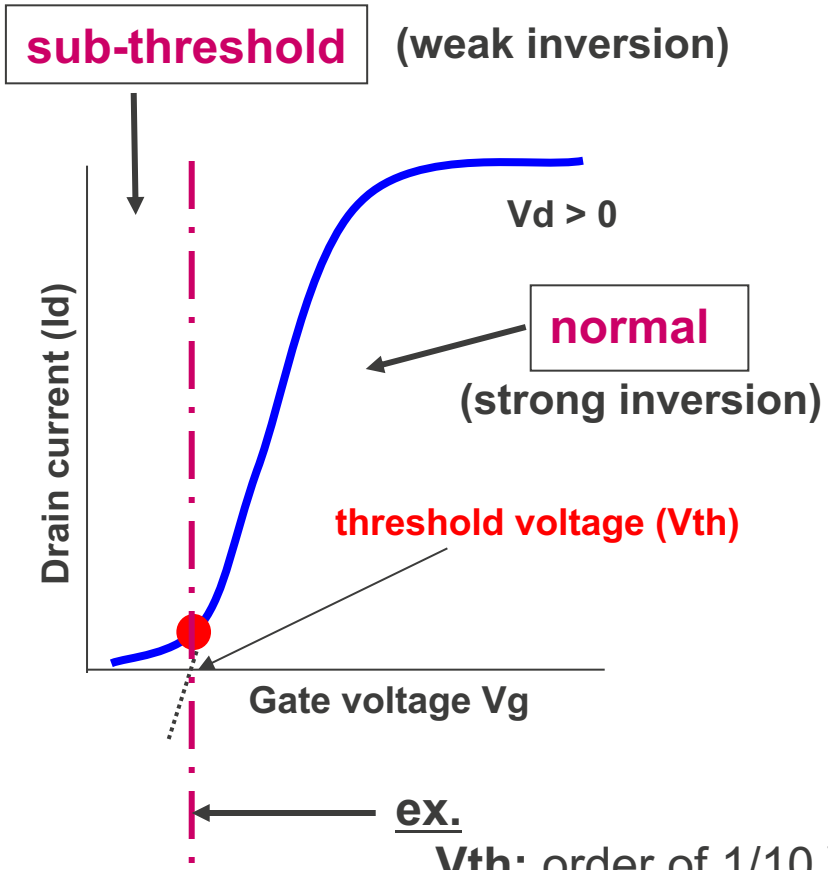




When Vg<Vth, the electric current is called sub-threshold current. This is one of the leakage currents.

Operation of N-channel MOSFET (3)

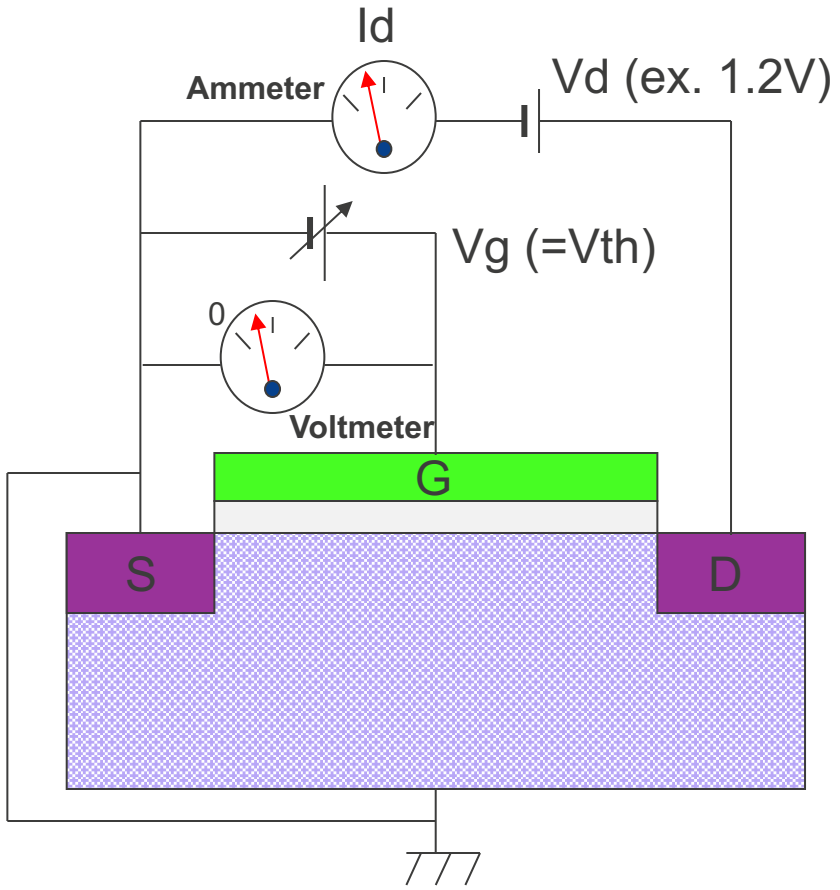
- Gate characteristics



ex.

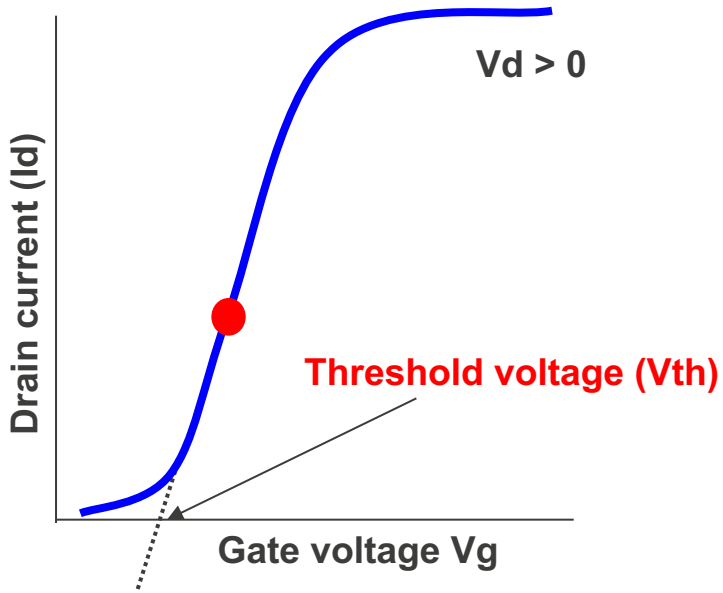
Vth: order of 1/10 V

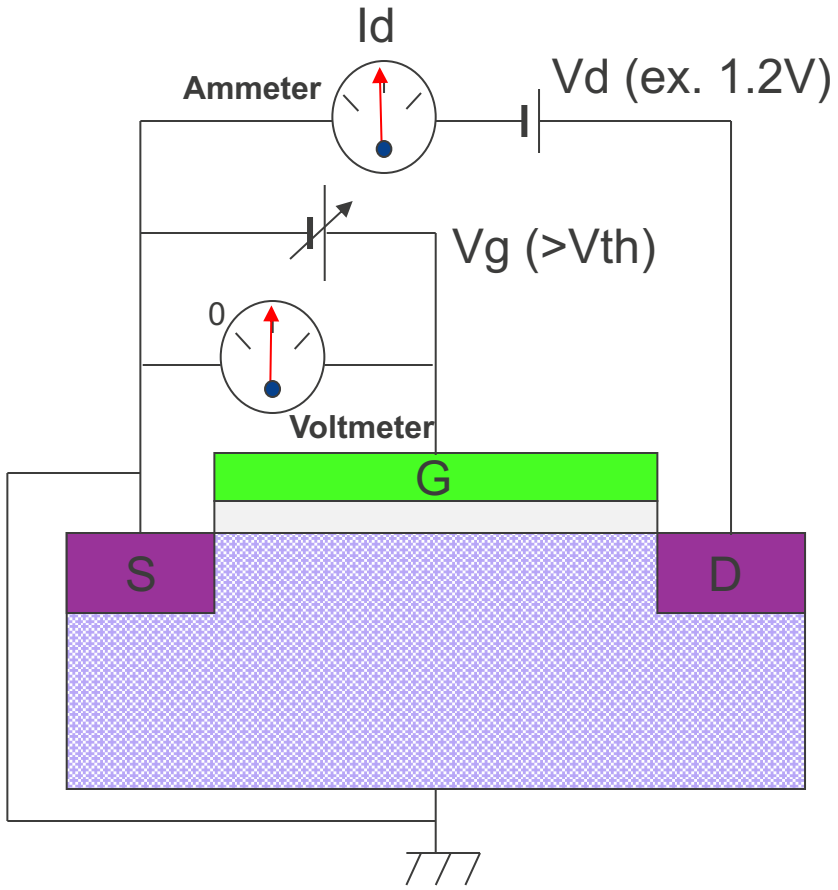
Id : order of nA



Operation of N-channel MOSFET (4)

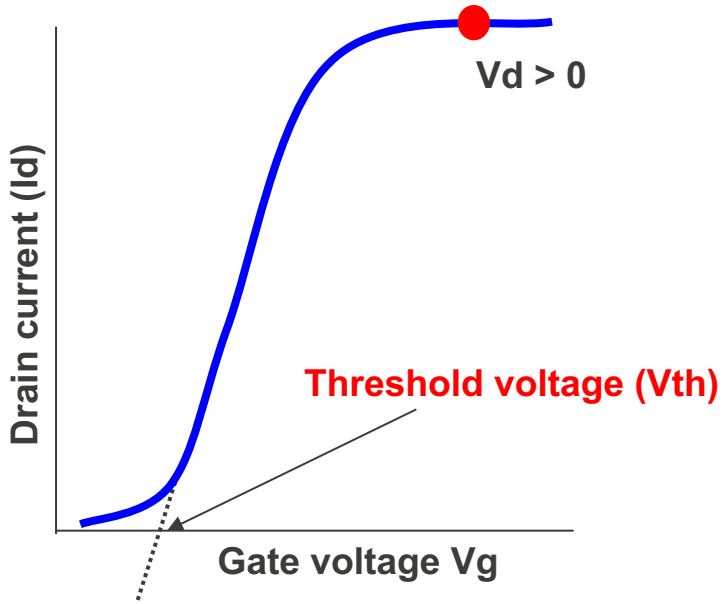
- Gate characteristics

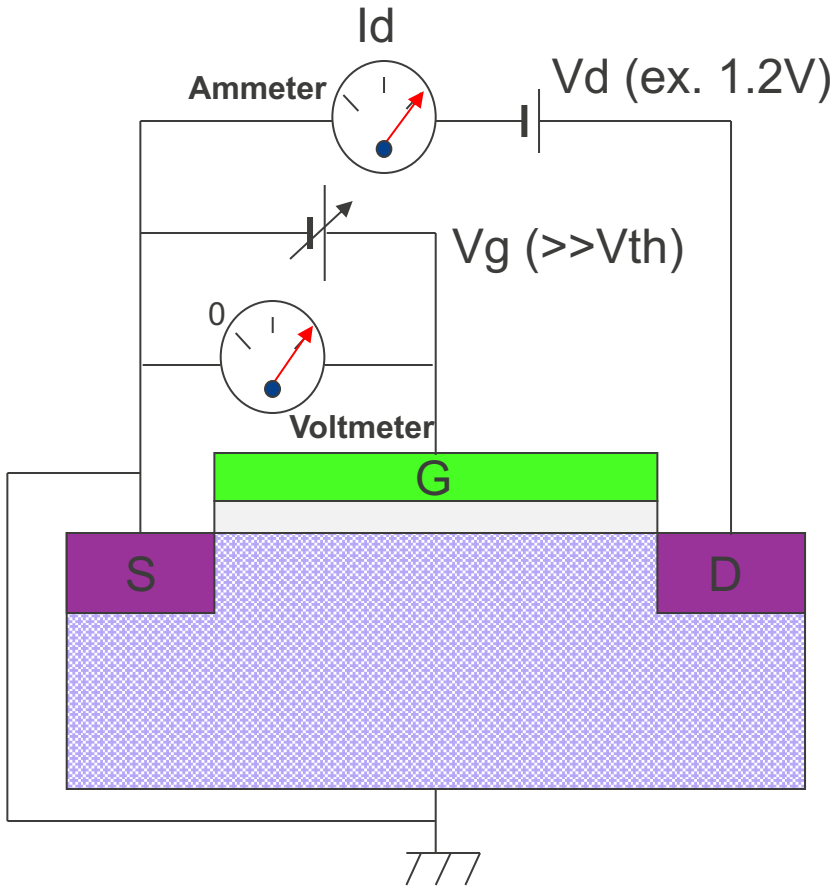




Operation of N-channel MOSFET (5)

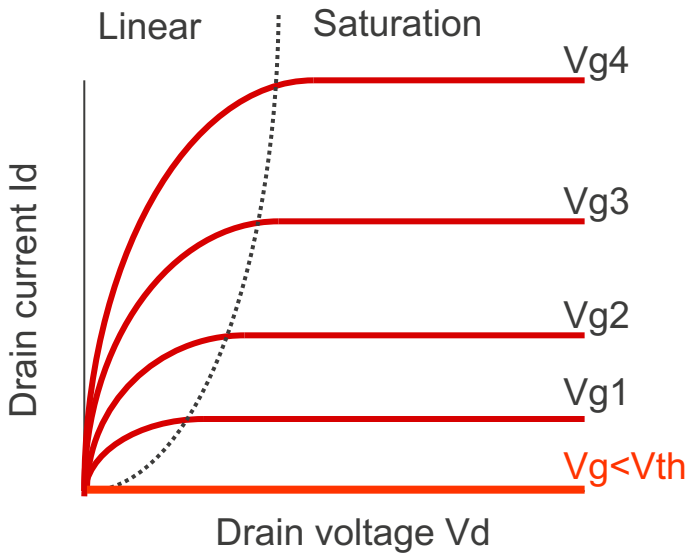
- Gate characteristics

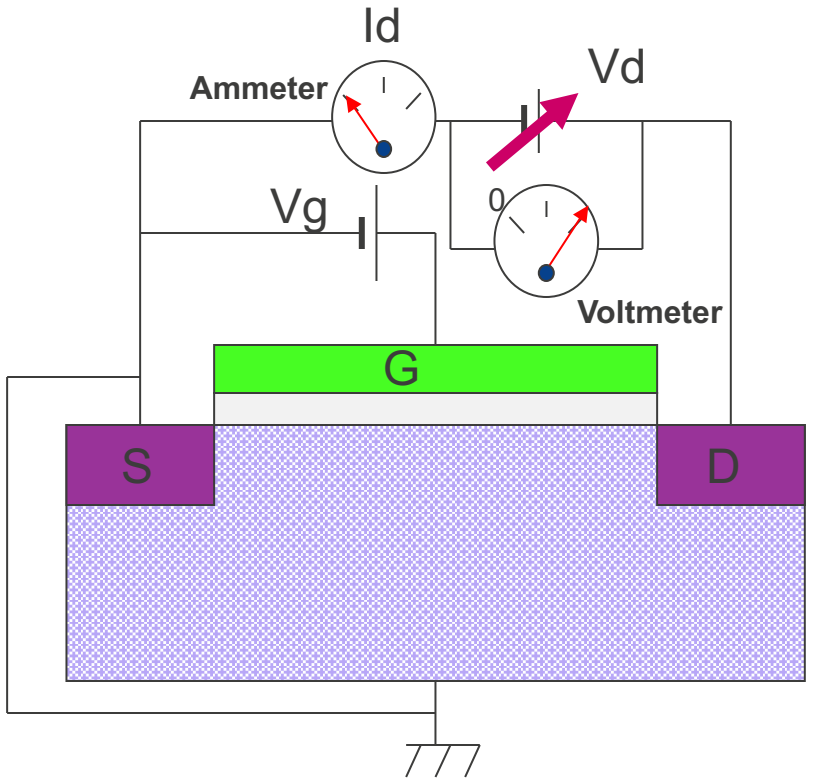




Operation of N-channel MOSFET (6)

- **Drain characteristics**

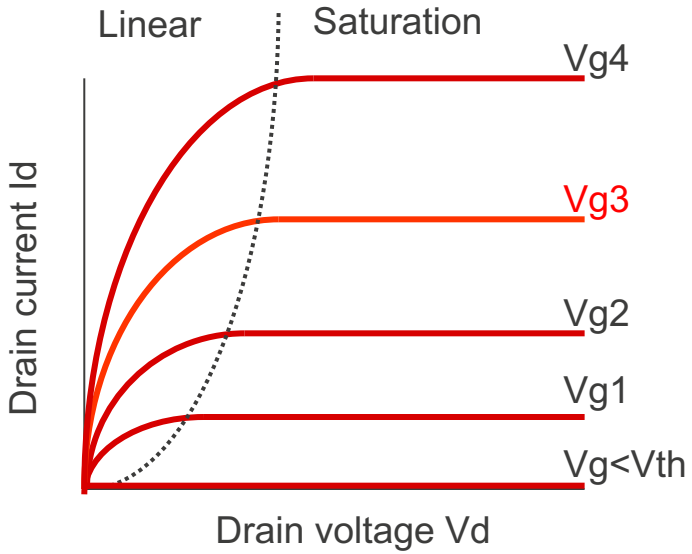


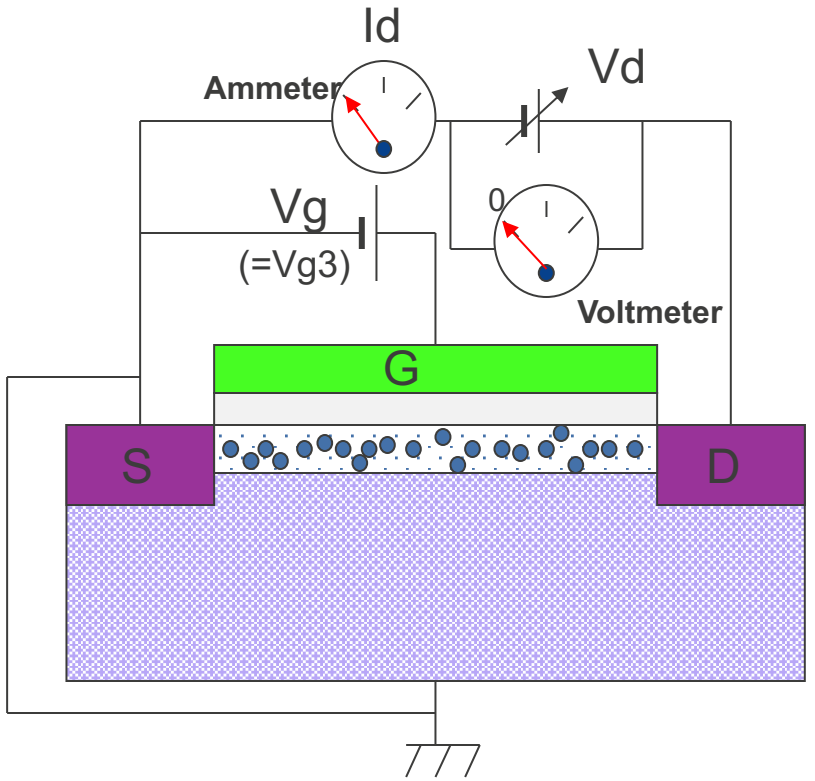


Even if Vd>0, there is no current (except leakage) when Vg<Vth.

Operation of N-channel MOSFET (7)

- **Drain characteristics**

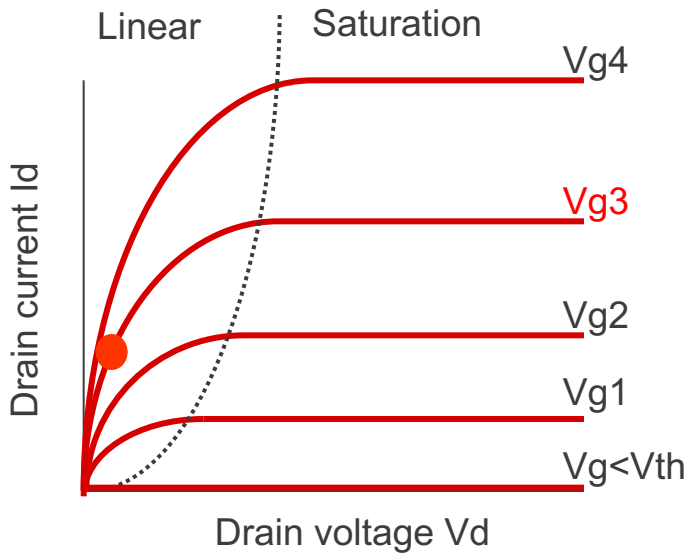


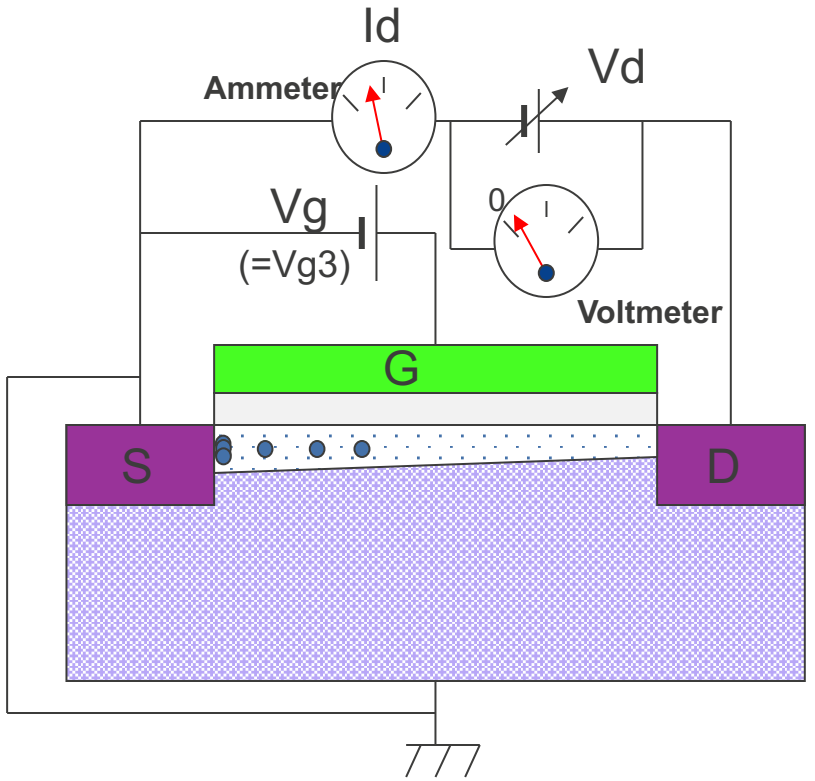


Apply Vg=Vg3, and watch what happens.

Operation of N-channel MOSFET (8)

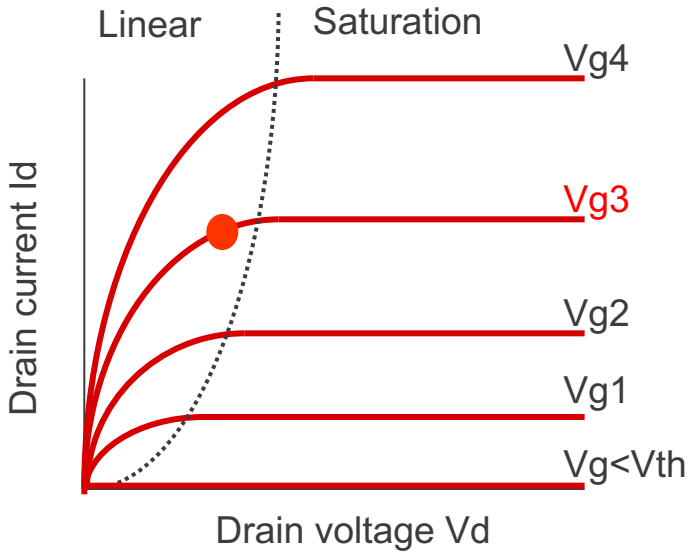
- **Drain characteristics**

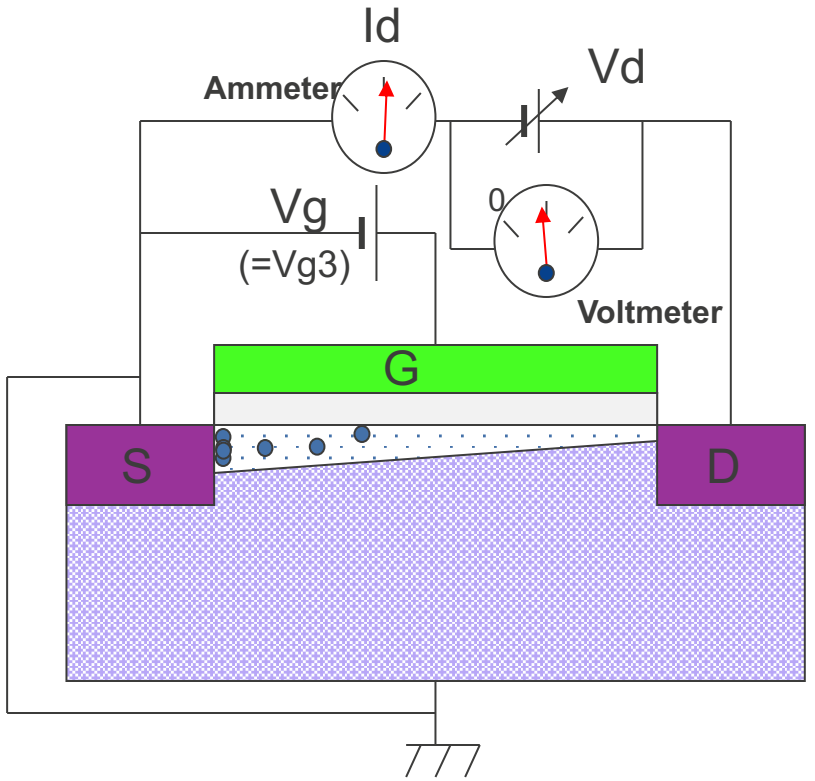




Operation of N-channel MOSFET (9)

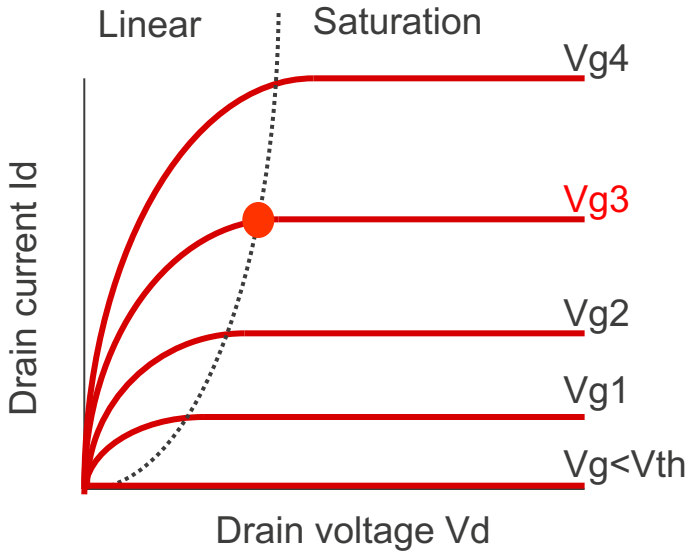
- **Drain characteristics**

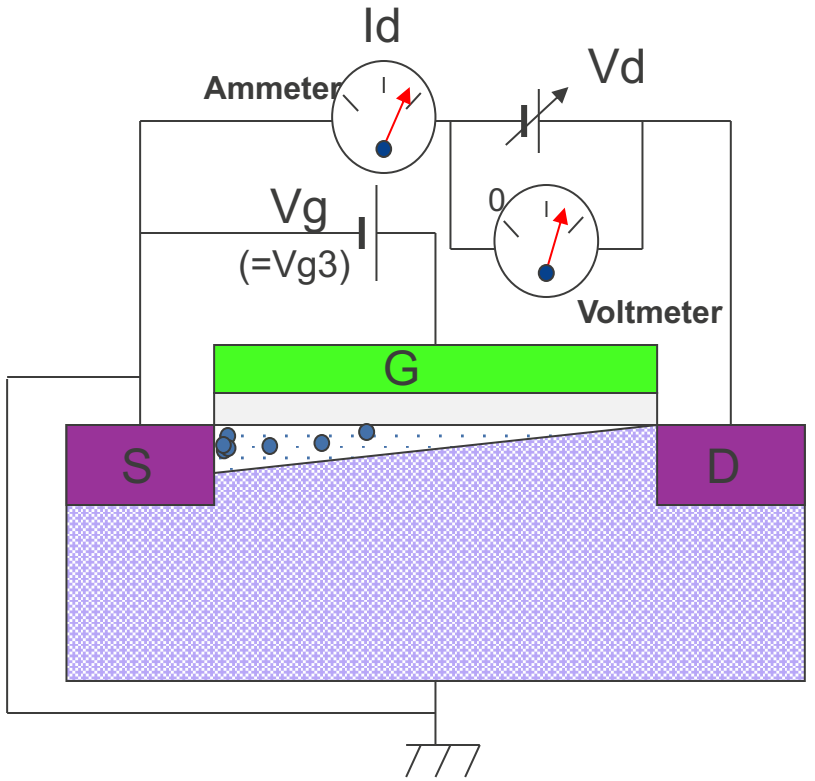




Operation of N-channel MOSFET (10)

- **Drain characteristics**

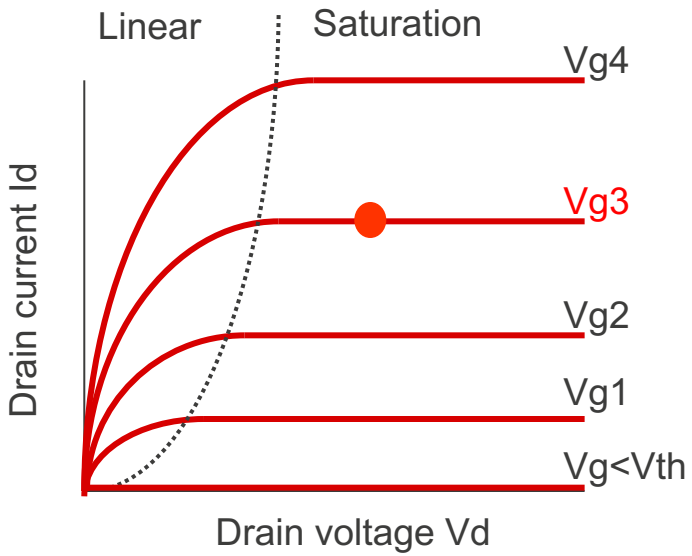


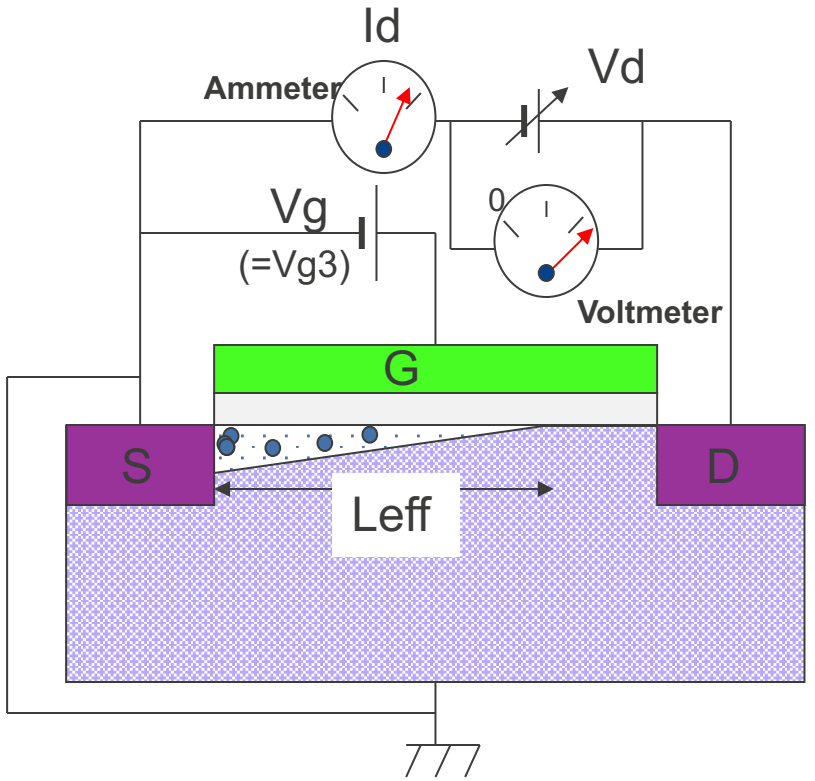


When Vd=Vg-Vth, it is called “pinch-off point”.

Operation of N-channel MOSFET (11)

- **Drain characteristics**





After pinch-off, the current becomes constant.
Electrons are attracted by drain field and flow through the depletion region.

Current characteristics of MOSFET (Summary)

<Fundamental Formula of drain current>

$$I_d = \begin{cases} \beta_n \{V_d(V_g - V_{thn}) - V_d^2/2\} \\ \quad \text{(Linear region } 0 \le V_d \le V_g - V_{thn}\text{)} \\ \beta_n (V_g - V_{thn})^2 / 2 \\ \quad \text{(Saturation region } V_d > V_g - V_{thn}\text{)} \end{cases}$$

$\beta_n = \mu C_{ox} W/L$

μ: Electron Mobility

C_{ox}: Gate capacitance per unit area

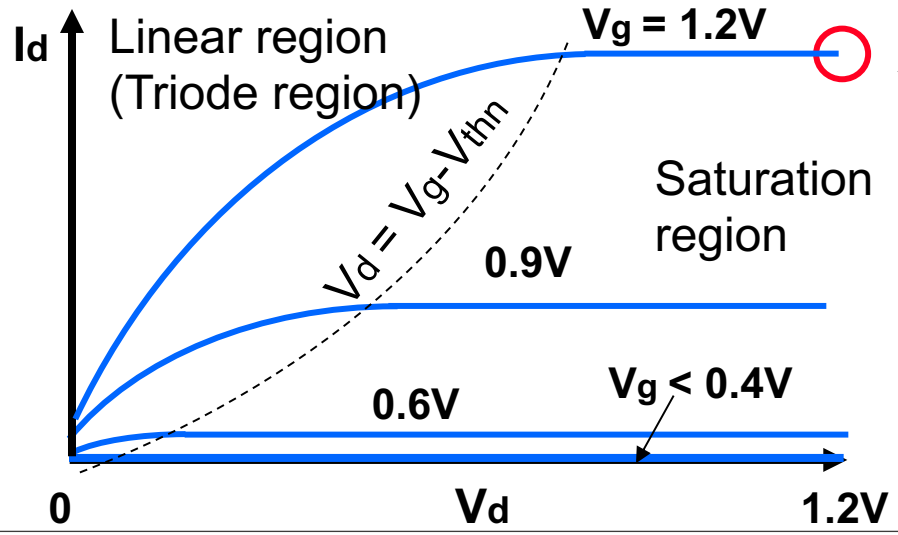
W: Gate width

L: Gate length

V_{thn} : Threshold voltage of NMOS

(gate voltage required to switch ON transistor)

<Characteristics of drain current >



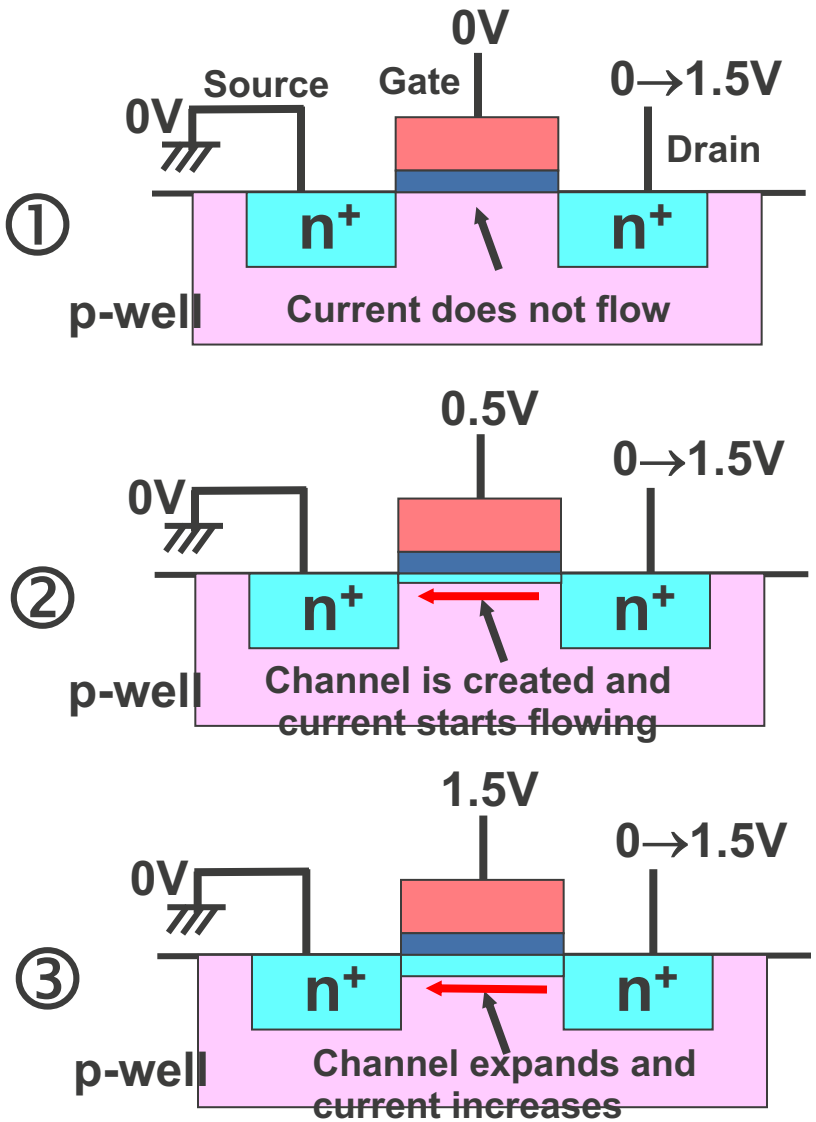
Drain current at $V_g = V_d = V_{dd}$ is called as

Saturation Conditions:

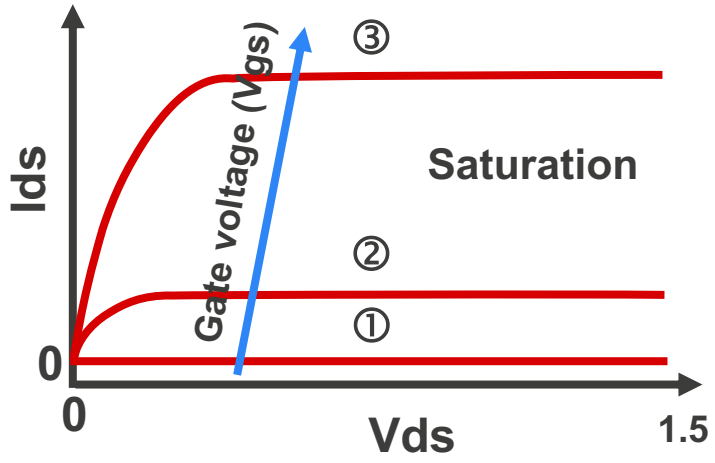
$V_{gs} - V_{th} > 0$

$V_{ds} > V_{gs} - V_{th}$

Operations of nMOS Transistor



<Characteristics of drain current >

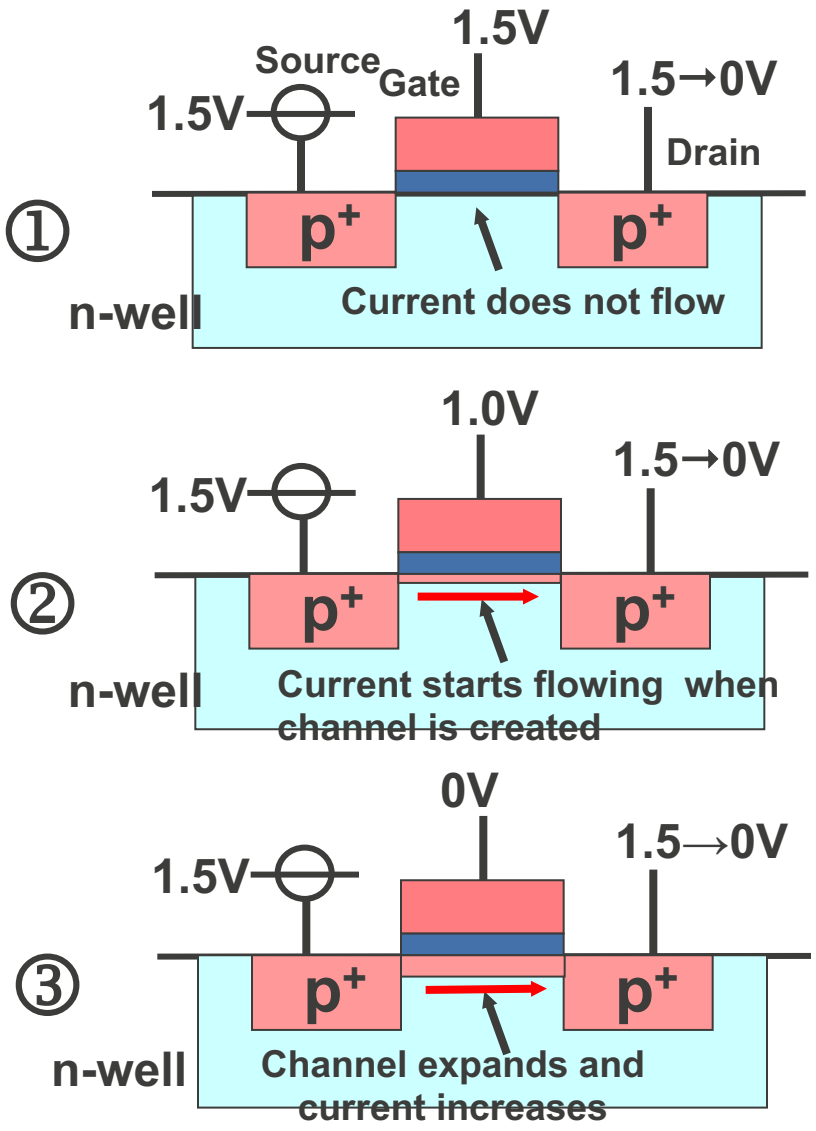


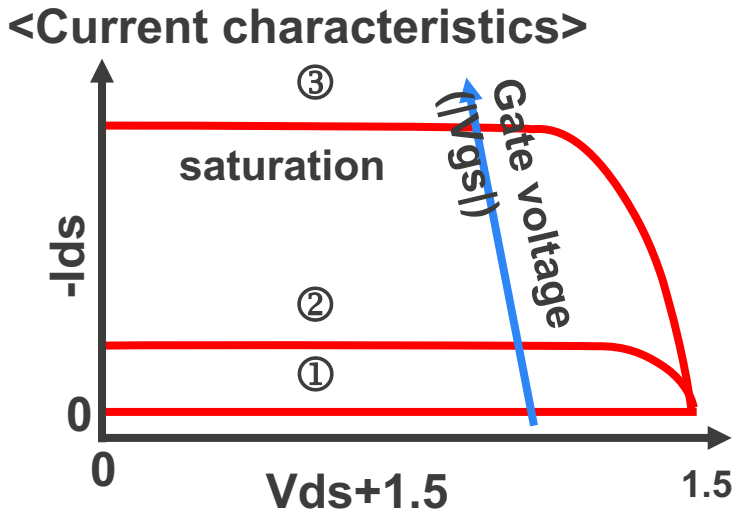
<Formula of drain current>

$$Ids = \begin{cases} \beta n \{Vd \cdot (Vg - Vthn) - Vd^2/2\} & (\text{when } 0 \le Vd \le Vg - Vthn) \\ \beta n (Vgs - Vthn)^2/2 & (\text{when } Vd > Vg - Vthn) \end{cases}$$

βn: proportionality coefficient
Vthn: threshold voltage (gate voltage required to switch ON transistor)

Operations of pMOS Transistor



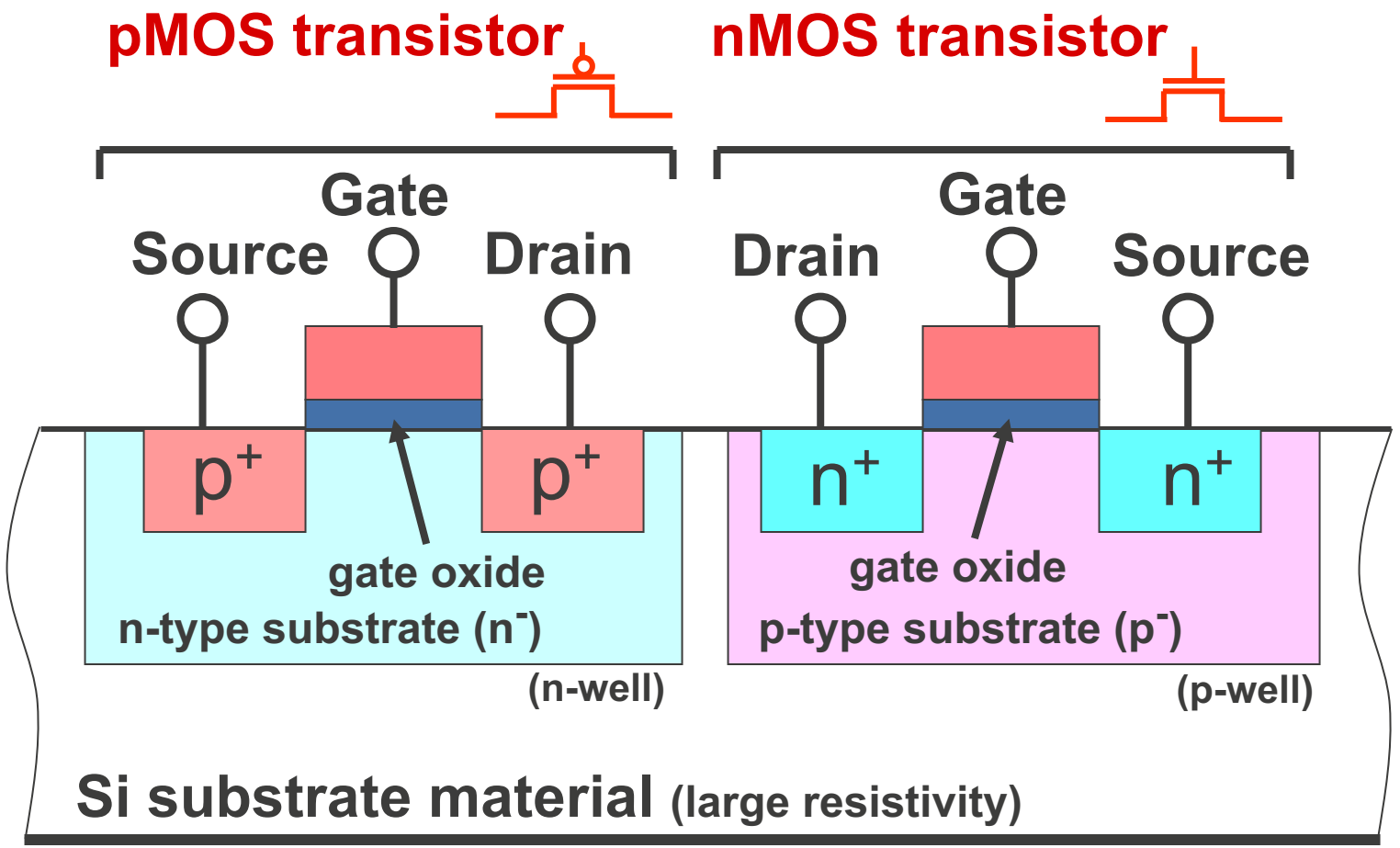


<Formula of current>

$$Ids = \begin{cases} -\beta p\{Vd\cdot(Vg-Vthp)-Vd^2/2\} \\ \quad (\text{when } Vg-Vthp \le Vd \le 0) \\ -\beta p(Vgs-Vthp)^2/2 \\ \quad (\text{when } Vds<Vgs-Vthp) \end{cases}$$

βp : proportionality coefficient
Vthp: threshold voltage (gate voltage required to switch ON transistor)

Structure of CMOS Transistor

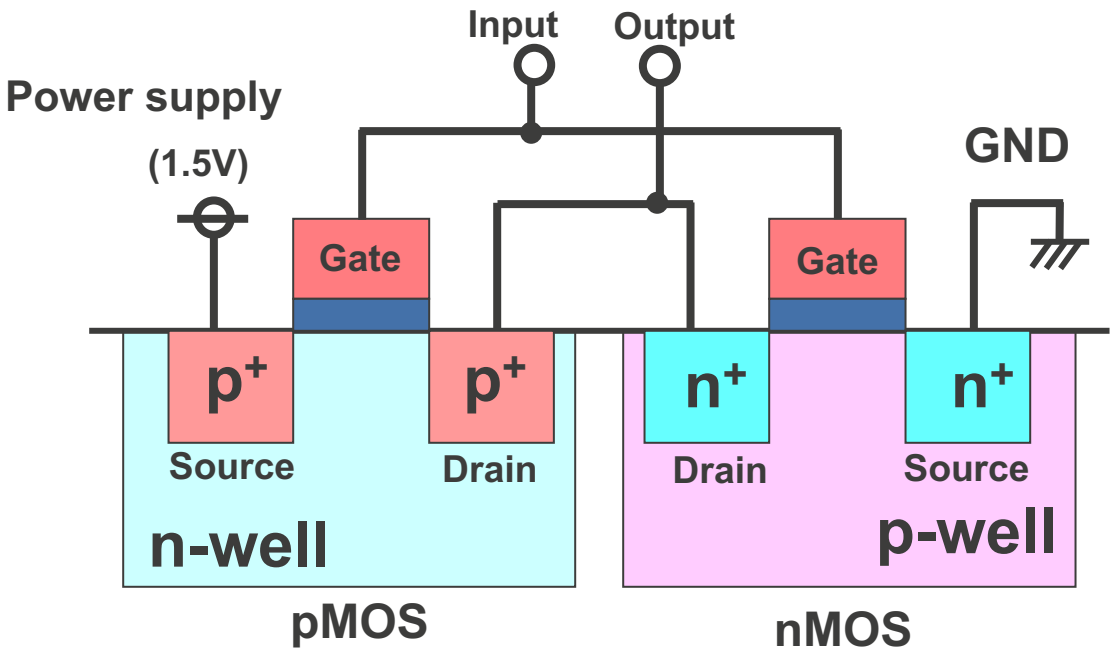


MOS: Metal-Oxide Semiconductor
CMOS: Complementally MOS

2.2 Logic Gate on Silicon

Inverter

<CMOS inverter Structure >



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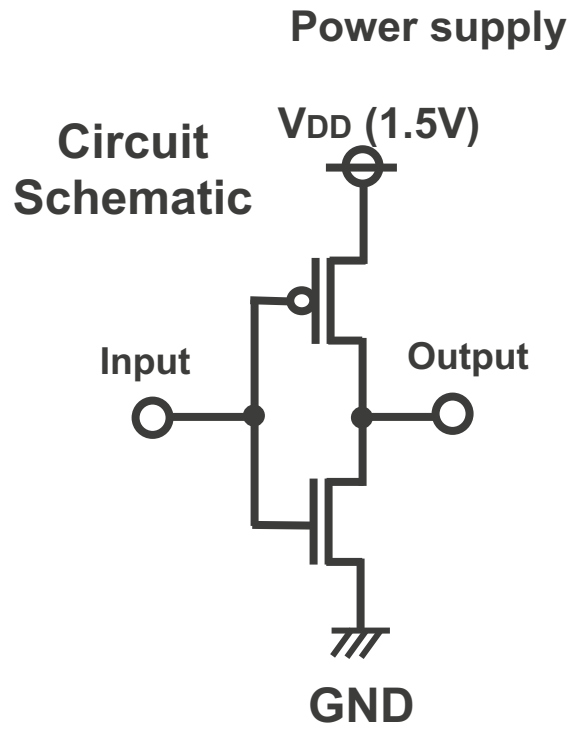
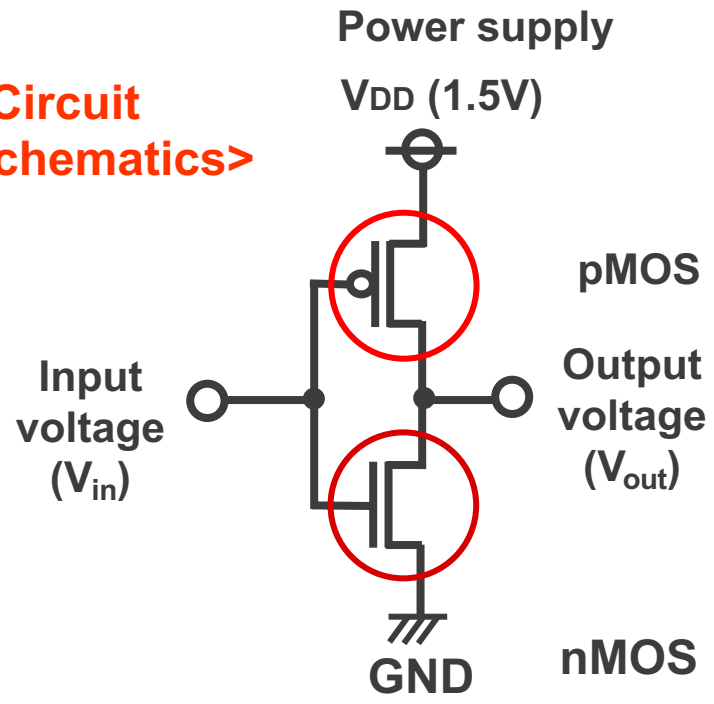


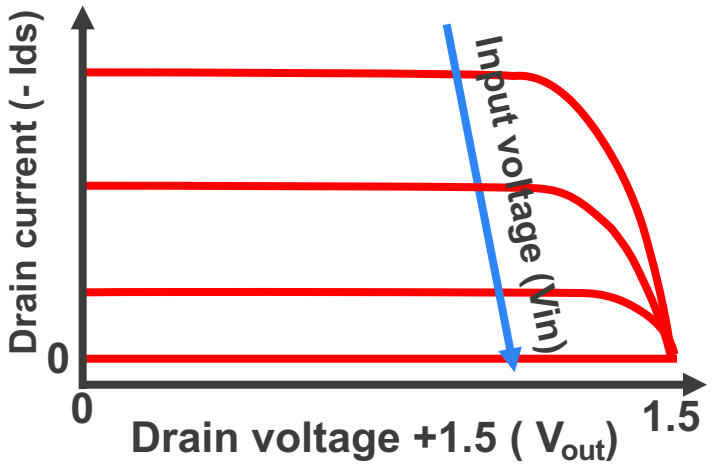
Simplest logic circuit with a pair of pMOS and nMOS transistors

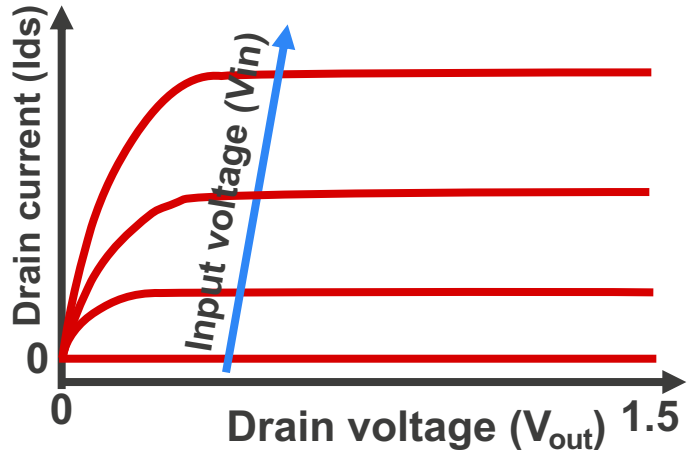
Logic Circuit on Silicon Chip

Inverter

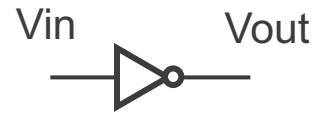
<Circuit Schematics>



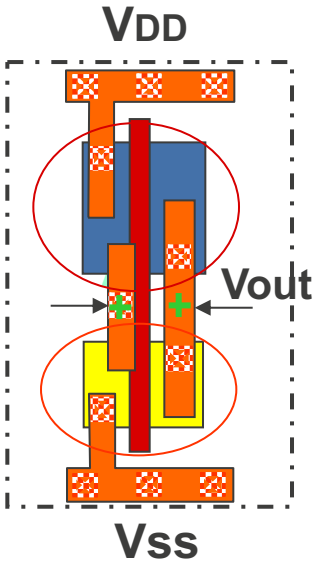




<Cell Symbol>



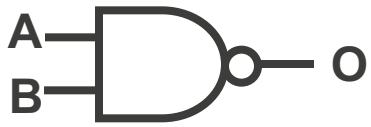
<Layout pattern>

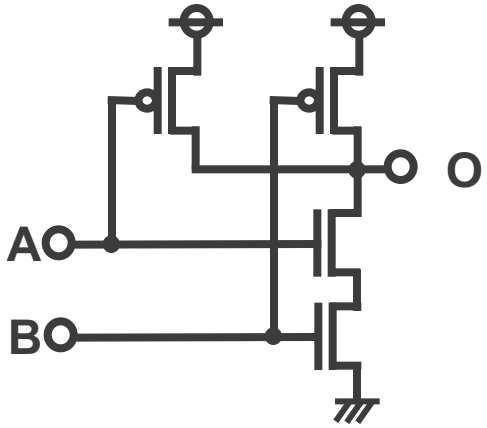


Inverter characteristics are defined by current characteristics of both transistors.

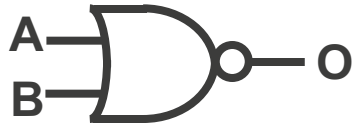
Logic Gate

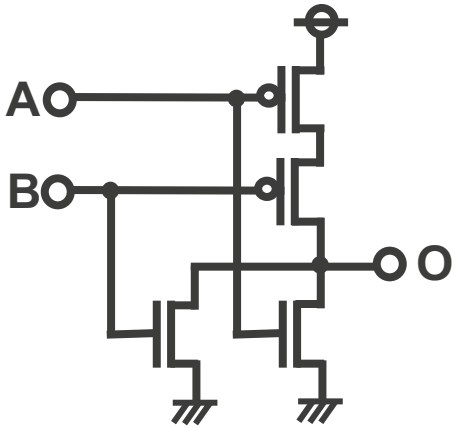
- 2 input NAND ($O=\overline{A \cdot B}$)



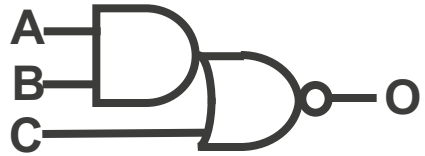


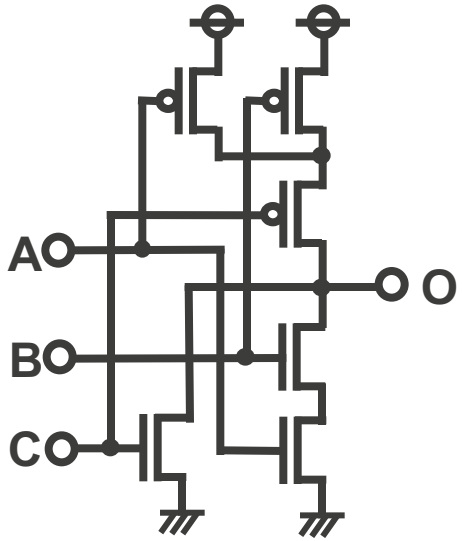
- 2 input NOR ($O=\overline{A+B}$)





- Combinational gate ($O=\overline{A \cdot B+C}$)

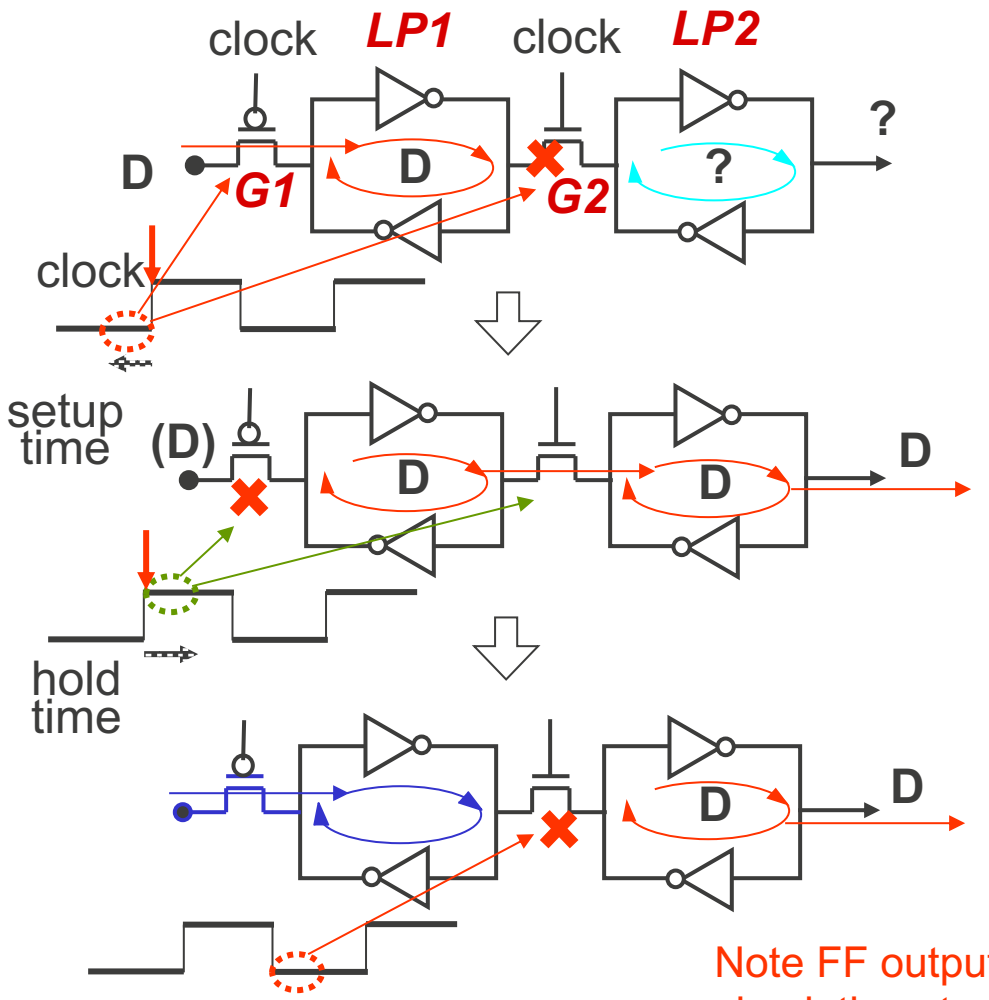




- With complementary transistor configurations, all logic circuits can be implemented.
- Basically their complementary operations are similar to those of an inverter.

Flip Flops

Principle of operation



1. Gate G1 is ON while clock remains low, and data D is taken into loop LP1.

2. When clock rises, G1 is OFF and G2 is ON to pass data D into next loop LP2.

3. When clock goes low, G2 is OFF and LP2 keeps its data D.

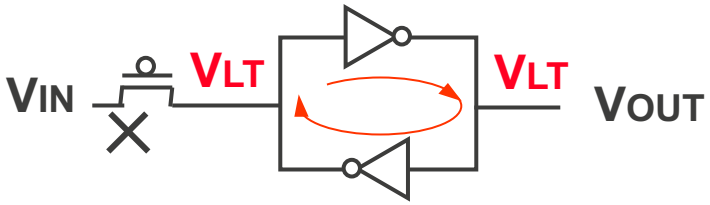
Note FF output is not determined until any value is set from outside from logic simulation standpoint. Especially cares should be taken after power on.

Flip Flops

Metastable State (Metastability)

- To set logical threshold voltage (V_{LT}) of each GATE at the same level is important to secure noise margin: V_{LT} = 1/2 V_{DD}.

- But big problem in FLIP FLOPs.



- When input V_{IN} is held at V_{LT} and then gate becomes OFF, the flip flop MIGHT may keep this level for unpredictable period.

- But actually when small plus noise is applied to left node of loop, V_{OUT} accordingly becomes 0. In minus case, Vout goes to 1.

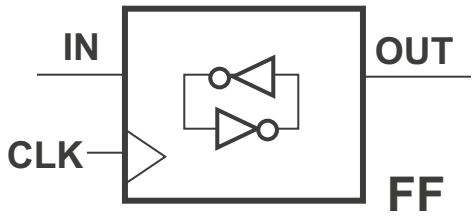
- Behavior of V_{OUT} is not predictable depending upon noise level: metastable.

< hypothetical case >

Flip Flops

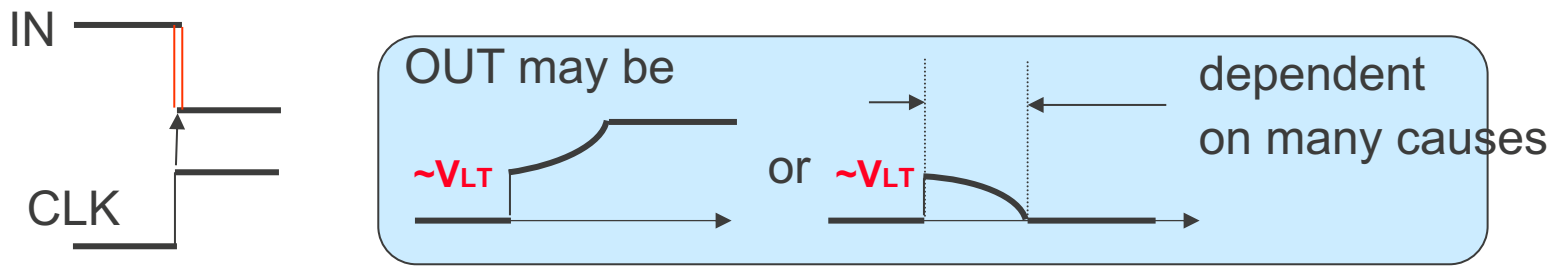
Metastable State (Metastability)

< actual case >



When falling edge of IN and rising edge of CLK are very close, voltages at inverter loop within FF become close to V_{LT} depending on timing of IN.

Succeeding behavior is unpredictable.

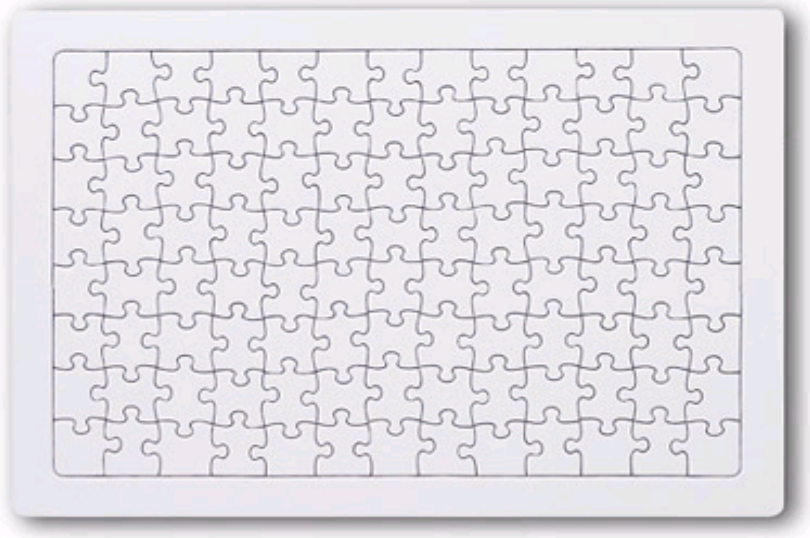


This phenomenon surely happens when IN is asynchronous with CLK. OUT must be sensed at least one clock cycle after CLK rising edge under focusing.

SoC Design and Jigsaw Puzzle

- **Jigsaw puzzle:**
  assemble whole picture from many of interlocking pieces.

- **SoC design:**
  assemble whole chip from components (cells) in circuits libraries, place and route them, so that they function harmoniously.



1. **Logic Cell library**
2. **Memory library**
3. **Analog Circuit library**

Circuit libraries on SoC

1. **Logic cell library**
   - Primitive cells (Inverter, Buffer, NAND, NOR, FF, etc.)
   - Data Path (Execution unit, selector, multiple-bit width)
   - Clock Buffer
   - Power Control Circuits (Power Switch, Substrate Bias Controller)

2. **Memory library**
   - Register File
   - RAM (Random Access Memory)
   - ROM (Read Only Memory)

3. **Analog Circuit library**
   - IO (Input and Output Buffer, Level Shifter)
   - PLL (Phased Locked Loop)
   - ADC (Analog to Digital Converter)
   - RF (Radio Frequency Circuit)
   - PA (Power Amplifier)

2.3 Electronic Signal Propagation on Silicon

Ideal wiring

Resistance(R) = 0
No signal attenuation.

Capacitance(C) = 0
Voltage can change at once

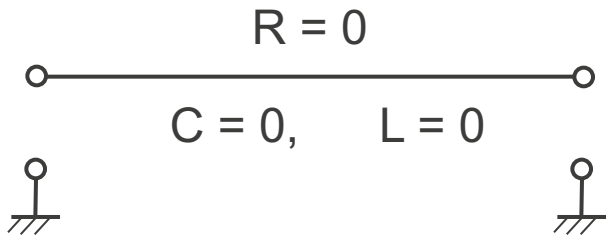
Reactance(L) = 0
Electric current can change at once

Actual wiring on the silicon

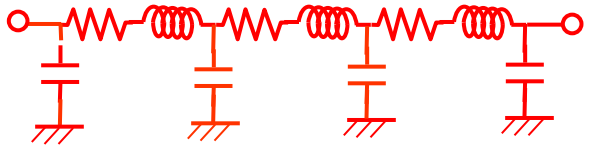
R ≠ 0
Voltage drops with current.
Power consumption.

C ≠ 0
Voltage cannot jump up or down

L ≠ 0
Current cannot jump up or down.

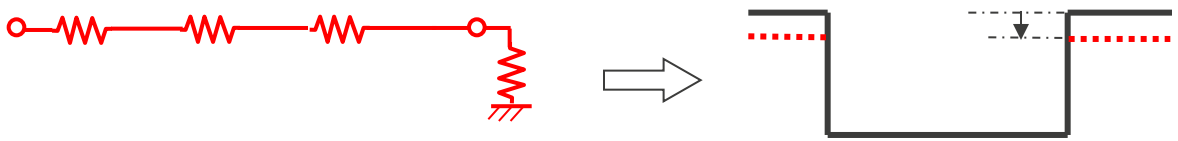


The ideal wire



Circuit model

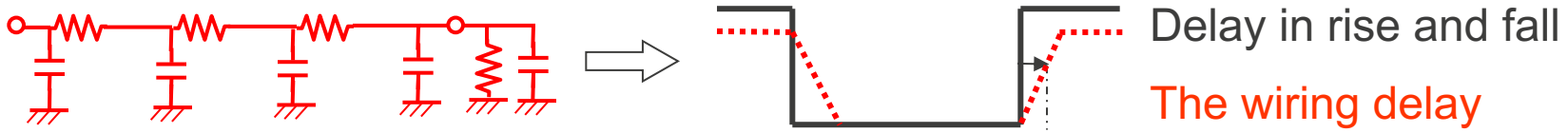
Effect of R, C and L



Voltage drop by R

The IR drop

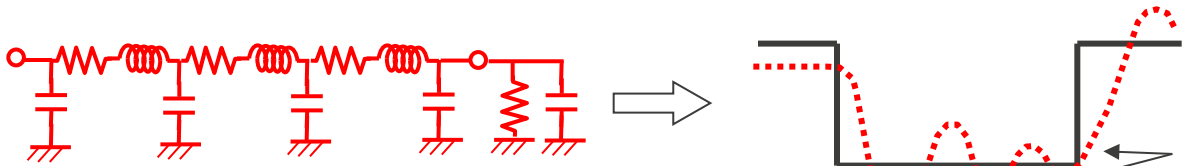
The effect of R



Delay in rise and fall

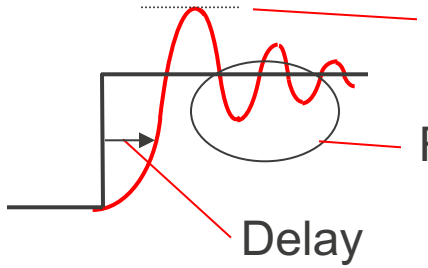
The wiring delay

The effect of C



Oscillation,
Delay increased

The effect of L



The actual waveform is more complicated.

Delay definitions

Logic delay through a gate is conveniently described by the propagation delay time, t_p. This is average time needed for the output to respond to a change in the input logic state:

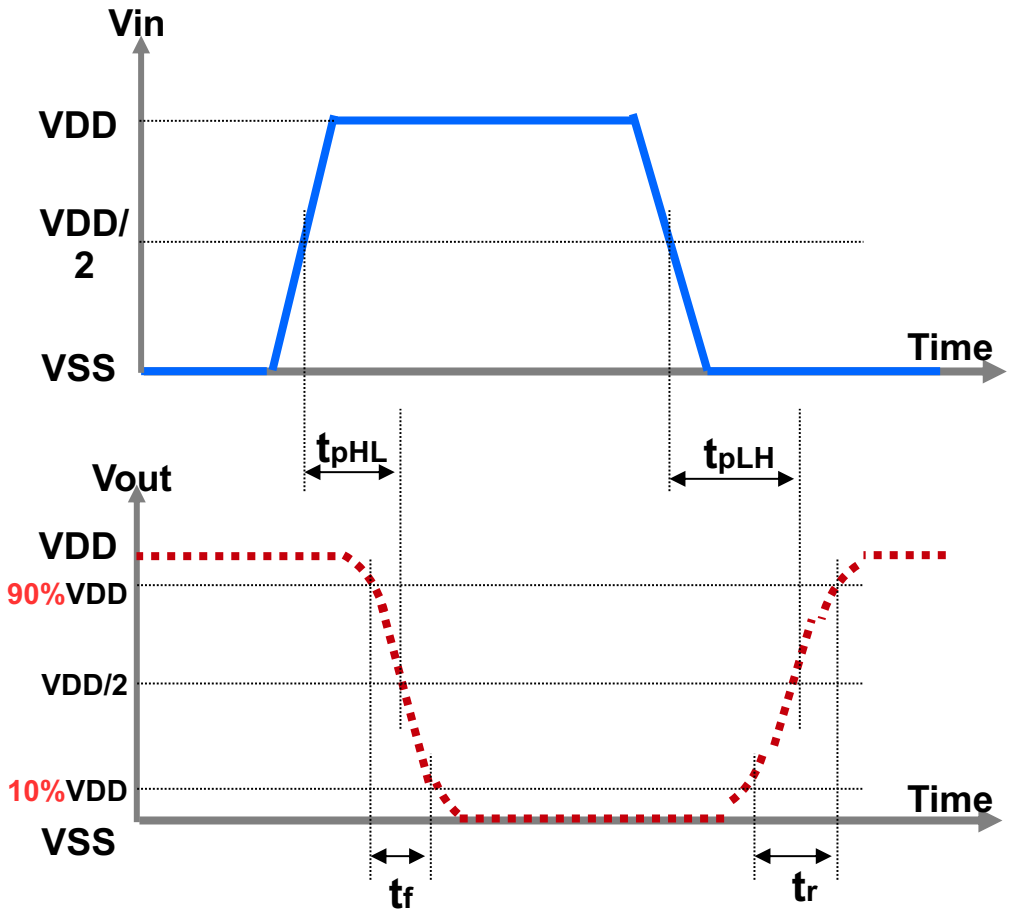
$$t_p = \frac{1}{2}(t_{pHL} + t_{pLH})$$

Falling propagation delay (t_{pHL}):
Time for output to fall by 50% of V_{DD} references to input changes by 50% of V_{DD}.

Rising propagation delay (t_{pLH}):
Time for output to rise by 50% of V_{DD} references to input changes by 50% of V_{DD}

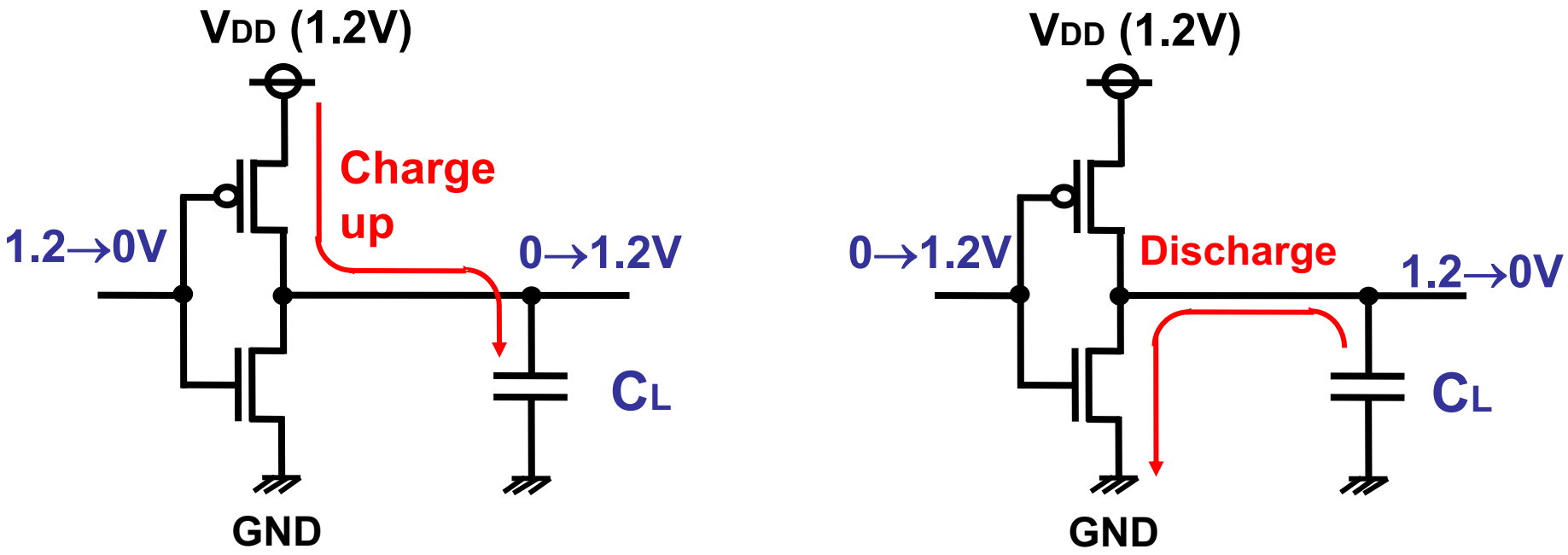
Fall time (t_f):
Time for output to fall from logical level "1" to level "0".

Rise time (t_r):
Time for output to rise from logical level "0" to level "1".



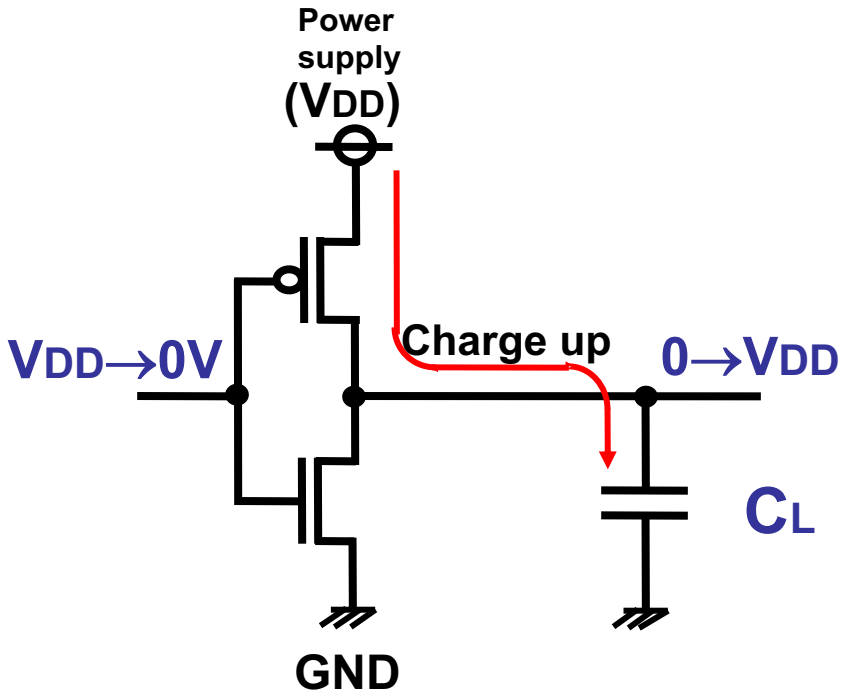
Logical level:
- Level "0": from V_{SS} to 10% of V_{DD};
- Level "1": from 90% of V_{DD} to V_{DD}.

Charge up & Discharge



Rise time and fall time: times required to charge or discharge the load capacitor.
Large load capacitance results in large delay.

Rise time - Delay of charge up



Note: Assume at initial state, C_L was fully dis-charged to 0V

- Current flows when pMOS is ON,

$$I_s = |I_{ds}| = (\beta_p/2)\cdot (V_{DD} - |V_{thp}|)^2$$

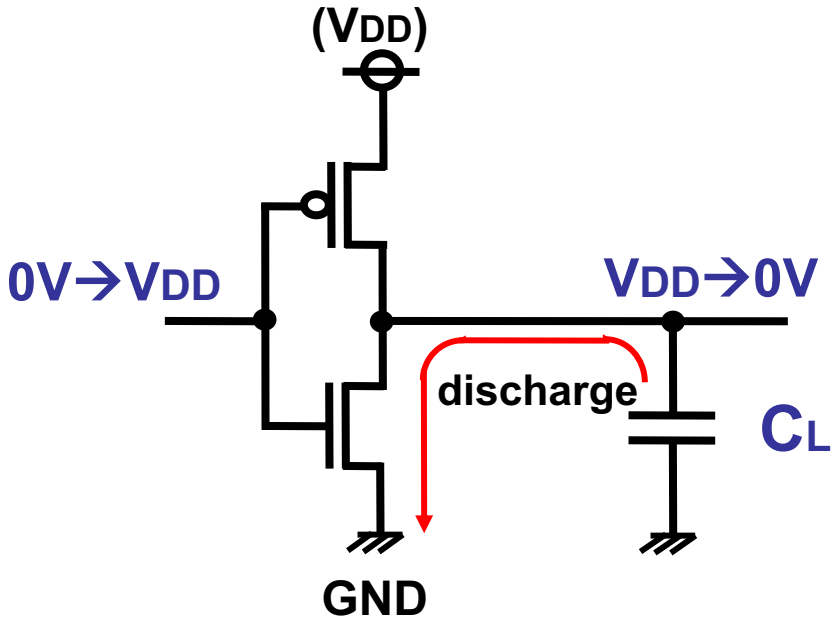
- Electric charge to be charged

$$Q = C_L \cdot V_{DD}$$

Rise time is:

$$t_r = Q/|I_{ds}| = \frac{C_L \cdot V_{DD}}{(\beta_p/2)\cdot (V_{DD}-|V_{thp}|)^2}$$

Fall time - Delay for discharge



Note: Assume at initial state, C_L was fully charged to V_{DD}

♦ **Current flows when nMOS is ON,**

$$I_{ds} = (\beta_n/2)\cdot(V_{DD}-V_{thn})^2$$

♦ **Electric charge to be discharged**

$$Q = C_L \cdot V_{DD}$$

Fall time is:

$$t_f = Q/I_{ds}$$

$$= \frac{C_L \cdot V_{DD}}{(\beta_n/2)\cdot(V_{DD}-V_{thn})^2}$$

Summary of delay time

$$\text{Delay time} = \begin{cases} \dfrac{C_L \cdot V_{DD}}{(\beta_p/2)\cdot(V_{DD}-|V_{thp}|)^2} & \text{: rise time} \\ \dfrac{C_L \cdot V_{DD}}{(\beta_n/2)\cdot(V_{DD}-V_{thn})^2} & \text{: fall time} \end{cases}$$

$\beta = \mu * C_{ox} * W/L$ ⇒

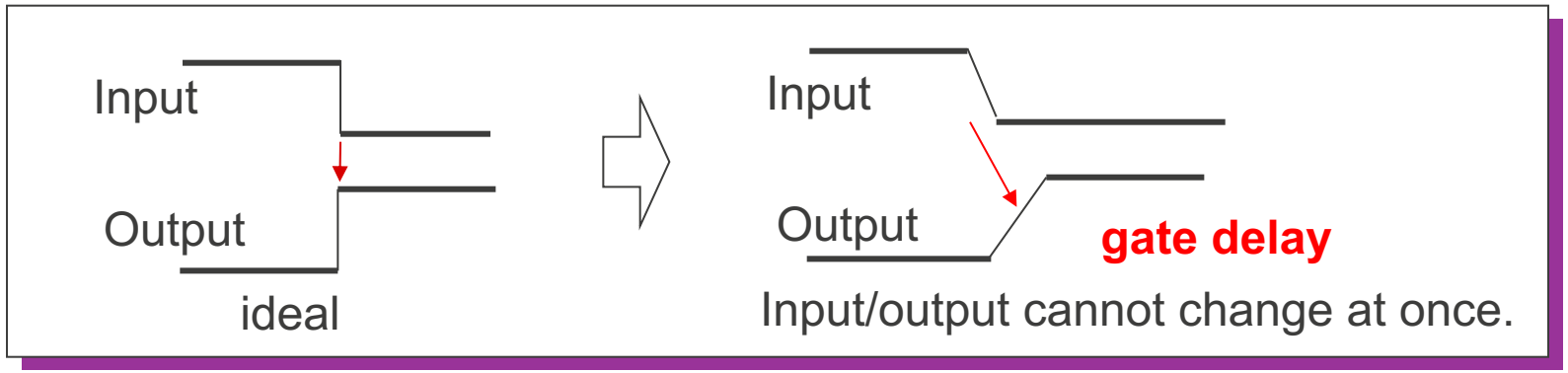
- Faster, if gate length L is shorter
- Faster, if gate width W is wider

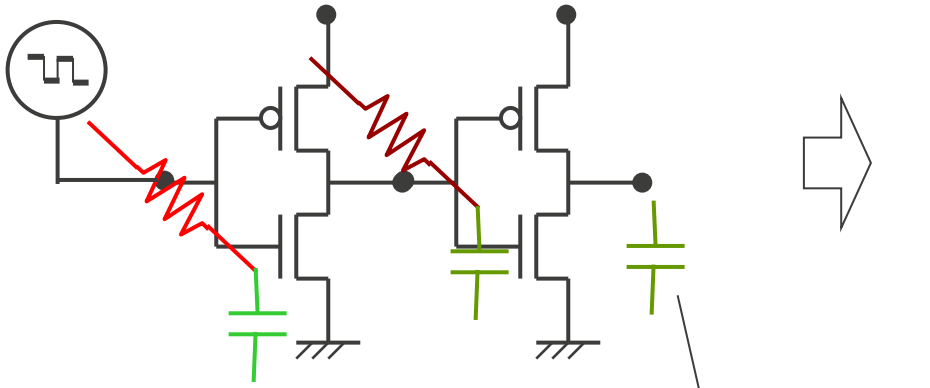
Mobility

Capacity of gate oxide per unit area

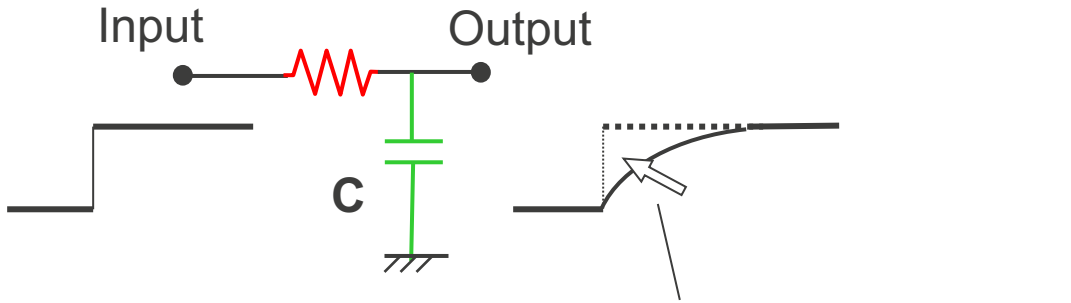
2.4 Problem with Electronic Signal

Gate Delay & Wiring Delay





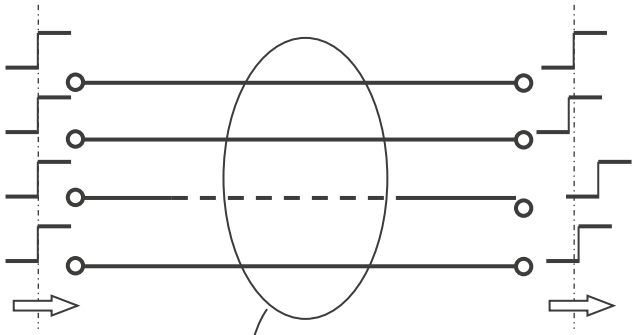
The capacity of the wiring to the next gate



Countermeasures for reducing delay

- Reduction of the resistance
- Reduction of the capacitance
- Larger driving force

Skew



Input all the signal at the same time.

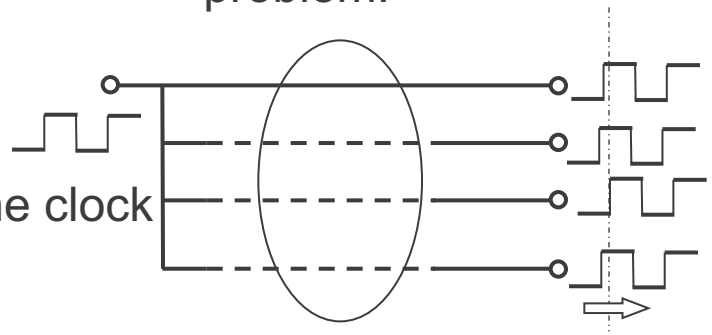
Arriving at each destination at different times.

These lines have different electrical (R, C, L) characteristics.

skew

For more-than-1-bit signal, skew is always a big problem.

Clock signal will always suffer from skew problem.

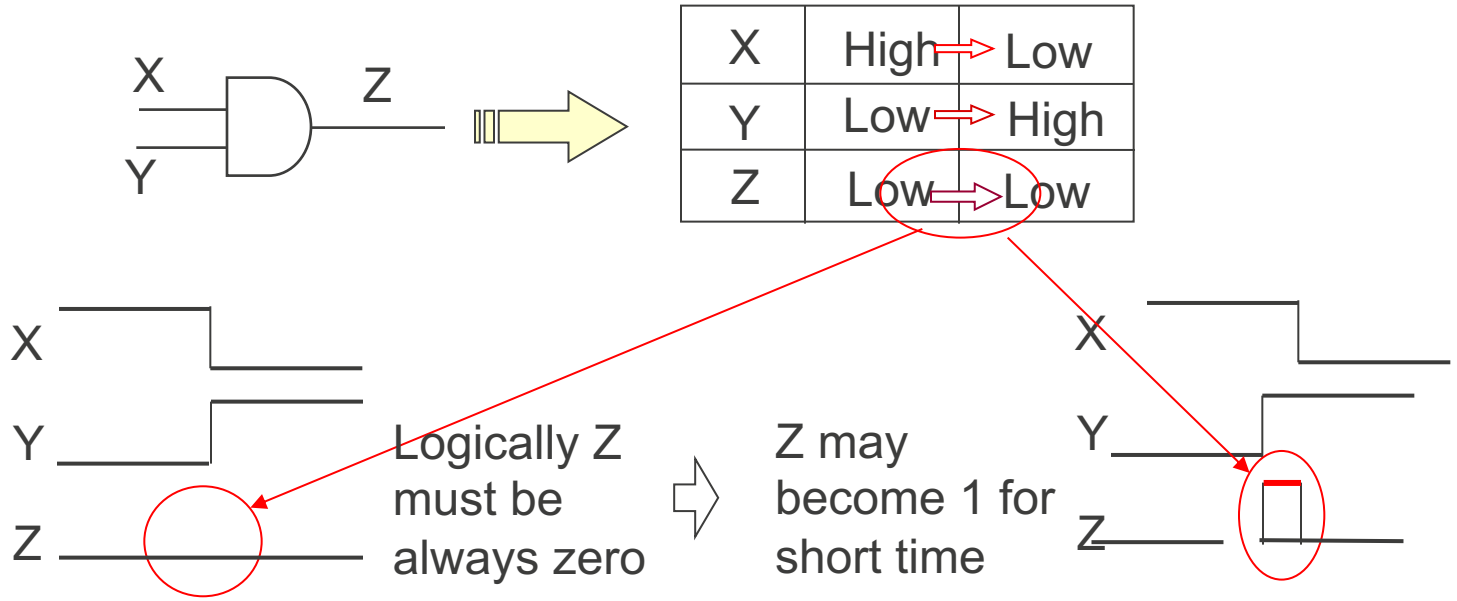


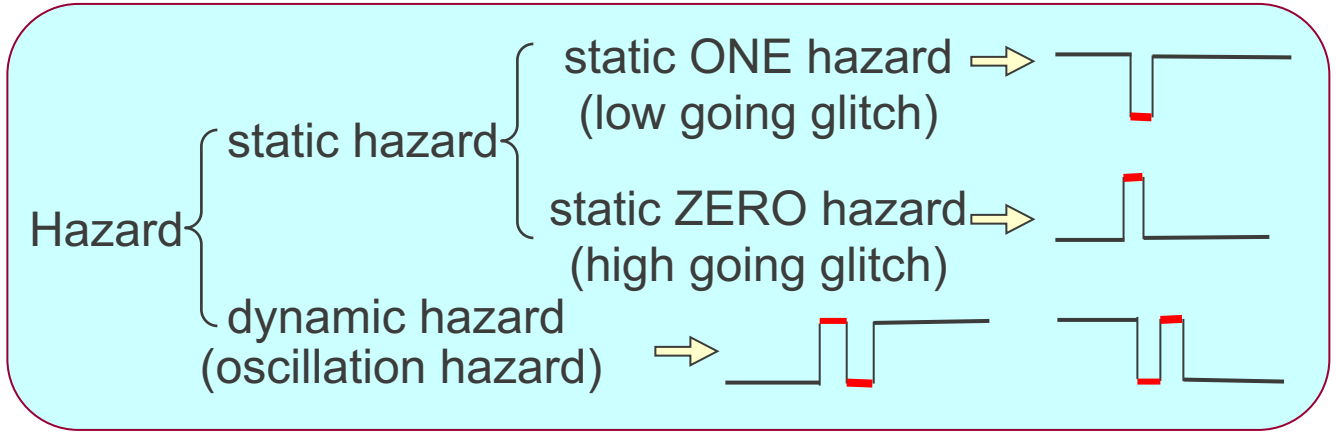
The clock skew

Skew causes difficulty in wiring clock lines, especially in higher frequency range and limits the clock speed.

Hazard & Glitch

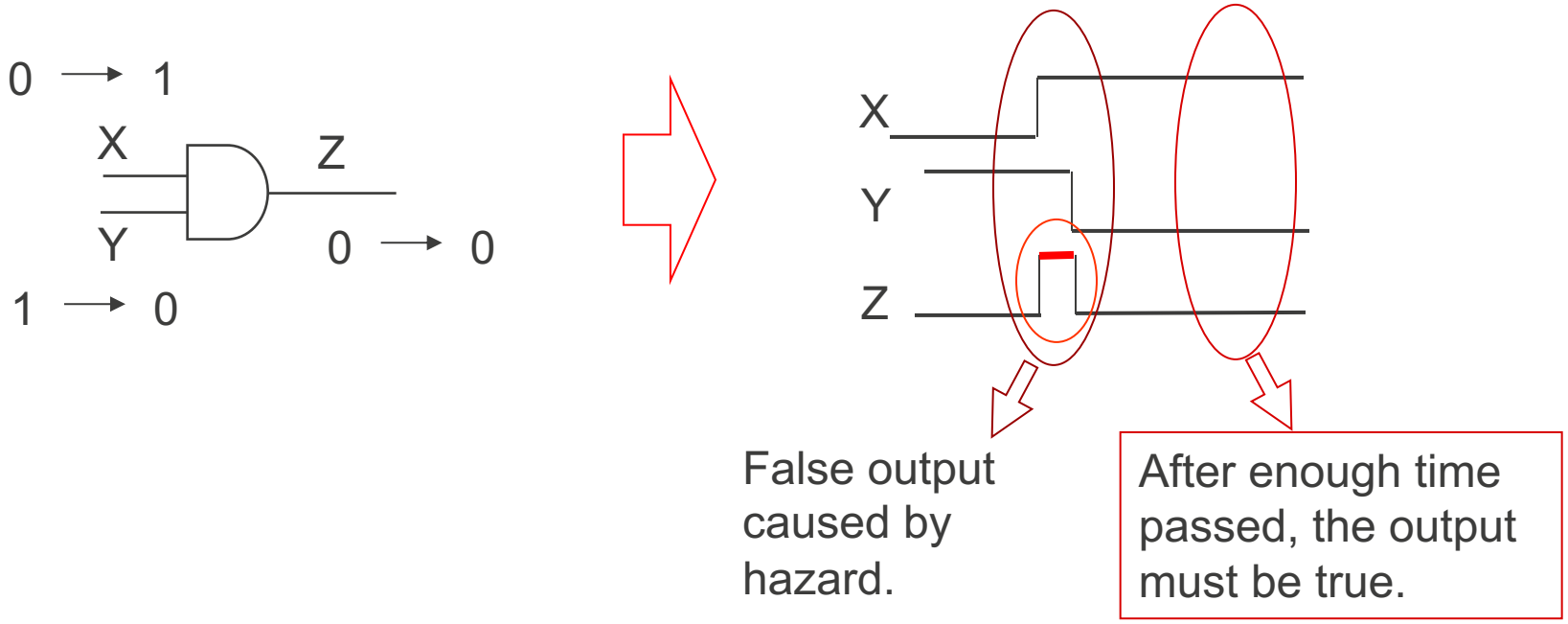
Hazard is a problem caused by a small timing difference among several signals.





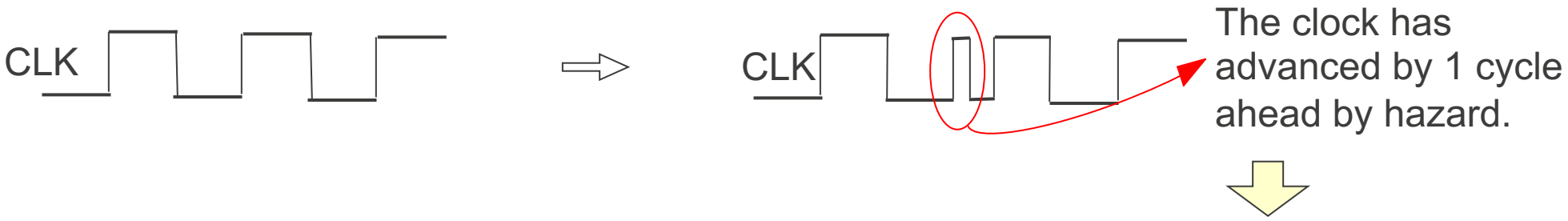
How to avoid hazard?

It is difficult to prevent hazard. However, we can avoid using hazard signal by selecting a timing to use the signal.



To avoid hazard, outputs of combinational logic must be used after proper time period passed since input signals become stable.

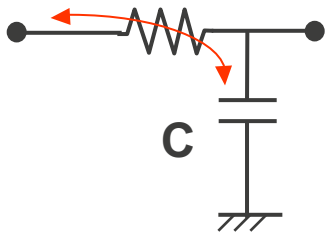
When handling edge signal, you must be very careful about hazard, because edge signal is very sensitive to hazard. Especially, clock signal is very sensitive to hazard.



Hazard cause big problems resulting in malfunction of a system. Synchronous design may help us to get out of these problems.

To avoid hazard on clock signal, do not insert any combinational logic in clock line.

Power Consumption



Electric power ~ V.I ~ V.Q/T ~ V.CV/T

~ $C.V^2/T$

~ $f.C.V^2$

The power consumption of CMOS

$P \sim f.C.V^2$

Dynamic power

The keys to reduce power consumption.

<1> Making operation voltage low

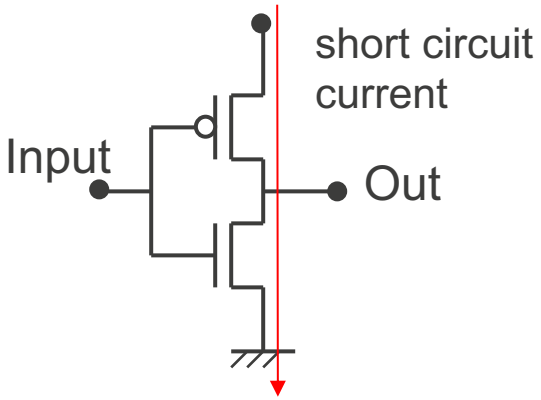
<2> Lowering an operating frequency.

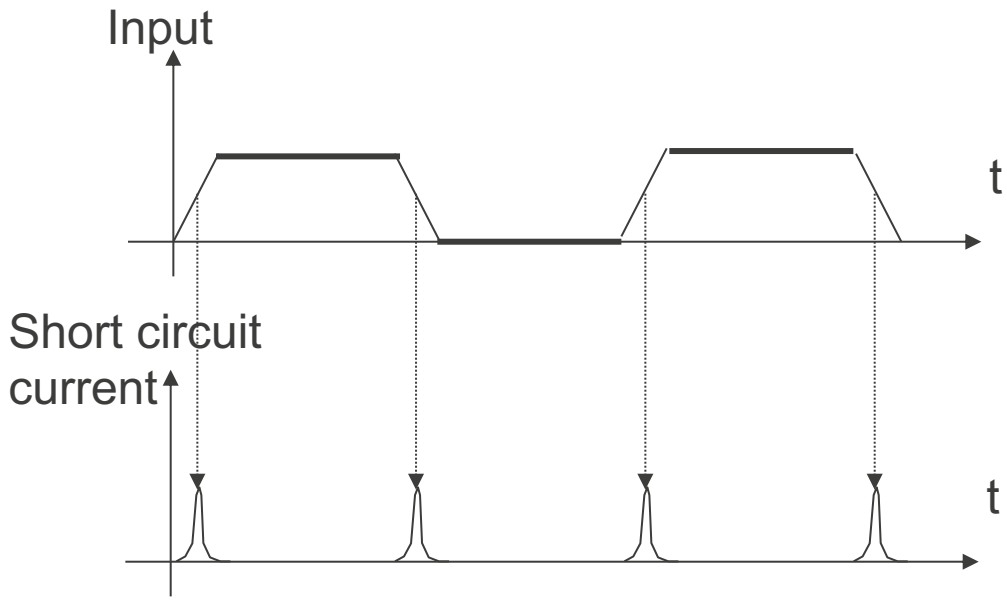
<3> Reducing capacitance and so on.

Power consumption limits the operating speed. Large power consumption makes it difficult to design packages.

However, the leakage current is becoming significant, we have to apply partial power off strategy to reduce power significantly.

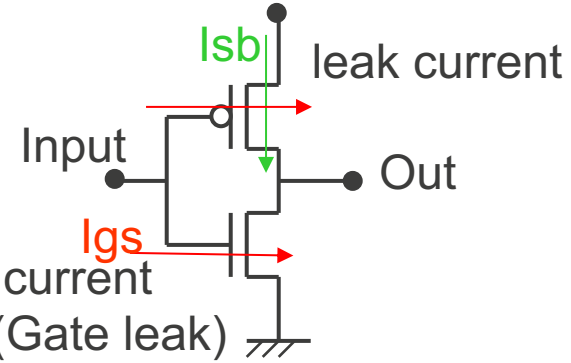
Short Circuit Power





Power consumption by short circuit current is about less than10 to 15% of the total power consumption

Leak Current



Devices with large leak current are not applicable to battery powered products.

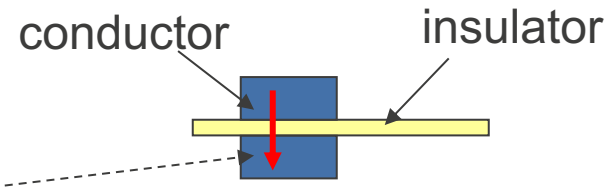
Gate size shrink and low voltage operation

⇩

Thinner gate insulator

⇩

The increase of the gate leak by the tunnel current

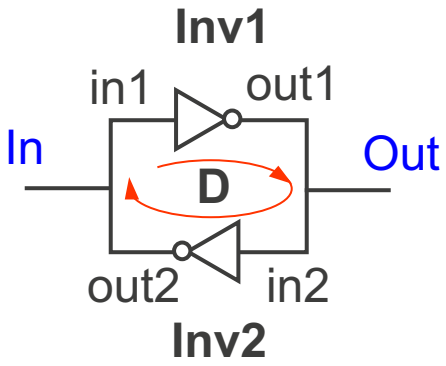


⇩

Counter measure ⇨ High K material
Partial power-off

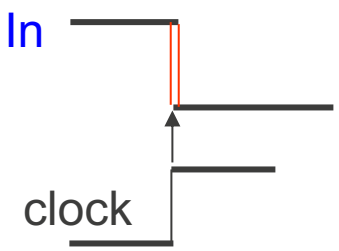
dielectric constant,
or electric permittivity

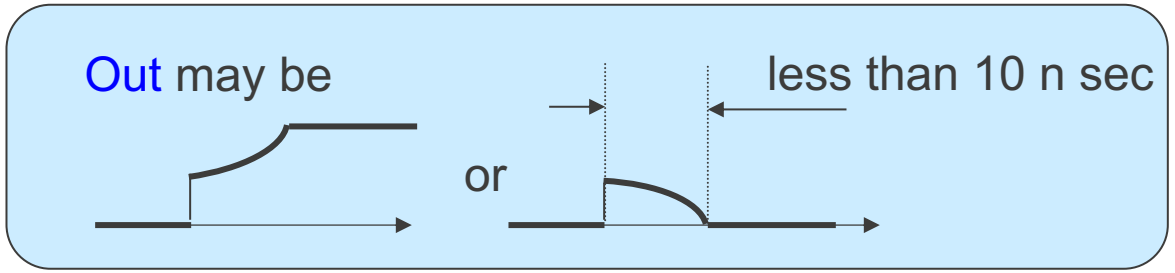
Metastability of Flip-Flop



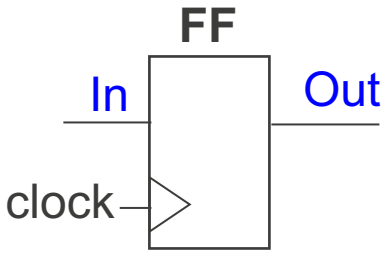
If In is given a value, such as mean value of low and high voltage, Out becomes unstable for some period and we can not tell what the final value shall be.

This is called “metastability”.



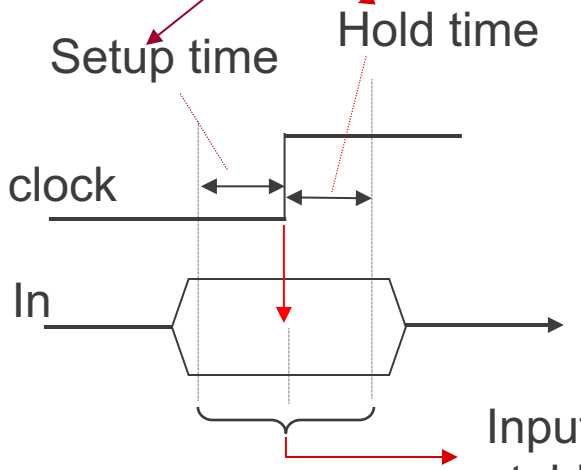


We cannot predict the result.



This may happen when input signal changes at the instant of the clock pulse.

In many cases, metastability can be avoided by ensuring that inputs are held constant for specified periods before and after the clock pulse.



If input signal changes during Setup and Hold time, metastability will occur.

Input data must be stable during this period.

In synchronous design, by applying STA, we can avoid metastability of FFs.

Typical Setup time or Hold time is less than 100 p sec.

Unknown initial value of Flip-Flop

We can not tell the value of FF right after power on. (How about SRAM?)

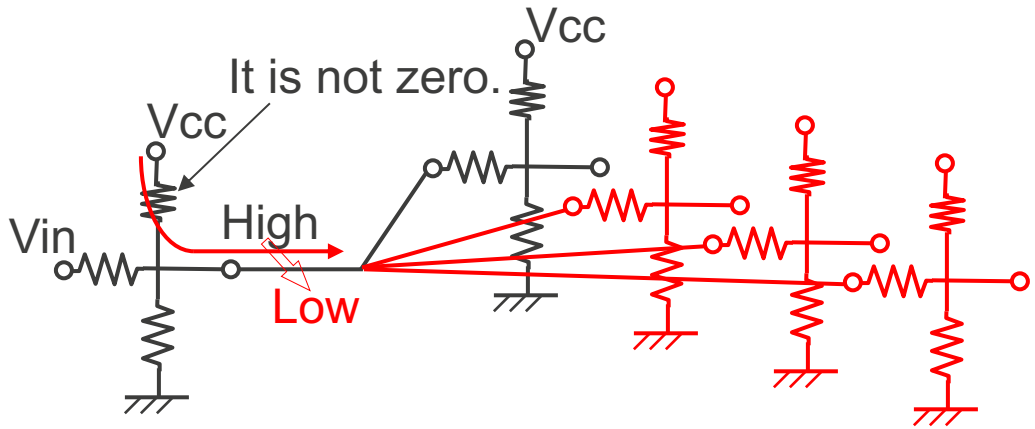
⇒ The output signal of FFs must be used after proper initialization sequence.

⇒ Many problems caused by unknown initial value of FF have been experienced. Pay special attention to this issue whenever you use FFs (or SRAM).

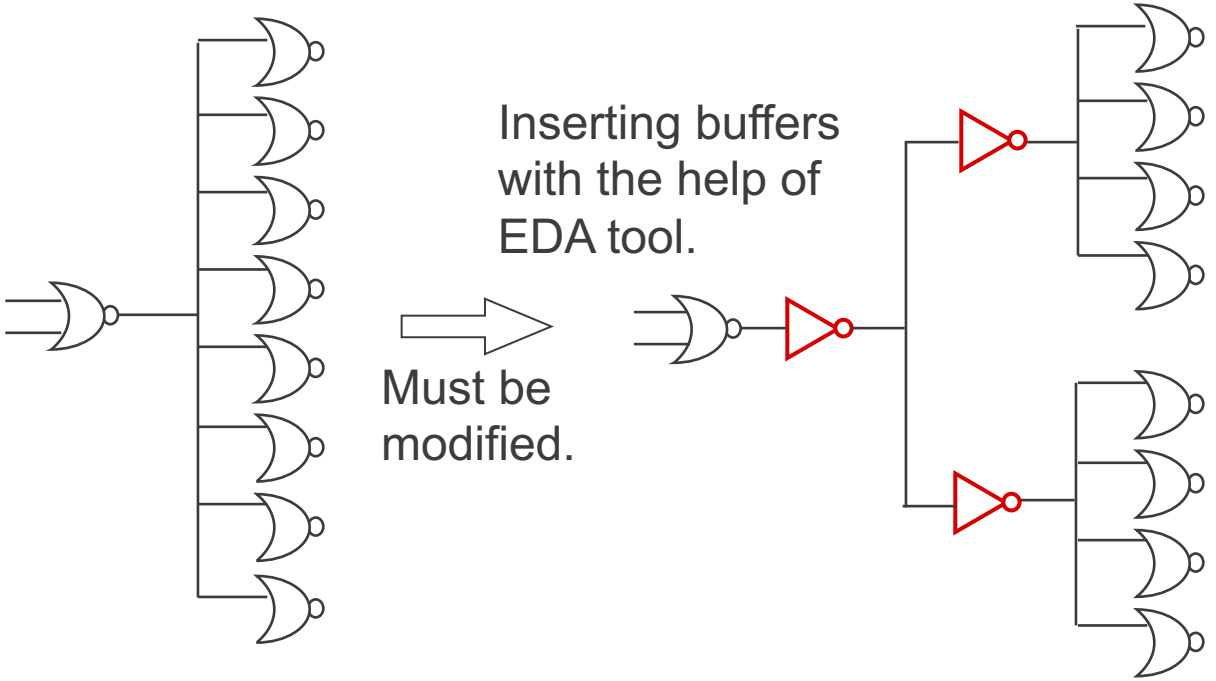
If a logic you designed uses the unknown initial values of FFs in a way that they cause unexpected operation, it means you have implemented a logic bug.

Fan-out

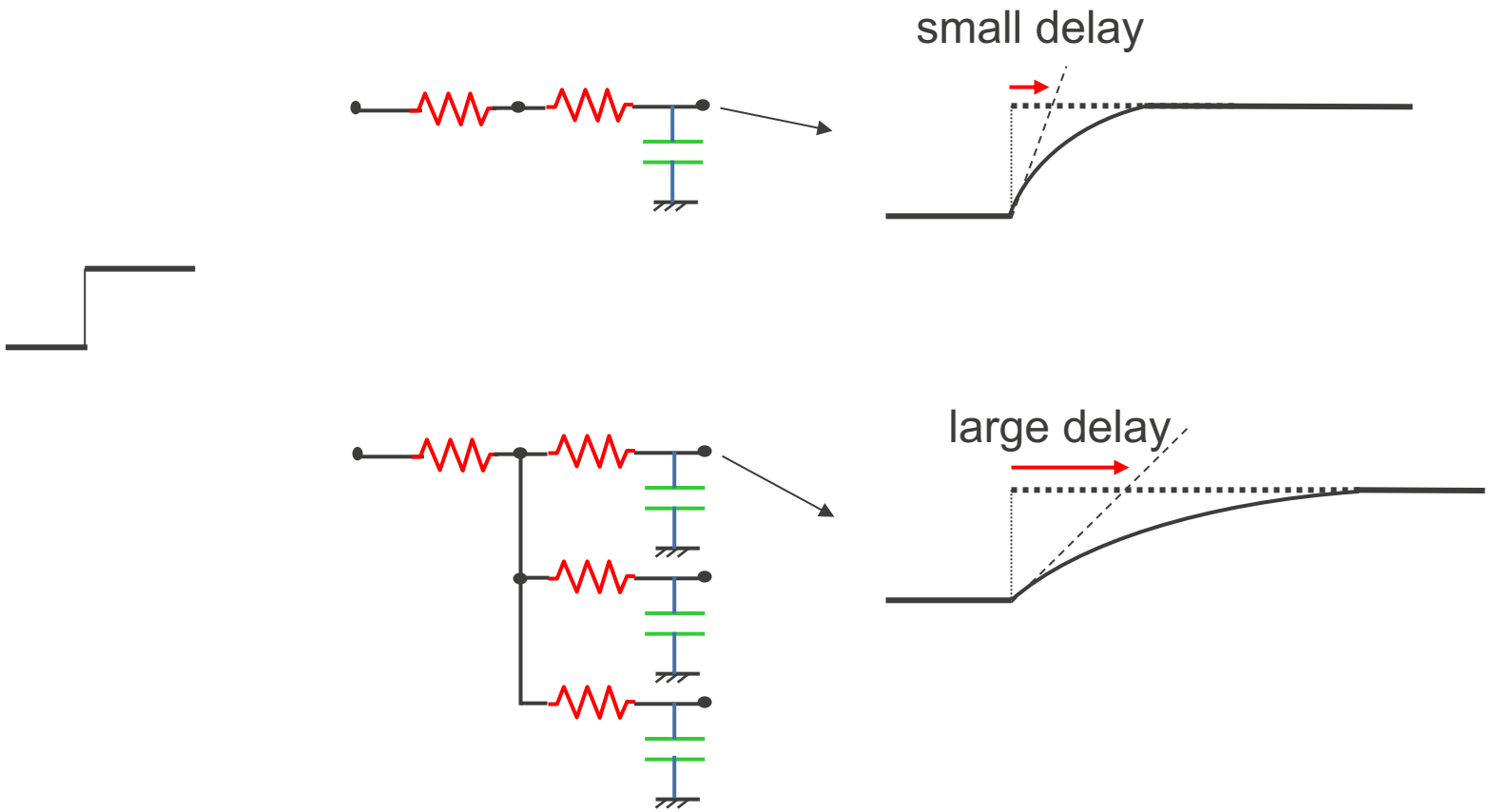
Because of output voltage drop, there is a limitation (fan-out) in the number of the circuits which can be connected to an output.



Fan-out problem causes malfunction of the circuits. EDA tools can help us to avoid this problem.

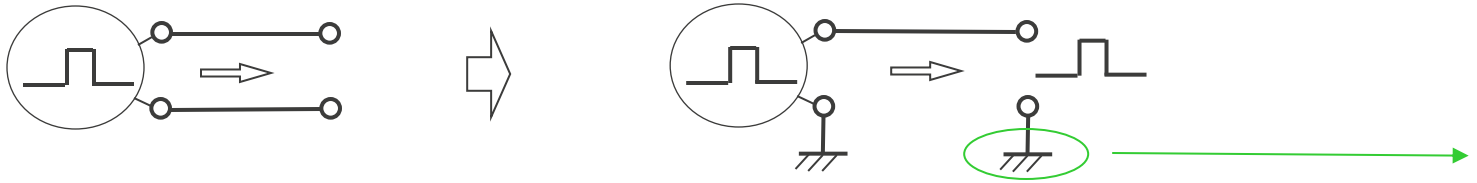


Because larger load result in larger delay as shown below, fan out issue is also related to speed.



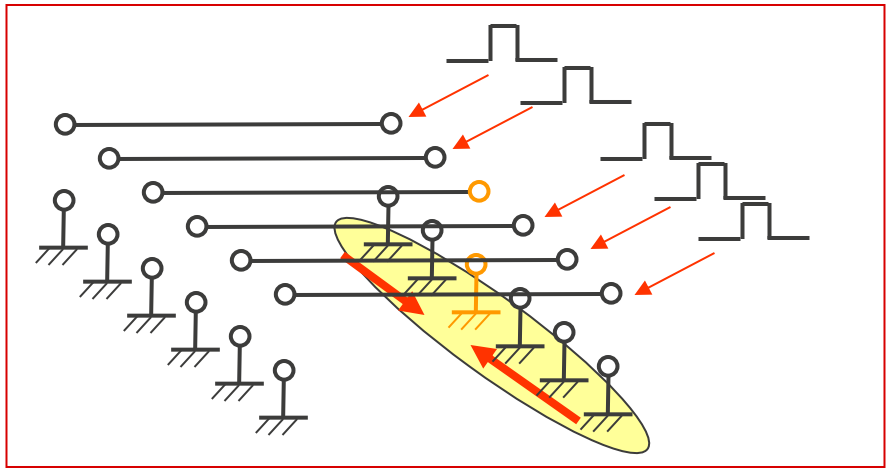
Sometimes delay of N stage gate logic is larger than that of having more stages gate logic if some gates have larger load.

Ground bounce



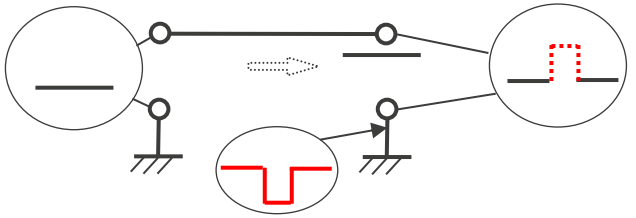
Cannot keep the potential of the ground at zero when there is a large current in the neighborhood.

Sharing the ground with other signals



Simultaneous signal change and ground bounce

A false signal can be observed when the potential of the ground is shaken by the other signal.



Ground bounce

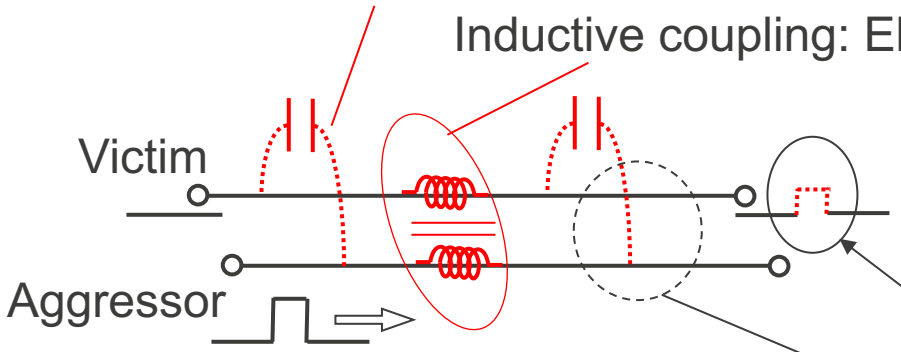
Ground bounce creates false signal on certain signal line, thus sometimes causes a malfunction of a device.

Cross talk

Capacitive coupling: Electrostatic induction

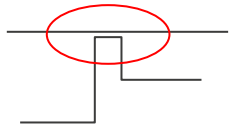
Inductive coupling: Electromagnetic induction

⇨ Cross talk



The signal, different from the input, appears at the other end of the line.

.5 mm will cause a big problem



Signal Integrity

IR Drop: Voltage drop proportional to the current.

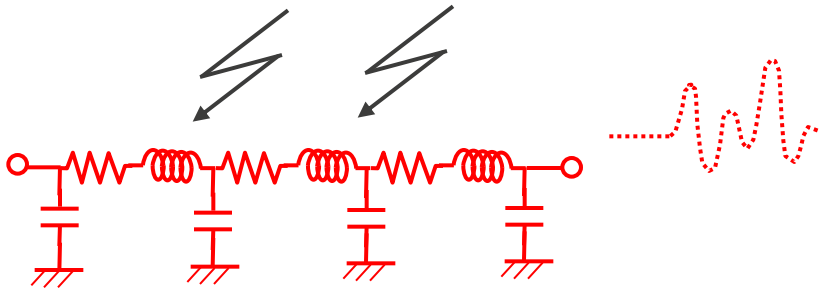
Cross talk: Wrong signal detected by the influence of the neighboring wire.

⇨ Cross talk creates false signal on certain signal line, thus sometimes causes a malfunction of a device.

⇨ IR drop creates insufficient power supply to certain circuit on silicon and limit miniaturization and operating frequency.

EMC/EMI

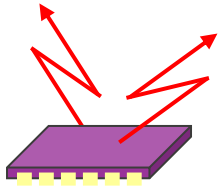
Electromagnetic pulse



Electromagnetic pulse

False signal will be observed caused by the electromagnetic disturbance.

Electromagnetic emission

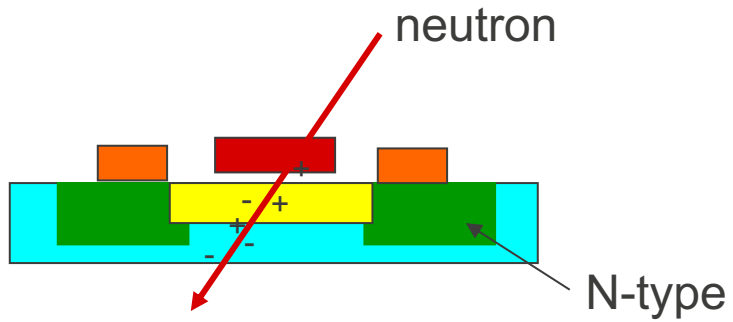


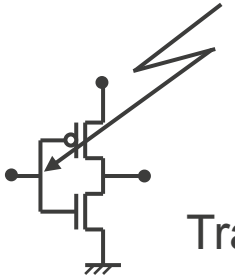
- EMI: Electromagnetic Interference
- EMS: Electromagnetic Sustainability
- EMC: Electromagnetic Compatibility

Electromagnetic interference may creates false signal on certain signal line, thus sometimes causes a malfunction of a device.
It becomes difficult to comply with EMC guide lines as operating frequency of devices goes high.

Radiation from the package and cosmic ray

The influence of neutron radiation and so on, are becoming significant.



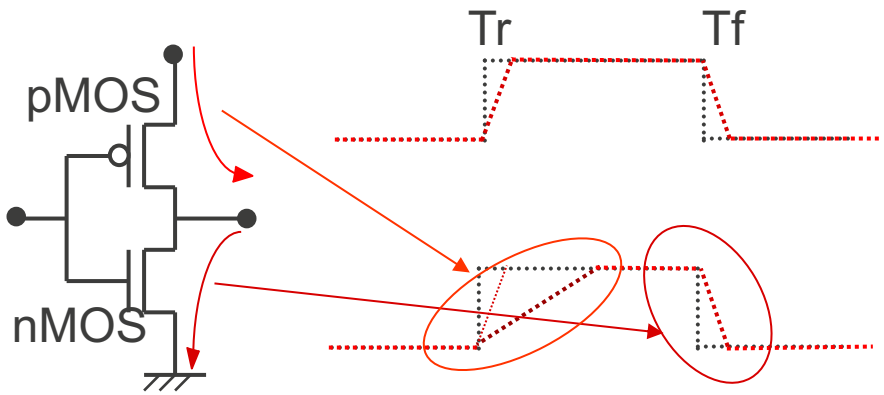


Alpha ray, gamma ray and neutron radiation

Transistor malfunctions caused by the radiation

Large scale memory can not avoid this problem, therefore some error correction system is necessary for such large scale memory.

The different characteristic of nMOS & pMOS



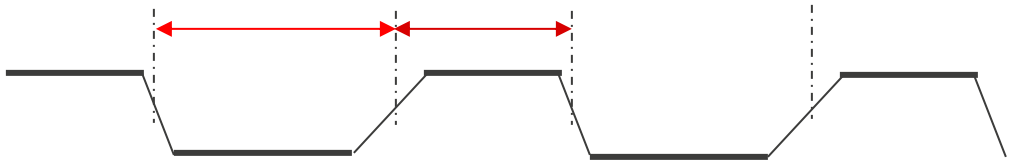
When the driving power of n/p MOS are the same

In case of N > P

Generally, nMOS has a bigger driving capability

The rising becomes gentle because the driving power of pMOS is weak.

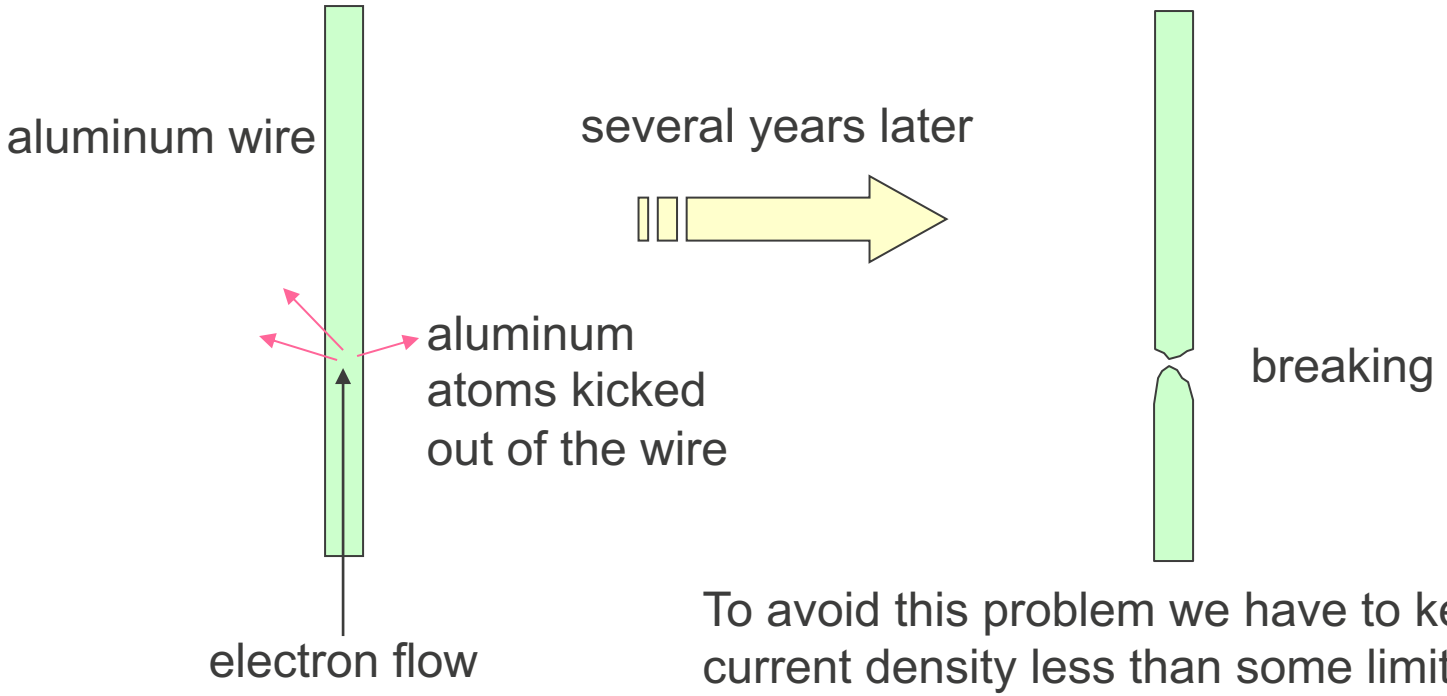
It becomes difficult to keep the duty ratio of on/off such as the clock at 50%.



Clock skew problem may become critical when inserting a buffer into the clock line.

Electron migration

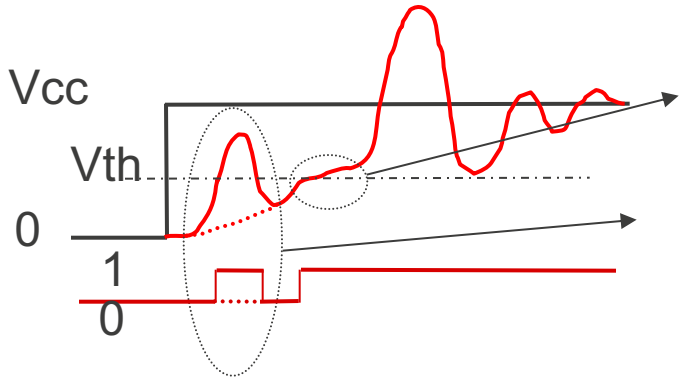
Atoms of wire material, aluminum or copper, are kicked out of the wire line by electrons. This sometimes causes a breaking of wire.



To avoid this problem we have to keep current density less than some limitation.

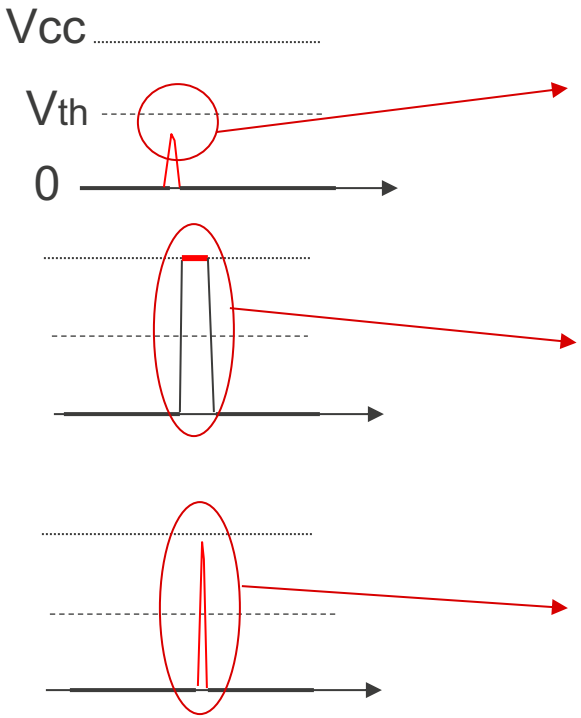
Some DA tool can give us warning that there may be electron migration problem.

Other issues



Slow rising of the input voltage around the Vth. ⇨ Over current of MOS

Ringing of the input voltage around the Vth. ⇨ False signal



Runt pulse: a narrow pulse which does not reach a valid high or low level

Glitch: a pulse shorter than the specified minimum

Spike: a short pulse similar to glitch but often caused by ringing or cross talk.

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