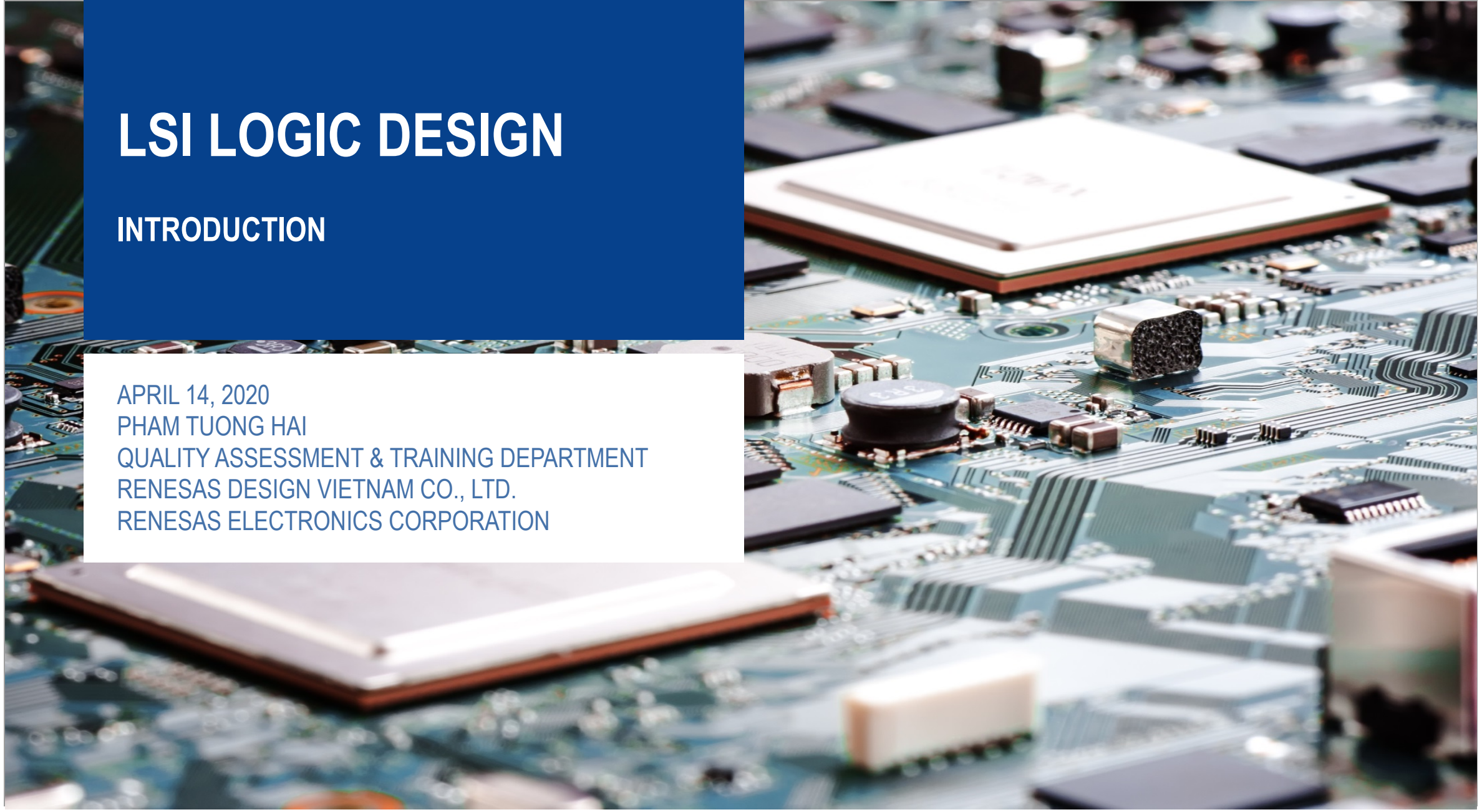
LSI LOGIC DESIGN

INTRODUCTION



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PHAM TUONG HAI
QUALITY ASSESSMENT & TRAINING DEPARTMENT
RENESAS DESIGN VIETNAM CO., LTD.
RENESAS ELECTRONICS CORPORATION

SELF-INTRODUCTION

- **Name**: Pham Tuong Hai.
- **1981 - 1986**: Bachelor degree of EE Engineering, HCMUT.
- **1986 - 1993**: Computer Center, HCMUT.
- **1993 - 1998**: Master, PhD degree of Fundamental Informatics & Parallelism, Université Toulouse III - Paul Sabatier.
- **1998 - 2008**: Faculty of Computer Science and Engineering, HCMUT.
- **2008 - Present**: Renesas Design Vietnam Co., Ltd.

THE SUBJECT TARGETS

- **Purpose of the subject**

  Train the fundamental technical, technological knowledge and skills to fresh engineers who join into the LSI design project.

- **Aims**

  - Introduce the whole picture of the semiconductor business and related terminology.
  - Comprehend the LSI development methodology/flow applied in industry.
  - Comprehend/practice the background and the details in each major phases of the LSI design.
  - Convey the thinking way and the working behavior of an professional engineer to audience.

- **Intended audience**

  - Students who have the background of Digital Design, RTL Design (Verilog or VHDL).

CONTENTS OF LECTURE PART

- **Chapter 1**. Introduction to LSI development.
- **Chapter 2**. Logic elements and electronic signal on silicon.
- **Chapter 3**. LSI logic design.
- **Chapter 4**. Synchronous design.
- **Chapter 5**. Design for testability (DFT).
- **Chapter 6**. Layout design.

CONTENTS OF LECTURE PART

- **Chapter 1**. Introduction to LSI development.
  1. 1.1. Semiconductor products
  2. 1.2. LSI Development flow
  3. 1.3. LSI Design flow and methodologies
  4. 1.4. An example
- **Chapter 4**. Synchronous design.
- **Chapter 5**. Design for testability (DFT).
- **Chapter 6**. Layout design.

CONTENTS OF LECTURE PART

- **Chapter 1**. Introduction to LSI development.
- **Chapter 2**. Logic elements and electronic signal on silicon.
  - 2.1. Digital logic and CMOS circuit
  - 2.2. Logic gate on silicon
  - 2.3. Electronic signal propagation on silicon
  - 2.4. Problem with electronic signal
- **Chapt**
- **Chapt**
- **Chapter 5**. Design for testability (DFT).
- **Chapter 6**. Layout design.

CONTENTS OF LECTURE PART

- **Chapter 1.** Introduction to LSI development.
- **Chapter 2.** Logic elements and electronic signal on silicon.
- **Chapter 3.** LSI logic design.
  - 3.1. Design and modeling
  - 3.2. RTL logic design and verification
  - 3.3. Logic synthesis and cell base design
  - 3.4. Gate level design and verification
  - 3.5. Layout design and verification

CONTENTS OF LECTURE PART

- **Chapter 1.** Introduction to LSI development.
- **Chapter 2.** Logic elements and electronic signal on silicon.
- **Chapter 3.** LSI logic design.
- **Chapter 4.** Synchronous design.
  - 4.1. Timing issue of logic data
  - 4.2. Synchronous design and Static Timing Analysis (STA)
- **Chapt**
- **Chapter 6.** Layout design.

CONTENTS OF LECTURE PART

- **Chapter 1**. Introduction to LSI development.
- **Chapter 2**. Logic elements and electronic signal on silicon.
- **Chapter 3**. LSI logic design.
- **Chapter 4**. Synchronous design.
- **Chapter 5**. Design for testability (DFT).
  - 5.1. Manufacturing defects
  - 5.2. Scan method
  - 5.3. Design flow with DFT
- **Chapt**

CONTENTS OF LECTURE PART

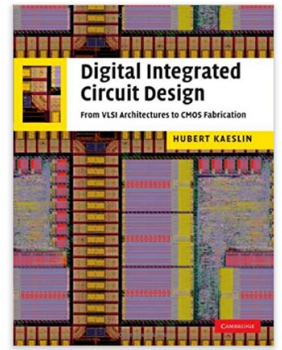
- **Chapter 1.** Introduction to LSI development.
- **Chapter 2.** Logic elements and electronic signal on silicon.
- **Chapter 3.** LSI logic design.
- **Chapter 4.** Synchronous design.
- **Chapter 5.** Design for testability (DFT).
- **Chapter 6.** Layout design.
  - 6.1. Layout design flow
  - 6.2. Design for manufacturing

CONTENTS OF LAB PART

- **Lab no. 1**. Verilog simulation, functional verification by Cadence EDA tools.
- **Lab no. 2**. Synthesis a RTL Verilog by Cadence EDA tools.
- **Lab no. 3**. Static Timing Analysis by Cadence EDA tools.
- **Lab no. 4**. Gate netlist verification, equivalence check by Cadence EDA tools.
- **Big exercise assignment** (optional).

REFERENCE

- "**Digital Integrated Circuit Design: From VLSI Architecture to CMOS Fabrication**", by Hubert Kaeslin,
  Cambridge University Press, 1st edition (April/2008).



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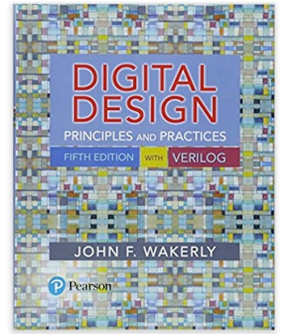
- "**Digital Design: Principles and Practices**", by John F. Wakerly,
  Pearson, 5th edition (Aug/2018).



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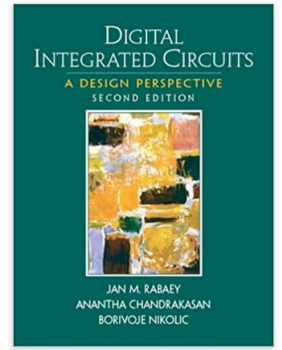
- "**Digital Integrated Circuits: A Design Perspective**", by Jan M. Rabaey,
  Pearson, 2nd edition (Jan/2003).



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