

VC Formal Lab

Automatically Extracted Property (AEP)

App Setup and Standard Usage

Learning Objectives

In this VC Formal lab, you will use a traffic light controller example to learn to do the following:

- Set up design and appmode
- Run interactively with Verdi GUI
- Review design complexity statistics and setup
- Enable AEP switch when read design
- Set up clocks and resets
- Establish initial state for formal
- Generate property
- Run checks and review results
- Debug failures
- Save and restore session
- Run in interactive shell without Verdi GUI
- Run in batch mode

Familiarity with basic formal verification concepts are required for this lab.



Lab Duration:
30 minutes

Files Location

All files for this VC Formal lab are in directory:
\$VC_STATIC_HOME/doc/vcst/examples/AEP/

Directory Structure	
AEP	Lab main directory
README_VCFormal_AEP.pdf	Lab instructions
design/	Verilog RTL code of the Device Under Test (DUT)
run/	Run directory
solution/	Solution directory

Resources

The following resources are available for in-depth guidance regarding VC Formal usage, commands, and variables.

VC Formal User Guide:

\$VC_STATIC_HOME/doc/vcst/VC_Forma_Docs/VC_Forma_UG.pdf

VC Formal Apps Quick References Guides:

\$VC_STATIC_HOME/doc/vcst/VC_Forma_Docs/Quick_Reference_Guides/

VC Formal Apps Tcl Templates:

\$VC_STATIC_HOME/doc/vcst/VC_Forma_Docs/Quick_Reference_Guides/vcf_tcl_templates/

Prepare your Environment

1. Set environment variable pointing to your VC Formal installation directory:

```
%setenv VC_STATIC_HOME /tools/synopsys/vcstatic
```

2. Add path \$VC_STATIC_HOME/bin to the PATH environment variable.
3. Change your working directory to AEP/run:

```
%cd AEP/run
```

Now you are ready to begin the lab.

Create a run.tcl Setup File

VC Formal has a Tcl-based command interface. It is common to start with a Tcl file to set up and compile a design. In this step, you will create a VC Formal Tcl file for the DUT, a traffic light controller, used in this lab.

The DUT files and filelist are located under AEP/design.

4. Open file run.tcl (any arbitrary name is ok to use) using any text editor:

```
%vi run.tcl
```

5. Add command to enable AEP App mode :

```
set_fml_appmode AEP
```

6. Specify DUT top level module name as Tcl variable:

```
set design traffic
```

7. Add command to compile DUT and SVA properties :

```
read_file -top $design -format verilog \
-vcs {-f ../design/filelist}
```

Or it can be separate into 2-step: analyze and elaborate
This is suitable for complex design or mix-language design.

```
analyze -format verilog -vcs {-f ../design/filelist}
elaborate $design
```

8. Save run.tcl file and exit editor.

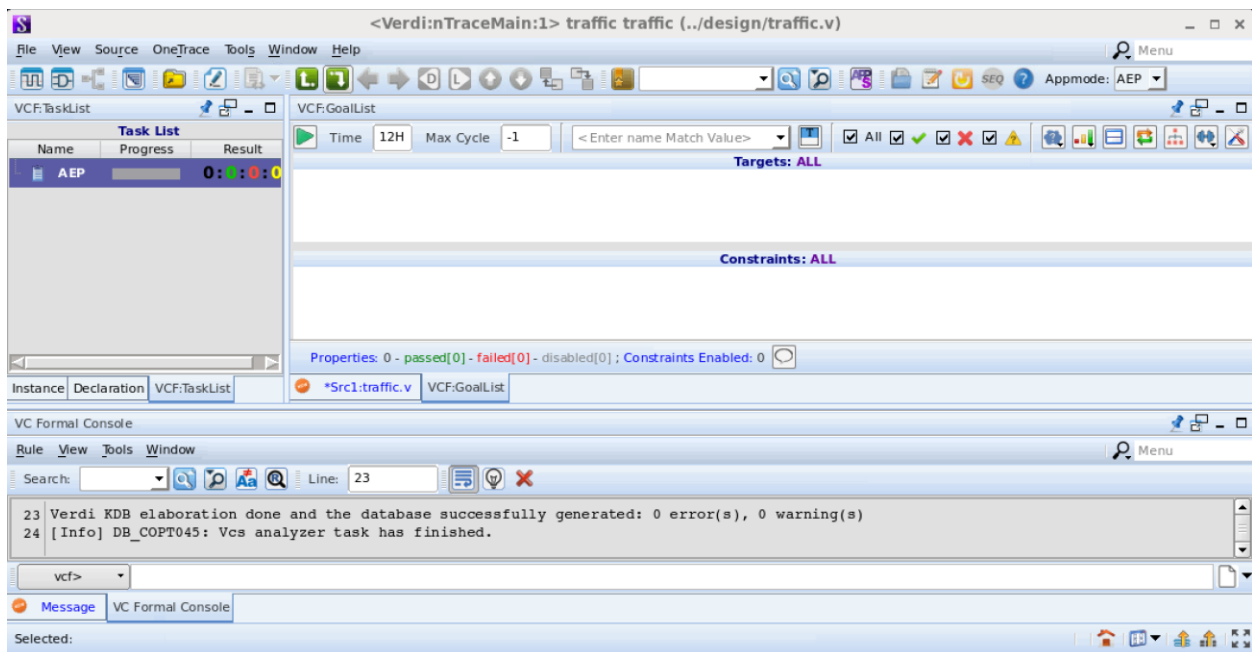
VC Formal can be run in three modes: interactive Verdi GUI mode, interactive without Verdi GUI using shell mode, and non-interactive batch mode.

Mode 1: Start VC Formal in Verdi GUI Mode

9. Start the tool in Verdi GUI mode:

```
%vcf -f run.tcl -verdi
```

VC Formal starts in the Verdi GUI mode, with icons, tables, tabs, and windows especially designed for property verification with the FPV App. The App mode is set to FPV by default. We had overridden this in our “run.tcl file via command “set_fml_appmode AEP” so GUI has AEP-mode set.



Initial configuration is shown with the “VCF:TaskList” tab on the top left, the “VCF:GoalList” tab on the top right, and the “VC Formal Console” shell at the bottom.


10. Get familiar with the Verdi GUI instance:

Check the source file tabs, properties to be checked under the “Targets: ALL” table as well as properties specified as constraints in the “Constraints: ALL” table.


Review Design Information and Setup

11. Review design information and setup  on top menu bar ensuring you are

in AEP-mode, and in TaskList you can see 0-AEP property.

12. Click on the Show Complexity icon  on the upper right above the property table. Examine items under “Missing Clock” and “Missing Reset” and trace from the source file to see that the active phase of rst is high.

Revise Setup and generate AEP

13. Click on the Edit Tcl Project File icon  on the upper left and add the missing switch “-aep all” to the existing command “read_file” in the Tcl file to generate AEP properties.

```
read_file -top $design -format verilog -aep all \
-vcs {-f ../design/filelist}
```

Or for the 2-step design:

```
elaborate $design -aep all
```

14. Add the missing clock and reset setup information to the Tcl file:

```
create_clock clk -period 100
create_reset rst -sense high
```

15. Add commands to initialize the DUT by holding reset active until sequential elements (latches and flip flops) values are stable. And save the initial state.

```
sim_run -stable
sim_save_reset
```

16. Save edited run.tcl Tcl file:

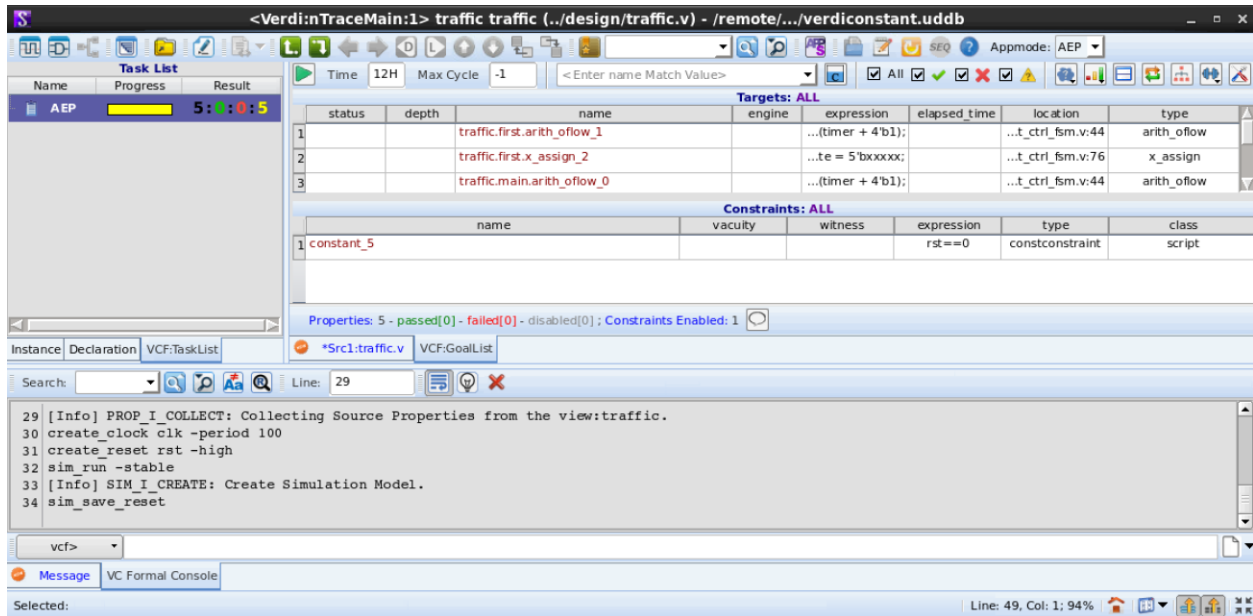
Click on the Save icon .

17. Restart VC Formal:

Click on the Restart VCST icon .

18. Check setup and design information:

There are 5-AEP properties show in TaskList, and the status for these properties is blank due to checks has not been run yet.



Run AEP check and Review Results

19. Start auto-extracted property verification:

Click on the Start Check icon .


20. Hide the constraints table:

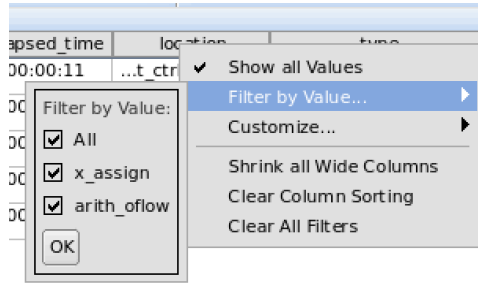
Click on the Targets+Constraints icon  at the top right.

21. Check result in Targets:ALL:

5-AEP: 4 proven , 1 falsified .


Targets: ALL							
status	depth	name	engine	expression	elapsed_time	location	type
1		traffic.first.arith_0flow_1	e1	...(timer + 4'b1);	00:00:11	...t_ctrl_fsm.v:44	arith_0flow
2		traffic.first.x_assign_2	e1	...te = 5'bxxxxx;	00:00:13	...t_ctrl_fsm.v:76	x_assign
3		traffic.main.arith_0flow_0	e1	...(timer + 4'b1);	00:00:03	...t_ctrl_fsm.v:44	arith_0flow
4		traffic.main.x_assign_1	e1	...te = 5'bxxxxx;	00:00:07	...t_ctrl_fsm.v:76	x_assign
5	1	traffic.x_assign_0	b8	..._reg <= 1'bx;	00:00:02	...ign/traffic.v:49	x_assign

Can click  to filter status or right click any title of Targets column, for example, right click “type” and select “Filter by Value”, can choose only “x_assign” type or “arith_oflow” type or all.



Debug Failure

22. Debug failure:

Double click on  under the status of property “traffic.x_assign_0” to open a counter-example waveform.
(Note that a double click on the “name” of a property will open the property in the source code window instead.)

The reason for property fails is due to reg assignment ‘dummy_reg’ is never activated at line#49.


```

47  always @(posedge clk or posedge rst)
48      if (rst) dummy_reg <= 0;
49  else dummy_reg <= 1'bx;

```

Correct Erroneous in RTL Design

23. To correct error, we need fix the RTL-source file ‘traffic.v’.

The design can be edit on the GUI interface by click on Verdi “Edit Source File” icon  and modify the file below:

Original design:

```

always @(posedge clk or posedge rst)
if (rst) dummy_reg <= 0;
else dummy_reg <= 1'bx;

```

Modified design:

```

always @(posedge clk or posedge rst)
if (rst) dummy_reg <= 0;
else dummy_reg <= 1'b1;

```

24. Save file:


Click on the Save icon .

Restart the Run and Verify Fix

25. Restart VC Formal with the modified assertion:

Click on the Restart VCST icon .

26. Re-run property verification:

Click on the Start Check icon .

Observe that there are no falsified properties and all are proven.

Save Session

27. Save session using default name from the VC Formal Shell:

```
vcf> save_session
```

Alternatively, click on File → Save Session... to open the “Save Session” dialog window.

28. Exit VC Formal:

Click on File → Exit

Restore Session

29. Start VC Formal using previous saved session:

```
%vcf -restore -verdi
```

30. Review setup and results then exit:

Click on File → Exit

Mode 2: Start VC Formal in Interactive Non-Verdi GUI Mode

31. Invoke VC Formal without Verdi GUI:

```
%vcf -f run.tcl
```

32. Enter run check command in VC Formal Shell:

```
vcf> check_fv
```

33. When check completes, report results:

```
vcf> report_fv -list
```

Alternatively, enter run check command with callback task:


```
vcf> check_fv -run_finish {report_fv -list > results.txt}
```

34. Start the Verdi GUI from within the VC Formal Shell:

```
vcf> start_gui
```

To debug failures, it is recommended to use the Verdi GUI.

Note that the VC Formal Shell panel will not be available in the Verdi GUI. Any Tcl command will need to be entered from the `vcf>` prompt where you used the `start_gui` command.

Also, the debug waveform may not be embedded in the same window as before. You can always click on  to dock (or undock) a window.

35. Exit VC Formal:

```
vcf> quit
```

Mode 3: Set Up and Run VC Formal in Batch (Regression) Mode

36. Copy Tcl file run.tcl to run_batch.tcl:

```
%cp run.tcl run_batch.tcl
```

37. Edit run_batch.tcl and add commands to run and save results:

```
check_fv -block  
report_fv -list > results.txt
```

38. Add command to save session:

```
save_session -session batch_results
```

39. Save run_batch.tcl file and exit editor.

40. Start VC Formal in batch mode with switch -batch:

```
%vcf -f run_batch.tcl -batch
```

Note that in batch mode VC Formal exits automatically after the execution of the Tcl command file and no need to add “quit” command in the end of Tcl file.