0.1 Temporal arbiter implementation

Given priority scores from all the candidate qubits, an arbiter circuit is needed to select the ones with the highest priority, in order for their syndromes to be routed to the allocated communication infrastructure for decoding.

The desired functionality is in essence a top-k argmax, which will give the indexes of the k logical qubits that produce the highest scores and thus are in most urgent need of complex correction. This would be relatively straightforward to implement the traditional way with arithmetic comparators and index multiplexers. However, this implementation carries a significant area cost for the limited budget allowed by the integration density of current superconducting fabrication processes.

To reduce the area and power requirements, as well as limit the latency, we instead use a race logic based design for the arbiter. First, the priority scores of each candidate qubit are translated into temporal signals. A priority score of $x \in [0, 5]$ gets encoded into a pulse arriving at time $T_x = x\Delta_t$, where Δ_t is a small constant delay. The encoded scores are then passed through a temporal bitonic sorter. The function of the temporal sorter is to route the input signals such that they appear in it's outputs in order from earlier to later arriving pulse. So if x_k is the k-th largest priority score and T_{sort} the constant latency of the sorter, the k-th output wire of the sorter will produce a pulse at time $x_k\Delta_t + T_{sort}$. Sorters are very well suited for temporal implementation, as only two functional cells are needed to sort two signals, leading to hardware efficiency impossible by other means. Of course, because we need the top-k argmax of the signals, not just their max, a sorter by itself is insufficient. Instead, the signals passing through the bitonic sorter are also used to control a small routing circuitry, which will lead select signals $return_i, i \in [0, k-1]$ for each of the top k maximum outputs of the sorter through the same path the corresponding data signals took to reach that output. This ends in a pulse being emitted at port $sel_i, i \in [0, n-1]$, for exactly those qubits whose priority score x_i is in the top-k largest priority scores. This approach avoids complicated index multiplexing and decoding circuitry and produces directly usable binary flags of qubit selection.

The basic element of the temporal arbiter is the comparator module, shown in fig?. Let $T(x)$ denote the time a pulse arrives at port or wire x. No more than one pulse will reach any port during an execution of our temporal circuit, so we only need to represent the time for that pulse. In cases where no pulse reaches x during an execution, we assign $T(x) = +\infty$.

The comparator module sorts two input temporal signals at ports x_a and x_b , such that the output x_{max} will re-emit the larger of the two encoded priorities, meaning the one for which a pulse arrived the latest, such that $T(x_{max}) = \max T(x_a), T(x_b) + \tau_c$, where τ_c a constant denoting the comparator's latency. The output x_{min} emits the smaller of x_a, x_b. In cases of ties the outputs are equivalent.

For the backward pass, the comparator module routes the select signal $return_{max}$ to the port sel_a if x_a arrived after x_b and to port sel_b if it arrived before it or at the same time. A pulse appearing at $return_{min}$ will be routed the opposite way. The encoding for the backward pass is simply binary rather than temporal, so we don't care about the arrival times of *return* signals as long as they occur after the inputs x_a, x_b.

This gives us $sel_a = \begin{cases} return_{max} & T(x_a) > T(x_b) \\ return_{min} & otherwise \end{cases}$. sel_b works similarly. The *sel* outputs encode the argmax of the two input priority scores.

To build the complete top-k argmax, comparator modules are arranged into a bitonic sorter, with x_{max} and x_{min} ports connected to x_a or x_b ports of the next layer's comparators and *sel* ports connected to *return* ports of preceding layer. First we pass pulses encoding the priority scores of n logical qubits to the n data input ports of the sorter circuit. After they have propagated through the sorter, the *return* ports corresponding to the top k outputs of the bitonic sorter are activated with a pulse. These pulses will follow the path their perspective data signal took through the comparators, thus only k ports at the first layer of the sorter will receive pulses at their related *sel* ports. The bitvector of these *sel* signals can then be used directly to route the syndromes of the selected logical qubits for external decoding.

However, we can see that a large portion of the sorter is sorting signals that can not belong to the top k, which is unnecessary. To improve on hardware efficiency, we can sparsify the bitonic sorter. First, we split the n inputs in groups of size k and pass each group through a full bitonic sorter of size k. We can then reduce the number of inputs by half by selecting the k largest outputs from each pair of k-sized sorters. This is done the same way that selecting the top half of values is done in bitonic sorting, by applying a comparator to the i-th output of the first sorter and the $(k-i)$-th one of the second sorter. We then pass the $\frac{n}{2}$ signals through a similar sort and reduce process. We repeat this until only k signals are left, from which the *return* signals will originate. This reduces the number of comparators from $\frac{n \log_2(n)(\log_2(n)+1)}{4}$ to $(\frac{k \log_2(k)(\log_2(k)+1)}{4} + \frac{k}{2})\frac{n}{k} + (\frac{n}{k} - 2)\frac{k \log_2(k)+k}{2}$, and the number of comparators a signal goes through from $\frac{\log_2(n)(\log_2(n)+1)}{2}$ to $\frac{\log_2(k)(\log_2(k)-1)}{2} + \log_2(\frac{n}{k})(\log_2(k) + 1)$, which minimizes latency.

Since we only keep the x_{max} output from the comparators that implement the $2k$ to k reduction between sort steps, and only need to route the $return_{max}$ signal to a *sel* port, we can use a smaller version of the comparator module for these cases.

0.2 Comparator circuit

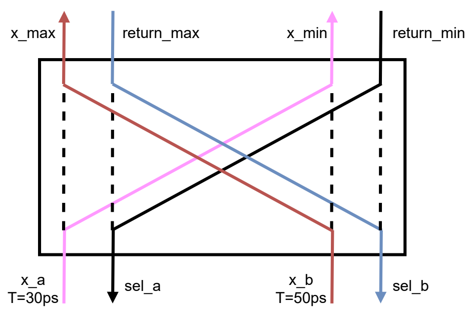
The first two race logic primitives we need for the arbiter are *First Arrival* (FA) and *Last Arrival* (LA), which correspond to min and max operations on temporal signals respectively. These can be implemented with a C element for LA and an inverted C element for FA. Both of theses cells are cheap area-wise and we have tuned them to have very similar delays, so differences in their propagation delay do not cause the order of signals' arrival to change for the

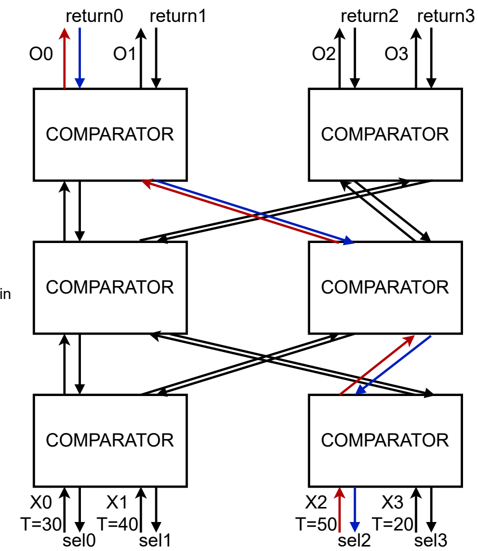
n	k	latency (ps)	area (JJ)
64	2	379	5580
128	4	588	23004
256	8	847	77760

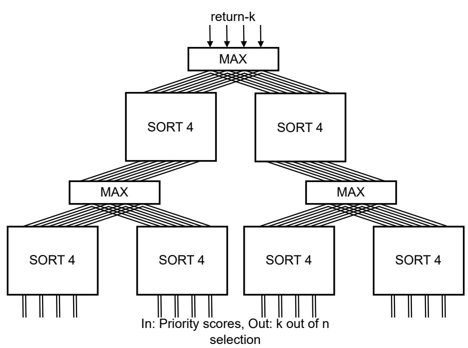
length of the sorter network. Thanks to this, synchronization to re-align the signals to their encoded value is not needed for the input sizes we consider.

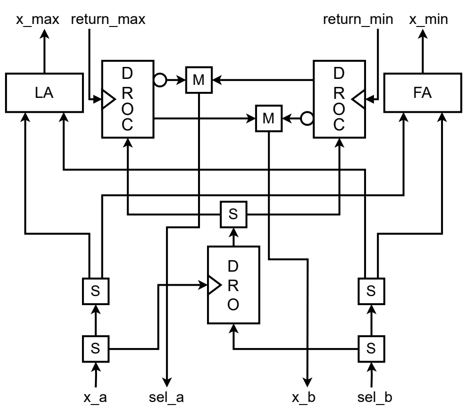
For the backrouting part of the comparator module, we need *a*) to detect whether a or b arrived first and *b*) to demultiplex the *return* signals based on that. The first case corresponds to an inhibit cell in temporal logic. $Inhibit(a, b)$ or $a \dashv b$ allows signal b to pass to the output only if a has not previously arrived, in which case it gets blocked. Typically in superconducting circuits clocked inverters are used as inhibit cells. Since in our case we only need to know whether input b came first or second, and not the temporal information of when it arrived, we can use the cheaper Destructive Readout(DRO) cell. Input a is mapped to the clock port of the DRO and b to the data input port. If a arrives before b, no pulse is stored in the DRO and thus no pulse is produced at the output. If instead the pulse at b arrives first at the data port of the DRO, it stores a pulse in the superconducting loop that propagates to the DRO output upon a's arrival. In the case the two signals a and b are close to each other, such that they encode the same discrete temporal value, their comparison is a tie and either the presence or absence of a pulse at the DRO output is a valid result. This is important for the correct operation of the system.

To demultiplex $return_{max}$, a Complementary output Destructive Readout (DROC) cell is used. Upon clock arrival, this cell produces a pulse at either it's first output if it has not received a pulse in the data input port, or at it's second output otherwise. Connecting the output of the $a \dashv b$ DRO in the data port of the DROC and the $return_{max}$ wire to it's clock port, as well as connecting the first and second DROC outputs to the comparator module's sel_b and sel_a, a pulse at $return_{max}$ gets routed to sel_a if a was the last signal of the two and to sel_b in the other case. Because we might need to select both of the comparator's operands for the top-k, we also need a second DROC with it's outputs swapped to route $return_{min}$ to the select signal of the input that came first. We use a splitter to pass $a \dashv b$ to the data input of both DROCs and two merger cells to combine their outputs for sel_a and sel_b. Four more splitters are used to send inputs a and b to the FA, LA and DRO cells. The comparator module only requires a handful of gates, significantly less than a bit-parallel implementation would, which allows it's usage in our resource constrained environment. As a bonus, this implementation is fully asynchronous and does not require an expensive clocking network, which is a problem for many superconducting designs.









0.3 Resetting procedure

The superconducting cells that comprise the arbiter are stateful, except for the splitter and merger. All cells that have a state other than their initial one after the arbiter's execution must be returned to their original state before a new execution can occur, in order to guarantee correct operation. Since all data inputs of the arbiter receive exactly one pulse, even those that denote priority score 0, and a comparator module that receives both data inputs fires at both it's x_{max} and x_{min} outputs, every FA and LA cell in the arbiter will receive pulses at both it's input ports, thus it will return to it's initial state. However, the DRO cells that serve as inhibits will still store a value of 1 at the end of execution if their data port receives it's pulse after the clock port does. Additionally, the DROC cells that route the *return* signals will not receive a clock pulse if they don't happen to be in the path of one of the top k largest inputs, which means the result of the inhibit operation will stay stored in them. The most straightforward way to solve this would be supplying an external reset signal to each of these cells. Unfortunately, this would require using significantly more expensive cells that offer such a reset port, as well as necessitating a distribution network for the reset signal to all of these cells, which would cost a lot of splitters that are necessary for the fanout. To avoid this, we designed a data-driven reset scheme, that returns all cells to their original state by only inserting signals to already existing ports in the design, without making any changes to it's internals. To start, we note that if a DRO or DROC cell receives a pulse at it's data port while allready storing one, the new input pulse does not affect it's state or produce output pulses. We make use of this property to clear the state of all inhibit DROs. The forward pass of the comparator module can be thought of as swapping the input signals if they are not in order, and propagating them unswapped if they are already ordered. Additionally if the two inputs are in order, the inhibit DRO will receive the data pulse before the clock pulse, and thus when the second input arrives it will fire and clear it's stored state. The comparators in the bitonic sorter are arranged such that a layer of comparators receiving a monotonically increasing sequence of pulses, $T_i = i * \Delta_t$ for T_i the time of arrival for the i-th input's pulse, will have all it's inhibit DROs fire and clear, as well as propagate the pulse sequence at the same order, meaning the next layer of comparators will also receive an ordered sequence and have the same effect. This also holds true for the reduced "max" layers that only implement the max operation instead of both max and min like most comparator layers. By induction, this means that inserting such a sequence of inputs where data input $i+1$ of the sorter receives a pulse Δ_t after the input i did, will cause every inhibit DRO in the design to fire and clear. While inserting this sequence of pulses for the reset sequence after an operation of the circuit takes more time than the operation itself, we have a large time gap of hundreds of nS between executions of the arbiter during which the external syndrome decoding happens, whereas the reset operation only takes up to a couple nS, that do not contribute to the decoding latency. Since every DRO fired, we know that now every DROC in the sorter holds a pulse. As such, we know the path a *return* signal inserted at any point in the circuit will take. At every "max" module in the design that combines the outputs of two sorters of size k to the k largest values, every *return* signal received from the following layer will now be routed to the same of the two sorters, as all of the larger signals came from it. Thus using mergers we insert pulses to the *return* signals at the input of every "max" layer that connect to the sorters from the previous layer that we know won't receive the *return* signals routed through the *max* layer. We also insert such pulses at the *return* ports for the top k selection at the final layer of the arbiter. These n inserted signals will traverse through every DROC in the arbiter on their way to the first layer, clearing the state all of them hold. Only n mergers and $n-1$ splitters are needed to insert this reset *return* signal. To produce a monotonically increasing sequence of pulses at the arbiter's data inputs for the DRO reset, we use a splitter chain of length n, where a pulse entering the i-th chain will be split into two pulses, one being merged into the

i-th input of the arbiter and one passing through a small number of JTL to add a bit of delay before entering the $i + 1$ part of the splitter chain. This costs n splitters, mergers and JTL chains. This data-driven reset scheme leaves the arbiter design untouched and only has a small overhead to insert pulses at $2n$ existing ports.