RISC-V SoC Microarchitecture Design & Optimization

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Group 23
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Problem

a. Moore's Law is Dying!

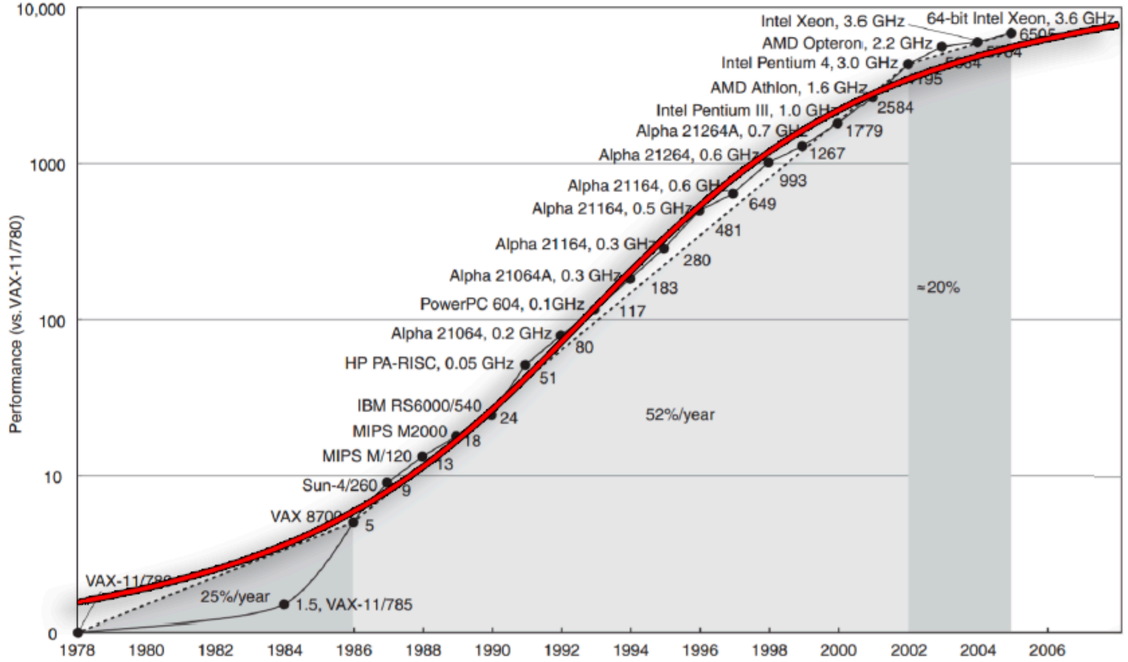


Figure 1. Growth in processor performance over 40 years.
Source: John L. Hennessy, David A. Patterson. *Computer Architecture: A Quantitative Approach* (Sixth Edition). Morgan Kaufmann, 2017.

b. Emerging Applications

Figure 2. Tesla self-driving cars.
Source: www.businessinsider.com/tesla-autopilotfull-self-driving-subscription-early-2021-elon-musk-2020-12

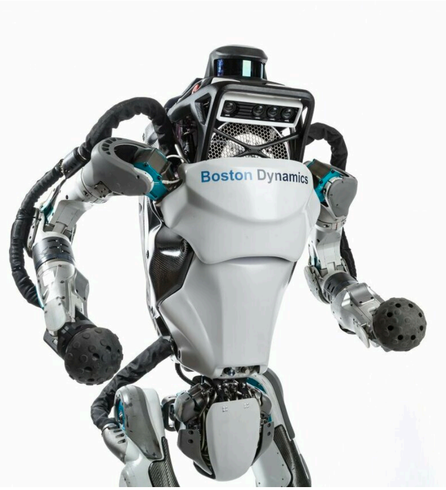


Figure 3. Boston Dynamics robots.
Source: techxplore.com/news/2019-01-ten-robotics-year.html

Need

Customer Requirement

Compatible with RISC-V apps

Inexpensive

Detailed docs

General

Run fast

Accurate

High fault tolerance

±5%

Performance

Easily configurable

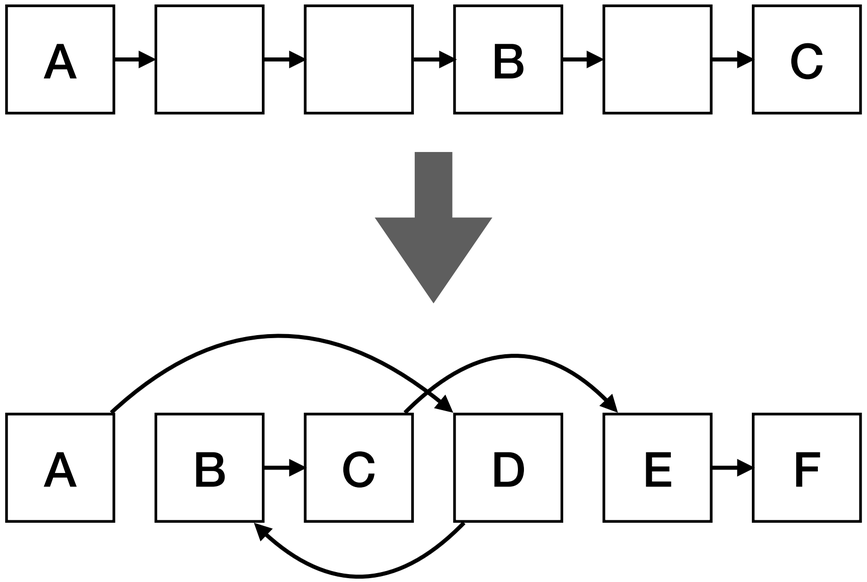
Low Power

Quick Response

Embedded-System

Solutions

Dynamic (Out-of-order) Instruction Scheduling



Instead of waiting until the next instructions is ready, we choose any ready instructions to execute.

Arithmetic Logic Unit

$3*7 = 21$

Floating Point Unit

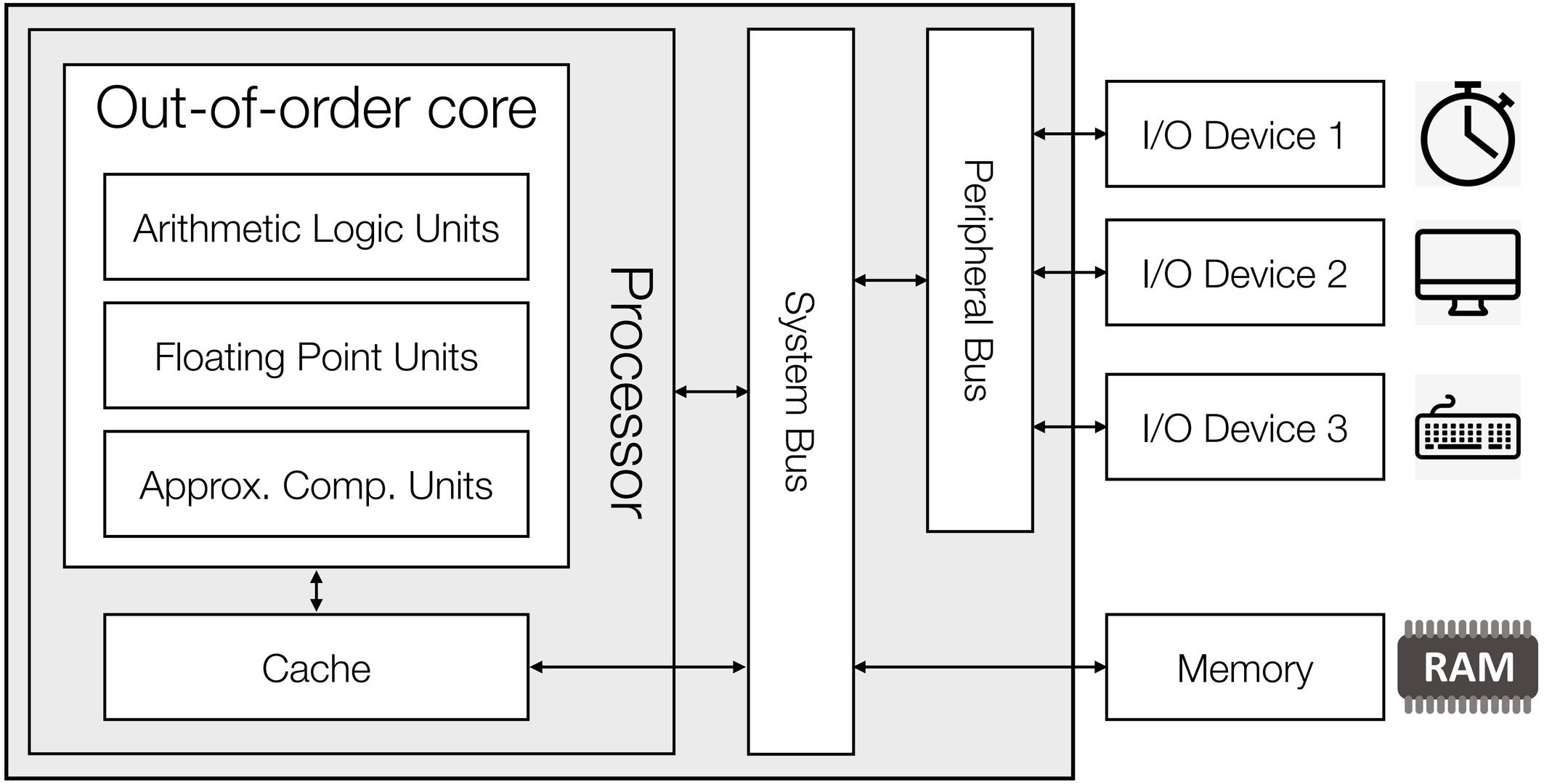
$3.4*2.8 = 9.52$

Approx. Comp. Unit

$3.4*2.8 \approx 9.5$

We apply multiple execution units to perform computation for different operations under different scenarios.

Concept Diagram



Grey area is our design