Jitter detection circuit

Mixed signal Very Large Scale Integration

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***Abstract*—The following paper would give an insight into the detection of jitter that is used in [1] at 45 nm scale. This would use centroid layout to have the symmetry of the circuit to save the area.**

***Index Terms*— jitter detection, comparator, xor gate, centroid layout, floor plan.**

I. INTRODUCTION

As the speeds of the microprocessor are increasing drastically now a days the importance of the jitter circuits have become prominent in todays world. The internal clock in a microprocessor is inherently subject to variation caused by power supply noise modulating the delay of the clock distribution network. The systematic accumulated/response error from PLL/clock generator further aggravates the uncertainty of the clock edge [2]. This leads to two types of jitter causing two different types of problems. First, the internal clock period and high/low times are distorted, reducing the maximum operating frequency of the circuit by reducing the time available in some clock cycles. Measurement of this on-chip jitter is aggravated by flip-chip packages that are difficult to probe, while buffering clocks to drive them off-chip is subject to the same delay variations that cause the jitter. Second; because clock edges are moved from their ideal locations the setup, hold, and output delay times observed on the pins of the chip are changed. This paper describes the innovative on-board instrumentation to comprehend the first type of jitter, which is purely internal to a chip and increasingly difficult to observe, since the second type of jitter is directly observable. This internally observed jitter is post-processed in several different ways to maximize the data gathering capabilities of the circuit. This project has been divided into 3 parts in which the 1st part would concentrate on creating the xor gate with least number of transistors in pass transistor technology. 2nd part is to create a comparator in 45nm technology where the design has been adopted from [1] and scaled down to 45nm technology. 3rd part is the final schematic where the capacitor is used to store the unmatched signal output and compare it with the reference voltage and give the output

II. DESIGN AND ANALYSIS

There are three important parts of the entire project of jitter circuit.

1) Design of Xor gate
2) Design of comparator.
3) Design of final schematic

1)Xor design

For the xor gate design various topologies have been considered and analyzed for best power to delay performance.

Few of which to be mentioned are described in the following.

i)

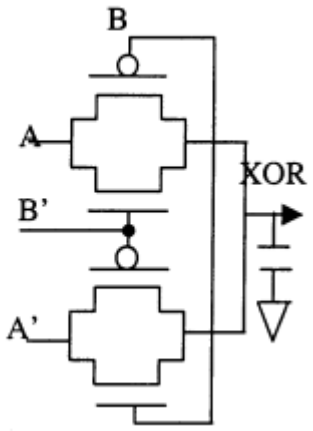


Figure 1: Xor gate using transmission gates

This xor gate design uses 4 transistors to process the xor gate logic and 4 more transistors for A` and B`.

ii)

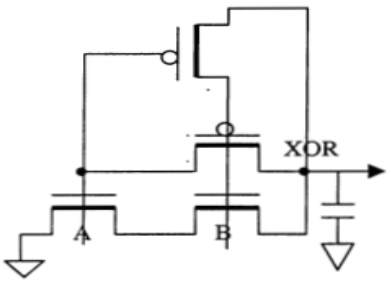


Figure 2: Describes the 4 transistor model of the xor design Where the PMOS and NMOS cannot pass a hard 0 or 1.

iii)

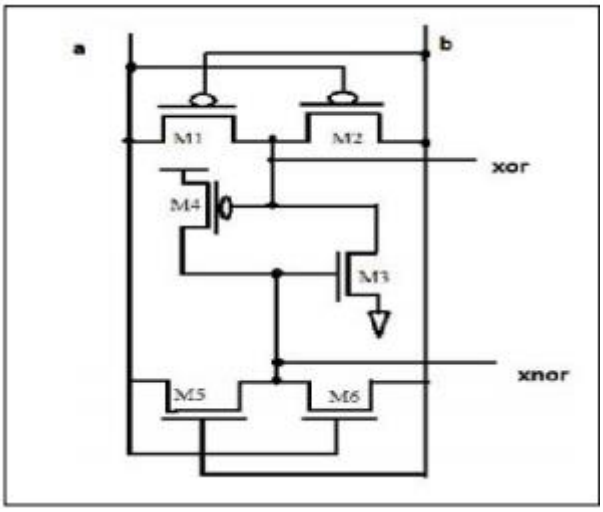


Figure 3 describes the 6 transistor model of the circuit where the inputs are just a and b

After analyization of both the number of transistors and power of the circuit the pass transistor model has been selected for the logic of the xor gate design. The logic that was used in the pass transistor model is the nmos logic. Therefore there hasn't been a strong passage of 1.1 via the nmos transistors since the nmos transistors can only pass vdd-vt through them. Hence in order to pass a strong 1 the pmos transistors have been connected in parallel with the nmos transistors. Now the pmos transistors would pass a hard 1 and nmos transistors would pass a hard zero.

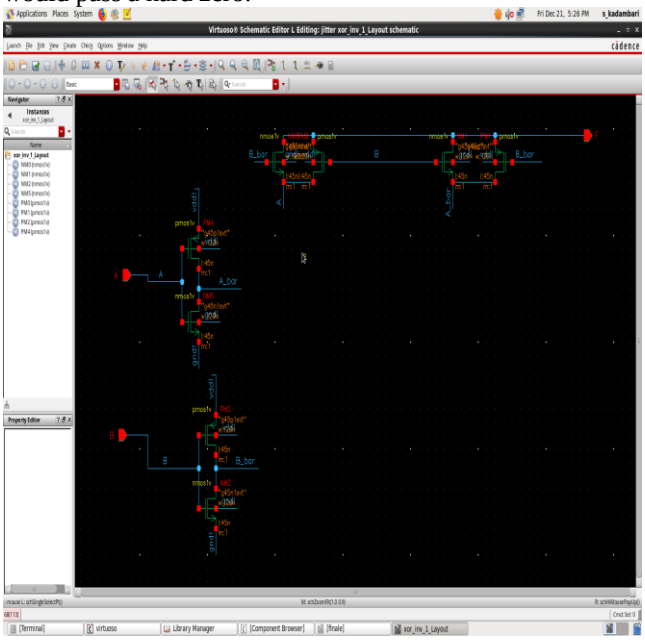


Figure 4: Describes the schematic used to create the xor design for the project.

Floorplan of the schematic for the xor design has been designed as follows

step 1: Power grid or laying out the power supplies

step 2: list all input and output signals

step 3: we must deal with special design requirements such as layout symmetry specific requirements.

Step 4: Finalize the size of the design and estimate the feasibility of meeting all the design requirements within the area scheduled.

An example of the full adder circuit has been taken to layout the xor gate model as shown in the figure below.

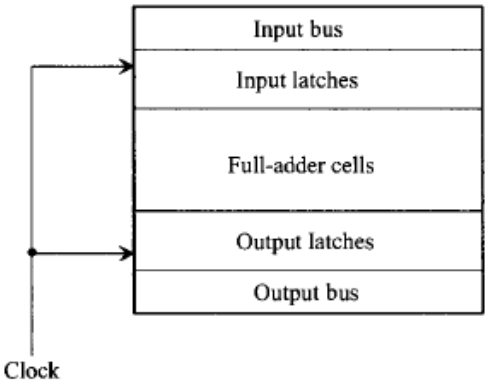


Figure 15.2 Floor plan for an adder.

Figure 5: the above figure has been derived from[2] as an example for the floorplan of xor design

In the similar manner the inputs of the xor gate have been arranged on top of the xor transistor logic and outputs below the transistor logic between the vdd and gnd rails . Before actually laying out the design it has been constructed on the stick diagrams. This can be observed in the figure below.

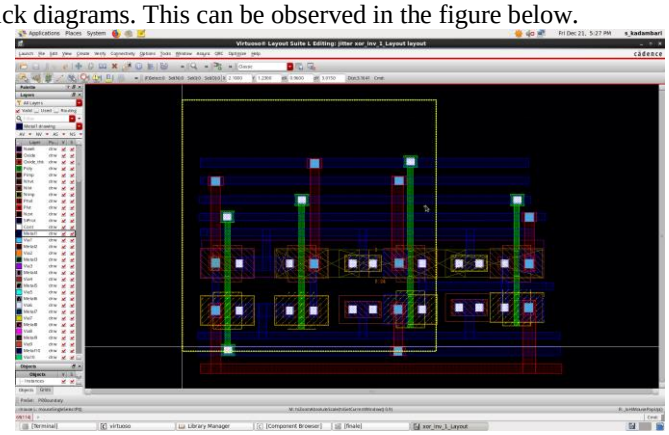


Figure 6: The above layout describes the xor gate with all the inputs and outputs on the top and bottom of the design.

The above rails consist of A, B inputs and A`, B` outputs along with vdd and the bottom rails are A` and A along with the gnd rail.

The transistors have been laid out in way that all the pmos to nmos have the same gates as B and B`. After the xor layout the extracted layout of the xor design has been simulated to verify the layout results with the schematic design.

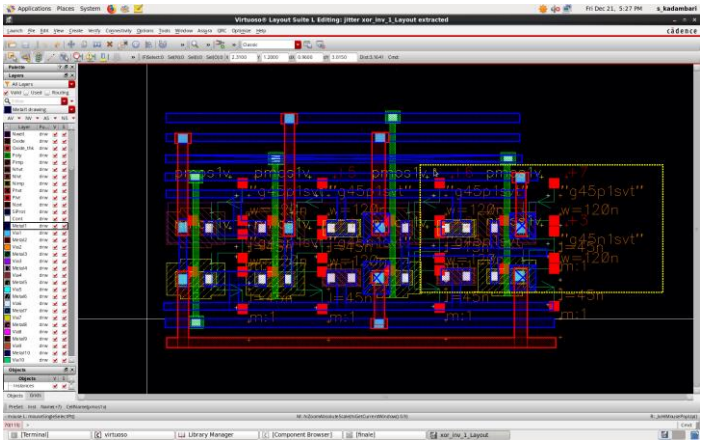


Figure 7: The above figure describes the extracted output of xor after the lvs.

The extracted laid output demonstrates the pmos and nmos connection in the layout and relates that to schematic representation for clear understanding of the design.

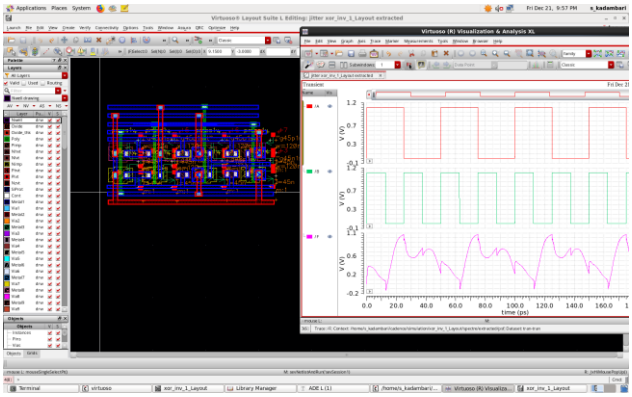


Figure 8: The above figure describes the extracted output of the xor design

As we can see the output of the or follows the output of the xor follows the input of A and input B this clearly demonstrates that there is a coupling happening between the xor output to the A input at 50ns time period. Th difference in the results operation can be clearly seen when compared this with respect to the schematic simulation result.

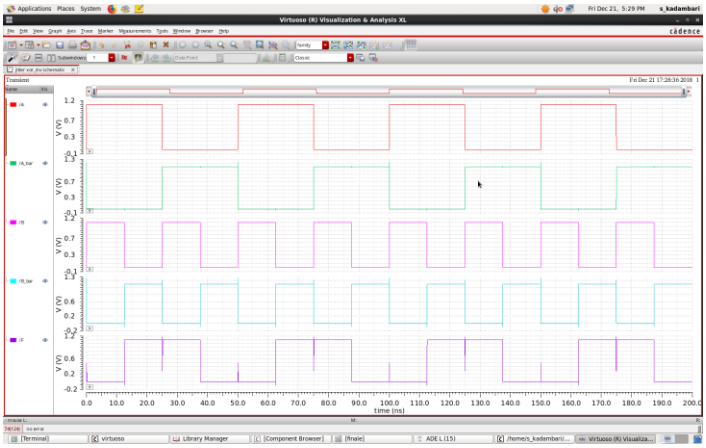


Figure 8: The above figure describes the output of the xor design at schematic level.

The narrow dibs in the xor gate when the output is at constant one is due to the difference in the raise and fall time of the inputs A and B and would be taken care with the help of capacitor as it would eradicate the sudden changes in the voltages that come into it.

2) Design of comparator

The design of the comparator was adopted from [1] which was designed for 180nm model.

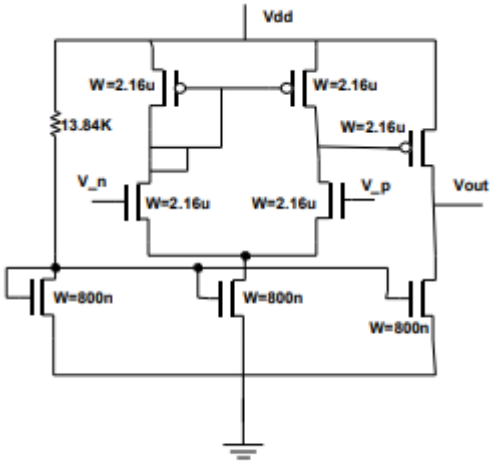


Fig. 3: Analog comparator topology.

Figure 9: The above circuit has been implimented in 180nm technology this designed has to be scaled down to 45nm

The first pairs of pmos and nmos transistors form a differential amplifier circuit and the lower part is to maintain current source for constant current flowing through it in order to maintain the transistos at linear region for amplification.

The schematic that we need to design is at 45 nm model which is scaled 4 times lower to the 185nm model. Therefore the resulting schematic would appear as below. Here all of the widths of the transistors have been scaled down to 540nm and 200nm where as the resistor value has stayed the same.

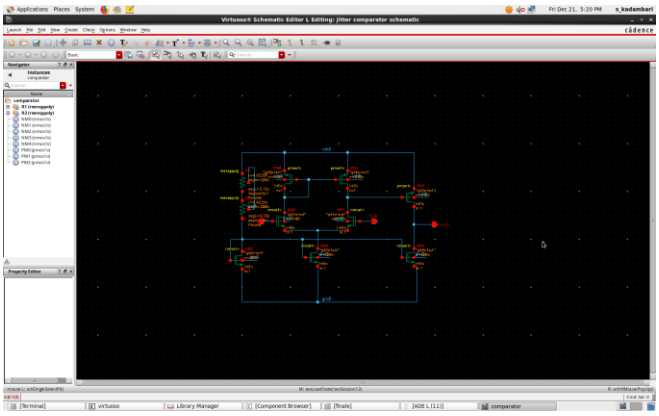
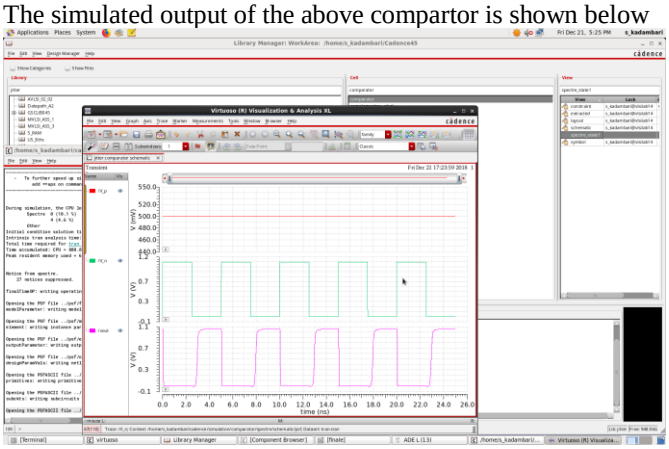


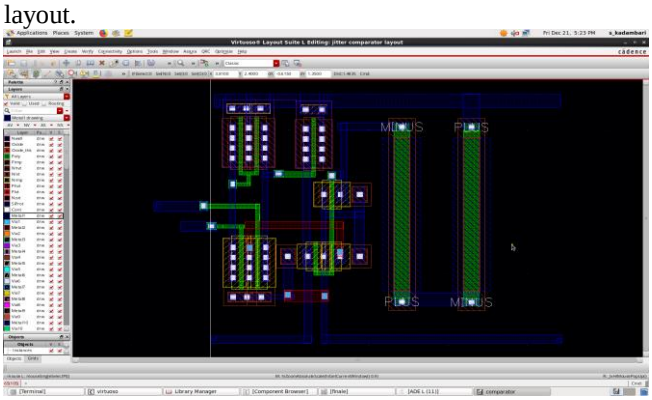
Figure 10: The above figure describes the comparator circuit in the 45nm scale.

The simulated output of the above compartor is shown below



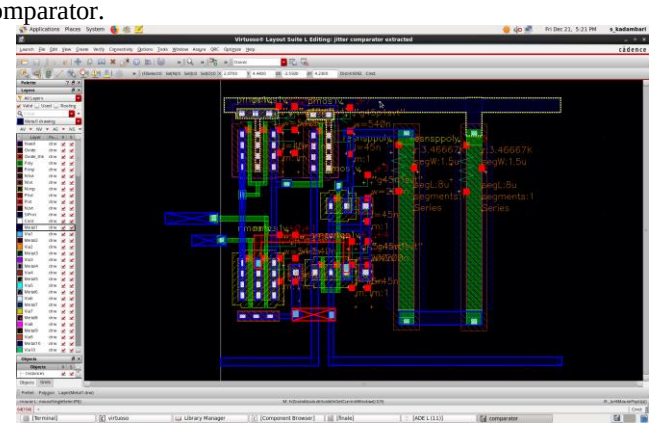
The above output demonstrates that the comparator circuit works as expected. The reference voltage for the comparator is 0.5v which is 500mv and the pulse that has been given to v_n terminal switches from 1.1v to gnd. Since the pulse has been given to the v_n the output would be an inverted form of the input.

In order to create the layout the size of the resistor is very big when compared with the entire design of the transistors model. Therefore the resistor has been divided into two sigments and the logic of interdigitated has been used on it to connect the resistor with the rest of the design. The layout of the entire design is drawn on the stick digrams first and then on the layout.

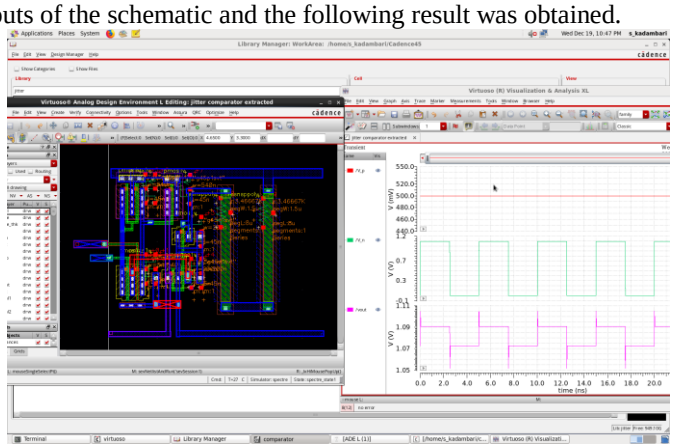


The differential pair of both nmos and pmos have been combined together and the gates of the pmos are connected to the drain on the left part of the circuit and the remaining three nmos and a pmos has been made symmetrical to the pmos width .The large resistors are connected on the right hand side as seen in the figure so the mirror symmetry is maintained.

The below figure demonstrates the extracted layout of the comparator.

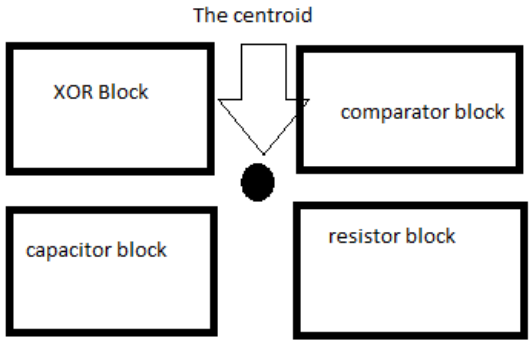


The comparator circuit has been simulated with the same inputs of the schematic and the following result was obtained.



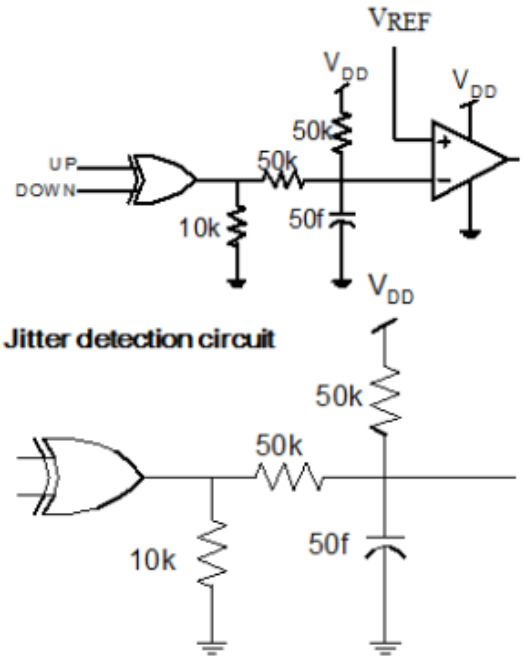
We can see the same coupling hapenning with the input to output of the compartor this is either due to the crosstalk between the lines of input and output or between the transistors.

Floor plan of the final circuit



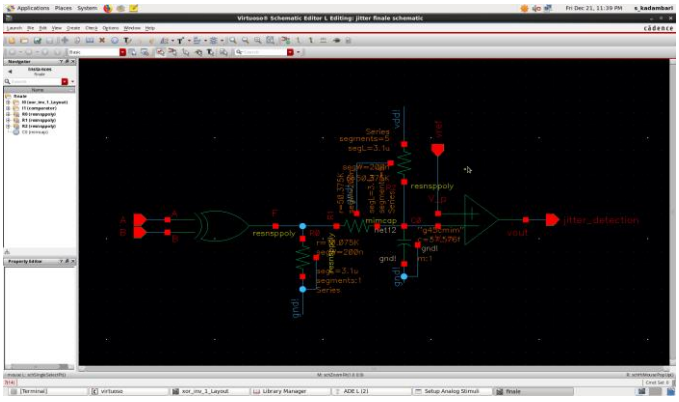
Jitter circuit floorplan

Jitter circuit

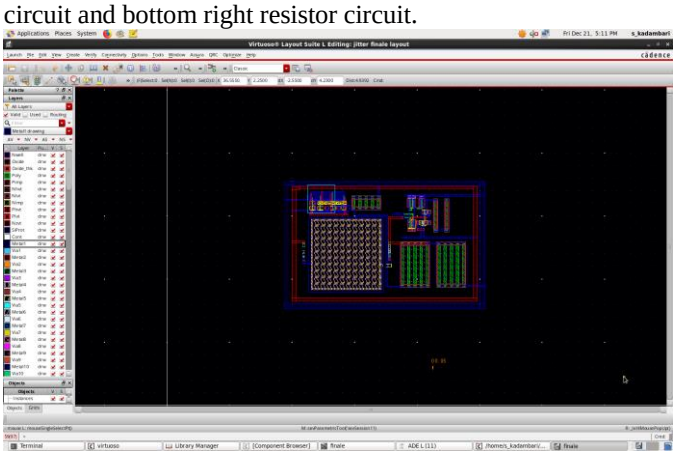


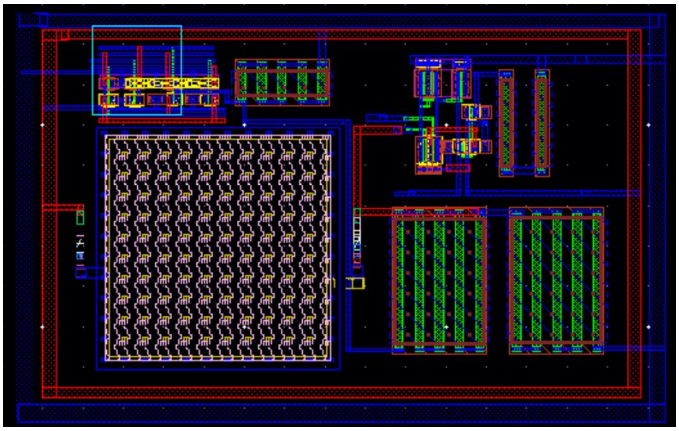
The above circuit is the final jitter detection circuit. When there is a difference in phase of either of the signals up or down there would be a 1 0 and 0 1 combination between the signals as there are not in sync hence when a 0 1 or 1 0 combination is given to the xor gate as inputs the xor output tends to go to 1 and then this 1 would be pulled down by the pull down resistor i.e 10k in order for the capacitor to limit from extra charging and also a discharging path for it as the input to the op amp is considered to be an open circuit and the 50K to 50f for the RC delay constant of the capacitor in order for it to charge and discharge.

The schematic for the above the ciruit is shown below



The xor design is adopted from the above design of xor using pass transistors and also the comparator circuit to which the resistor and capacitor circuit has been attached. The resistors attached to it are poly resistors where the bulk of them has been connected to the gnd terminal and also have been segmented into 5 segments for each 50k ohms. The layout was arranged as planned on the floor plan. Where towards the left the xor circuit is placed along with the 10k ohms resistor and towards the right the comparator circuit ,Bottom left capacitor circuit and bottom right resistor circuit.

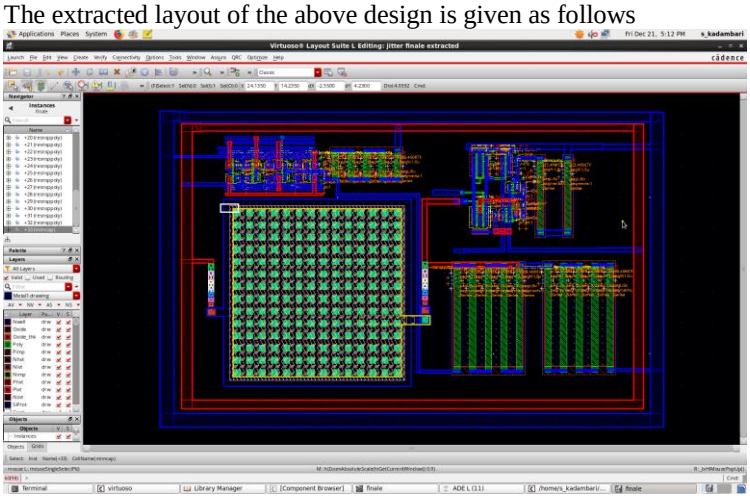




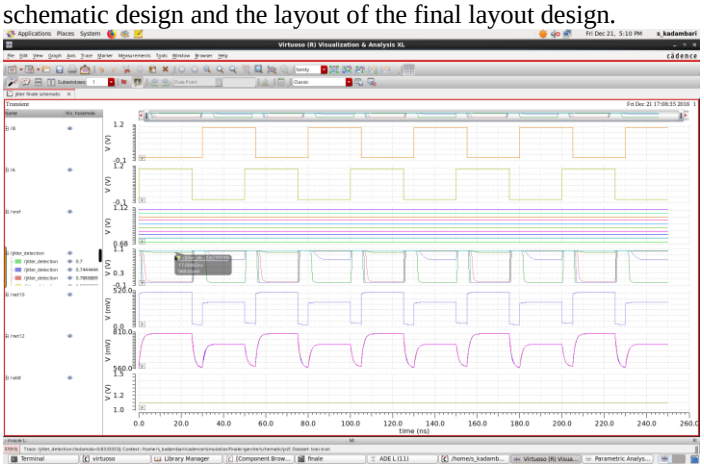
Top left xor design and 10k resistor, top right comparator circuit , bottom left capacitor, bottom right resistor.

The whole circuit is surrounded by the vdd and ground lines so that all the components would have the access of connecting their terminals.

The extracted layout of the above design is given as follows



The extracted layout of the final schematic verifies with the schematic design and the layout of the final layout design.



The schematic results depict the jitter detection of the phase difference between inputs A and B when the reference voltage is swept from 75% of vdd to vdd i.e 0.7 to 1.1v. It can be observed from the output that jitter is detected upto 0.8 volts reference voltage but above 0.8v its just constant 1.0v volts.

The above figure is the extracted output of the entire jitter circuit.

III. CONCLUSION

when designing a multiple high speed clock domain the frequency and phase of the clock is important jitter detection circuit would help detect jitter at ps difference level.

REFERENCES

[1] Kevin Sliech , Martin Margala “A Digital BIST for Phase-Locked Loops”, 2008 IEEE International Symposium on Defect and Fault Tolerance of VLSI Systems, 10 October 2008, .

[2] Tang, Makara, "Comparison of CMOS XOR and XNOR gate design" (2002). Scholar Archive. 3219.