Design and Simulation of a 4-bit ALU using CMOS Logic in Cadence Virtuoso

Abstract

This project presents the design and simulation of a **4-bit ALU using CMOS logic in Cadence Virtuoso**. The ALU was built hierarchically, starting from basic CMOS gates (AND, OR, XOR) to derived gates and arithmetic modules (Adder, Subtractor), combined into a 1-bit ALU and then a 4-bit ALU. It supports **eight arithmetic and logical operations**, all verified through simulation. The design demonstrates the effectiveness of hierarchical CMOS design and provides a solid foundation for understanding digital VLSI systems.

Introduction

An **Arithmetic Logic Unit (ALU)** is a key component of a CPU that performs both arithmetic (addition, subtraction) and logical (AND, OR, XOR) operations, forming the core of processor computations. Designing the ALU using **CMOS logic in Cadence Virtuoso** provides hands-on experience at the transistor level, enabling understanding of gate-level design, hierarchical modules, and VLSI implementation. This approach is valuable for academic learning and placements in semiconductor and embedded systems.

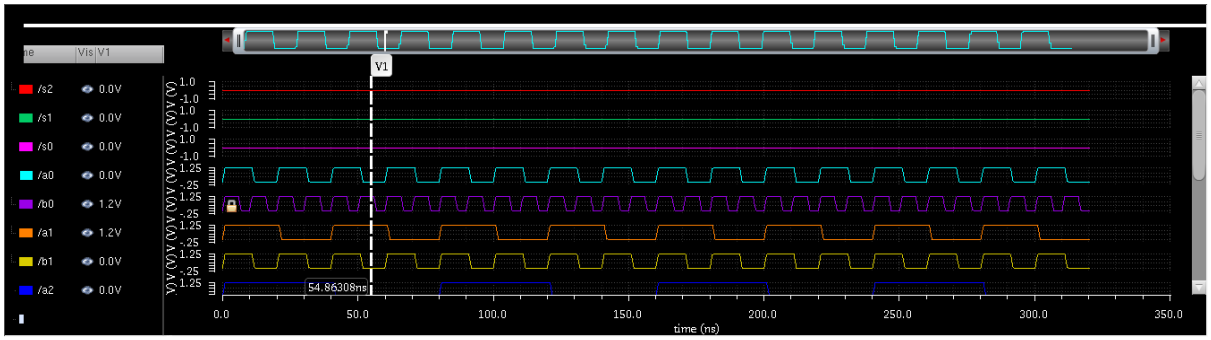
Objectives

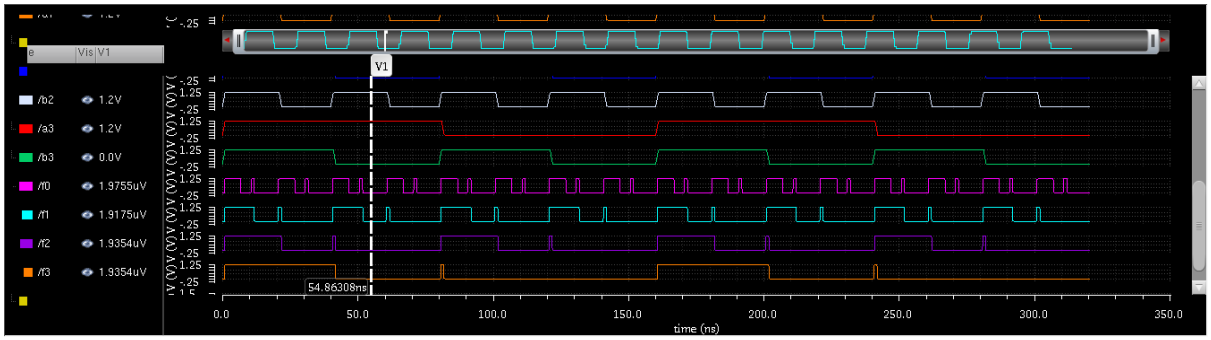
- To design a **4-bit ALU using CMOS logic gates**.
- To implement **eight fundamental operations**: AND, NAND,OR, NOR, XOR, XNOR, ADD, SUB.
- To verify **ALU functionality through Cadence Virtuoso simulation plots**.
- To understand **hierarchical design methodology from transistor to system level**.

Methodology

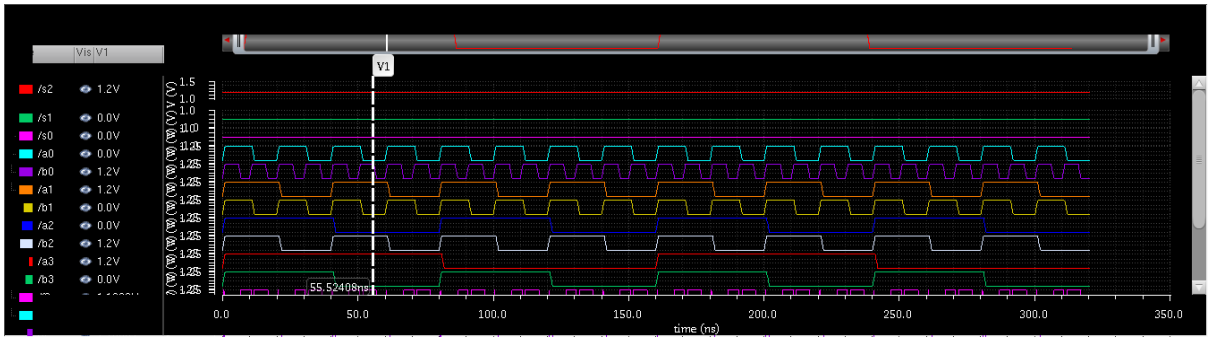
1. **Gate-Level Design**: Built CMOS-based AND, OR, XOR gates and derived NAND, NOR, XNOR gates.
2. **Arithmetic Modules**: Designed Full Adder and Subtractor using the created gates.
3. **1-bit ALU**: Combined gates and arithmetic modules into a 1-bit ALU with selection lines.
4. **4-bit ALU**: Cascaded four 1-bit ALUs to form a 4-bit ALU.
5. **Simulation & Verification**: Tested all eight operations using Cadence Virtuoso and verified results through waveform analysis.

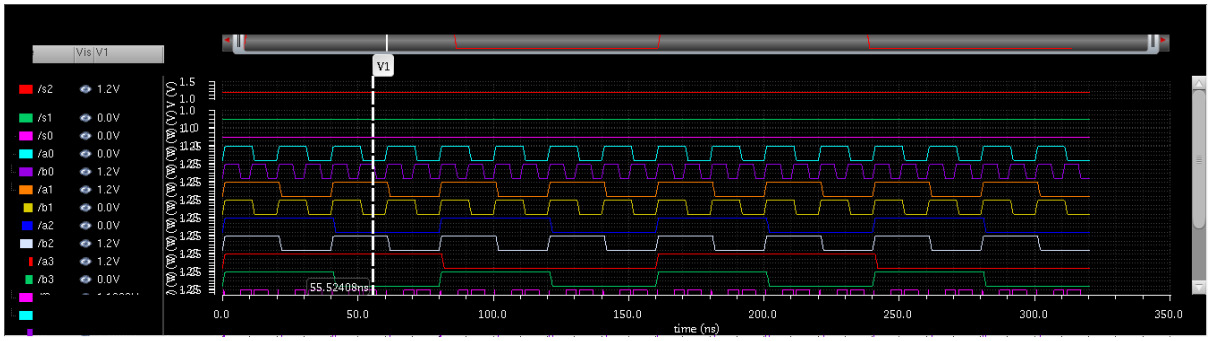
AND OPERATION



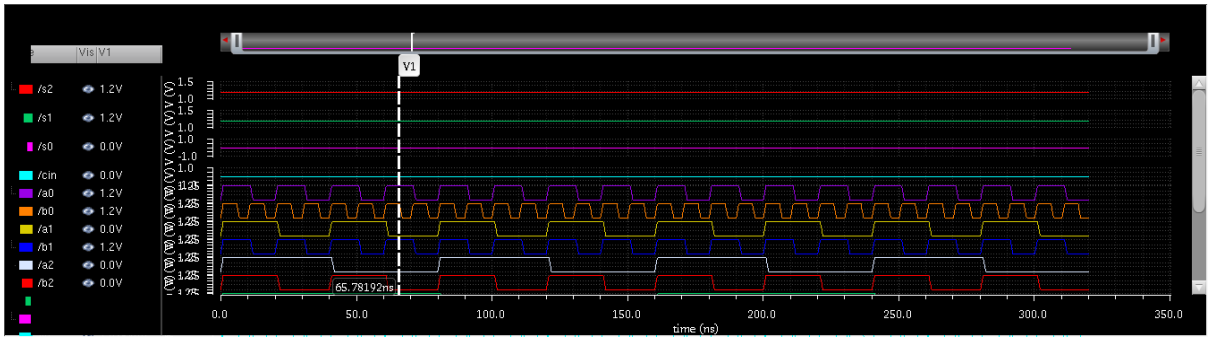


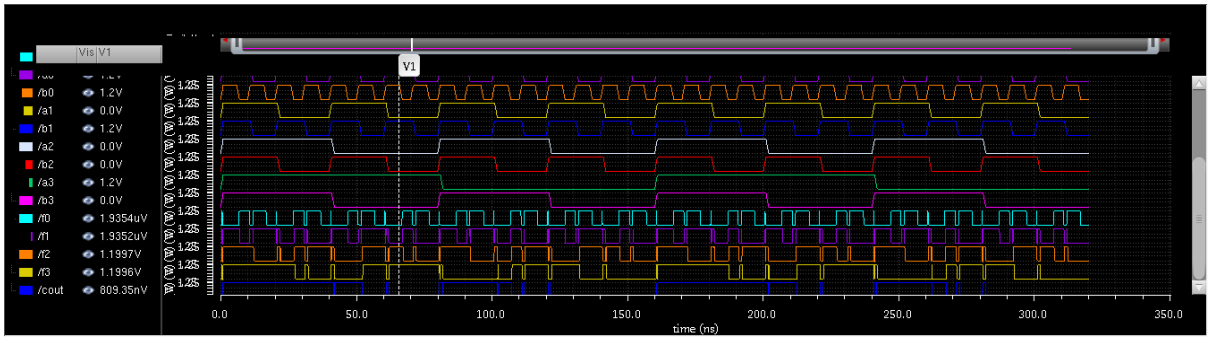
XOR OPERATION





ADDER OPERATION





Significance

- Demonstrates **bottom-up VLSI design** (transistor → gate → ALU).
- Useful for **placements in semiconductor/VLSI roles**.
- Builds strong understanding of **digital design fundamentals**.

Learning Outcomes

- Hands-on experience with **Cadence Virtuoso**.
- CMOS logic design and verification skills.
- Hierarchical design methodology.
- Improved knowledge of simulation and analysis.

Future Scope

- Extend to **8-bit/16-bit ALU**.
- Add **advanced operations** (Multiplication, Division, Shifts, Comparisons).