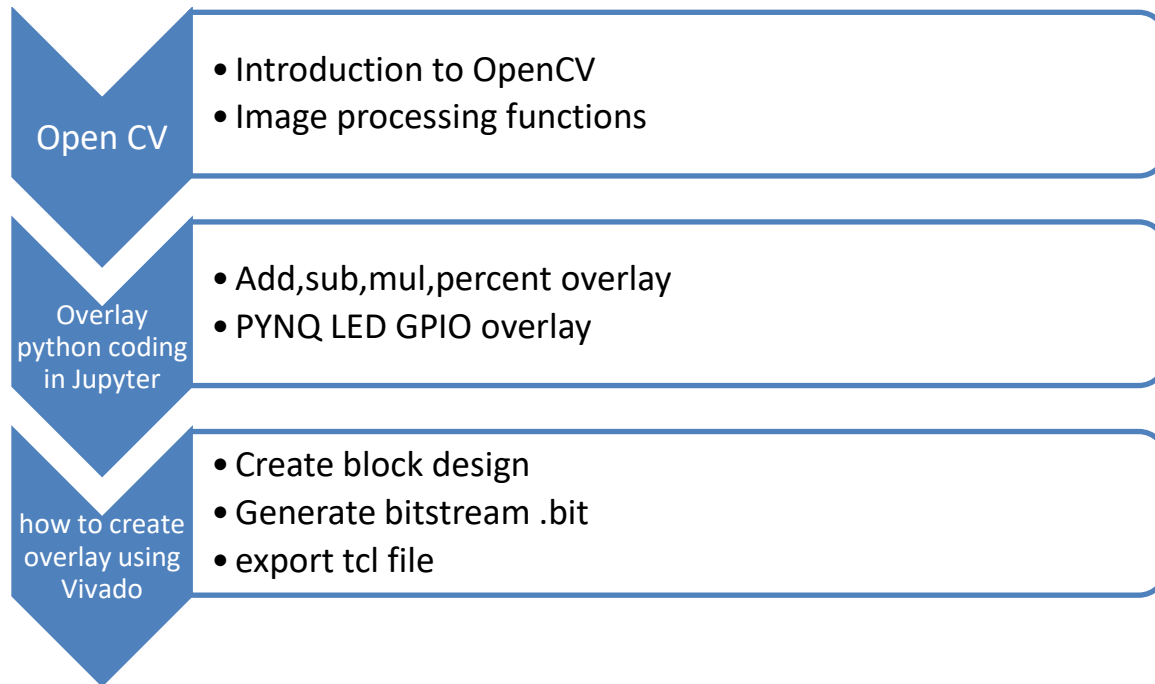


# Laboratory on vivado using PYNQ FPGA

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## Flow of Laboratory:



Install Angry IP scanner to know IP: <https://angryip.org/download/#windows>

## PYNQ Jupyter

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User name: xilinx

Password: xilinx

Copy files in pynq board from github use command “git clone link of github”

GitHub:<https://github.com/UMONSMicroelectronics>

Mail ID: [patelmonalumons@gmail.com](mailto:patelmonalumons@gmail.com)

# Steps for creating Overlay in VIVADO

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**Note:** To see Device PYNQ in tools, download zip folder from given link and put in VIVADO >Board parts

[https://github.com/cathalmccabe/pynq-z1\\_board\\_files](https://github.com/cathalmccabe/pynq-z1_board_files)

## **Tutorial:**

[https://pynq.readthedocs.io/en/v2.5.1/overlay\\_design\\_methodology/overlay\\_tutorial.html](https://pynq.readthedocs.io/en/v2.5.1/overlay_design_methodology/overlay_tutorial.html)

<https://discuss.pynq.io/t/tutorial-creating-a-hardware-design-for-pynq/145>

**Step 1:** Open **vivado HLS** 2020.1 or 2018.2 (**Note:** Version for vivado is important)

**Step 2:** Create new project>project configuration>add files>device selection (PYNQ Board)

**Step 3:** Put C coding of IP in .cpp file it's in Source >save file>run C Synthesis >generated synthesis report

**Step 4:** Export RTL

**Step 5:** Make note of register offsets , check in Solution 1>impl>misc>drivers>add v1>src>hw.h file

**Step 6:** Open **VIVADO** 2020.1 or 2018.2

**Step 7:** create new project>project name>project type>device selection>finish

**Step 8:** click on Create block Design >add ip using (+) ZYNQ Processing >run block automatic

**Step9:** Add IP of adder or... go to tools>setting>IP>repository>add files which we created using vivado hls(created IP)

**Step 10:** add ip of adder or....> in block property change name i.e scalar\_add>run block automatic

**Step 11:** Source >design1 right click >create HDL Wrapper

**Step12:** Generate bit stream

**Step13:** Generate TCL File >go to file>export>export block design

**Step 14:** Upload .bit and .tcl file in PYNQ Board and check overlay using python

# **Lab.1**

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## **Latest version of PYNQ Manual:**

<https://buildmedia.readthedocs.org/media/pdf/pynq/latest/pynq.pdf>

## **PYNQ Board reference Manual:**

[https://reference.digilentinc.com/\\_media/reference/programmable-logic/pynq-z1/pynq-rm.pdf](https://reference.digilentinc.com/_media/reference/programmable-logic/pynq-z1/pynq-rm.pdf)

## **Downloadable PYNQ Image:**

<http://www.pynq.io/board.html>

## **PYNQ Tutorial :**

[https://github.com/Xilinx/PYNQ\\_Workshop](https://github.com/Xilinx/PYNQ_Workshop)

## **Overlay Create Tutorial**

[https://pynq.readthedocs.io/en/v2.5.1/overlay\\_design\\_methodology/overlay\\_tutorial.html](https://pynq.readthedocs.io/en/v2.5.1/overlay_design_methodology/overlay_tutorial.html)

<https://discuss.pynq.io/t/tutorial-creating-a-hardware-design-for-pynq/145>