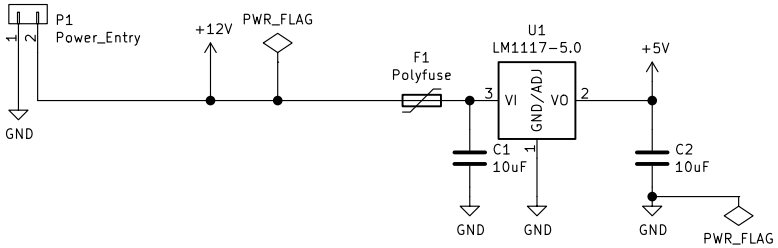

NOTES:
R3 * C3 = a time constant such that it takes 500ms for the SD line to go low when both comparator outputs are low. Given the diode drop and the logic-low threshold of the flipflop, RC = 1.2 (approximately). (0.3 * VCC) = (VCC - 0.7)*(1-e^(-0.5/(RC))
There is no hysteresis on the comparators because the impedances between In+ and VCC/GND are variable. In practice this should not be an issue due to the long time constant of the RC pair. The polyfuse should have a 1A trip current (a fault would be much greater than that).
The theoretical current consumption of the circuit is on the order of 10's of mA.