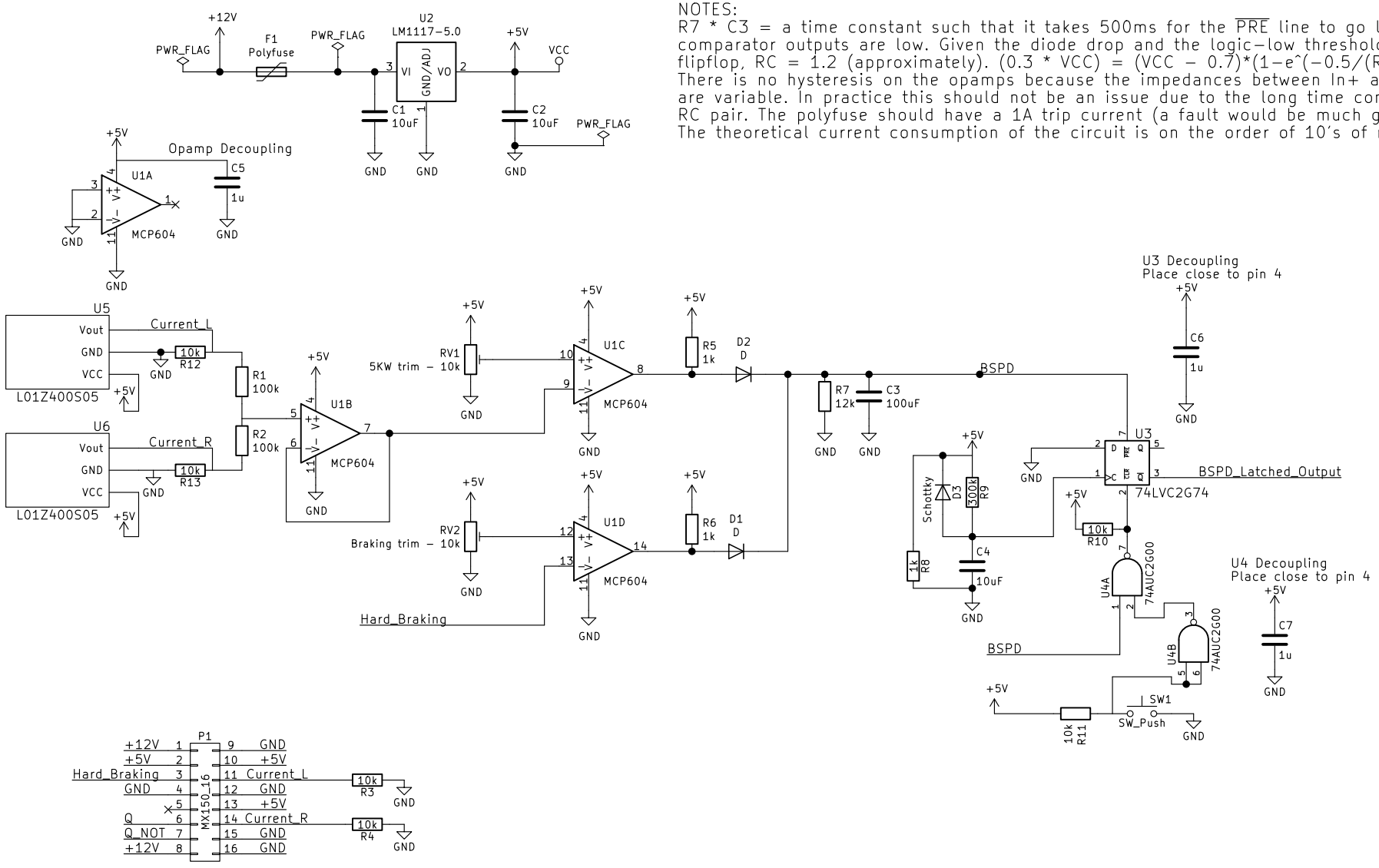
NOTES:
R7 * C3 = a time constant such that it takes 500ms for the PRE line to go low when both comparator outputs are low. Given the diode drop and the logic-low threshold of the flipflop, RC = 1.2 (approximately). (0.3 * VCC) = (VCC - 0.7)*(1-e^(-0.5/(RC))
There is no hysteresis on the opamps because the impedances between In+ and VCC/GND are variable. In practice this should not be an issue due to the long time constant of the RC pair. The polyfuse should have a 1A trip current (a fault would be much greater than that).
The theoretical current consumption of the circuit is on the order of 10's of mA.
+12V
PWR_FLAG
F1
Polyfuse
U2
LM1117-5.0
VI
GND/ADJ
VO
+5V
VCC
C1
10uF
C2
10uF
Opamp Decoupling
U1A
MCP604
C5
1u
U5
L01Z400S05
Vout
GND
VCC
Current_L
R12
10k
R1
100k
U6
Current_R
R13
R2
100k
U1B
RV1
5KW trim - 10k
U1C
R5
1k
D2
R7
12k
C3
100uF
BSPD
RV2
Braking trim - 10k
U1D
R6
1k
D1
Hard_Braking
U3 Decoupling
Place close to pin 4
C6
1u
U3
74LVC2G74
BSPD_Latched_Output
Schottky
D3
300k
R9
C4
10uF
R8
1k
R10
10k
U4A
74AUC2G00
U4B
U4 Decoupling
Place close to pin 4
C7
1u
SW1
SW_Push
R11
10k
P1
MX150_16
+12V
+5V
Hard_Braking
GND
Q
Q_NOT
Current_L
Current_R
R3
10k
R4
10k