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ELECTRONICS LABORATORY EXPERIMENTS ACCESSIBLE VIA INTERNET

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1.1 INTRODUCTION

Remote-distance, interactive learning is an important emerging educational trend. The Internet is an ideal medium for remote instruction purposes, offering interesting possibilities for disseminating educational material to students, both locally and as part of remote education. Its ubiquity and protocol standards make data communication and front-end graphical user interfaces relatively easy to implement.

Laboratory experiments are an indispensable part of engineering education that until recently have been considered impractical for distance learning. However, the advances over the last decade in the Internet, World Wide Web tech-

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nologies, and computer-controlled instrumentation presently allow net-based techniques to be utilized for setting up remote laboratory access, permitting remote education to be enhanced by experimental modules.

Currently, remote educational laboratories over the Internet, particularly in the area of electronics and instrumentation, have become operational at several sites (see Shen et al., 1999; Gustavsson, 2001; Geoffroy et al., 2001; Berntzen et al., 2001; del Alamo et al., 2002; Wulff et al., 2002; Söderlund and Jeppson, 2002). With these facilities, novel pedagogical uses have also emerged, including experimental demonstrations to enhance traditional classroom lectures, adding laboratory modules as homework exercises in regular courses, establishing studio classrooms where students do supervised laboratory exercises on individual terminals, and encouraging individual discovery activities among students. All of these activities fit nicely into a modern strategy for distance learning.

In a broader perspective, the Internet lab technology can be offered to remote students on a global scale, removing a major obstacle for establishing a boundless and complete remote engineering education curriculum. As an added benefit, such systems may offer students the opportunity to work with sophisticated equipment of the kind they are more likely to find in an industrial setting and that may be too expensive for most schools to purchase and maintain for educational purposes.

Our work on remote lab systems started in 1997 as a collaboration between Rensselaer Polytechnic Institute (RPI) in Troy, New York, and the Norwegian University of Science and Technology (NTNU) in Norway. Presently, we operate three sites: AIM-Lab (Automatic Internet Measurement Laboratory) at RPI, LAB-on-WEB at UniK—University Graduate Center near Oslo, Norway (affiliated with NTNU and the University of Oslo), and NGL (Next Generation Laboratory) at NTNU in Trondheim, Norway. At these sites, we have explored and developed different system technologies, as will be explained below and in Chapter 4 of this book. However, all systems are based on a server-client architecture, where the clients (students) communicate over the net with a server and its experimental setup using modern web browsers. For the most part, we have developed dedicated system software that does not require any download by the client, but in some cases optional solutions are offered based on software that can be downloaded from the Internet for free.

Biased by our background in physics and electronics, we have emphasized the establishment of laboratories dedicated to semiconductor device characterization, with experiments performed on microelectronic test chips and on commercial devices. Our labs have been used in courses on semiconductor devices and circuits at the senior or first-year graduate level at all our institutions. At our sites in Norway and the United States, we have jointly investigated several practical solutions for establishing such laboratories. Central objectives were to create a user-friendly and efficient technology for interactive, on-line operation of the lab experiments, to allow communication with minimum overhead, to

provide a functional client interface, to establish a variety of experiments, and to allow flexibility in configuring experiments from the client side.

The AIM-Lab site at RPI is based on a TCP/IP (Transmission Control Protocol/Internet Protocol) communication solution, which uses a Java applet on the client side. This was achieved by means of a JVM (Java virtual machine) in the web browser that can download and execute Java code. The client sees a pop-up window that provides interaction and communication directly with the server. This system is described in Section 1.2.

LAB-on-WEB at the UniK site relies on modern web and instrument control technologies, including COM+ (component object model with extensions), ASPs (active server pages), ISAPI (Internet server application programming interface), and LabVIEW (Laboratory Virtual Instrument Engineering Workbench) version 6i from National Instruments. Advanced functionalities of modern web browsers are utilized, allowing the system to communicate in terms of XML (eXtensible Markup Language) and SVG (scalable vector graphics). SVG is a vector-based, open-standard file format developed by the World Wide Web Consortium, which represents a new generation of dynamic, data-driven, and interactive graphics. The LAB-on-WEB system is described in Section 1.3.

At the NGL site at NTNU, Microsoft's new .NET technology was adopted. This solution is described in Chapter 4 of this book.

In Section 1.4, we discuss by way of examples some of the experiments available at AIM-Lab and LAB-on-WEB.

This presentation emphasizes the technological aspects of our remote lab systems and the specific experiments offered. We have so far not performed systematic evaluations of the educational benefits derived from using these labs. Obvious benefits to the students are apparent in terms of availability and ubiquity, likewise the presentation of “live” lab demonstrations in the classroom. Our subjective impressions are that the students show a positive interest and curiosity, and we register a positive attitude to the freedom offered in terms of scheduling their lab sessions.

1.2 AIM-LAB AT RPI

1.2.1 System Architecture

The AIM-Lab system architecture is shown in Figure 1.1. The server, written in Microsoft Visual C++, includes two main components. One of them is a TCP/IP server socket that receives commands sent over the Internet. The second component, the driver interface layer (DIL), interfaces between the instrument driver and the higher levels of the server (Shen et al., 1999; Fjeldly et al., 2000). The DIL sends the commands to the instrument driver, which uses the GPIB (general-purpose instrument bus) Institute of Electrical and Electronics Engineers (IEEE) 488.2 standard protocol to drive the instruments. A third com-

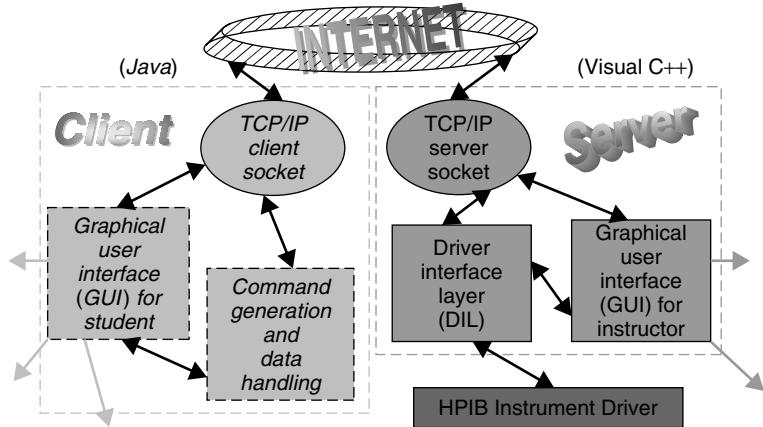


Figure 1.1 System configuration for AIM-Lab using TCP/IP communication (after Shen et al., 1999).

ponent is the GUI (graphical user interface) for the instructor. This interface on the server side allows the instructor to monitor and control the server process as well as modify the configuration of the instrumentation.

The client side is a Java applet that initially appears as a push button on the AIM-Lab web page. By pressing the button, the applet creates a pop-up window that provides the GUI interface to the user. The client's command generator issues commands according to the parameter set specified by the user and sends them via the TCP/IP client socket to the server. The experimental results sent back by the server are then handled and displayed in the client window.

In AIM-Lab, Java is the programming language of choice on the client side, since it offers the flexibility of a GUI design, convenient network programming, and platform independence. The operation is achieved by means of a JVM in the client's web browser that can download and execute Java code. The client sees a pop-up window that, on the one hand, provides GUI interactions to the user and, on the other hand, communicates directly with the server. The GUI interface is created according to the information on the experiments received from the server upon client initialization.

The AIM-Lab system is designed to minimize the overhead of the data communication through the Internet, maximize the server performance and efficiency, ensure the data accuracy and integrity, and provide an easy access to the user. In order to maximize the server performance and efficiency, we developed the server as a Windows-based MDI (multidocument interface) application. This is a multiuser and multiexperiment environment with a task queue. For each user, it records all the commands and data in a dedicated document window.

The experiment requests are sent to the instrument driver in the order of

receipt, and the resulting data are sent back accordingly. No experiment failure or error caused by the clients leads to a malfunction of the server. Any experiment that takes an exceedingly long time to finish (which might suggest a failure) is discarded and hence does not affect the other experiments. The server does not parse or interpret the commands. It assumes that the command generator of the client program correctly generates the commands. In case of an error, the server will discard the commands as described above. This reduces the processing overhead of the server and makes the server very flexible. When an instrument or a circuit is changed, the server sends the information about the change to all the running clients.

1.2.2 AIM-Lab Operation

The system provides easy access for the user and maximizes the speed of the on-line measurements. No file needs to be downloaded in order to perform the experiments, which is an advantage compared to other realizations in terms of speed and security. All the user has to do is to access the AIM-Lab website (<http://nina.ecse.rpi.edu/shur/remote/>) and start the client window by pressing a button. The user can set up experiments and send experiment requests by activating pop-up dialog boxes. The results of the measurements are displayed in the client window, and the user can navigate between the experimental plots with ease. The resulting data and plots can be saved using **Copy** and **Paste** functions of the Windows and Unix systems.

The communication overhead is minimized by sending only the absolutely necessary information via the Internet and by organizing the generated commands, data results, and server messages in the most compact format. We have tested the system off-campus using a commercial 56-kbps modem. According to our test, the time needed to access the website and start the client window is about 50 sec. It takes less than 10 sec for the system to perform a complete experiment, including sending commands and receiving and plotting the data.

The user accesses the AIM-Lab website using a standard web browser. When logging in, the server application is launched and all information on the available experiments is read from a library file and sent to the client. The client window behaves as a stand-alone application in which the user selects an experiment and specifies experimental parameters (e.g., voltage range, step size) in pop-up dialog boxes. Consecutive experiments can be set up and sent to the server without waiting for the previous experiment to finish. An experiment is initiated by activating the **Start Experiment** menu item in the **Operation** pop-up menu. Some of the client windows encountered are shown in Figure 1.2.

The instructions from the client are then sent via the TCP/IP client socket to the server, which runs the experiment and returns the experimental data to the client. The results are presented in the client browser window as columns of numerical data and a graph. The numerical data can be copied from the window for further processing by the user. As an example, Figure 1.3

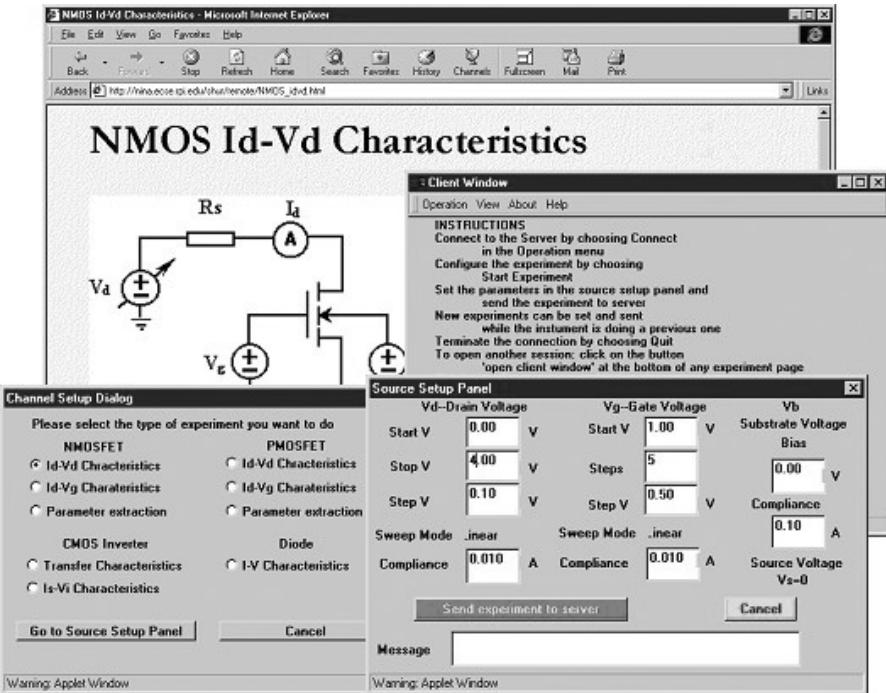


Figure 1.2 AIM-Lab client windows with information on experiment (background), with menus and instructions for running experiment (middle right), for selecting experiment (lower left), and with panel for setting experimental parameters and initiating experiment (lower right).

shows the current–voltage (I – V) characteristics of an n -channel metal–oxide–semiconductor field effect transistor (MOSFET).

Java applets provide good control. However, unsigned applets make it awkward for the client to store and present data received from the server side and to transfer them to other applications (except by cut-and-paste) because of Java’s security structure. A further problem with Java is that the functionality of an applet may vary between different browsers. While Java 2 has better support for the user interface, some of the new classes included in this version are not automatically compatible with JVM, requiring an additional plug-in to be installed in the browser. For many potential users, this is a problem, partly because of skepticism toward plug-ins and partly because of local security regulations in many organizations. Besides, the future support of Java is uncertain.

1.2.3 AIM-Lab Experimental Setup

1.2.3.1 Device Test Structures AIM-Lab is presently dedicated to the characterization of a group of test devices that includes a set of complementary metal–oxide–semiconductor (CMOS) devices and a set of light-emitting diodes

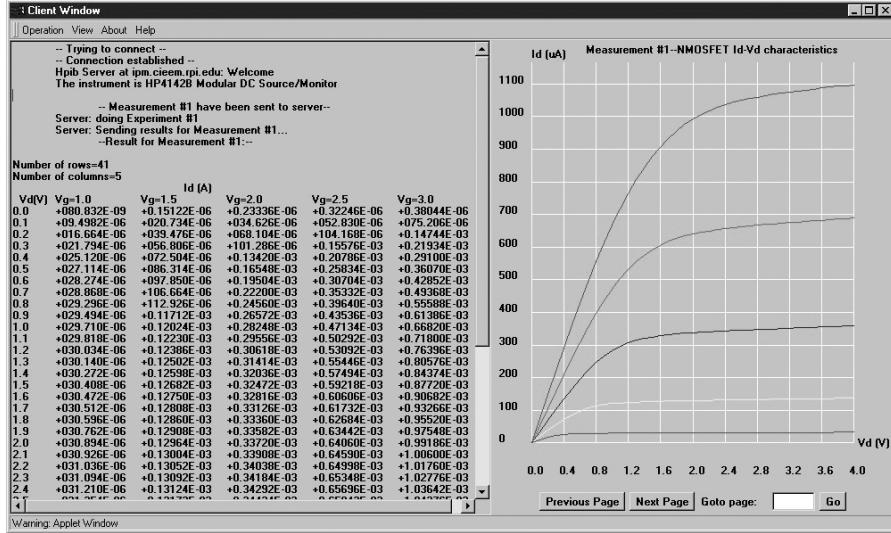


Figure 1.3 Example of AIM-Lab client-side window with experimental results (NMOS $I-V$ characteristics) corresponding to instructions submitted by client (see Figure 1.2).

(LEDs) made from different compound semiconductors. CMOS is the most important integrated circuit technology, far outselling all other semiconductor technologies, including bipolar, thin-film transistor (TFT), and compound semiconductor technologies. The importance and proliferation of CMOS necessitate a good understanding of its operation by very large scale integrated (VLSI) designers and users alike. The best way to teach the basics of CMOS technology is by a hands-on approach, which combines the basic theory of operation with measurements, parameter extraction, and CMOS circuit simulation (see Lee et al., 1993; Fjeldly et al., 1998).

AIM-Lab presently allows experiments to be performed on the CMOS test chip shown in Figure 1.4. This chip, designed, fabricated, and characterized by our group, includes two arrays of NMOS (n -channel MOSFET) and PMOS (p -channel MOSFET) devices with a wide range of gate geometries for the purpose of investigating the scaling properties of the devices. In each array, all source electrodes are interconnected, so are all the gates and all the substrate electrodes. Only the drain electrodes have separate contact pads. Additional diagnostic structures are also available, including a loaded and an unloaded ring oscillator. Since each experimental configuration is hard-wired at the server site, only a limited number of the possible experiments are available to the remote user at any given time. Presently, six experiments are specified, involving measurements of MOSFET and inverter characteristics used for device characterization.

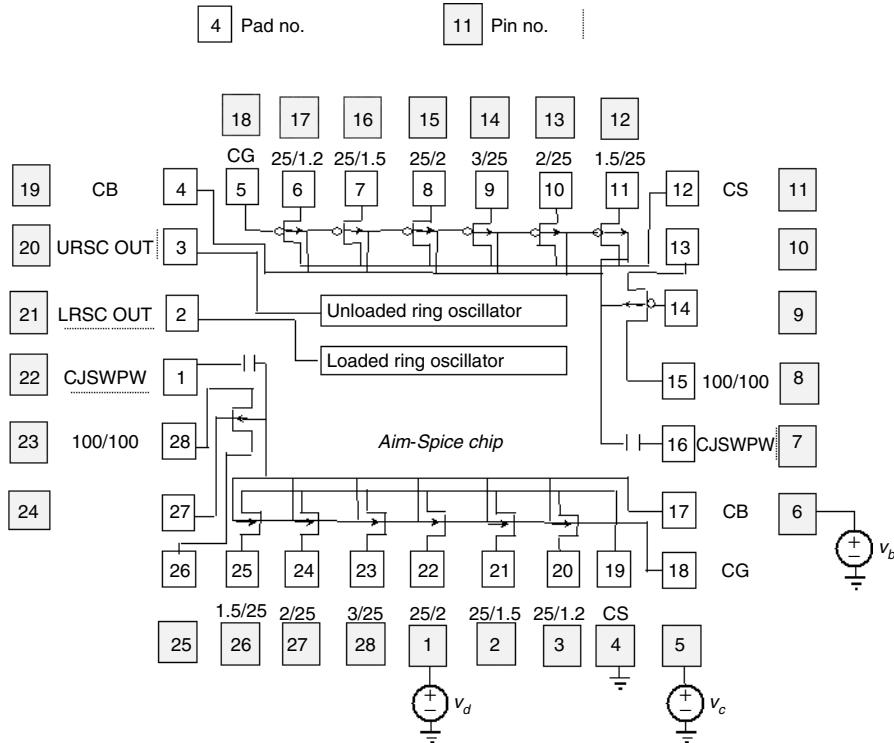


Figure 1.4 Layout of AIM-Spice CMOS test chip. PMOS and NMOS transistors of different dimensions are shown in upper and lower sections of chip, respectively. Gate width W and length L in micrometers are shown as W/L next to each MOSFET. Biases shown are those used for obtaining current–voltage characteristics of NMOS with $W/L = \frac{25}{2}$. (Shen et al., 1999).

Additional AIM-Lab experiments involve LEDs that emit light of different colors—green, yellow, and blue. The colors, or wavelengths, of the emitted light are related to the electronic band gaps of the compound semiconductor materials from which the diodes are fabricated. The band gaps can be roughly estimated from the turn-on voltages of the diodes, as observed by measuring the I – V characteristics. The emitted light colors from the different LEDs can be observed with a web camera.

1.2.3.2 AIM-Lab Instrumentation The experimental instrumentation in AIM-Lab consists of a Hewlett-Packard (HP 4142B) direct-current (DC) source/monitor with one source monitor unit (SMU) for each separate voltage source or measurement node. The sever is an HP D3695 host computer using the Microsoft NT operating system with Peer Web Services installed. An GPIB instrument driver installed in the host personal computer (PC) handles the communication with the HP 4142B instrument. The HP 4142B has a very high resolution and speed and an embedded processor that accepts high-level commands. However, this equipment is expensive and not very portable. In an

alternative configuration, we have also investigated the use of peripheral component interconnect/industry standard architecture (PCI/ISA) cards that can be installed in the expansion slots of the host PC (see Shen et al., 2000). In this case, the HPIB driver and the HP 4142B instrument were replaced by low-cost voltage output and data collection cards. These cards have simple functionalities for outputting a single voltage and converting it into a digital signal that can be read by the host PC. However, they suffer from lower resolution. Besides, the sampling resistors for the current measurements have to be selected with care.

1.3 LAB-ON-WEB AT UNIK

LAB-on-WEB at UniK in Norway was developed in several phases from 1999 to the present, mostly through student master's theses and externally funded projects, notably by Nordunet2, a program financed by the Nordic Council of Ministers. We initially explored alternative network and server solutions to those used in AIM-Lab (see Section 1.2), considering both ActiveX-based solutions, such as ISAPI and COM+, and LabVIEW solutions based on the Internet-adapted version 6i. Later, we investigated ways to use switching matrices for the purpose of expanding the number of available experiments and to enable on-line reconfiguration of simple circuits by the clients. The objective of the latter is to provide the students with more freedom to pursue "individual discovery."

The first complete lab system was built around the CMOS test chip shown in Figure 1.4. The central measurement instrument was the HP 4142B modular DC source/monitor with HP 41421B source monitor units (SMUs). Presently, we have replaced the test object by a more comprehensive CMOS lab-on-a-chip unit that allows a much richer variety of experiments to be performed (see Section 1.3.1.1). To fully utilize this potential, new instruments have also been added to the LAB-on-WEB setup.

1.3.1 LAB-on-WEB Experimental Setup

1.3.1.1 Alfa Chip Test Structure The present version of LAB-on-WEB includes a comprehensive electronic device laboratory on a chip that significantly enhances the learning experience of our remote lab. This so-called Alfa chip was developed as part of project number 3.0284.5 within the ALFA exchange program between universities in the European Union and Latin America under the auspices of the European Commission (see Delmas Bendhia et al., 1998). The project had participation from France (E. Sicard), Germany (F. Schwiertz), Mexico (E. Gutierrez), Norway (T. A. Fjeldly), Spain (E. G. Moreno), and Venezuela (A. O. Conde). The integrated circuit was designed by the ALFA partners using the Microwind* tool developed by Institut National des Sciences

*Microwind is a PC freeware tool featuring layout design and built-in analog simulation.

Appliquée (INSA), Toulouse (Sicard, 2000). The chip was fabricated at ATMEL Rousset in France using a two-metal 0.7- μm CMOS process.

The Alfa chip contains diodes, capacitors, transistors, inverters, and other test structures, all fabricated in CMOS technology. Besides providing a valuable familiarity with the static and dynamic behavior of the building blocks of modern integrated circuits, the lab is also designed for the extraction of device and processing parameters needed for circuit design. The extracted parameters are suitable for use with circuit simulators such as AIM-Spice (<http://www.aimsice.com>; see also Fjeldly et al., 1998) to predict the behavior of more complicated circuits such as the ring oscillator also included on the chip.

The Alfa chip layout is shown in Figure 1.5, where the relevant devices used by LAB-on-WEB are highlighted. The chip is packaged in a pin gate array

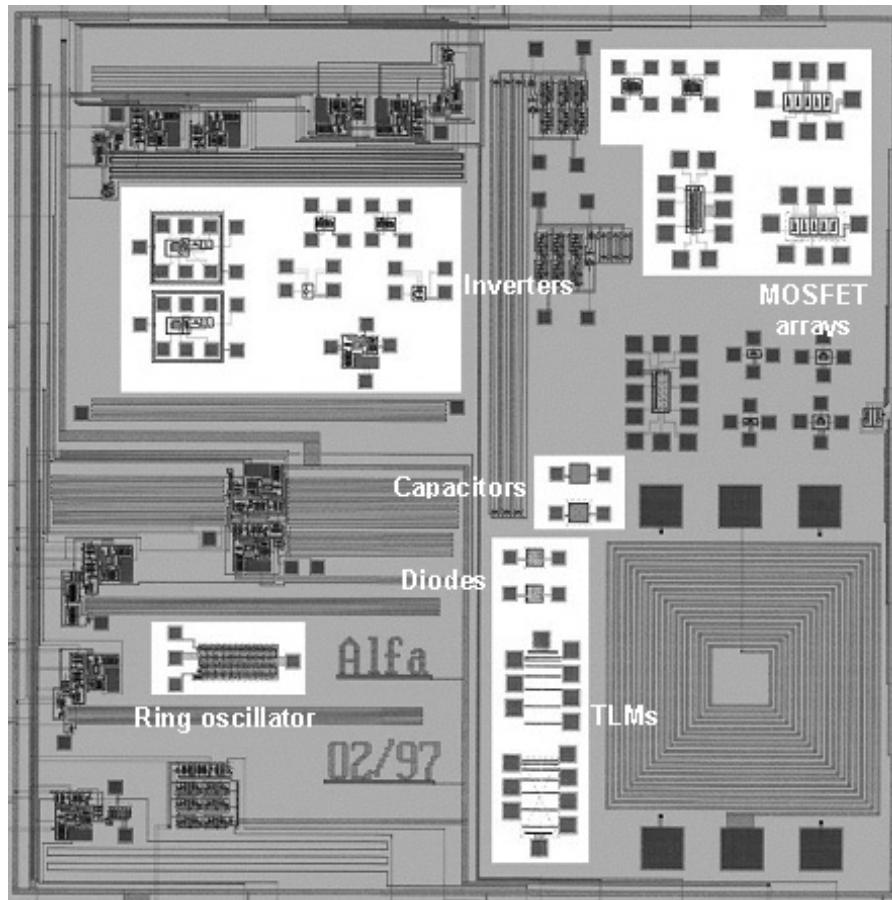


Figure 1.5 Alfa chip layout. Devices in highlighted areas are used in LAB-on-WEB (Fjeldly et al., 2002).

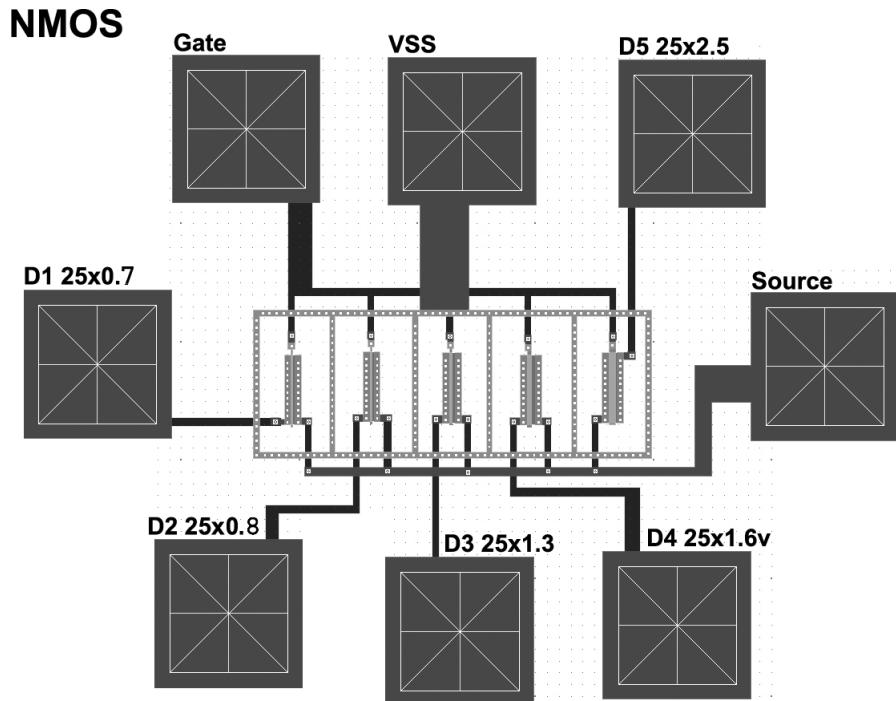


Figure 1.6 Layout of NMOS array. All gates are 25 μm wide while gate lengths vary between 0.7 and 2.5 μm . The Alfa chip also contains a PMOS array with the same geometries (Fjeldly et al., 2002).

(PGA) 144 chip carrier and the various contact pads, each of size $40 \times 40 \mu\text{m}^2$, are bonded to the carrier pins.

Figure 1.6 shows a more detailed view of the array of NMOS transistors located in the upper right corner of the Alfa chip. It contains five *n*-channel MOSFETs with a gate width W of 25 μm and gate lengths L varying from 0.7 to 2.5 μm . The MOSFETs have separate drain contacts, but all the gate electrodes are interconnected and so are the source contacts. The Alfa chip also contains a PMOS array with the same geometries. These arrays are suitable for characterization of individual MOSFETs, for extracting their model parameters, and for studying the effects of geometric scaling of these devices.

The Alfa chip includes two separate CMOS inverters with different geometries (upper left area of Figure 1.5). The one shown in Figure 1.7 has $W = 25 \mu\text{m}$ and $L = 0.8 \mu\text{m}$ for both the NMOS and the PMOS transistor. The second inverter has the same gate length but a gate width of 1.2 μm . Note that inverters with other geometries can also be formed by making suitable external connections between devices in the two MOSFET arrays discussed above.

A ring oscillator consists of a cascade of an odd number of inverters, where the signal from the last inverter is fed back into the first one. The individual

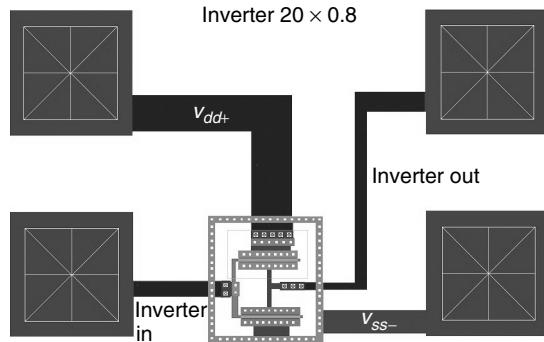


Figure 1.7 Layout of CMOS inverter with NMOS (lower) and PMOS (upper) devices both with gate width $W = 20 \mu\text{m}$ and gate length $L = 0.8 \mu\text{m}$. Alfa chip also contains CMOS inverter with $W = 1.2 \mu\text{m}$ and $L = 0.8 \mu\text{m}$ (Fjeldly et al., 2002).

elements are visible in Figure 1.8. The oscillation is triggered by an external signal input at the enable pad and is sensed at the output pad. The oscillation frequency is the inverse of the sum of the signal delays experienced by each inverter. The NMOS gate geometry is $W = 1.6 \mu\text{m}$ and $L = 0.8 \mu\text{m}$, and the PMOS gate geometry is $W = 2.4 \mu\text{m}$ and $L = 0.8 \mu\text{m}$. The difference in gate widths between the NMOS and PMOS serves to compensate for differences in electrical properties of the two types of devices. Hence, from a measurement of the oscillation frequency and using the number of inverters in the device, the single-stage delay can be extracted. This is a very important parameter that expresses the speed of digital signal transmission between the elements.

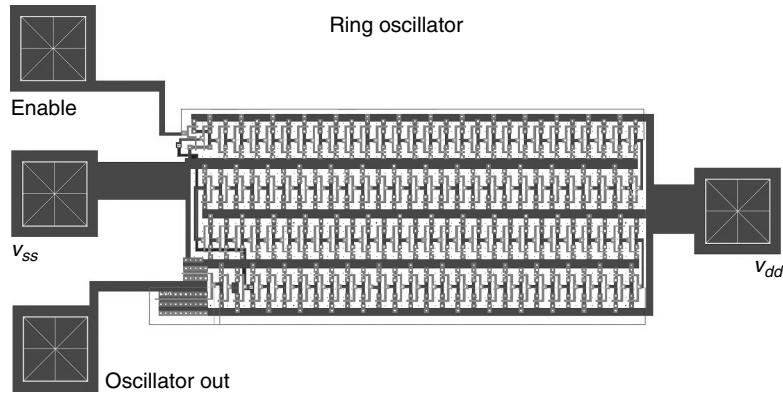


Figure 1.8 Layout of CMOS ring oscillator consisting of 110 inverters and one NAND gate at Enable pad. NMOS gate geometry is $W = 1.6 \mu\text{m}$ and $L = 0.8 \mu\text{m}$, and PMOS gate geometry is $W = 2.4 \mu\text{m}$ and $L = 0.8 \mu\text{m}$ (Fjeldly et al., 2002).

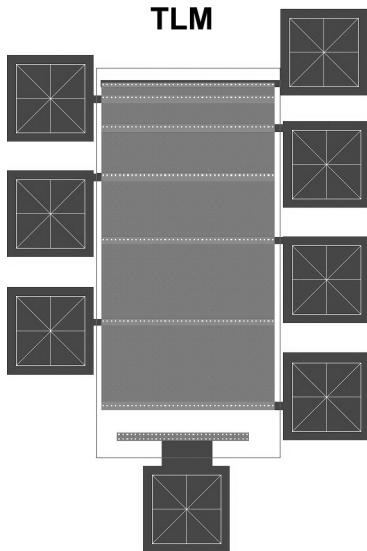


Figure 1.9 TLM pattern for determining contact and sheet resistance of ohmic contact regions (Fjeldly et al., 2002).

The structure shown in Figure 1.9 consists of a series of unevenly spaced electrodes across a region of doped material, typically of the same kind as that used in the ohmic source and drain regions of the MOSFETs. This structure is called a transmission line model (TLM) (see Shur, 1995). By measuring the total resistances between the adjacent contacts and plotting these versus their contact separations, the contact resistance can be determined by extrapolating the resulting straight line to zero separation. From the slope of this plot, the sheet resistance of the doped semiconductor region is found. The TLM regions are 120 μm wide and the distances between adjacent contacts are 5, 15, 25, 35, 45, and 45 μm .

In addition, the Alfa chip contains a pair of capacitors and a pair of diodes, which are very useful for the extraction of important parameters such as gate oxide thickness, parasitic capacitances associated with source and drain, flat-band voltage, and substrate doping.

Note that not all the devices described above will be made available at LAB-on-WEB at any given time. At times, LAB-on-WEB also will include experiments on other semiconductor devices and structures, including bipolar devices such as diodes and junction transistors.

1.3.1.2 Instrumentation The LAB-on-WEB server is a Dell Power Edge 4300 computer with a 500-MHz Pentium III processor, a Windows 2000 server operating system, and an MIIS (Microsoft Internet Information Server) version 5.0. The server and the instruments are connected via a GPIB.

The main instrument is an HP 4142B modular DC source/monitor, which is the same type of instrument as in the AIM-Lab setup. This is a high-speed,

accurate, and computer-controlled DC parametric measurement instrument for characterizing semiconductor devices. Voltages and currents can be applied or measured within 4 msec, and up to 1023 data samples can be stored in the internal memory. Up to eight different plug-in modules can be used with this instrument, allowing us to tailor the instrument to suit our needs. In our setup, three HP 4142B SMUs are installed, in addition to the built-in 0-V source GNDU (ground unit).

By means of a switch matrix, the client is given the option to remotely re-configure the experiment by changing the connections between the instruments and the CMOS test chip. This technique is still under development, and only a limited range of configurations are possible, serving merely as a demonstration of the functionality and potential of this approach.

A Tektronix TDS 3052, 500-MHz oscilloscope is also included, for both servicing and testing the setup but also for allowing the clients to measure transient events or waveforms.

Experimental Setup Version 1 The first version of the LAB-on-WEB server/laboratory setup is shown in Figure 1.10. Here, we used an HP 34970A data

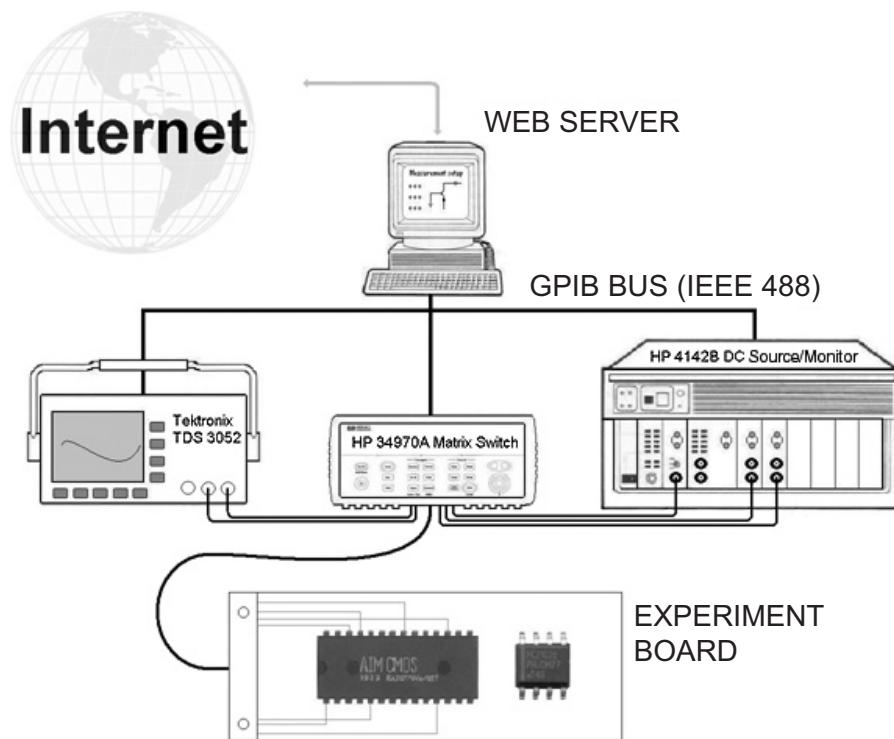


Figure 1.10 Setup of LAB-on-WEB version 1. Test objects to left on experiment board is AIM-Spice CMOS test chip (see Figure 1.4).

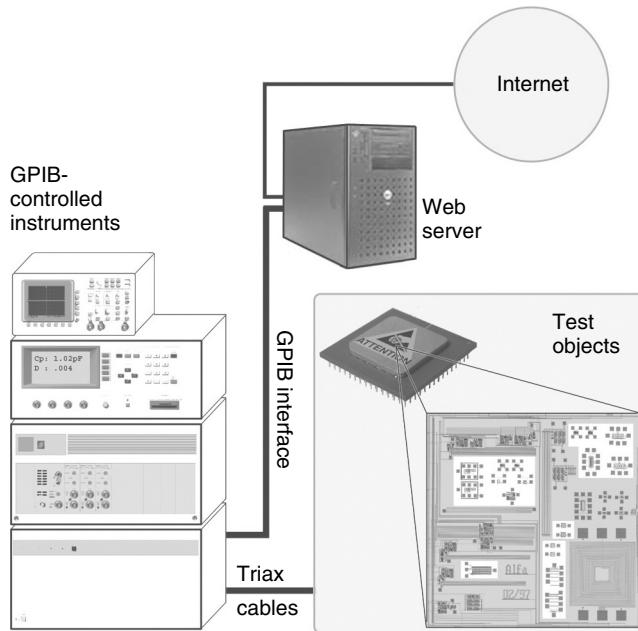


Figure 1.11 Setup of LAB-on-WEB version 2. Instruments to left are, from below, Agilent E5250A low-leakage switch unit, HP 4142B modular DC source/monitor with HP 41421B SMUs, Agilent 4284A precision *LCR* meter, and Tektronix TDS 3052, 500-MHz digital oscilloscope. Test object is Alfa chip discussed above (Fjeldly et al., 2002).

acquisition/switch unit with HP 34904A plug-in modules as a switch matrix. However, this instrument adds a fair amount of noise to the measurements, making it difficult to measure current levels below about 10^{-5} A. This is unacceptable for a precise characterization of reverse-bias currents in bipolar devices and of subthreshold behavior in field effect transistors (FETs). An alternative to HP 34970A is the much more expensive instrument Agilent E5250A low-leakage switch unit used in the second version of LAB-on-WEB (see below).

Experimental Setup Version 2 The current experimental setup of the LAB-on-WEB server/laboratory unit is shown in Figure 1.11. It includes the same instruments as in version 1, except that the HP 34970A data acquisition/switch unit was replaced by the Agilent E5250A low-leakage switch unit to allow measurements of ultralow currents (the former instrument can, of course, still be used in parallel with the new one for less sensitive applications). The switch mainframe is equipped with two E5252A 10×12 matrix switch plug-in modules, for a total of 10 inputs and 24 outputs. A maximum of four modules can be installed, creating a 10×48 matrix. Figure 1.12 shows a block diagram of

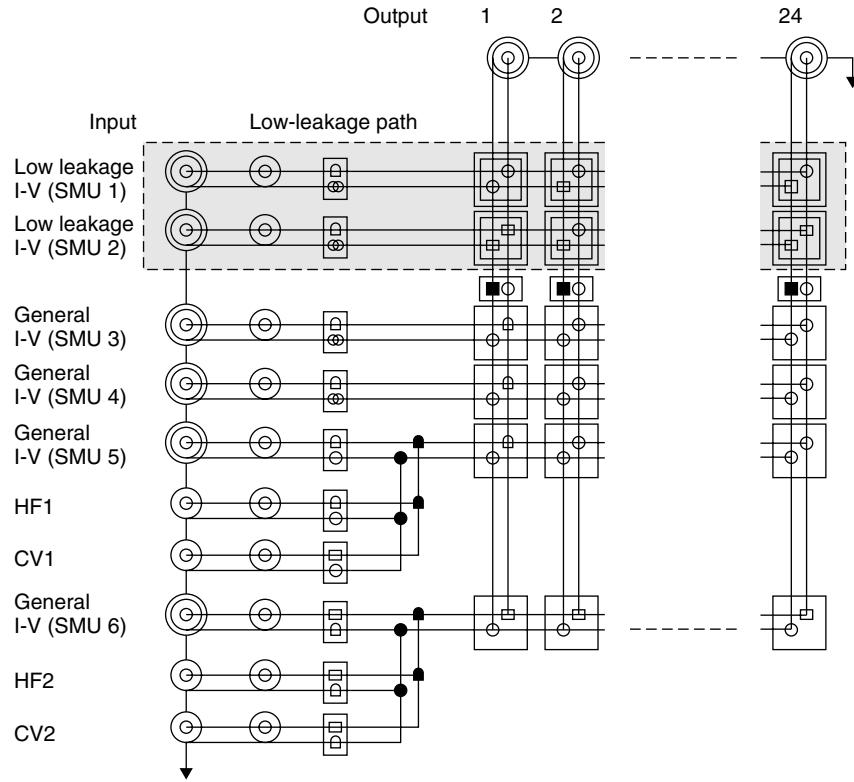


Figure 1.12 Block diagram of low-leakage switching matrix.

the low-leakage switching matrix. Among the 10 inputs are 2 each for low-noise I - V , capacitance–voltage (C - V), and high-frequency measurements.

The present setup also includes an Agilent 4284A precision LCR (induction, capacitance, and resistance) meter for measuring C - V characteristics.

1.3.2 LAB-on-WEB Architectures

Compared to AIM-Lab, LAB-on-WEB is based on more flexible solutions that utilize the rich functionalities of modern web browsers, allowing the server system to respond in many different formats, such as JavaScript, HTML (HyperText Markup Language), XML, and SVG, which give the client great flexibility in storing, processing, and presenting the data received (Berntzen et al., 2001). Among the server-side web solutions investigated are ISAPI server extensions COM+ (Strandman et al., 2002) and .NET (see Chapter 4 of this book).

Another alternative investigated is the use of the LabVIEW 6i software from National Instruments (Berntzen et al., 2001). In this solution, the server runs a

full version of LabVIEW 6i, which incorporates Internet communication capabilities and functionalities to access and control instruments and to obtain and return data. The client can communicate with the server and the experimental setup in two ways: by means of a web browser, which runs a dedicated CGI (common gateway interface) script in the server, or using the LabVIEW Player (alternatively, the full version of LabVIEW 6i).

1.3.2.1 ISAPI Server Extensions The ISAPI server extensions enhance the capabilities of the HTTP (Hypertext Transport Protocol) server included in the MIIS, allowing browser programs to interact with scripts or separate executable programs running on the server. Compared to the CGI standard incorporated into HTTP, the ISAPI extensions are faster and have added functionality.

ISAPI server extensions are implemented as a DDL (dynamic link library) file on the web server. For our purpose, they are programmed in Visual C++ by means of a wizard that comes with Microsoft Visual Studio. In response to calls from the client, they return HTML or XML code that can include Java-Scripts or applets, allowing the data to be presented as rich graphs and tables in the client terminal.

In addition to the ISAPI extensions, different kinds of ISAPI filter functions can be implemented to perform various useful tasks. Port management and encryption filters can provide access control, data encryption, and server authentication. The log filter can trap client information, from which an activity log can be created. The page translation filter can be used to transform XML to, for example, HTML or WML (Wireless Markup Language) using XSL (Extensible Stylesheet Language) stylesheets. The XSL transformation can take place either on the client side or in the server based on logged information about the client web browser.

The ISAPI solution is shown schematically in Figure 1.13. This solution was tested and found to be quite satisfactory. However, it is presently not implemented in LAB-on-WEB since the solutions discussed below were found to be superior in several respects.

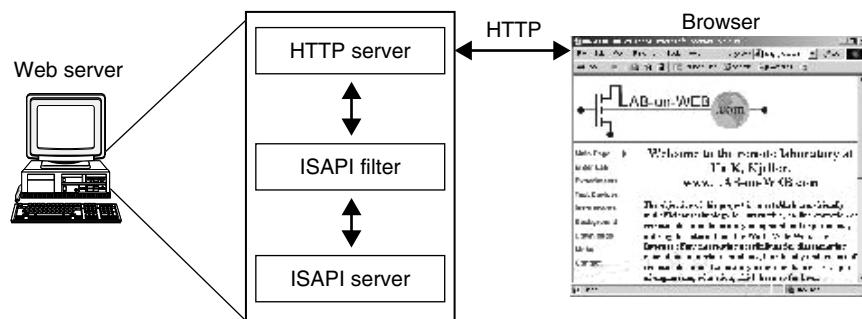


Figure 1.13 ISAPI architecture (Strandman et al., 2002).

1.3.2.2 COM+ Solution COM+ is the second generation of COM (component object model), which is a set of services that allows us to create object-oriented, customizable, and upgradeable, component-based, distributed applications. One of the primary goals of COM is to ease the creation of multilayer applications that can be reused from any programming language. COM+ includes added features that make COM easier to use and simplifies the development. Some of these features are component load balancing, just-in-time activation, asynchronous method invocation, in-memory database, queued components, and improved administrative services.

COM+ applications are typically middle-tier applications; that is, they move information between clients and back-end resources such as databases (in our case, measurement data from instruments). The COM+ component developed for the remote laboratory is a library application that is compiled to a DLL and is loaded into the process of the client. The LAB-on-WEB communication process is indicated in Figure 1.14. In this architecture, the COM+ component

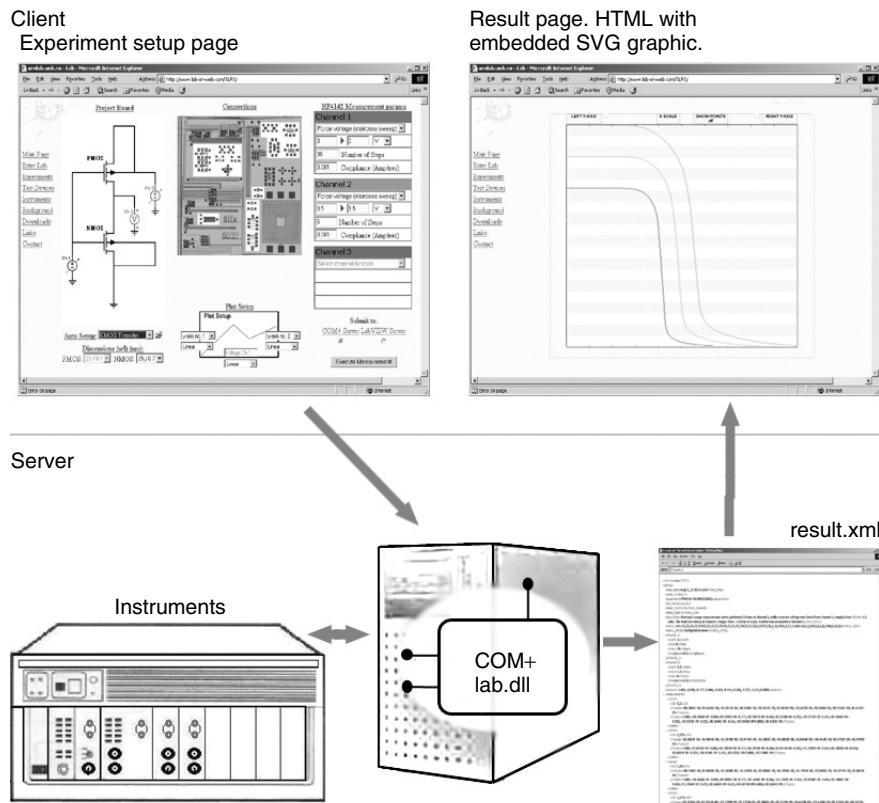


Figure 1.14 LAB-on-WEB architecture based on COM+ solution. From SVG client interface (upper left), client calls COM+ component via ASP. Measurement data are returned in XML format and presented in client browser (upper right).

is called from an HTML form in the active client page (see below) via an ASP, initiating the transfer of specifications on the desired measurement series to be performed. Subsequently, the instrument receives the necessary commands to perform the measurements. When the series is completed, the ASP receives the measurement results from the component and relays them to the client in XML format. The presentation of the results in the client browser can, for example, be in the form of an SVG plot along with a table of the raw data. The graph shown in the upper right of Figure 1.14 is an example of how data can be presented in the client browser using the SVG graphics.

LabVIEW version 6i from National Instruments is a powerful graphical programming development environment for data acquisition and control, data analysis, and data presentation. It comes with advanced Internet-ready capabilities and the concept of measurement intelligence, which includes automatic measurement hardware configuration for fast application development. Instead of writing program code, we build virtual instruments (VIs) with front-panel user interfaces that may contain, for example, numeric displays, meters, charts, and advanced graphs. The functionality is specified in block diagrams. The VIs allow control of any GPIB instrument.

In LAB-on-WEB, the client may execute experiments in two different modes, either with the executable LabVIEW Player (alternatively with the full LabVIEW 6i) or using a web browser.

LabVIEW Player is available free of charge from National Instruments. It is designed specifically for sharing measurement and automation knowledge across the Web in the form of secure LabVIEW VIs. By downloading and installing LabVIEW Player, the client can open and run LabVIEW VIs located in the LAB-on-WEB server. Player is equipped with functionalities for processing the data received to fit the user's need. Hence, clients obtain test results and measurement data from remote locations by means of built-in Internet tools. LabVIEW Player is richly equipped with functionalities for manipulating the data received and the graphs generated to fit the user's need. When further analysis is needed, the experimental data received by the client can be forwarded to an Excel document with the push of a button.

A drawback of LabVIEW Player is its considerable size, about 17.2 MB. This makes it inconvenient for downloading via a telephone modem for home use.

Using the LabVIEW Internet Developers Toolkit, it is possible to utilize the built-in HTTP server to make the VI front panels viewable from regular web browsers by means of CGI scripts. This solution provides additional flexibility in the transmission of measurement data, permitting different formats such as JavaScript, HTML, or XML. Hence, in this case, there is no need to download the large LabVIEW Player executable, allowing, for example, the interactive SVG client windows, such as the one shown in the upper right of Figure 1.14, to be used for configuring experimental setups. Figure 1.15 shows an example of a LabVIEW VI diagram with building blocks constituting a CGI solution.

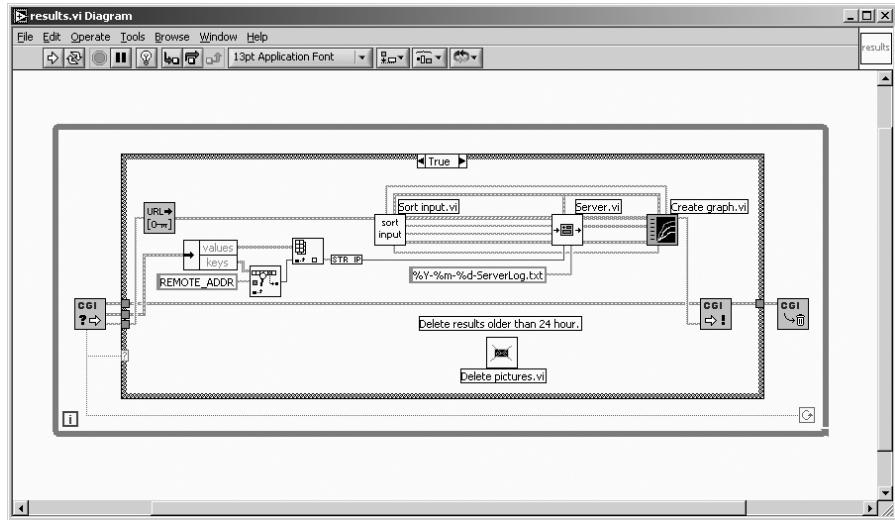


Figure 1.15 Block diagram of LabVIEW virtual instrument for CGI solution.

1.3.3 LAB-on-WEB Client Interfaces

An important aspect of using the Internet for educational purposes is to provide a user-friendly client-side interface designed to enhance the learning experience. In our case, we had to weigh functionality against the use of lablike impressions. However, we decided to use images of circuits and instrument to visualize the selections made by the client, including the interactive reconfiguration of the experiments. Two versions of the main LAB-on-WEB client interface, one used with the AIM-Spice CMOS chip and the other with the Alfa chip, are shown below. These interfaces were realized by means of JavaScript and the SVG file format and are designed for use with all the system architectures described above when the client uses a web browser. However, to achieve a full functionality, the SVG plug-in is required.

As discussed above (see Section 1.3.2.3), we have also implemented two additional client interfaces based on LabVIEW.

1.3.3.1 SVG Client Interface Version 1 Figure 1.16 shows the client interface for the AIM-Spice CMOS chip. Several experimental configurations are prepared for direct selection, as indicated in the table at the lower left-hand side. By clicking on one of the entries in this table, an arrow will be displayed to confirm the selection made, and the corresponding circuit diagram pops up in the middle of the page. However, by clicking on the various elements in the circuit diagram, a given circuit configuration may be further customized, and the external connections between the instrument and the test chip, shown as color-coded lines in the upper right of Figure 1.16, will be updated. The experimental parameter settings are entered in the tables in the lower right. The

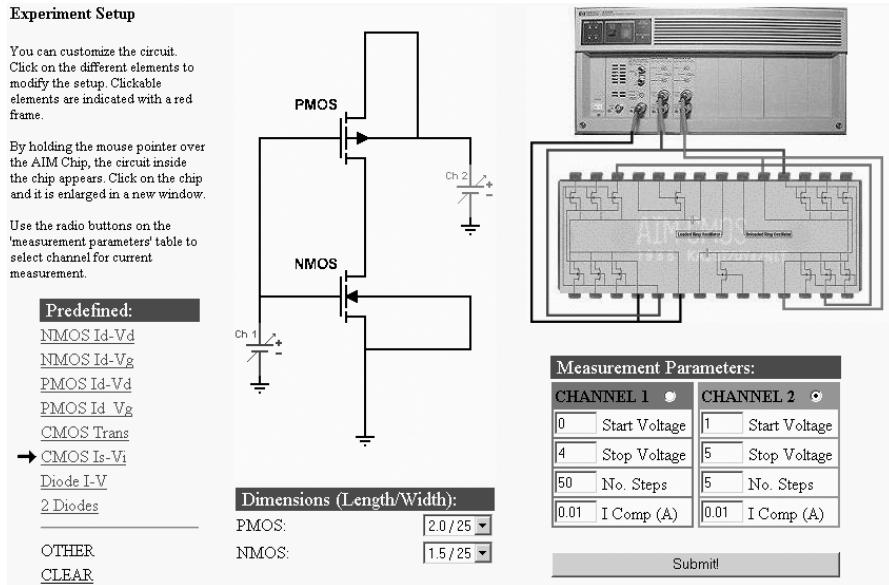


Figure 1.16 Version 1 of interactive SVG client window used for configuring experiments based on AIM-Spice CMOS chip and for setting experimental parameters. Selections are submitted by pressing Submit panel.

external connections are physically implemented via the matrix switch once the Submit button is activated.

1.3.3.2 SVG Client Interface Version 2 The client interface for the Alfa chip is shown in Figure 1.17. In this case, an even wider range of predefined experimental configurations are prepared for direct selection from the drop-down table at the lower left of the page. When a selection is made, the corresponding circuit diagram immediately pops up in the field above, and the upper middle field zooms in on the relevant part of the chip. Here, the external connections are indicated by matching color coding of the device pads and the force/sense elements of the circuit diagram. Again, by clicking on the various elements in the circuit diagram, the configuration may be further customized. The experimental parameter settings are entered in the tables to the right.

Using Plot Setup in the lower middle field, the client can configure the presentation of the experimental results. The diagram can be selected with one or two vertical axes, which can be individually formatted in a linear or a logarithmic scale.

The experiment can be directed to either the COM+ server or the LabVIEW server using the buttons in the lower right of the client page. The external connections are physically implemented via the matrix switch once the Execute Measurement field is pressed.

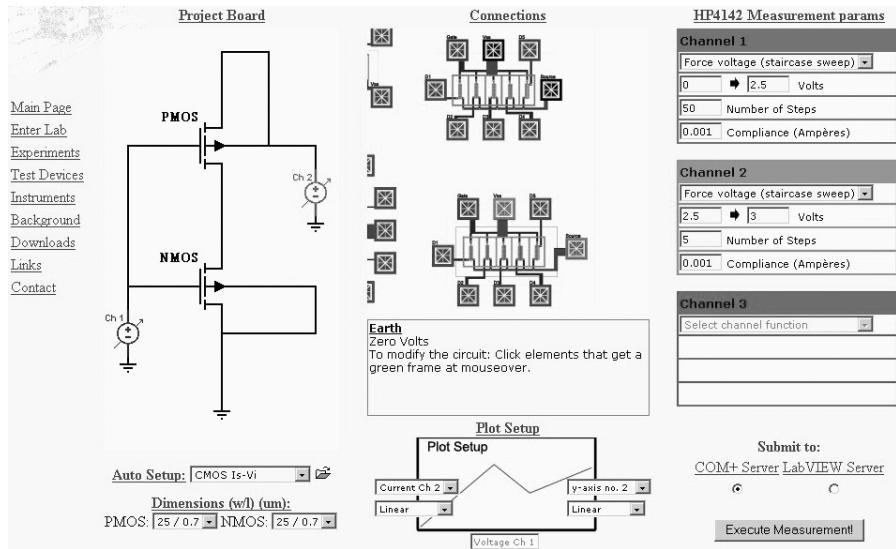


Figure 1.17 Interactive client interface for selecting and configuring experiments, setting experimental parameters, and specifying output graph. Selections are submitted by pressing Execute Measurement panel.

As an example of the SVG output using this client interface, Figure 1.18 shows the short-circuit current profiles obtained from an inverter connection in the Alfa chip.

1.3.3.3 LabVIEW Player Interface Figure 1.19 shows a LabVIEW VI client panel with a list of preselected experiments located in the upper left-hand side. Once an experiment is selected from this list, a corresponding circuit diagram pops up on the right. The experimental parameters are entered in the tables at the lower left side. Figure 1.20 shows an example of experimental CMOS inverter transfer characteristics obtained using the LabVIEW Player solution.

1.3.3.4 LabVIEW CGI Interface A dedicated client window for the LabVIEW CGI solution is shown in Figure 1.21. This interface can be selected from a web browser as an alternative to the LabVIEW Player interface of Figure 1.19. Figure 1.22 shows a presentation of NMOS characteristics obtained using the CGI interface.

By means of the built-in HTTP server, it is possible for the VI to respond to multiple clients and to continuously update their displays. This is an example of how the Toolkit libraries can be programmed to convert VIs into image files for

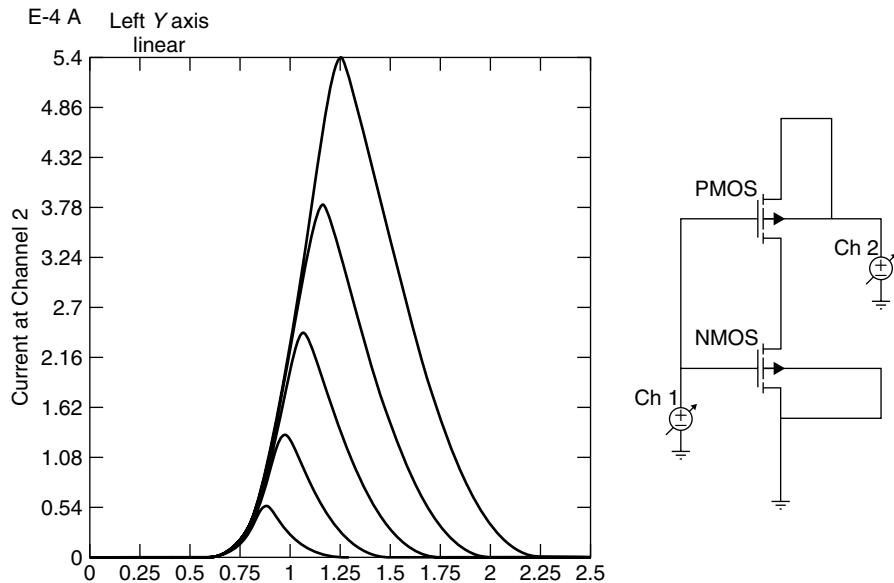


Figure 1.18 Short-circuit current profiles of inverter configuration of Alfa chip measured in Ch. 2 as function of input voltage at Ch. 1 at different supply voltages applied to Ch. 2.

display within HTML pages. Security levels can also be incorporated into the server to limit access to front panels and data. Likewise, access to the VIs can be password controlled based on the user's IP address.

1.4 EXAMPLE EXPERIMENTS

The following example experiments can be performed using either AIM-Lab located at RPI in Troy, New York, or LAB-on-WEB located at UniK near Oslo, Norway. The two sites can be accessed at <http://nina.ecse.rpi.edu/shur/remote> and <http://www.lab-on-web.com/>, respectively. Note that both system work best with MS Explorer.

The main page of AIM-Lab is shown in Figure 1.23. Using the various links on this page, information on the laboratory and the experiments can be obtained. The experiments can be accessed by selecting **Connect to the measurement setup** in the panel shown at the bottom.

The main page of LAB-on-WEB is shown in Figure 1.24. Using the various links on this page, information on the laboratory, the experiments, the instruments, and the test structures can be obtained. The client interfaces can be accessed by selecting **Enter Lab** in the panel to the left.

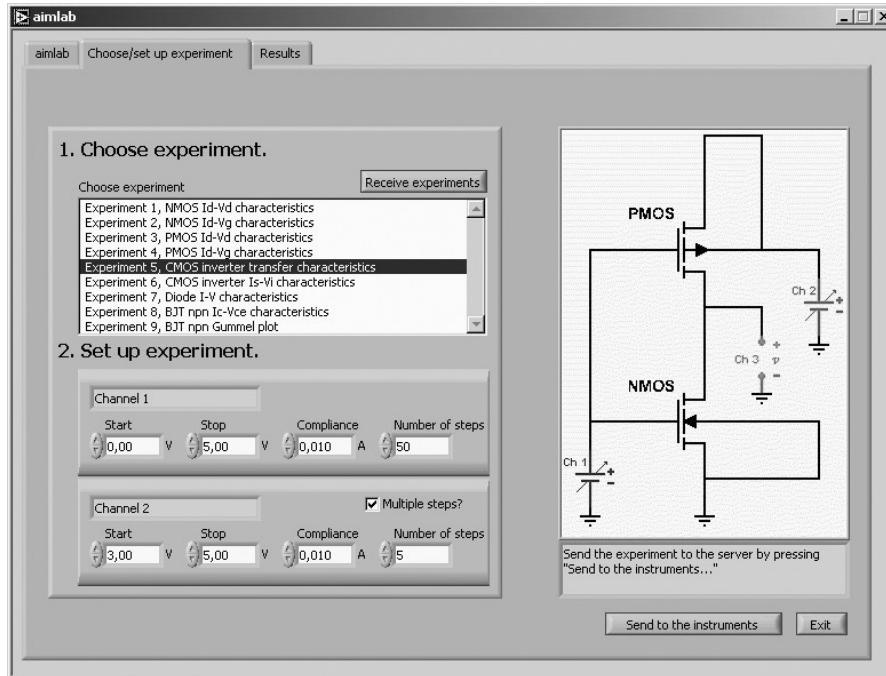


Figure 1.19 Interactive client interface for selecting and configuring experiments, setting experimental parameters, and specifying output graph. Selections are submitted by pressing **Send to Instruments** panel.

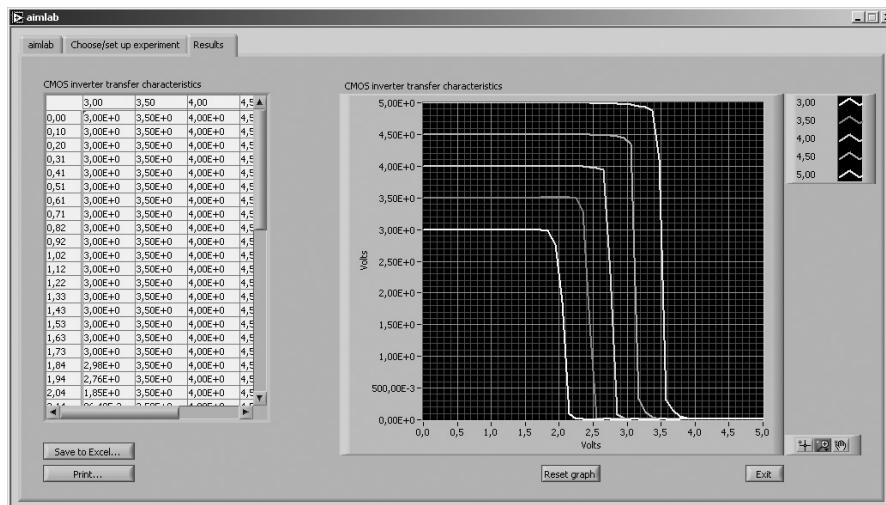


Figure 1.20 Measured CMOS transfer characteristics obtained using LabVIEW Player virtual instrument client window of Figure 1.19.

Experiment setup

Follow these three simple steps to make a measurement:

1. Choose one of the following experiments:

NMOS characteristics:

- NMOS Id-Vd Select dimension (width / length): ALFA NMOS 1
- NMOS Id-Vg Select dimension (width / length): ALFA NMOS 1

PMOS characteristics:

- PMOS Id-Vd Select dimension (width / length): ALFA PMOS 1
- PMOS Id-Vg Select dimension (width / length): ALFA PMOS 1

CMOS inverter characteristics:

- CMOS inverter transfer Select dimensions (width / length): PMOS: ALFA PMOS 1, NMOS: ALFA NMOS 1
- CMOS inverter Is-Vi Select dimensions (width / length): PMOS: ALFA PMOS 1, NMOS: ALFA NMOS 1

Diode characteristics:

- Diode I-V Select diode: Diode 1N4001

BJT characteristics:

- BJT npn i_C - V_{CE} Select BJT: AC127
- BJT npn Gummel plot Select BJT: AC127

2. Set up the voltage source(s):

Channel 1:

Start: V

Stop: V

Number of steps:

Compliance: A

Channel 2:

Start: V

Stop: V

Number of steps:

Compliance: A

3. Send to the server:

Do you want the results to open in a new window or in this window?

New window This window

Push the "Submit" button to send the experiment to the server.

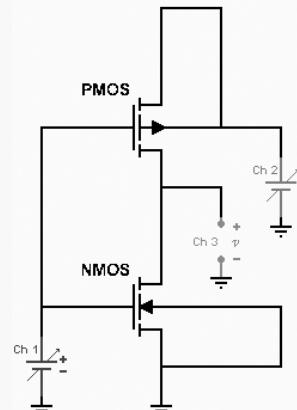


Figure 1.21 Client window used with LabVIEW CGI script for selection of predefined experiments and setup parameters.

1.4.1 AIM-Lab CMOS Experiment

1.4.1.1 CMOS Assignment

- Go to <http://nina.ecse.rpi.edu/shur/remote>.
- Scroll down and push the button marked Connect to the measurement setup.

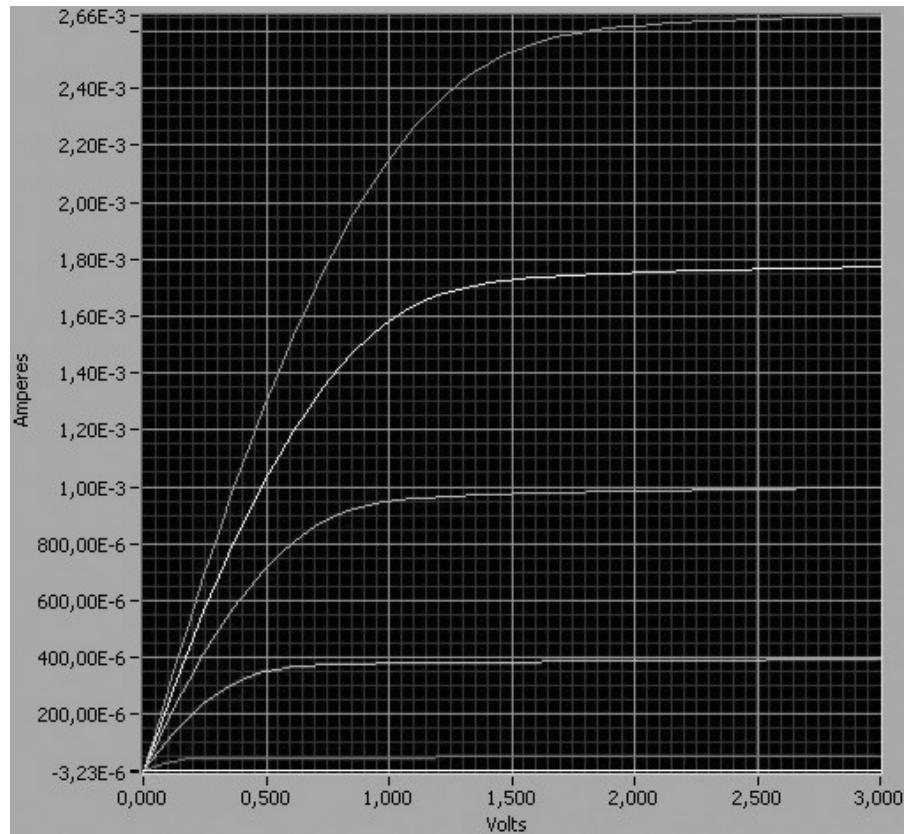
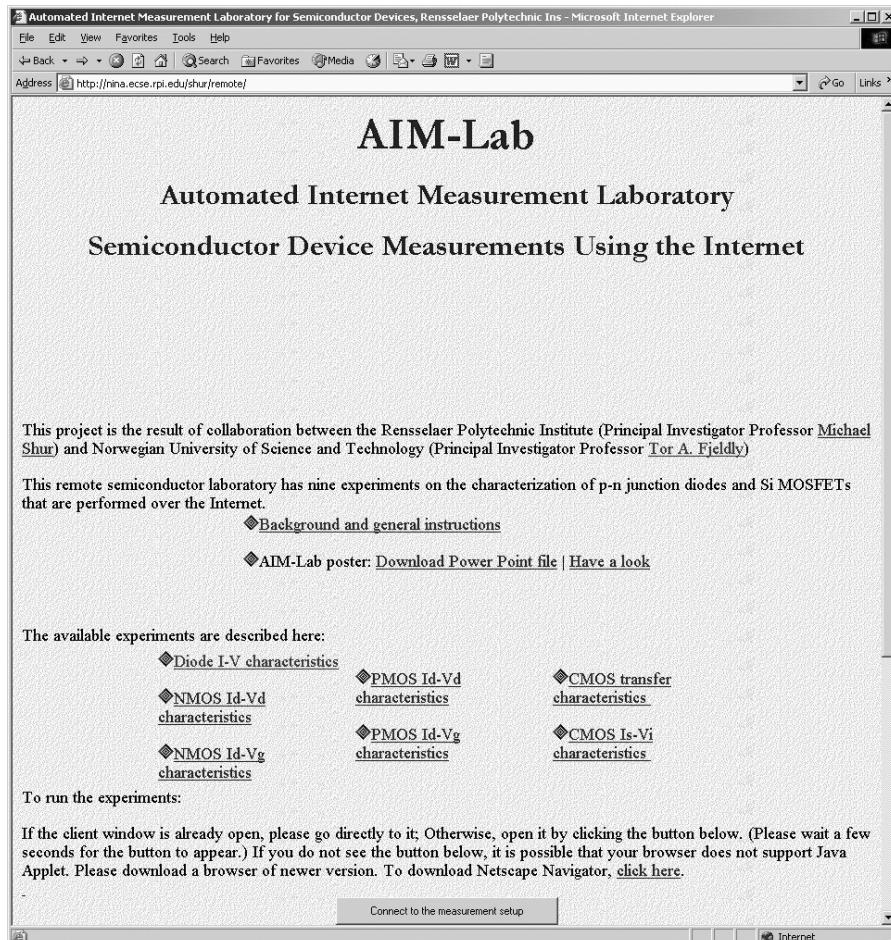


Figure 1.22 Client-side display of experimental NMOS characteristics using LabVIEW CGI solution.

- The Client window appears. Go to the Operation menu and choose Start experiment.
- The Channel Setup Dialog box appears. Select first NMOS Id-Vd characteristics.
- The Source Setup panel appears. This is the table where we enter the experimental parameters.

Note that the source and substrate of the transistor are connected to ground. Examples of client interactive pages in AIM-Lab are shown in Figure 1.2. The two transistors considered (NMOS and PMOS) have gate length $L = 2 \mu\text{m}$ and width $W = 25 \mu\text{m}$.

1. Measure the NMOS $I-V$ characteristics (i.e., drain current versus drain voltage). Choose different combinations of inputs to the parameter table.

**Figure 1.23** Main page of LAB-on-WEB.

2. Measure the NMOS transfer characteristics (i.e., drain current versus gate voltage) by selecting **NMOS Id-Vg characteristics** in the **Channel Setup Dialog** box. Choose a drain bias that corresponds to saturation for the range of V_{GS} used (see the characteristics in Figure 1.3). Since we are investigating a long-channel device, we may use the simple charge control model to approximate the measured dependence by the following equation:

$$I_{\text{sat}} = \beta_n V_{GT}^2 \quad \text{where} \quad \beta_n \equiv \frac{W\mu_n C_i}{2L} \quad \text{and} \quad V_{GT} \equiv V_{GS} - V_{Tn} \quad (1.1)$$

Here I_{sat} is the saturation current, μ_n is the electron mobility in the chan-

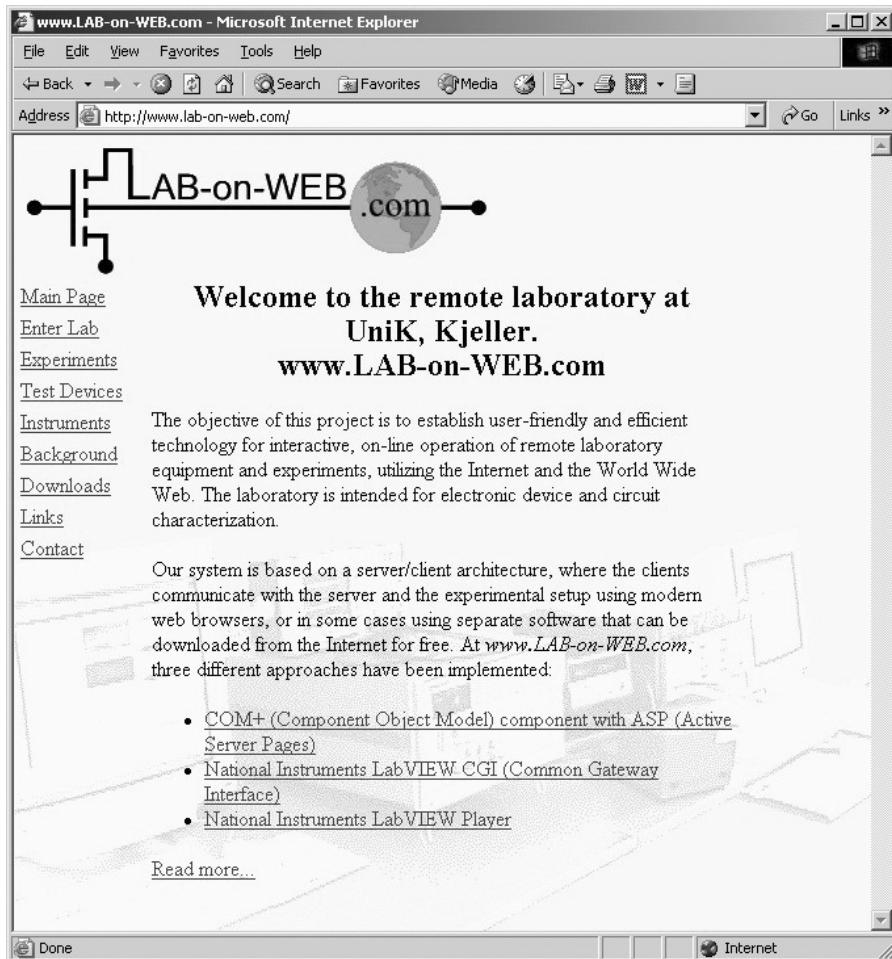


Figure 1.24 Main page of LAB-on-WEB.

nel, and C_i is the oxide capacitance per unit area. Plot $\sqrt{I_{\text{sat}}}$ versus V_{GS} and extract the value of β_n and the threshold voltage V_{Th} .

3. Do a similar set of measurements for the PMOS. In this case the equations become

$$I_{\text{sat}} = \beta_p V_{GT}^2 \quad \text{where} \quad \beta_p \equiv \frac{W\mu_p C_i}{2L} \quad \text{and} \quad V_{GT} \equiv V_{GS} - V_{Tp} \quad (1.2)$$

Here μ_p is the hole mobility. Extract the value of β_p and the threshold voltage V_{Tp} . Note that in this case the currents and voltages have opposite sign of those of the NMOS.

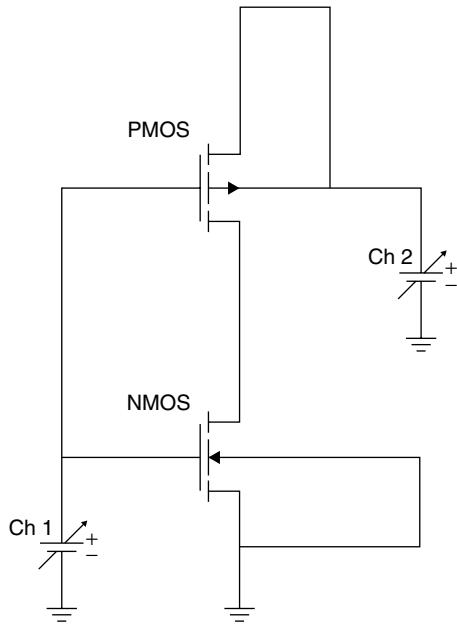


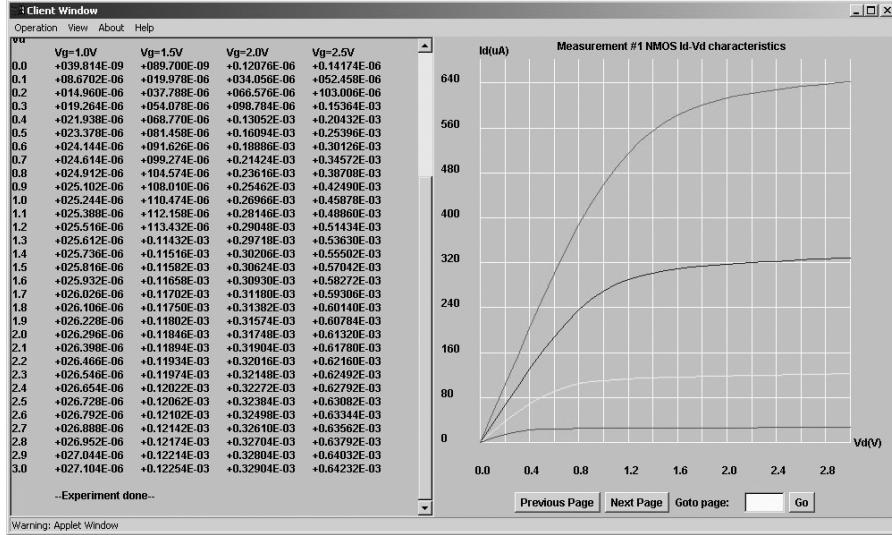
Figure 1.25 CMOS inverter. Input voltage V_{in} and voltage source V_{DD} are labeled Ch1 and Ch2, respectively.

4. Figure 1.25 shows a CMOS inverter circuit. Use Eqs. 1.1 and 1.2 to derive the following equation for the switching voltage of this inverter:

$$V_{sw} = \frac{V_{DD} + V_{Tp} + V_{Tn}\sqrt{\beta_n/\beta_p}}{1 + \sqrt{\beta_n/\beta_p}} \quad (1.3)$$

Hint: Note that the currents through both transistors are the same. For $V_{in} = V_{sw}$ assume that the PMOS and NMOS are in the saturation regime.

5. Measure CMOS inverter transfer characteristics by selecting **CMOS transfer characteristics** in the **Channel Setup Dialog** box. Note that the CMOS inverter consists of the same two devices investigated above. Compare the switching voltages with those predicted by Eq. 1.3.
6. Use the circuit description below and insert the values for β_n , V_{Tn} , β_p , and V_{Tp} found above to simulate the CMOS inverter transfer characteristics. (Note that the SPICE parameter $k_p = \mu c_i$ for NMOS and PMOS are obtained from β_n and β_p and the device geometry L , W). SPICE uses the symbol `vto` for the threshold voltage. Compare with the experiments and comment.

Figure 1.26 NMOS I_d - V_{DS} characteristics for $V_{GS} = 1\text{--}2.5 \text{ V}$.

```

CMOS inverter
vdd 1 0 5
vin 2 0 0
m1 3 2 1 1 mp w=25u l=2u
m2 3 2 0 0 mn w=25u l=2u
.model mn nmos level=1 kp=xxxx vto=yyyyy
.model mp pmos level=1 kp=zzzz vto=uuuu

```

1.4.1.2 Results

- First the NMOS I_d - V_{DS} characteristics are measured. An example is shown in Figure 1.26 for the default parameters in AIM-Lab.
- For the parameter extraction, we also need the NMOS transfer characteristics (I_d versus V_{GS}). Such a characteristic is shown in Figure 1.27 for a drain bias of 4 V. The data in Figure 1.27 is used for calculating the dependence of $\sqrt{I_d}$ on V_{GS} , as shown in Figure 1.28. Fitting the above-threshold part with a straight line, we can extract the parameters β_n and V_{Tn} as follows:

$$|I_{\text{sat}}| = \beta_n (V_{GS} - V_{Tn})^2 \Leftrightarrow \sqrt{I_{\text{sat}}} = \sqrt{\beta_n} (V_{GS} - V_{Tn}) \quad (1.4)$$

which gives

$$\sqrt{\beta_n} \approx 1.3 \times 10^{-2} \Omega^{-1} \quad V_{Tn} \approx \frac{7.02 \times 10^{-3}}{1.3 \times 10^{-2}} \approx 0.538 \text{ V} \quad (1.5)$$

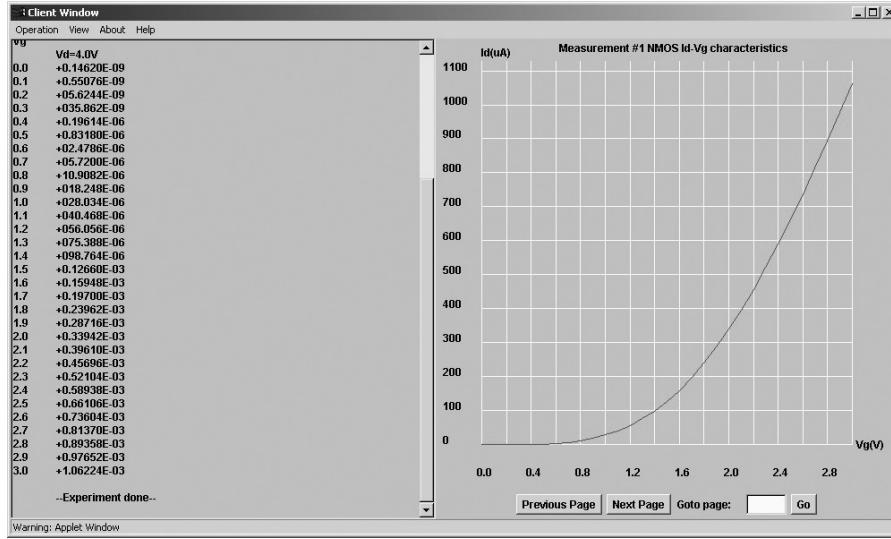


Figure 1.27 NMOS I_d - V_{DS} characteristics for $V_{GS} = 4$ V.

3. The PMOS device is characterized and the parameters are extracted similarly (see Figure 1.29). Here we find

$$\sqrt{\beta_p} \approx 9.553 \times 10^{-3} \Omega^{-1}$$

$$V_{Tp} \approx -\frac{4.348 \times 10^{-3}}{9.553 \times 10^{-3}} \approx -0.455 \text{ V} \quad (1.6)$$

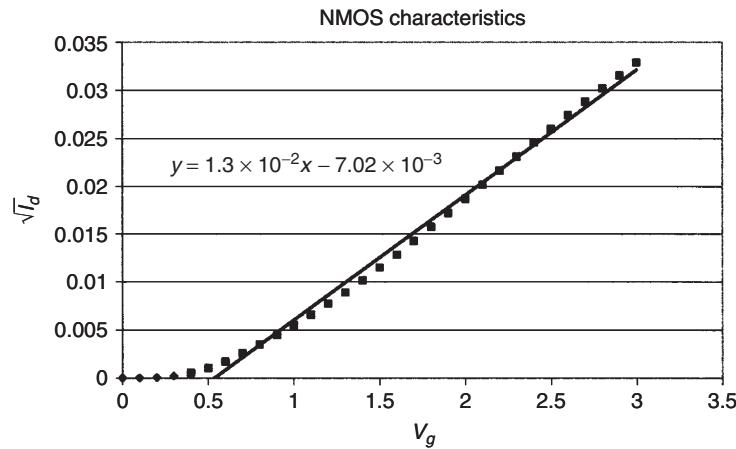


Figure 1.28 Experiment results and parameter extraction for NMOS device ($V_{DS} = 4$ V).

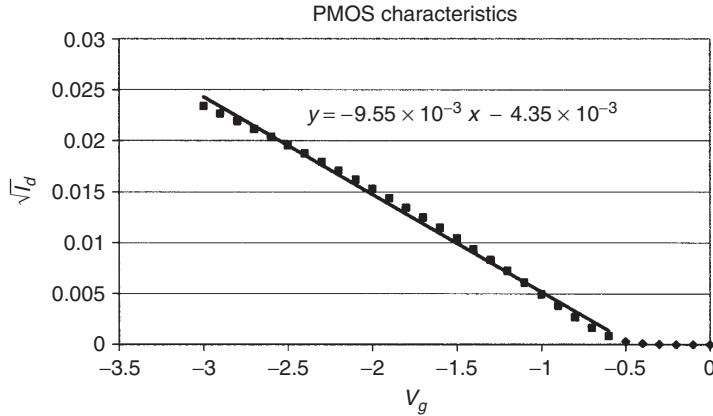


Figure 1.29 Experiment results and parameter extraction for the PMOS device ($V_{DS} = -4$ V).

4. Equating the square root of the NMOS and PMOS saturation currents at the switching point, we find

$$\sqrt{\beta_n}(V_{GSn} - V_{Tn}) = \sqrt{\beta_p}(-V_{GSp} + V_{Tp}) \quad (1.7)$$

Substituting $V_{GSn} = V_{in} = V_{sw}$, $V_{GSp} = V_{in} - V_{DD} = V_{sw} - V_{DD}$, and solving for V_{sw} , we obtain

$$V_{sw} = \frac{V_{DD} + V_{TP} + V_{TN}\sqrt{\beta_n/\beta_p}}{1 + \sqrt{\beta_n/\beta_p}} \quad (1.8)$$

From the parameters extracted above, we find

$$V_{sw} \approx \frac{V_{DD} + 0.2794}{2.366} \quad (1.9)$$

5. The measured CMOS inverter transfer characteristics are shown in Figure 1.30. Next, Figure 1.31 shows a comparison of the result from the above expression for V_{sw} with values obtained from Figure 1.30. Considering the accuracy of the fit and the precision of the V_{sw} readings obtained from Figure 1.30, Eq. 1.9 gives a good prediction of the CMOS inverter switching point.
6. The simulation results are compared with the experimental inverter transfer characteristics in Figure 1.32. Good agreement was obtained between experiments and simulations considering that only the simplest MOSFET SPICE model (level 1) was used. This shows that the PMOS and NMOS transistors with gate lengths of 2 μm used in this experiment can be considered as long-channel devices, for which the MOSFET level 1 SPICE model is applicable.

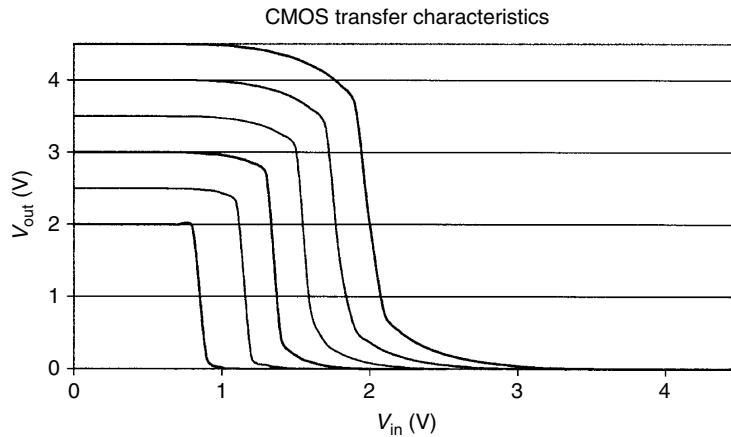


Figure 1.30 CMOS inverter transfer characteristics (V_{DD} ranges from 2 to 4.5 V with 0.5-V step).

1.4.2 LAB-on-WEB Subthreshold MOSFET Experiment

1.4.2.1 Background Very simplistically, the subthreshold regime of a MOSFET is considered an *off* state of the device, ideally blocking all drain current. In practice, however, there will always be some leakage current in this state owing to a finite amount of mobile charge in the channel and a finite injection rate of carriers from the source terminal into the channel.

The subthreshold current can be analyzed in a straightforward manner by considering a long-channel MOSFET with a gate length of a few micrometers or more. When such a device is biased in the subthreshold regime, the applied

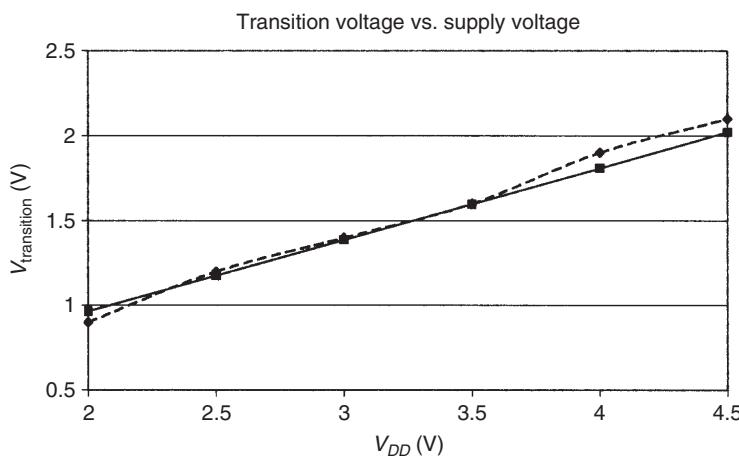


Figure 1.31 Comparison of result from Figure 1.30 (dashed curve) and Eq. 1.9 (solid line).

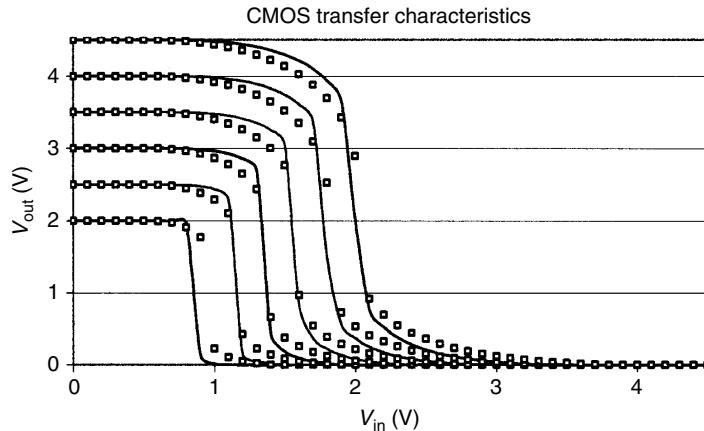


Figure 1.32 Comparison of experimental and simulated CMOS inverter transfer characteristics (experiments: solid lines; AIM-Spice simulations: symbols).

drain–source voltage will drop across the drain depletion zone of the channel. The remaining part of the channel is essentially at a constant potential (flat energy bands), where diffusion is the primary mode of charge transport. For this case, we easily find the following relationship of the MOSFET subthreshold drain current (see, e.g., Fjeldly et al., 1998):

$$I_{d,\text{sub}} \propto \exp\left(\frac{V_{gt}}{\eta V_{th}}\right) \left[1 - \exp\left(-\frac{V_{ds}}{V_{th}}\right)\right] \quad (1.10)$$

Here $V_{gt} = V_{gs} - V_T$ is the gate voltage swing, V_T is the threshold voltage [which separates the above-threshold behavior ($V_{gt} > 0$) from the subthreshold behavior ($V_{gt} < 0$)], V_{th} is the thermal voltage (0.026 V at room temperature), and η is an ideality factor related to the division of V_{gs} between the gate oxide and the semiconductor. We notice from Eq. 1.10 that $I_{d,\text{sub}}$ is an exponential function of V_{gt} and, when $V_{ds} > 2V_{th}$, it becomes independent of V_{ds} (saturation).

However, in modern-day MOSFETs, with submicrometer gate lengths, the subthreshold energy bands are no longer flat owing to the reduced geometry combined with a nonideal scaling of the devices. Moreover, the applied drain–source voltage will be distributed over the length of the channel, giving rise to a shift of the conduction band edge near the source end of the channel, as illustrated in Figure 1.33. This effect, known as drain-induced barrier lowering (DIBL), represents an effective lowering of the injection barrier for electrons from the source into the channel. Since the dominant injection mechanism is thermionic emission, the DIBL effect gives rise to a significant rise in the subthreshold current with increasing V_{ds} . This phenomenon can conveniently be

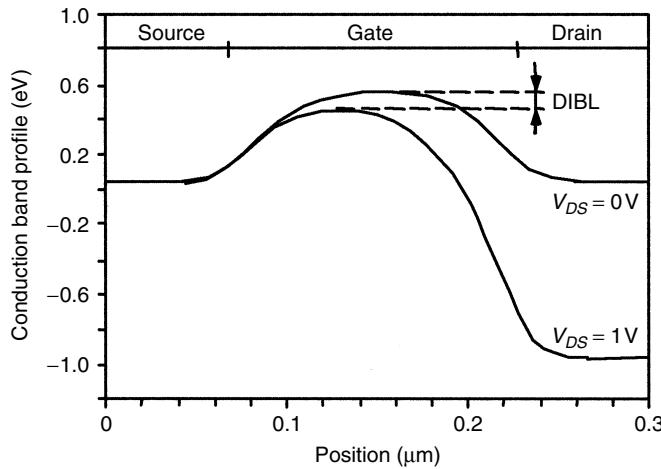


Figure 1.33 Conduction band profile at semiconductor–insulator interface of short *n*-channel MOSFET with and without drain bias. Figure indicates origin of DIBL (from Fjeldly et al., 1998).

described in terms of a shift in the threshold voltage. The dependence of V_T on the channel length L and the drain bias can be expressed as

$$V_T(L) = V_{T0}(L) - \sigma(L)V_{DS} \quad (1.11)$$

where $V_{T0}(L)$ describes the scaling of the threshold voltage at zero drain bias with L and $\sigma(L)$ is the channel-length-dependent DIBL parameter.

Clearly, the subthreshold current is very important since it has consequences for the bias and logic levels needed to achieve a satisfactory *off* state in digital operations. Hence, it affects the power dissipation in logic circuits. Likewise, the holding time in dynamic memory circuits is controlled by the magnitude of the subthreshold current. The DIBL effect tends to increase the power dissipation in the subthreshold regime and also increase the above-threshold current at high drain biases. However, well above threshold, the injection barrier is much reduced and the DIBL effect eventually disappears.

The objective of this assignment is to study the dependence of the threshold voltage on gate length and drain bias for the Alfa chip NMOS devices (see Section 1.2.1.1).

1.4.2.2 Subthreshold MOSFET Assignment

- Go to <http://www.lab-on-Web.com/>.
- Get acquainted with LAB-on-WEB by looking through the pages of the website.

- Look up NMOS Id-Vg (Drain Current–Gate Voltage) Characteristic under Experiments.
 - Select Enter Laboratory.
 - Choose SVG Graphics Interface.
 - Under Auto Setup select the predefined experiment NMOS Id-Vg.
 - Under Dimensions select NMOS 25/0.7.
 - Enter measurement parameters in the ch. 1 ($V_g \equiv V_{gs}$) and ch. 2 ($V_d \equiv V_{ds}$) tables.
 - Under Plot Setup select Logarithmic on the left vertical axis.
 - Press Execute Measurement.
1. Measure the NMOS 25/0.7 $I_d - V_g$ characteristics for V_{gs} between 0.3 and 1.3 V for the following values of V_{ds} : 0.05, 1.05, 2.05, and 3.05 V.
 2. Extract the slope of the semilogarithmic (base 10) characteristics in the subthreshold regime (typically for $V_{gs} < 0.6$ V) and determine the ideality factor η in Eq. 1.10.
 3. From the subthreshold region, determine the threshold voltage shift ΔV_T for the various applied drain biases. Use the characteristic for $V_{ds} = 0.05$ V as a reference. Plot ΔV_T versus V_{ds} and estimate the DIBL parameter σ .
 4. Repeat the procedure for the NMOS 25/0.8, 25/1.3, and 25/1.6 and use the results to plot σ versus L . Discuss the results.

1.4.2.3 Results

1. Figure 1.34 shows the NMOS 25/0.7 $I_d - V_g$ characteristics for the following values of V_{ds} : 0.05, 1.05, 2.05, and 3.05 V.
2. We find that the linear part of the plots in Figure 1.34 can be expressed, in agreement with Eq. 1.10, as

$$\log_{10}\left(\frac{I_{d,\text{sub}}}{I_0}\right) = \frac{V_{gs}}{\eta V_{\text{th}}} \log_{10}(e) \quad (1.12)$$

where I_0 corresponds to the current at $V_{gs} = \eta V_{\text{th}}$. Selecting two arbitrary points in the linear part of the plot, we extract the following reasonable value of the ideality factor:

$$\eta \approx 1.5$$

3. The threshold voltage shift $\Delta V_T(V_{ds})$ is obtained from Figure 1.33 by measuring the horizontal shifts of the different characteristics using $V_{ds} = 0.05$ V as a reference, and ΔV_T versus ΔV_{ds} measured at

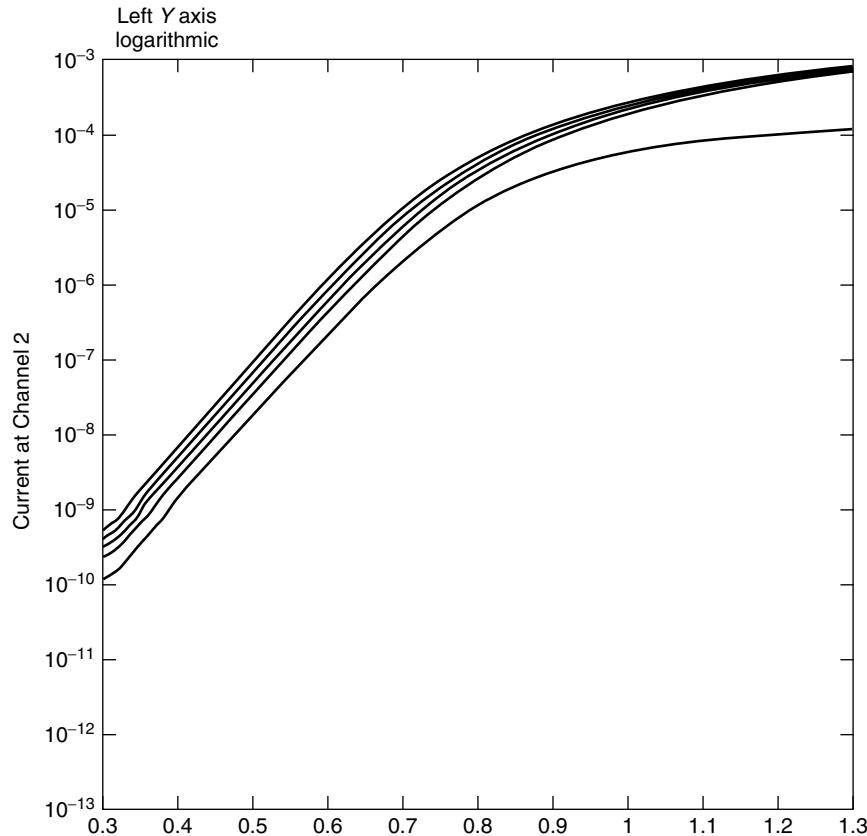


Figure 1.34 Semilogarithmic plot of NMOS 25/0.7 I_d - V_g characteristics for V_{ds} between 0.05 V (lower curve) and 4.05 V (upper curve), 1-V step. Vertical axis: drain current (A). Horizontal axis: drain-source bias (V).

$I_{d,\text{sub}} = 10^{-7}$ A is presented in Figure 1.35. The straight line corresponds to the following DIBL parameter:

$$\sigma = \frac{\Delta V_{Tp}}{\Delta V_{ds}} \approx 0.018$$

4. For increasing gate length, we will notice a decreasing shift of the subthreshold portion of the $\log(I_{d,\text{sub}})$ versus V_{gs} characteristics. Figure 1.36 shows the results measured for the gate length, $L = 1.6$ μm . Estimating the values of σ using only the curves corresponding to V_{gs} values of 0.05 and 4.05 V, we find the scaling of σ versus L plotted in Figure 1.37. The obtained scaling shows the expected trend. As L increases, the device approaches the ideal, long-channel, subthreshold behavior described by Eq. 1.10, where the DIBL effect becomes negligible.

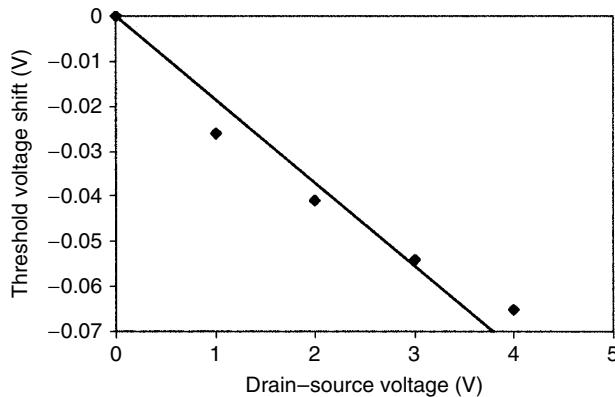


Figure 1.35 Plot of ΔV_T versus V_{ds} for NMOS 25/0.7. Experimental values (symbols) were obtained from Figure 1.34. Straight line corresponds to best linear fit. Slope of this line is DIBL parameter σ .

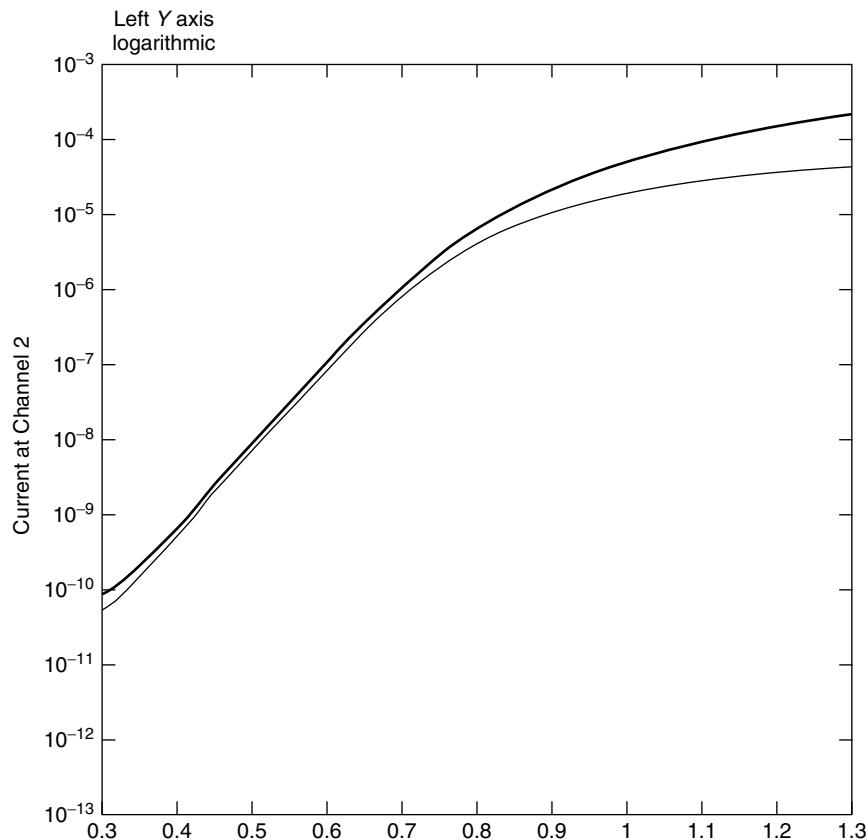


Figure 1.36 Semilogarithmic plot of NMOS 25/1.6 I_d - V_g characteristics for V_{ds} between 0.05 V (lower curve) and 4.05 V (upper curve), 1-V step. Vertical axis: drain current (A). Horizontal axis: drain-source bias (V).

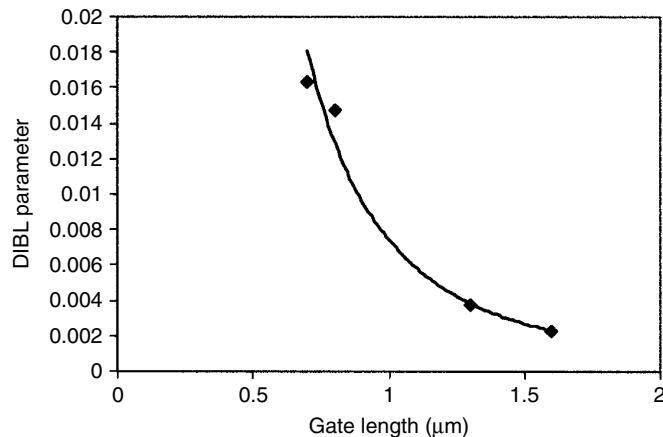


Figure 1.37 Plot of DIBL parameter σ versus gate length L of Alfa chip NMOS transistors. Experimental data are shown as symbols. Curve indicates the trend.

1.4.3 LAB-on-WEB Diode Experiment

1.4.3.1 Assignment

- Go to <http://www.lab-on-web.com/>.
 - Get acquainted with LAB-on-WEB by looking through the pages of the website.
 - Look up Diode I–V (Current–Voltage) Characteristic under Experiments.
 - Select Enter Laboratory.
 - Choose LabVIEW CGI Interface.
 - Select the predefined experiment Diode I–V (diode 1N 4001).
 - Enter measurement parameters in the Ch. 1 table under Set up the voltage source(s).
 - Press Submit.
1. Measure the I – V characteristic between 0.05 and 0.7 V. Replot the curve in a semilogarithmic scale by copying and pasting the data in another application, such as Excel (note that you may have to replace periods by commas to be able to plot in some applications). Discuss the various regions of the curve.
 2. Consider the semilogarithmic plot (base 10) for the voltage range between approximately 0.3 and 0.6 V. Extract the saturation current I_s and the ideality factor η from an extrapolation of $\log_{10}(I_s)$ to 0 V and from the slope, respectively. What does the value of η reveal about the current mechanism? What does the change of slope below 0.3 V signify?

3. Measure the current–voltage characteristic of the diode in the range -0.01 to $+0.01$ V. Use this curve to extract the ratio $I_s/(\eta V_{th})$ from the slope of the diode characteristic close to 0 V ($V_{th} = 0.026$ V is the thermal voltage assuming room temperature). Compare with the results from 2 and comment on the difference, if any.
4. Measure the reverse diode characteristic from 0 to -3 V. Comment on the voltage dependence of the reverse current.

1.4.3.2 Results

1. *Forward Bias.* Figure 1.38 shows the characteristic for diode 1N 4001 in a linear plot obtained using the LabVIEW CGI interface in LAB-on-WEB. The accompanying raw data were exported to Excel and are shown in a semi-logarithmic plot (base 10) in Figure 1.39. The straight line in this figure indicates the approximate fit to the “ideal” diode region for applied voltages V

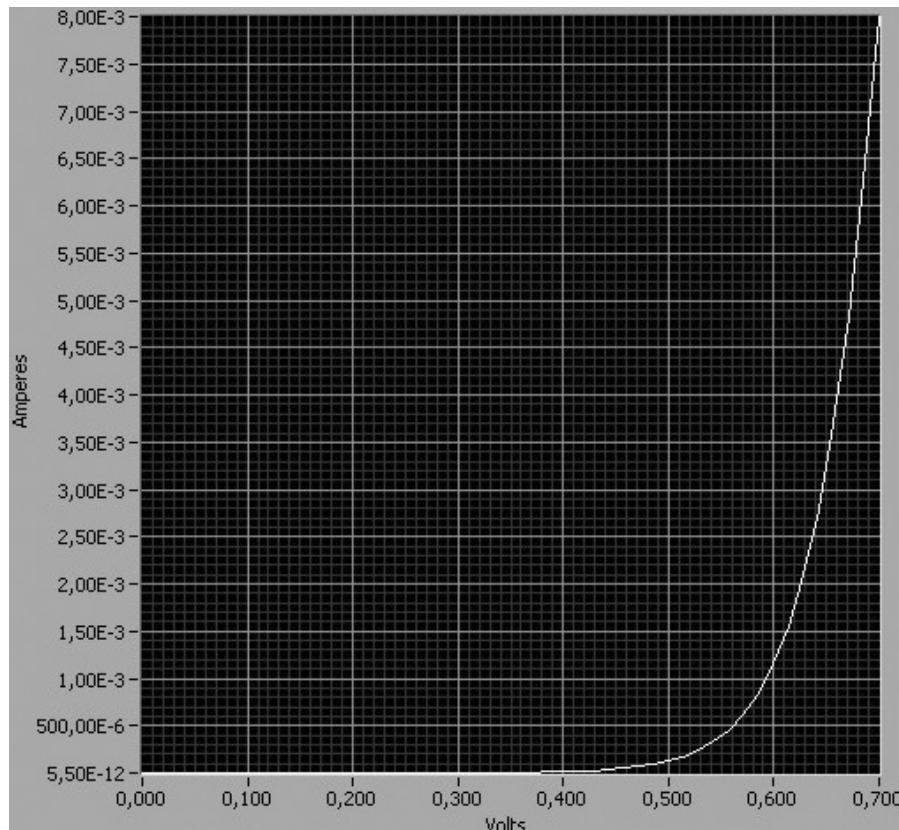


Figure 1.38 Diode characteristics in linear plot.

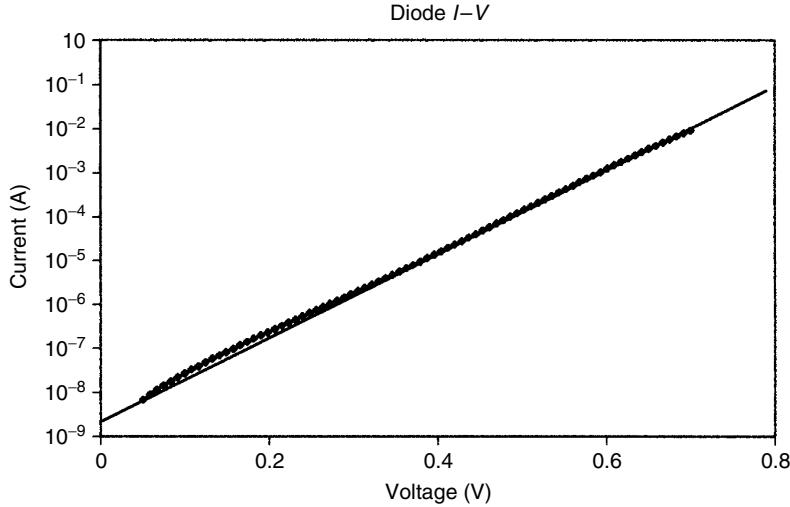


Figure 1.39 Diode characteristics in semilogarithmic plot.

between 0.3 and 0.6 V, given by the familiar diode equation

$$I = I_s \left[\exp\left(\frac{V}{\eta V_{th}}\right) - 1 \right] \quad (1.13)$$

Here I_s is the saturation current, η is the ideality factor (usually between 1 and 2), and $V_{th} = 26$ mV is the thermal voltage at room temperature. Note that for the voltage range considered the exponential term will dominate in Eq. 1.13 since $V \gg \eta V_{th}$. At the lower voltage range, we notice a slight deviation from the ideal line resulting from excess current owing to recombination processes. Above 0.6 V, we see indications of a reduction below the ideal line owing to high-injection effects and the series resistance.

2. Parameter Extraction. The saturation current is found by extrapolating the straight line to the vertical axis at $V = 0$ V. The intercept gives $I_s = 2 \times 10^{-9}$ A. The slope of the curve can be obtained from

$$\log_{10}\left(\frac{I}{I_s}\right) = \frac{V}{\eta V_{th}} \log_{10}(e) \quad (1.14)$$

Taking the derivative of $\log_{10}(I/I_s)$ with respect to V , we find the slope $\log_{10}(e)/\eta V_{th}$. From the curve, we obtain the slope 9.6. Using $\log_{10}(e) = 0.4343$, we find the ideality factor $\eta = 1.74$. This is a high number, indicating the presence of nonideal effects throughout the characteristic. A reduced slope below 0.3 V normally indicates the presence of recombination mechanisms.

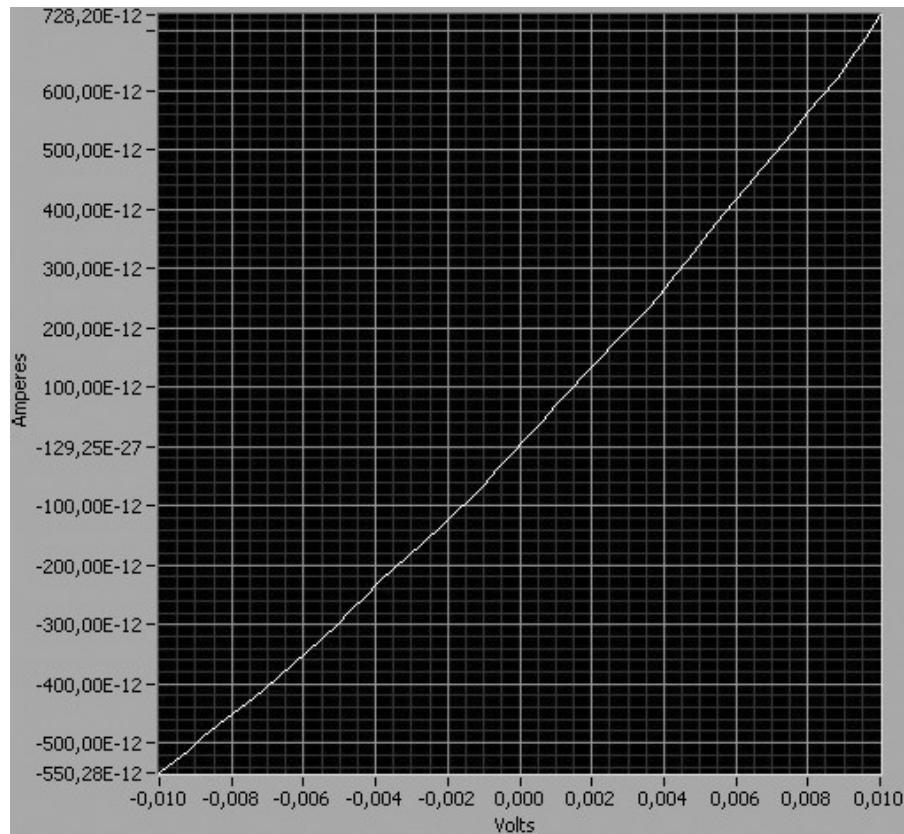


Figure 1.40 Diode characteristics in linear plot for small voltages.

3. *Small Forward Bias.* Figure 1.40 shows the diode characteristic measured for small voltages in the range from -0.01 to $+0.01$ V. For very small voltages, the exponential function of the diode equation can be expanded to first order to give $I = VI_s/\eta V_{th}$ and the slope becomes $I_s/\eta V_{th}$. From Figure 1.40, we find $I_s/\eta V_{th} = 6.5 \times 10^{-8}$ A/V. From 2, we find the corresponding value of 4.4×10^{-8} A/V. This indicates basically that the saturation current corresponding to the generation/recombination current is somewhat larger than that of higher voltages, as could be expected. However, the difference is not very significant, which is in agreement with the observation in Figure 1.39. The large ideality factor, even at the higher voltage range, may indicate that the diode is doped with recombination centers (e.g., to make the diode faster).

4. *Reverse Bias.* The diode characteristic for reverse bias is shown in Figure 1.41. We notice that this current does not really saturate with increasing reverse bias. Instead, it increases gradually. This behavior is related to the fact that the generation current is proportional to the width of the depletion zone. In fact,

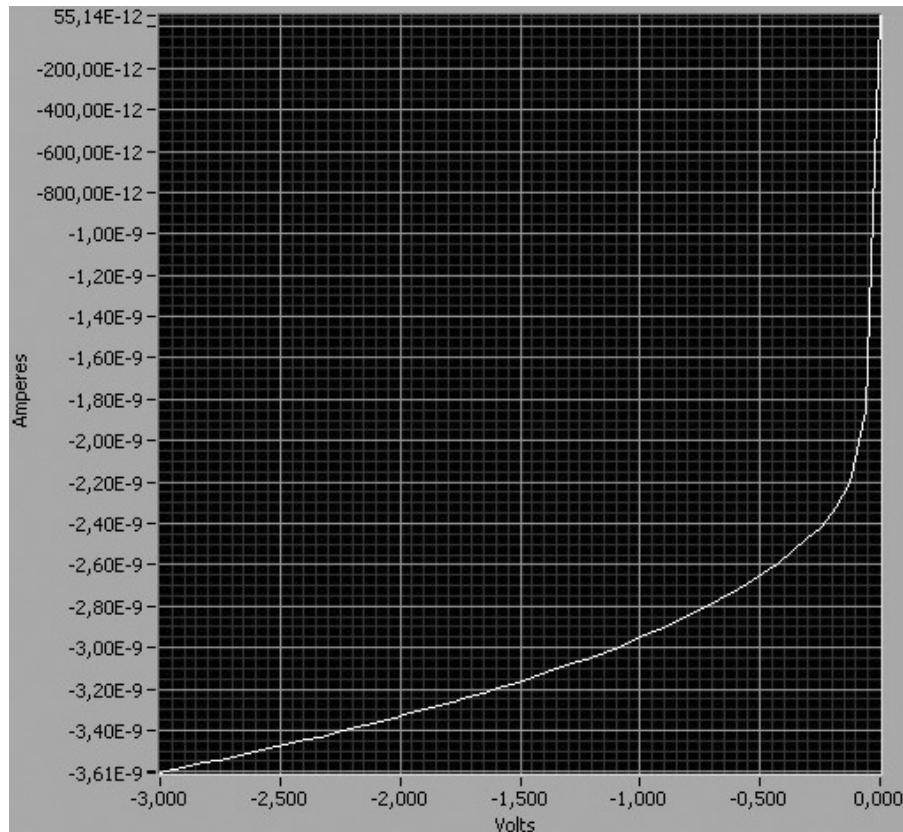


Figure 1.41 Diode characteristics in reverse bias (linear plot).

we should expect to see a square-root dependence of the generation current junction versus $(V_{bi} + |V|)$, with some adjustment for the deviation in the doping profiles through the diode from that of an abrupt junction.

1.5 EDUCATIONAL EXPERIENCE AND FUTURE PLANS

We have experience of the use of our remote laboratories as modules in the first-year graduate course Semiconductor Devices and Models I (SDM-1) at RPI and in the senior course Device Modeling and Circuit Simulation at UniK/NTNU. Both courses were offered as parts of a distance-learning program at the two institutions. The experiments included those discussed in the examples of Section 1.4 and additional experiments on bipolar transistors and photodiodes. Several of the experiments are available from both locations, with different devices, interfaces, and experimental details.

SDM-1 at RPI was a course for first-year graduate students and qualified seniors offered to both on-campus students and distance-learning students from General Motors, IBM, Pitney Bowes, and other companies. A total of 23 students were enrolled in the pilot course. All course materials were posted on the Web, and students did not have to remember any additional Universal Resource Locators (URLs). The experiments in AIM-Lab were used in the classroom to illustrate and reinforce the basic principles of the operation of the FET as well as to demonstrate some nonideal effects, which limit the FET performance. The ability to change the voltage and current ranges and to zoom in on certain features of the current–voltage characteristics was especially useful.

We also compared the measured data with FET models. This was done in two different ways. First, the students had to comment if the results of the measurements made sense given only the geometry of the device under test. They used order-of-magnitude values of the electron mobility and saturation velocity to roughly estimate the maximum device current and transconductance. This led to a fairly lively discussion in class. Only then were different FET models used, from a very simple constant-mobility model to the more sophisticated models, in order to try to fit the device characteristics. The students were also asked to provide a feedback and critique the user interface. Their comments and critique helped to improve the remote laboratory. It was a very positive and rewarding experience.

Similar experiences were gained at UniK/NTNU. Here, local and remote students sit at different campuses that are interconnected by a high-speed network, allowing us to stream two-way video over the Internet (IP). Overheads, SPICE simulations, and remote lab experimental demonstrations are also transmitted over the Internet using the NetMeeting application by Microsoft. This high-quality communication system allows projections on large screens to create a classroomlike environment also for the remote students, which seems to help in reducing the barrier for students to engage in two-way interaction.

The student lab assignments at UniK/NTNU are performed using LAB-on-WEB and occasionally AIM-Lab, as a mandatory module in the course SIE4090 Device Modeling and Circuit Simulation. This course is based on the text by Fjeldly et al. (1998), and the experiments are designed to illustrate and reinforce the subject matter being taught. The assignment typically consists of background theory, measurements, parameter extraction, circuit simulations, and discussion of results. The experiments concern basic properties and nonideal effects of devices and subcircuits, including $p-n$ diodes (see Section 1.4.3), bipolar junction transistors (diode characteristics, Gummel plots, current gain), and MOSFETs (see Sections 1.4.2 and 1.4.4). The objective is to provide future circuit designers with a deeper insight into the models used in computer-aided design (CAD), to appreciate the strengths and weaknesses of the models, to understand the limitations of the models, and to familiarize themselves with the meaning of the model parameters.

All in all, AIM-Lab and LAB-on-WEB did provide a new and very useful

dimension to the courses, so much so that we want to expand the labs to include several additional experiments using more advanced CMOSs (see, e.g., Chapter 4 of this book), bipolar junction transistor (BJT) integrated circuits, and also alternative technologies such as Group III–V metal–semiconductor FETs (MESFETs) and heterostructure FETs (HFETs).

We also plan to start developing remote lab experiments on logic circuit elements based on the use of FPGAs (field programmable logic arrays) for use in introductory electronic and computer engineering classes. These classes often have large numbers of students (typically about 500 at NTNU), where the use of remote lab technology may ease severe logistic and cost problems encountered in conventional labs.

We envision an increased collaboration in the development, establishment, and maintenance of remote laboratories between universities. This way, resources will be better utilized, laboratories will be made accessible to less endowed schools (including schools in developing countries), students will be able to use more advanced instruments, and the number and quality of available experiments may be vastly expanded. RPI and UniK/NTNU have already enjoyed such collaboration for several years.

We also foresee the establishment of Internet access to major research and engineering laboratory facilities. In such a case, scientists or engineers may, for example, submit their sample by mail and have it mounted by local staff, whereupon they are enabled to run their experiments remotely without the need for time-consuming and costly travel. Another possibility is for device and systems manufacturers, vendors, or independent entrepreneurs to establish remotely operated test stations where new products can be tested and evaluated by potential customers from all over the world.

1.6 CONCLUSION

We have developed and investigated different system solutions for allowing remote clients (students) to perform real laboratory experiments via the Internet. We have established two physical laboratory sites, AIM-Lab at RPI in the United States and LAB-on-WEB at UniK/NTNU in Norway. Both sites provide experiments on semiconductor devices that are accessible to clients worldwide.

The AIM-Lab site at RPI is based on a TCP/IP communication solution that uses a Java applet on the client side. This is achieved by means of a Java virtual machine in the web browser that can download and execute Java code. LAB-on-WEB at UniK/NTNU presently offers several different system solutions based on modern web and instrument control technologies, such as COM+ and LabVIEW 6i, and the advanced functionalities of today's web browsers. COM+ has a well-structured and flexible development environment that has been widely adopted by the web community. It also performs useful tasks related to security, queuing, and logging. LabVIEW solutions are easily

developed by means of the graphical program development utility. Presently, two solutions based on CGI scripts and the LabVIEW Player executable are implemented in LAB-on-WEB.

Here, we have discussed our remote lab systems in some detail and provided examples of lab assignments that are presently being used as integral parts of courses at our institutions. The experience so far has been both positive and encouraging, with valuable feedback received from other users worldwide. Eventually, based on the remote lab concept, courses and course modules within many disciplines of engineering and science may be offered to remote students located any place in the world, including students who otherwise would be precluded by distance and lack of resources. We also foresee future applications where major research and engineering facilities open for remote experimentation and where sophisticated on-line test stations are established to provide potential customers with the opportunity to perform remote testing of new products.

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