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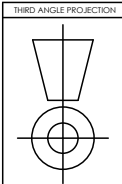
REV STATUS OF SHEETS	REV											REVISIONS				
	SHEET										ZONE	REV	DESCRIPTION	DATE	APPROVED	

Uses JLCPCB 7268 stackup  
for controlled impedance

Layer Stack Legend

Material	Layer	Thickness	Dielectric Material	Type	Gerber
	Top Overlay			Legend	GTO
Surface Material	Top Solder	0.020mm	SM-001	Solder Mask	GTS
PbSn	Top Surface Finish	0.020mm		Surface Finish	
CF-004	Top Layer	0.035mm		Signal	GTL
Prepreg		0.210mm	PP-017	Dielectric	
CF-004	Int1 (GND)	0.015mm		Internal Plane	GP1
Core		1.065mm	Core-039	Dielectric	
CF-004	Int2 (PWR)	0.015mm		Internal Plane	GP2
Prepreg		0.210mm	PP-017	Dielectric	
CF-004	Bottom Layer	0.035mm		Signal	GBL
PbSn	Bottom Surface Finish	0.020mm		Surface Finish	
Surface Material	Bottom Solder	0.020mm	SM-001	Solder Mask	GBS
	Bottom Overlay			Legend	GBO
Total thickness: 1.667mm					

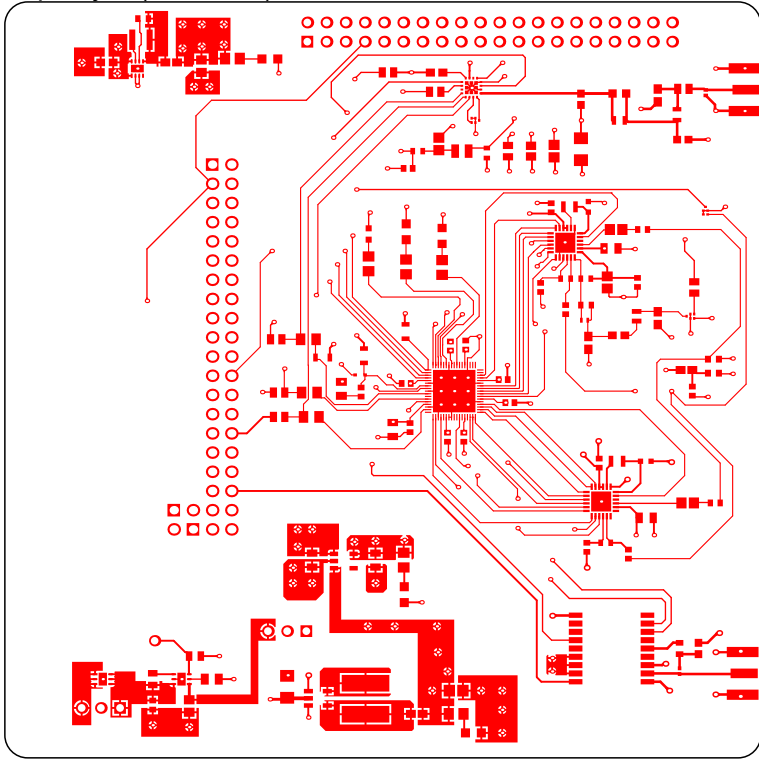
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SCALE:		FILE NAME: concentrator_pcb.PCBDwf		SHEET: 2		OF 6			



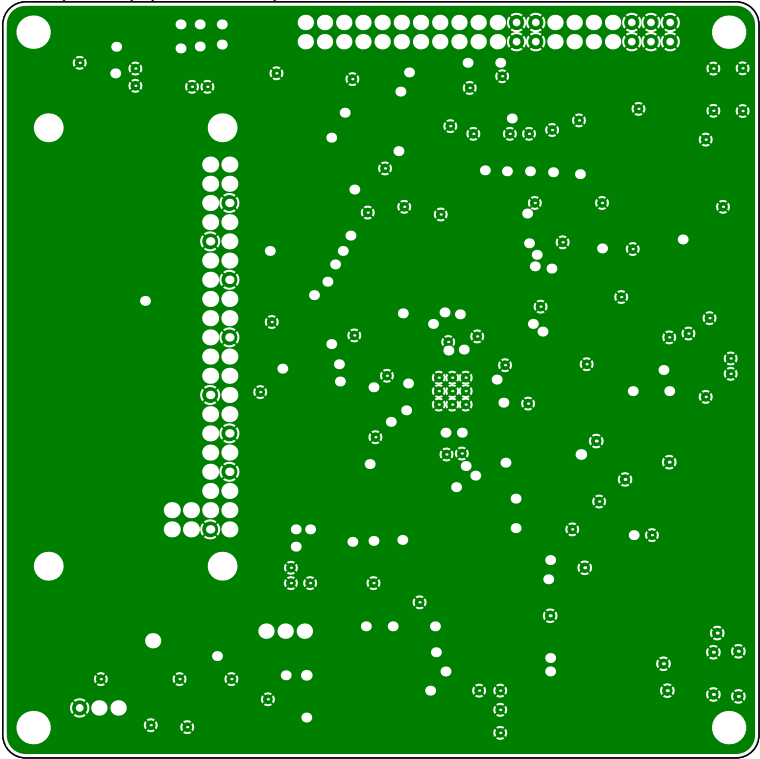
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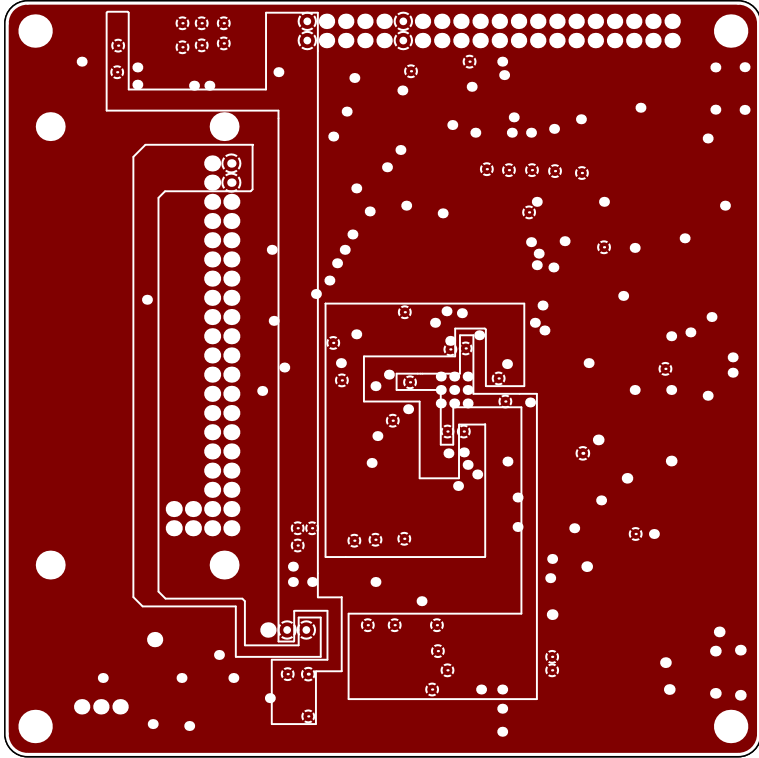
Top Layer (Scale 1:1)



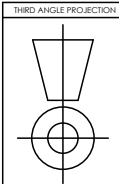
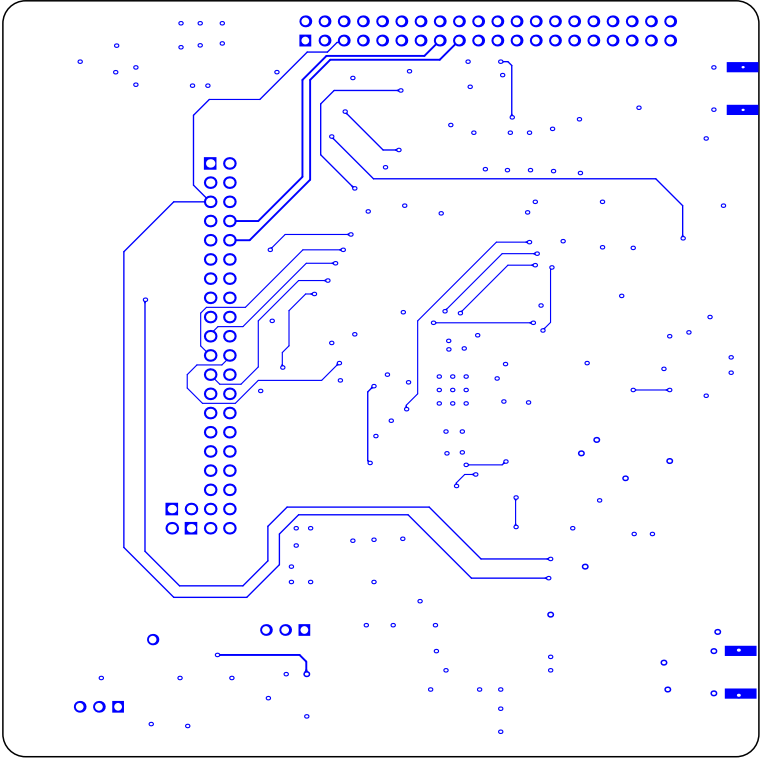
Int1 (GND) (Scale 1:1)



Int2 (PWR) (Scale 1:1)



Bottom Layer (Scale 1:1)

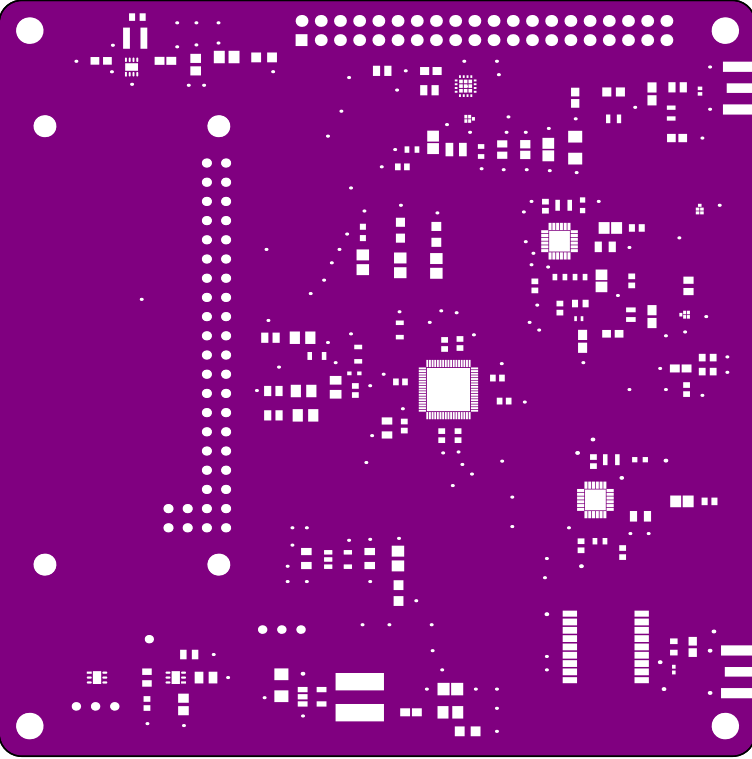


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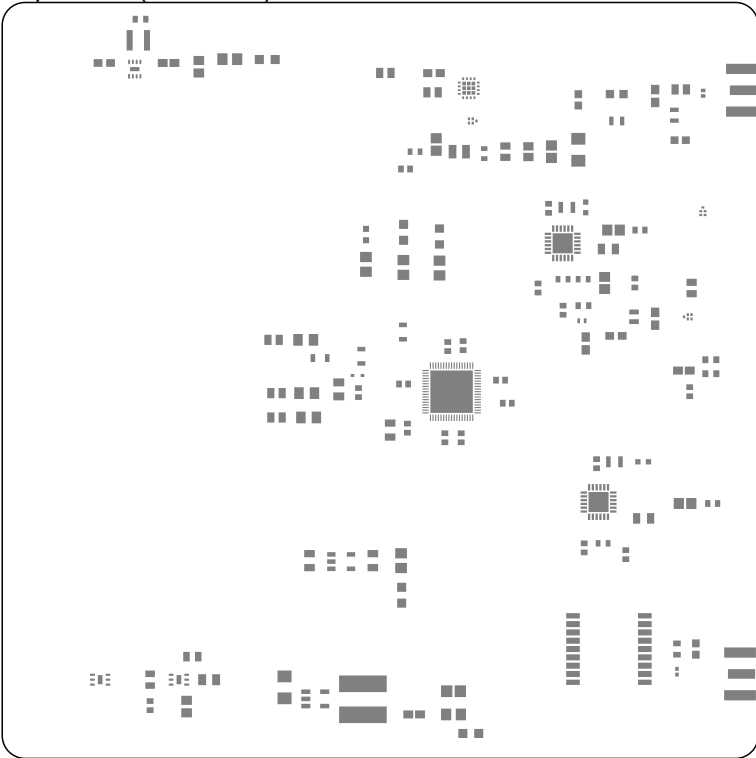
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[illegible]

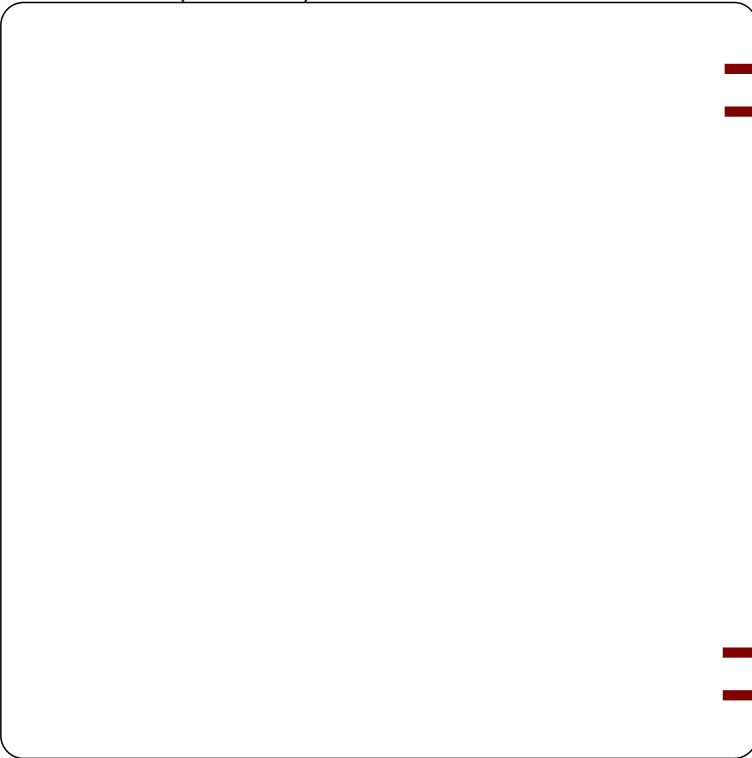
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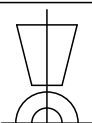


### Top Paste (Scale 1:1)



### Bottom Paste (Scale 1:1)

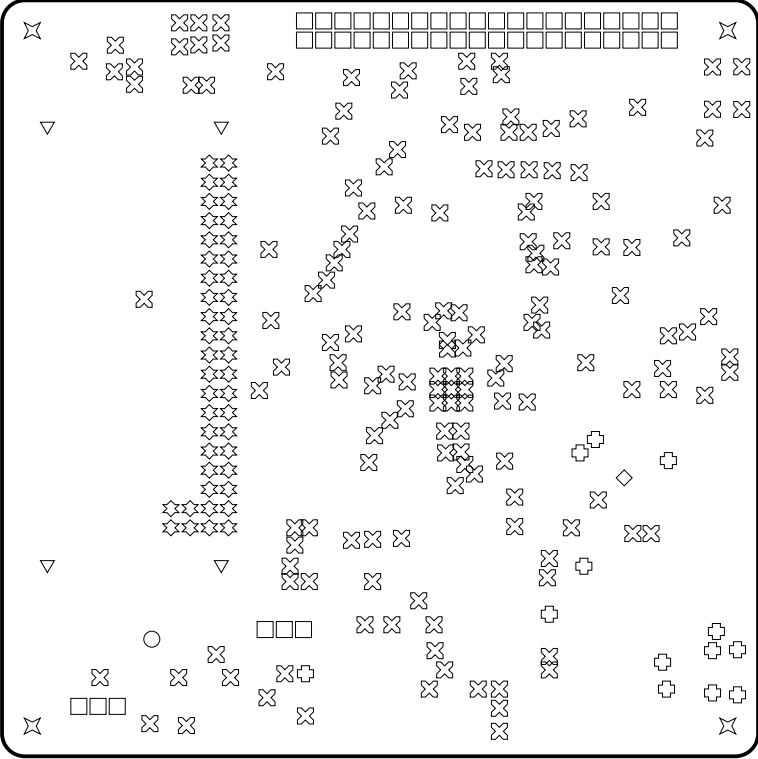


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NEXT ASSY		USED ON		APPLICATION			

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
REV STATUS OF SHEETS	REV										REVISIONS						
	SHEET										ZONE	REV	DESCRIPTION	DATE	APPROVED		

### Drill Drawing View (Scale 1:1)



## Drill Table

Symbol	Count	Hole Size	Plated	Hole Tolerance
⊗	163	0.30mm	Plated	
◇	1	0.38mm	Plated	
⊕	13	0.40mm	Plated	
○	1	1.00mm	Plated	
□	46	1.02mm	Plated	
☆	44	1.11mm	Plated	
▽	4	2.80mm	Non-Plated	
✱	4	3.40mm	Non-Plated	
276 Total				


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	SHEET										ZONE	REV	DESCRIPTION	DATE	APPROVED			

### Notes:

- 1 Vias should be untented and unplugged
- 2 There are 298 DRC errors cause of the minimum solder mask sliver (solder bridge) constraint of 0.2mm.

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APPLICATION											

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